APEX
PRECISION POWER

Product Data Book

POWER ANALOG ICs, MODULES AND HYBRIDS

VOLTAGE REFERENCES

HIGH VOLTAGE, HIGH CURRENT PWM AMPLIFIERS

HIGH VOLTAGE, HIGH CURRENT LINEAR AMPLIFIERS

HIGH SPEED LINEAR AMPLIFIERS

EVALUATION KITS

ACCESSORIES

PACKAGING

APPLICATION NOTES

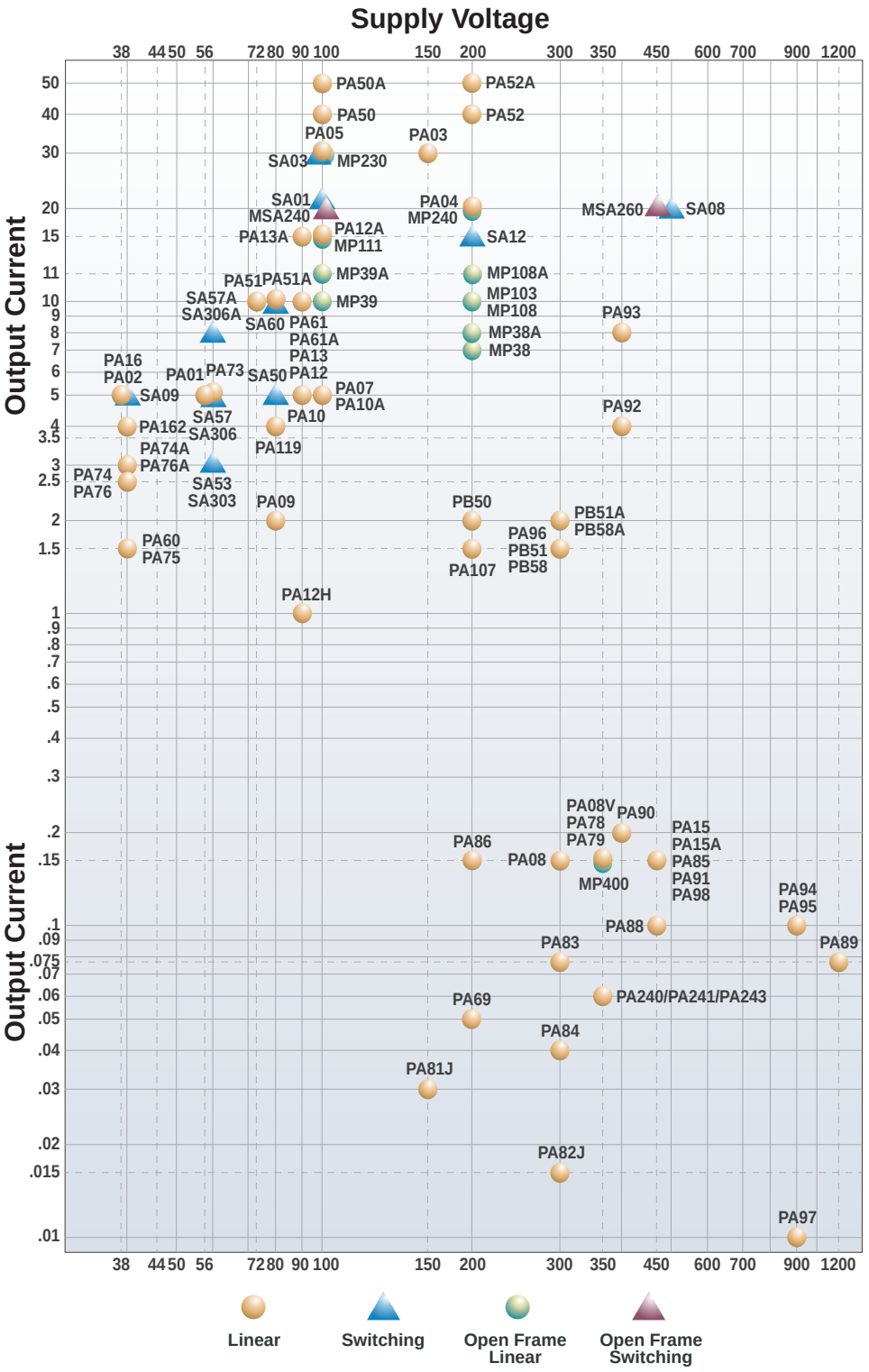
Volume 15

ISO9001

Product Innovation from Cirrus Logic

CIRRUS LOGIC®

PRODUCT SELECTOR MATRIX – AMPLIFIERS



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Volume 15

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CIRRUS LOGIC®

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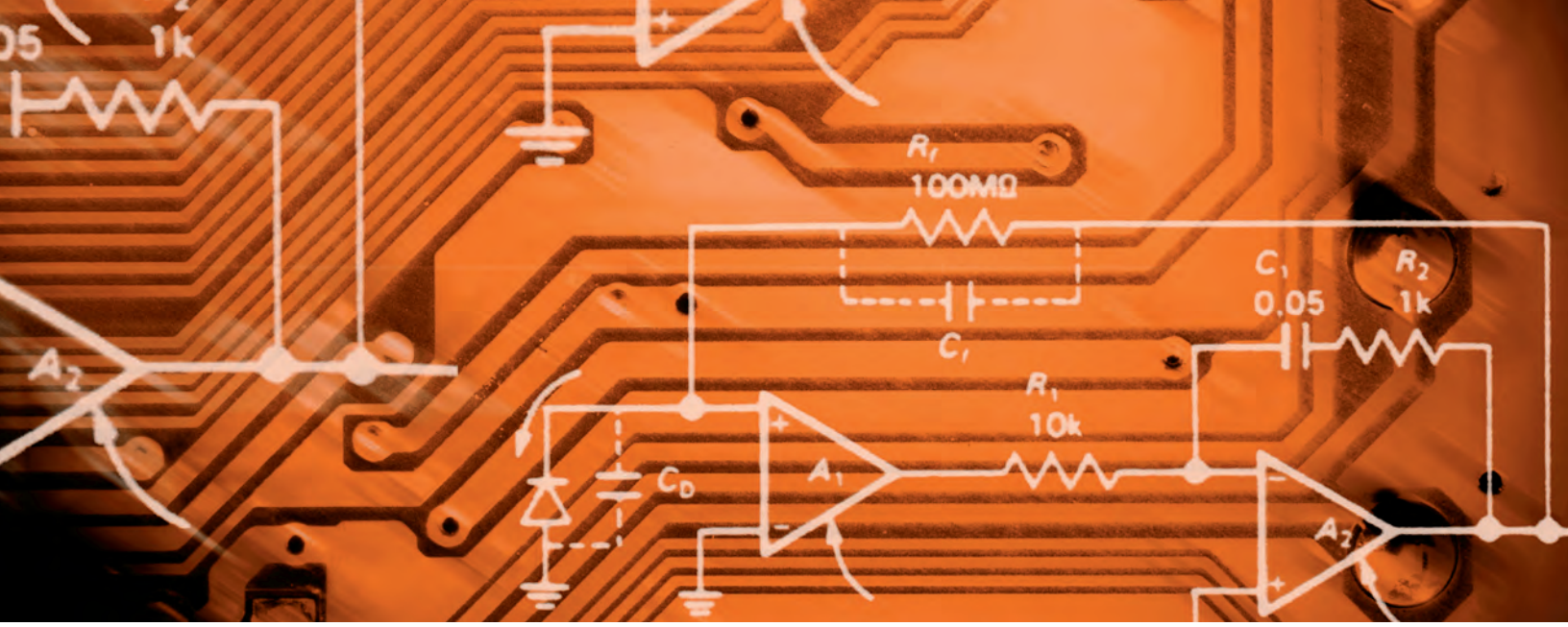

CIRRUS LOGIC

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ISO9001

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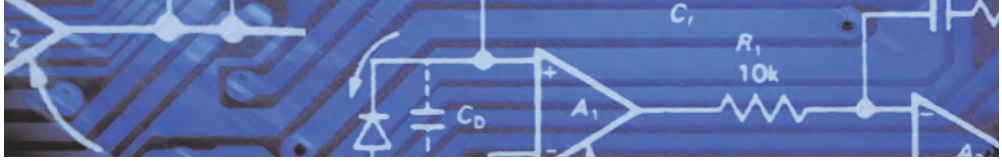

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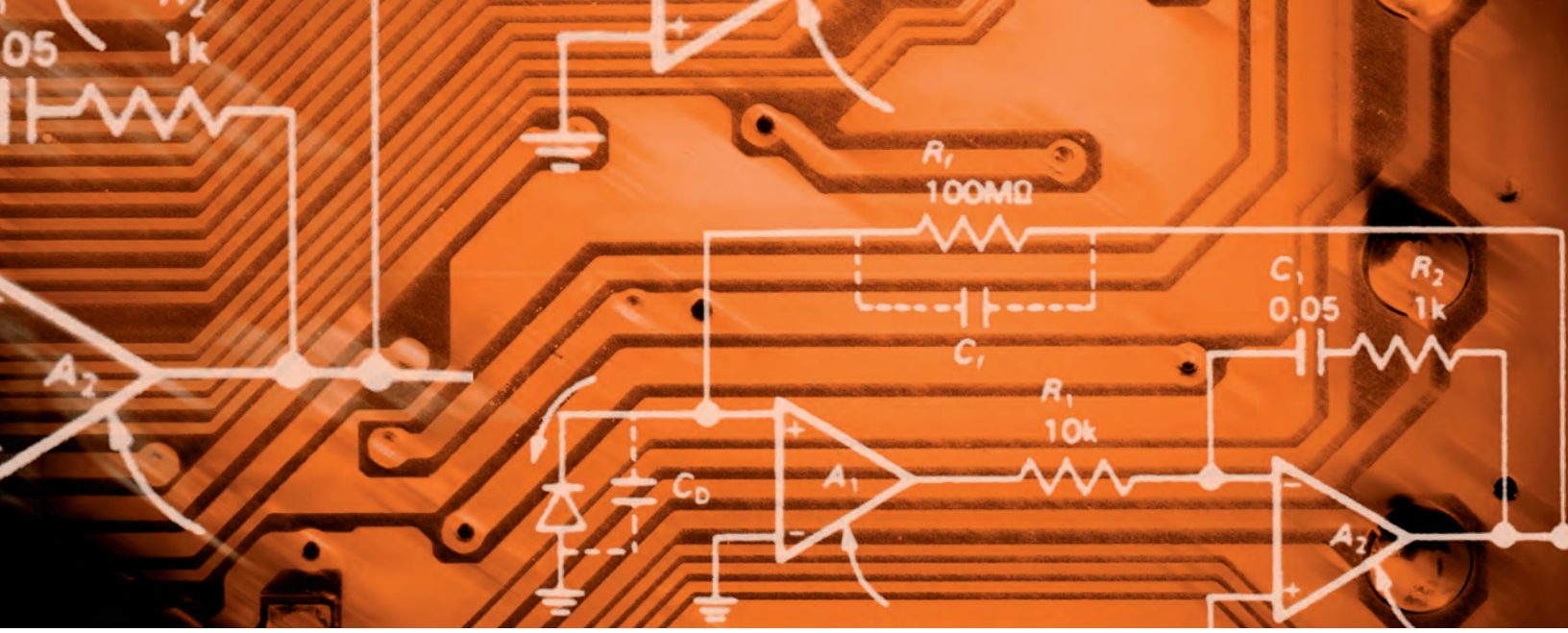


TECHNICAL SUPPORT AND CUSTOMER SERVICE

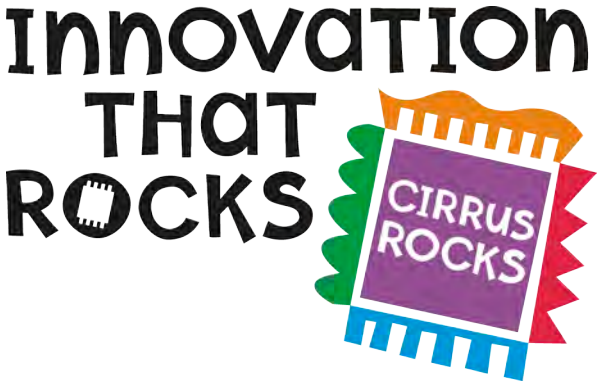
PRODUCT TECHNICAL SUPPORT

For product selection assistance, design suggestions, schematic review and circuit debugging with Apex Precision Power™ products, contact our team of dedicated power analog applications engineers.

Call Toll-Free +1-800-546-2739
eMail apex.support@cirrus.com

SALES SUPPORT

Sales support for Apex Precision Power products from Cirrus Logic is provided by our extensive network of worldwide third party sales representatives and distributors. Sample requests, pricing information and product volume orders can be obtained online under "Sales Support" at **www.cirrus.com**.



CORPORATE MISSION

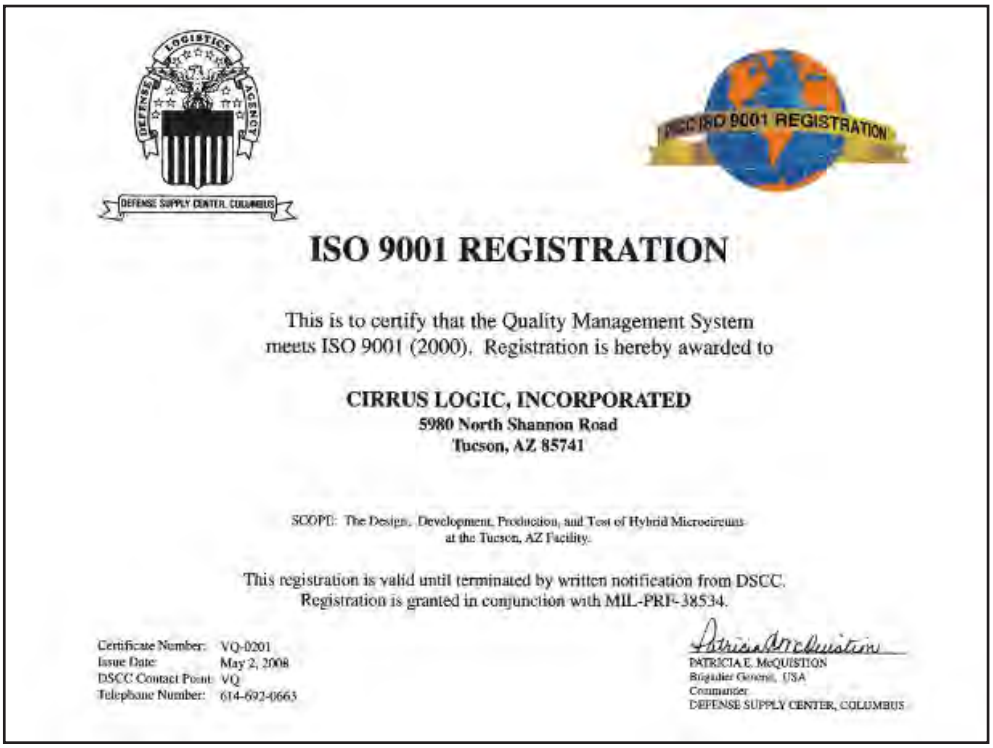
Cirrus Logic provides innovative, high-performance analog and digital signal processing components that "rock" (advance our customers, benefit our shareholders and reward our employees)

- To exceed our customers' expectations
- Deliver solid value to our shareholders
- Build confidence and pride in our company

NOTES:

Quality, Grade Comparisons, Screening Program , RoHS Compliance

B



ISO 9001 REGISTRATION

This is to certify that the Quality Management System meets ISO 9001 (2000). Registration is hereby awarded to

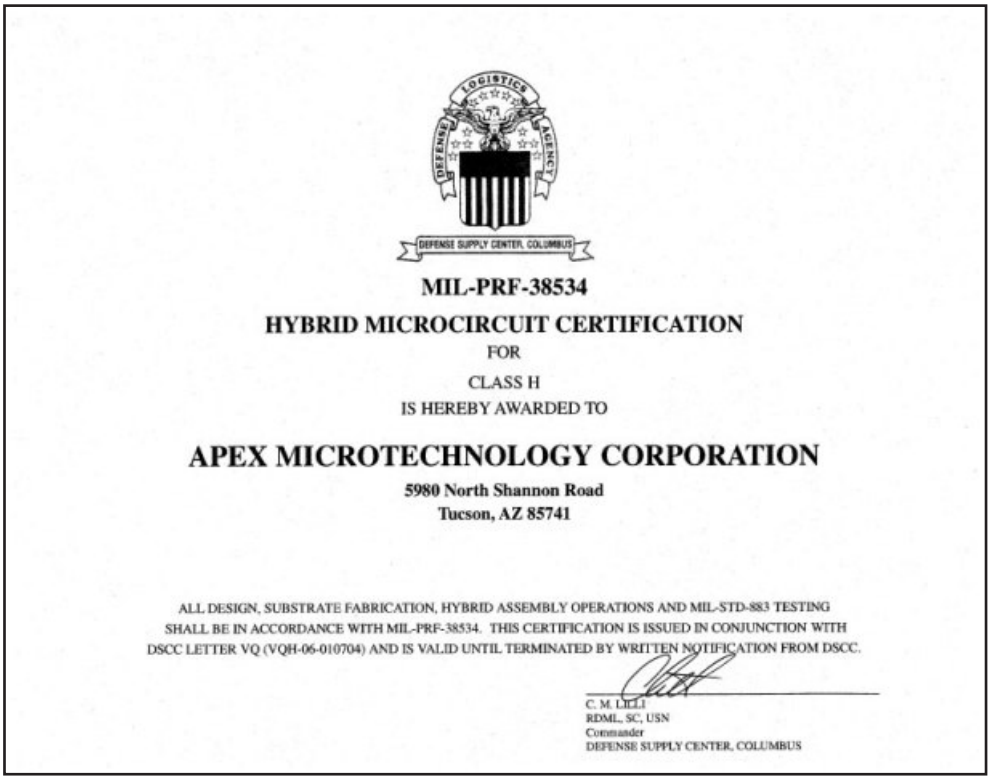
CIRRUS LOGIC, INCORPORATED
5980 North Shannon Road
Tucson, AZ 85741

SCOPE: The Design, Development, Production, and Test of Hybrid Microcircuits at the Tucson, AZ Facility.

This registration is valid until terminated by written notification from DSCC. Registration is granted in conjunction with MIL-PRF-38534.

Certificate Number: VQ-0201
Issue Date: May 2, 2008
DSCC Contact Point: VQ
Telephone Number: 614-692-0663

PATRICIA E. McQUISTION
Brigadier General, USA
Commander
DEFENSE SUPPLY CENTER, COLUMBUS



MIL-PRF-38534

HYBRID MICROCIRCUIT CERTIFICATION

FOR

CLASS H

IS HEREBY AWARDED TO

APEX MICROTECHNOLOGY CORPORATION

5980 North Shannon Road
Tucson, AZ 85741

ALL DESIGN, SUBSTRATE FABRICATION, HYBRID ASSEMBLY OPERATIONS AND MIL-STD-883 TESTING SHALL BE IN ACCORDANCE WITH MIL-PRF-38534. THIS CERTIFICATION IS ISSUED IN CONJUNCTION WITH DSCC LETTER VQ (VQH-06-010704) AND IS VALID UNTIL TERMINATED BY WRITTEN NOTIFICATION FROM DSCC.

C. M. LILLI
RDML, SC, USN
Commander
DEFENSE SUPPLY CENTER, COLUMBUS

See www.cirrus.com for current ISO9001 and MIL-PRF-38534 Certificates

Apex Precision Power™ Products Grade Comparisons: Industrial, Non-Compliant "M", /883 Military Grade

Apex Precision Power™ products from Cirrus Logic are available in different levels of quality screening: INDUSTRIAL, NON-COMPLIANT MILITARY or "M", and M/883 COMPLIANT MILITARY. All INDUSTRIAL grade products are 100% static and dynamic tested at +25°C. MILITARY grade product is 100% tested over the product's respective full temperature range for both static and dynamic parameters. Below is a re-cap of the static and dynamic test operations performed for each available grade.

OPERATION	INDUSTRIAL	NON-COMPLIANT "M"	/883 COMPLIANT MILITARY
Clean Room Procesing	Yes	Yes	Yes
Clean Room Testing	Yes	Yes	Yes
Solder Integrity Testing	Yes	Yes	Yes
Wire Bond Integrity	Yes	Yes	Yes
All Processing Under Document Control	Yes	Yes	Yes
High Power Die Inspection	No	Yes	Yes
Processed on Military Line	Yes	Yes	Yes
Maximum Number of Re-work Cycles Specified:			
Solder	Yes	Yes	Yes
Epoxy	No	Yes	Yes
Wirebond	Yes	Yes	Yes
Pre-cap Visual	Sample	100%	100%
Pre-seal Vacuum Bake	Yes	Yes	Yes
Welded in Controlled Atmosphere[2]	Yes	Yes	Yes
Each Unit Checked for Hermeticity[2]	No	Yes	Yes
Temperature Cycle: -65°C to +150°C for 10 cycles	No	Yes	Yes
Constant Acceleration Condition 5000G	No	Yes	Yes
Burn-In: 160 hours @ TC = 125°C	No	Yes	Yes
Dynamic Testing	+25°C	–55°C, +25°C, +125°C	–55°C, +25°C, +125°C
External Visual	Yes	Yes	Yes
Pin Finish	Ni or Solder	Solder	Solder

[1] Open Frame, Hybrid models
[2] Metal Packaged Hybrid models

Industrial and Military Products

Several Apex Precision Power™ products from Cirrus Logic are available with Standard Military Drawing (SMD) numbers. Below is a sample listing. Please check online at www.cirrus.com for updates.

BASE MODEL	STOCKED SMD #
PA02	5962-9067901HXA
PA07	5962-9063801HXA
PA08	5962-9072301HXA
PA09	5962-9170001HXA
PA10	5962-9082801HXA
PA12	5962-9065901HXA
PA51	5962-8762001,02YA
PA83	5962-9162101HXA
PA84	5962-9073601HXA

RoHS Compliance

Cirrus Logic is actively committed to our role in protecting the environment by reducing the amount of hazardous substances in our products. As a member of JEDEC, the semiconductor standardization body of the Electronics Industries Alliance (EIA), Cirrus Logic is working with customers and suppliers to comply with industry standards. The European Union has enacted legislation (Directive 2002/95/EC) effective July 1st, 2006, that restricts the use of Lead, Cadmium, Mercury, Hexavalent Chromium, Poly-Brominated Bi-Phenyls (PBB), and Poly-Brominated Di-Phenyl Ethers (PBDE) in a wide variety of electronic products and applications.

RoHS Compliant Devices

The following Apex Precision Power™ devices are RoHS compliant as of the date code listed. Please refer to the "Quality/RoHS" area for Apex Precision Power products at www.cirrus.com for the most current information regarding RoHS complaint status.

RoHS Compliant Monolithic Devices

The following Apex Precision Power™ monolithic devices are RoHS compliant sice release:

Model	Package
PA60EU	12 Pin Plastic SIP
PA69EU	12 Pin Plastic SIP
PA75CC	7DDPAK
PA75CD	7TO220
PA75CX	7TO220 SL
PA78DK	12 Pin PSOP
PA78EU	12 Pin Plastic SIP
PA79DK	12 Pin PSOP

Model	Package
PA86EU	12 Pin Plastic SIP
PA162DK	20 Pin PSOP
PA240CC	7DDPAK
PA240CX	7TO220 SL
CPA241	Die
PA241CE	TO-3
PA241DF	24 Pin PSOP
PA243DF	24 Pin PSOP

Model	Package
SA53-IHZ	64 Pin QFP
SA57-IHZ	64 Pin QFP
SA57A-FHZ	64 Pin QFP
SA303-IHZ	64 Pin QFP
SA306-IHZ	64 Pin QFP
SA306A-FHZ	64 Pin QFP

RoHS Compliant Hybrid Devices

The following Apex Precision Power™ hybrid devices from Cirrus Logic are RoHS compliant in both standard and A grades (e.g. the PA51 is listed; therefore, the PA51 and the PA51A are both compliant). For listed Voltage Regulators (VRE###), any devices listed are compliant in all grades (e.g. VRE100 is listed; therefore VRE100C, VRE100CA, VRE100M and VRE100MA are all compliant). Unless otherwise noted by a date, all devices below have been compliant since July 1, 2006, or earlier:

PA01	PA02	PA04	PA05	PA07	PA08	PA08V
PA09	PA10	PA12	PA12H	PA50	PA51	PA52
PA61	PA74	PA76	PA81J	PA82J	PA83	PA84
PA85	PA88	PA89	PA90 (5/25/09)	PA91 (5/25/09)	PA92 (5/25/09)	PA94 (1/15/09)
PA95 (5/25/09)	PA96CE	PA119	PB50	PB51 (5/25/09)	PB58	SA01
SA03	SA08	SA09 (since release)	SA12	SA60 (5/25/09)	SWR200	VRE100
VRE101	VRE102	VRE104	VRE107	VRE117	VRE119	VRE202
VRE204	VRE205	VRE210	VRE302	VRE304	VRE305	VRE306
VRE310	VRE405	VRE410	VRE505	VRE3025	VRE3041	VRE3050
VRE4112	VRE4125	VRE4141				

Non-RoHS Compliant Hybrid Devices

The following Apex Precision Power™ devices are not currently offered in a RoHS compliant package:

PA03	PA12A-S	PA13	PA15FL	PA16	PA93	PA97DR	PA98
PA241DW	SA50CE						

Non-RoHS Compliant Open Frame Products

The following Apex Precision Power™ devices are not currently offered in a RoHS compliant package:

MP38CL	MP39CL	MP108FL	MP111FL	MP230FC	MP240FC	MSA240KC	MSA260KC

RoHS Compliant Accessories

The following Apex Precision Power™ accessories are RoHS compliant:

DB53R	DB63R	DB64R	DB303R	CLAMP02	CLAMP04	CLAMP05	HS01
HS02	HS03	HS04	HS05	HS06	HS09	HS11	HS13
HS14	HS16	HS18	HS20	HS21	HS22	HS23	HS26
HS27	HS28	HS29	HS31	HS32	HS33	MS02	MS03
MS04	MS05	MS06	TW03	TW05	TW07	TW09	TW10
TW12	TW13	TW14					

Non-RoHS Compliant Accessories

The following Apex Precision Power™ devices are not currently offered in a RoHS compliant package:

EK01	EK03	EK06	EK07	EK09	EK11	EK13	EK14
EK15	EK16	EK17	EK19	EK21	EK26	EK27	EK28
EK29	EK33	EK34	EK42	EK50	EK51	EK52	EK56
EK57	EK59	EK60	EK61	EK65	EK-SA50	HK26	HS24
MS11							

Additional Information Regarding RoHS Compliance

1. Cirrus Logic is working on qualifying the following PSIP line of products to RoHS compliant versions by 9/30/09: PA13, PA15FL, PA16, PA93 and PA98. Other PSIP products will be introduced in RoHS compliant versions at a later date (PA241DW and PA97DR).
2. Due to the high power performance of Apex Precision Power™ products, a significant number of customer applications involve large-scale stationary industrial tools. The use of APEX products in “large scale industrial tools” is exempt under the RoHS directive, even if the product contains levels of RoHS prohibited materials higher than otherwise allowed. Please refer to websites such as www.pb-free.info/rohsexemptions.htm for specific details regarding this exemption.
3. At this time, Cirrus anticipates that certain APEX models will remain non-compliant due to physical or customer requirements. These models include PA03, PA03A, M/883 compliant devices, and ‘M’ grade devices (except for VRE series M grades).
4. Cirrus understands the lead and cadmium used in thickfilm hybrid applications (except for the VRE/SWR series) is exempt per points 5 and 38 respectively of the 2002/95/EC Annex. The VRE/SWR series are similarly exempt per points 5 and 8 of the 2002/95/EC Annex.

Disclaimer

Cirrus Logic will continue to pursue reasonable steps in providing representative and accurate information regarding product compliancy with the RoHS Directive. To the maximum extent permitted by law, Cirrus Logic shall not be liable for any indirect, special, incidental, consequential or any other exemplary damages arising out of the information provided herein, or arising out of its provision of non-RoHS compliant electronic products or materials.

Additional Assistance

For questions regarding the RoHS compliance status of Apex Precision Power™ products, please contact the Cirrus Logic Quality Engineering Team for Apex Precision Power products at apex.quality@cirrus.com.

M and /883 Screening Program

DESCRIPTION

Apex Precision Power™ products from Cirrus Logic have been screened to MIL-PRF-38534, Class H and manufactured in a DSCC Certified Facility using the baseline documents listed herein. These products provide a high reliability product option and satisfy the requirements for components used in airborne and ground-based military applications. Compliance with these requirements is signified by the "/883" suffix in the model number. "Non-compliant" version is identified using "M" only in the model number.

Complete description of an APEX "M" or "/883" product consists of the following:

1. **Industrial Grade Data Sheet** (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. **"M" Data Sheet** (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of –55°C to +125°C.
3. **"/883" Screening Program Data Sheet** (i.e. this document).
   This defines the manufacturing processes and screening steps for an "M" or "/883" product. (Refer to Figure 1 for order of flow.)
4. **Package and Accessories Information Data Sheet**
   This contains the package outline dimensions (i.e. 8-pin TO-3).
   All applications data and performance optimization suggestions given for the Industrial product apply to the "M" or "/883" versions of a given product family as well. Package outlines are identical except that the "M" or "/883" grade pins are hot solder dipped over nickel plating to meet the solderability requirements of MIL-STD-883, Method 2003.

QML-38534 FACILITY APPROVAL STATUS

The Cirrus Logic manufacturing facility for Apex Precision Power products in Tucson, AZ, USA, is a DSCC certified and qualified QML-38534 facility. Certification has been maintained since November 8, 1989, and a QML listing as of May 31, 1990.

CONSTRUCTION

These power products have been built and assembled using standard compliant hybrid processes including high temperature solder and conductive epoxy. A metallized ceramic (beryllia) substrate has thickfilm resistors, thickfilm gold conductors and thickfilm silver conductor. Die to substrate and pin to substrate wirebonds are aluminum. The package is hermetically sealed using resistance welding in a dry nitrogen atmosphere.

1.0 APPLICABLE DOCUMENTS

1.1 SPECIFICATIONS

MIL-PRF-38534 General Specification for Hybrid Microcircuits

1.2 STANDARDS

MIL-STD-883 Test Methods and Procedures for Microelectronics

1.3 BASELINE DOCUMENTS

Cirrus Logic maintains on file the procedures, process specifications and process qualification reports that are in general the documents which have established the baseline for Cirrus Logic in satisfying the requirements of certification in accordance with Appendix D of MIL-PRF-38534.

1.4 PERFORMANCE SPECIFICATIONS

The performance specifications for a particular "M" or "/883" hybrid circuit are contained in the following documents:

1. Industrial Grade Data Sheet (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. "M" Data Sheet (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of -55°C to +125°C.

In the event of conflicting requirements, the order of precedence will be: purchase order, customer's SCD, the APEX "M" data sheet, and other reference documents.

2.0 GENERAL REQUIREMENTS

The individual requirements are specified herein and in accordance with the applicable APEX "M" data sheet. The static and dynamic electrical performance requirements for the hybrid circuit and test conditions are as specified in the applicable APEX "M" data sheet.

2.1 PROCESS CONDITIONING, TESTING, RELIABIITY, and QUALITY ASSURANCE SCREENING

Process conditioning, screening and testing are as specified in Section 4.0. Figure 1 illustrates the process flow for "M" or "/883" products processed to MIL-PRF-38534, Class H.

2.1.1 PRODUCT or PROCESS CHANGE

Cirrus Logic will not implement any major change, as listed in MIL-PRF-38534, to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability, or interchangeability of the circuit without full or partial re-qualification. "M" product is a HI-REL non-compliant product.

2.2 QUALITY CONFORMANCE

The "M" or "/883" hybrid circuits furnished under this specification are products which have been produced and tested in conformance with all the provisions of this specification.

2.3 MARKING

2.3.1 MARKING EACH DEVICE

The following marking is placed on each product:

a) Index point (see 2.3.4)
b) Part number (see 2.3.5)
c) CAGE code number (see 2.3.6)
d) Lot identification code (see 2.3.7)
e) Manufacturer's identification (see 2.3.8)
f) Country of origin (see 2.3.9)
g) BeO warning (if applicable, see 2.3.10)
h) ESD identifier Δ

These units are Class 1 as defined in MIL-PRF-38534; therefore, the ESD identifier Δ is incorporated in the mark.

2.3.2 MARKING ON INITIAL CONTAINER

Marking on initial anti-static packaging for delivery includes:

a) Manufacturer's identification
b) Customer name
c) Customer's P.O. number
d) Quantity packaged
e) Lot code
f) Date packaged
g) Packaging operator's initials

2.3.3 MARKING PERMANENCE

Marking is permanent in nature to MIL-STD-883, Method 2015.

2.3.4 INDEX POINT

The index point, denoting location of Pin 1, is indicated as shown on the appropriate Package Outline.

2.3.5 PART NUMBER
The part number is the APEX generic part number and DSCC SMD part number, when applicable.

2.3.6 CAGE CODE NUMBER
The CAGE code number for APEX is 60024 as designated by the Federal government.

2.3.7 LOT IDENTIFICATION CODE
The lot identification and date code are shown as one alphanumeric string. The first 5 characters are the lot number identification. The last 4 digits are the date code as YYWW.

2.3.8 MANUFACTURER'S IDENTIFICATION
The manufacturer's identification is signified by the name, logo, or trademark of APEX incorporated in the mark.

2.3.9 COUNTRY OF ORIGIN
The country of origin is signified by USA incorporated in the mark.

2.3.10 BeO WARNING
Since hybrid circuits contain beryllium oxide substrates, the "BeO" identifier is marked on the package as an alert to the user, that if the package seal is broken, not to crush, machine, or subject the substrate to temperatures in excess of 850°C to avoid generating toxic fumes or inhalable particles.

3.0 CONDITIONS AND METHODS OF TEST
Conditions and methods of test are to MIL-PRF-38534 and as specified herein. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application. All tests are performed on a 100% basis except where indicated.

3.1 HIGH POWER DIE INSPECTION
High power die inspection is performed to MIL-STD-750 Method 2072 and 2073, and MIL-STD-883 Method 2010.

3.2 INTERNAL VISUAL INSPECTION (PRECAP)
Internal visual inspection is performed to MIL-STD-883, Method 2017 and 2032.

3.3 TEMPERATURE CYCLING
Temperature cycling is performed to MIL-STD-883, Method 1010, Condition C, using 10 cycles from –65°C to +150°C.

3.4 BURN-IN
Burn-in is performed to MIL-STD-883, Method 1015, Condition D for 160 hours at a case temperature of 125°C.

3.5 CONSTANT ACCELERATION
Constant acceleration is performed to MIL-STD-883, Method 2001, Condition A, at 5,000 G's, in the Y1 axis only.

3.6 FINAL ELECTRICAL TEST
Final electrical tests are performed to MIL-PRF-38534*. Both static and dynamic parameters from Group A, Subgroups 1-6, are 100% tested to the "M" data sheet limits at –55°C, +25°C and +125°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to static (DC) measurements at +25°C.

3.7 HERMITICITY
Hermiticity tests are performed per the following:

3.7.1 FINE LEAK TESTING
Fine leak testing is performed to MIL-STD-883, Method 1014, Condition A2, at $1X10^{-7}$ cc/sec standard leak rate.

3.7.2 GROSS LEAK TESTING
Gross leak testing is performed to MIL-STD-883, Method 1014, Condition C, at 60 PSIG pre-pressurization.

3.8 EXTERNAL VISUAL INSPECTION
All “M” and “/883” circuits receive external visual to MIL-STD-883, Method 2009.

4.0 QUALITY ASSURANCE PROVISION* SEE FIGURE 1.
4.1 QUALITY CONFORMANCE INSPECTION
Quality Conformance Inspection (QCI) is to MIL-PRF-38534, Option 1, in-line qualification method. Lots failing to meet quality conformance inspection for a given product assurance level are rejected.

4.1.1 GROUP A ELECTRICAL TESTING
Group A electrical testing is performed using in-line verification in accordance with Option 1 of MIL-PRF-38534. Electrical parameters and test limits are as shown in the “M” data sheet.

4.1.2 GROUP B INSPECTION
Group B inspection is satisfied by performing in-line inspection sampling, to MIL-PRF-38534, Option 1.

4.1.3 GROUP C INSPECTION
Group C inspection is performed on the first lot submitted for inspection and as required to evaluate or qualify changes in manufacturing processes per MIL-PRF-38534, Option 1.

4.1.4 GROUP D INSPECTION
Group D testing in accordance with MIL-PRF-38534, Option 1, is accomplished during package evaluation at in-coming inspection and is not repeated.

5.0 DATA AND REPORTS*
5.1 CERTIFICATE of COMPLIANCE
All “/883” circuits are accompanied by a Certificate of Compliance.

5.2 QUALITY CONFORMANCE REPORTS
MIL-PRF-38534, Option 1, Group A lot data is kept on file with the production records. In-line Groups B, C and D (reference 4.1.4) generic data is also on file.

5.3 TRACEABILITY
Traceability is in accordance with MIL-PRF-38534. Each circuit is traceable to the production lot. Re-worked or repaired circuits maintain traceability.

6.0 PACKAGING
Packing and packaging are to MIL-STD-2073/1D.

7.0 CUSTOM MARKING
Production quantities of “M” and “/883” devices may be dual or solely marked with an applicable SCD number.

* Applies to compliant (/883) product only.

FIGURE 1: CIRRUS LOGIC MILITARY PROCESS FLOW FOR APEX PRECISION POWER™ PRODUCT

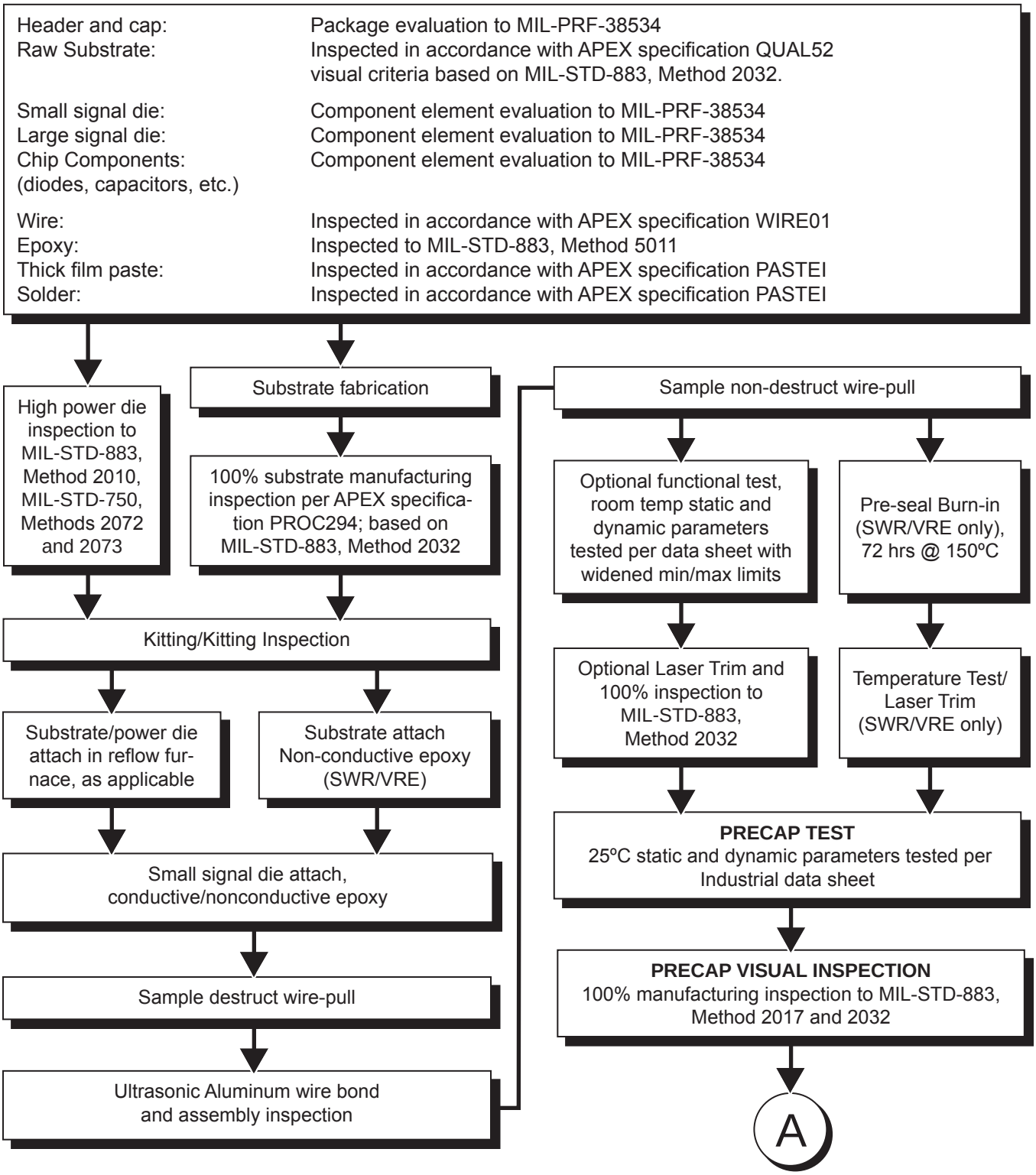
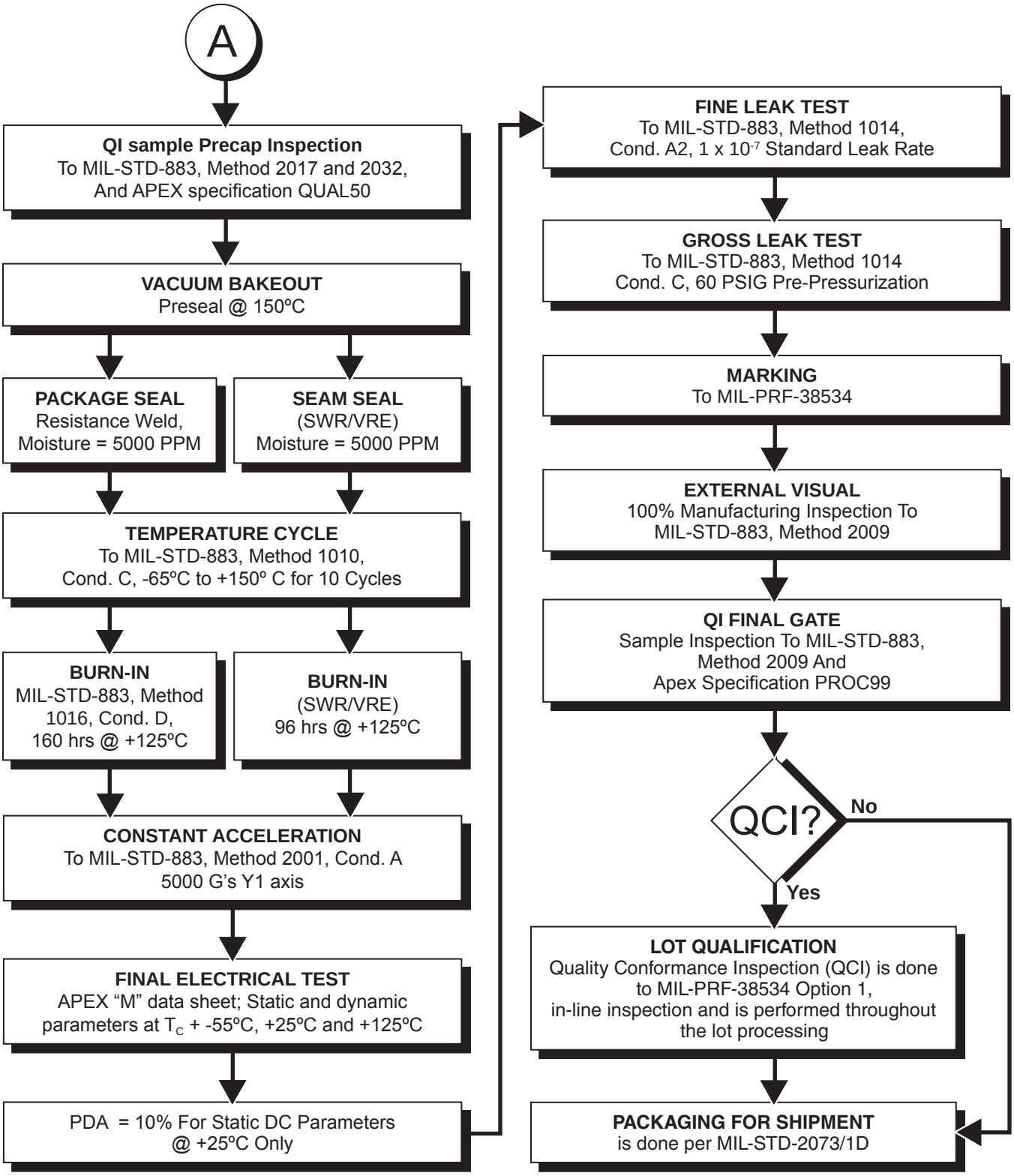
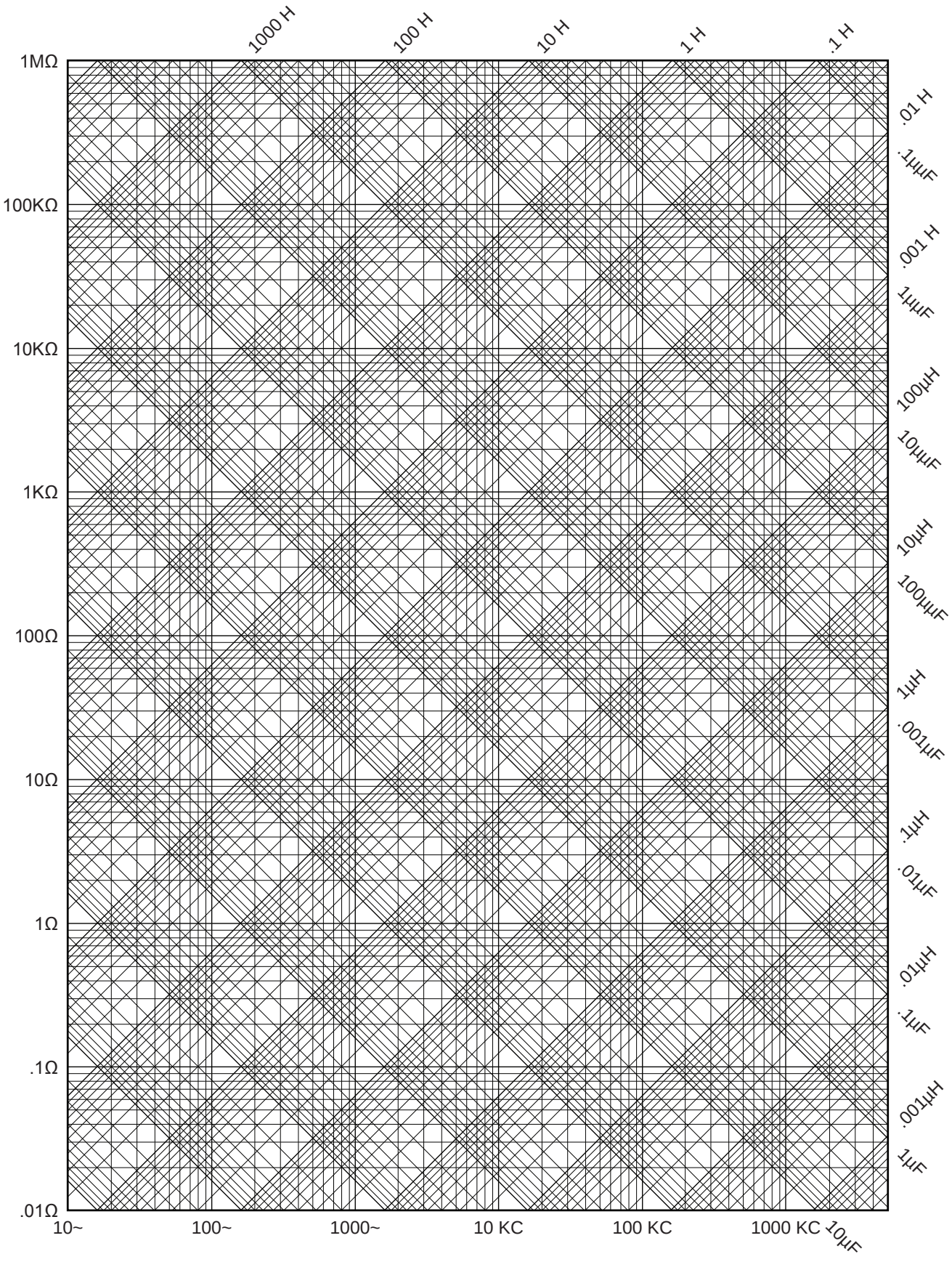


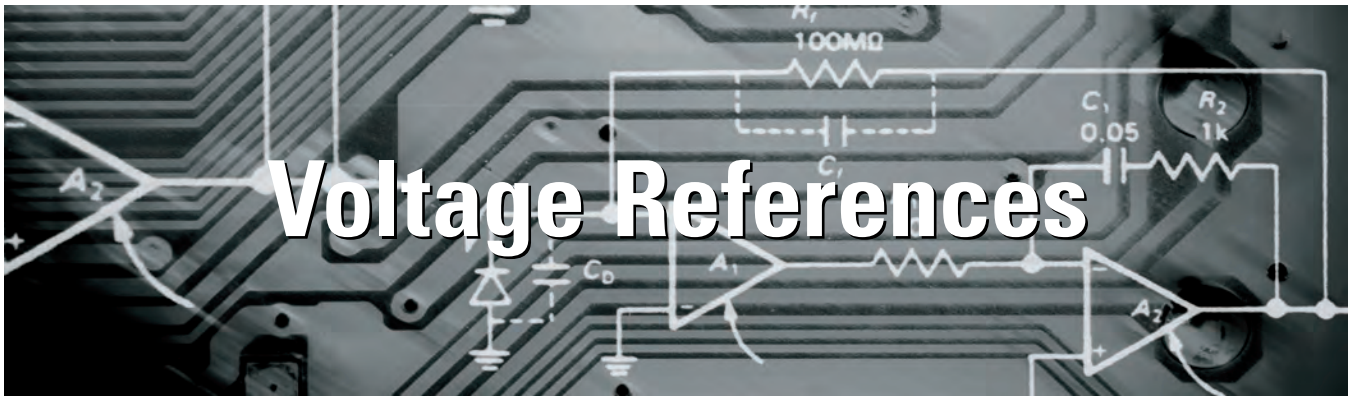
FIGURE 1: CIRRUS LOGIC MILITARY PROCESS FLOW FOR APEX PRECISION POWER™ PRODUCT



Reactance Chart



NOTES:



Voltage References

C

Precision Sine Wave Reference

FEATURES

- Very High Accuracy: +7.071 Vrms ±0.05%
- Extremely Low Drift: 30 ppm/°C (-55°C to +125°C)
- Excellent Stability: 10 ppm/1000 Hrs. Typical
- Low Distortion: 0.1% Thd @ f = 3300 Hz
- Hermetic 14-pin Ceramic DIP
- Military Processing Option

APPLICATIONS

- Transducer Excitation
- High Resolution Servo Systems
- High Precision Test and Measurement Instruments
- AC Voltage Standard
- L_{VDT} Or R_{VDT} Reference
- Multiplying D/A Reference

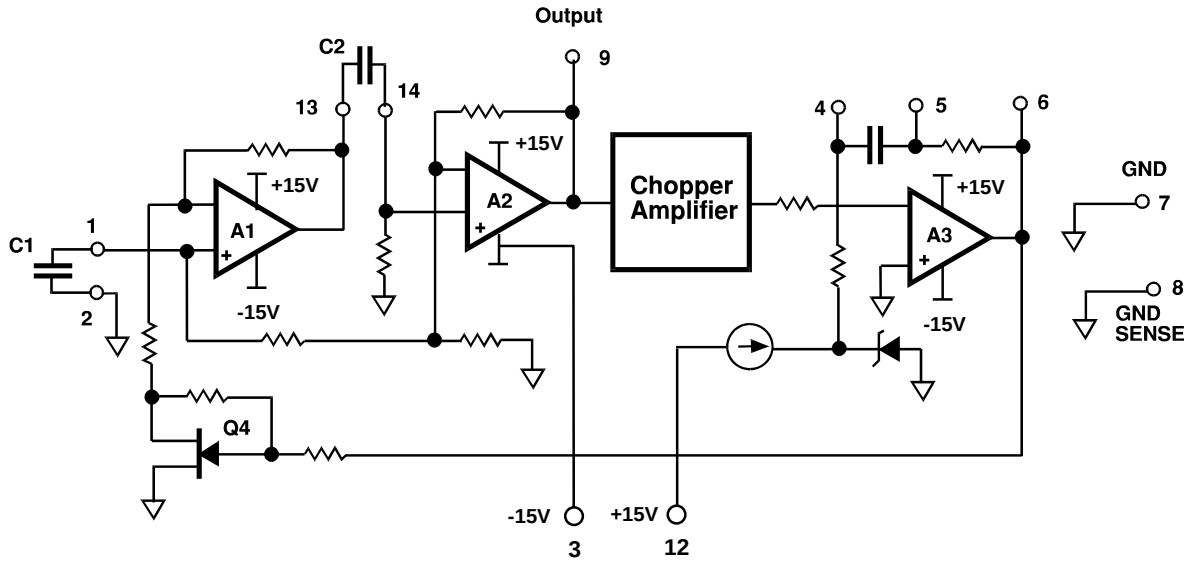
DESCRIPTION

SWR200 is a Precision Sine Wave Reference providing an ultra stable sine wave output of +7.071 V at ±0.05% initial accuracy and temperature coefficient as low as 30 ppm/°C over the full military temperature range. The extreme accuracy is made possible by a chopper-based AGC circuit. The temperature characteristic of the chopper circuit compensates the typical nonlinearity of the internal DC zener reference, resulting in a nearly linear amplitude-temperature characteristic. Frequency of the SWR200 is programmable with two external capacitors.

The SWR200 is available in a 14-pin bottom braze package. They are hermetically sealed and “M” versions are screened for high reliability and quality.

SWR200 is well suited for any application requiring a stable sine wave source. The SWR200 can be used as a reference source in precision sensing systems based on L_{VDT} or R_{VDT} position sensors. A programmable AC reference can be constructed using the SWR200 as a reference for a high accuracy multiplying Digital to Analog Converter.

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Type	Output (Typ.)	Temperature Operating Range	Package
SWR200C	+7.071V	-25°C to +85°C	DIP
SWR200M	+7.071V	-55°C to +125°C	DIP

Hermetic 14-pin Ceramic DIP
Package Style HC

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25°C, R_L = 10KΩ UNLESS OTHERWISE NOTED.

Model	SWR200C			SWR200M			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	±13.5	±15	±22	*	*	*	V
Operating Temperature	-25		+85	-55		+125	ºC
Storage Temperature	-65		+85	*		*	ºC
Short Circuit Protection		Continuous			*		Vrms
OUTPUT VOLTAGE		7.071			*		V
OUTPUT VOLTAGE ERRORS							
Initial Error			±0.05			*	%
Warmup Drift		100			*		µV
DC Offset			3			*	mV
DC Offset Over Temp.		3	18		*	*	µV/ ºC
T_{MIN} - T_{MAX}		1	20.0		1	30.0	ppm/ ºC
Long-Term Stability		10			*		ppm/ ºC
OUTPUT CURRENT							
Range	±10			*			mA
REGULATION							
Line		10			*		ppm/V
Load		3			*		ppm/mA
POWER SUPPLY CURRENTS							
+PS		10.5	13		*	*	mA
-PS		9.5	13		*	*	mA
DISTORTION			0.5			*	%
FREQUENCY							
Range (f) $f = \frac{10^{-5}}{\sqrt{C_1 C_2}}$	.98	1	1.02	*	*	*	Hz
	400		10K	*		*	Hz
$\frac{\Delta f}{f}$ vs. temperature			15			*	ppm/ºC

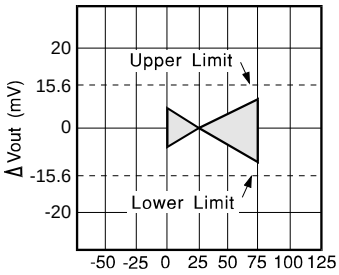
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at +25°C over the specified operating temperature range.
2. The specified values are unloaded.
3. Pin 8 is internally connected to Pin 7 and can be used as Ref. GND.
4. The frequency range can be extended to any desired lower value by using 2 external AGC capacitors (see AN-3).
5. The increase in distrotion at lower frequencies can be eliminated by using external AGC capacitors (see AN-3).

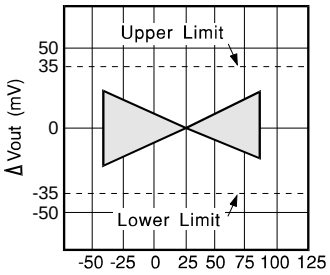
2. TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



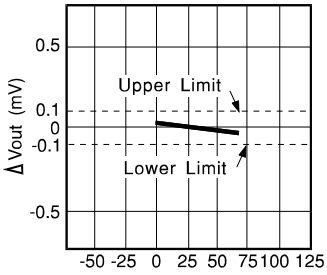
Temperature °C
SWR200C

V_{OUT} vs. TEMPERATURE



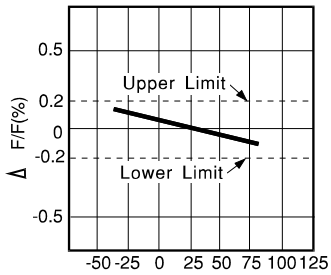
Temperature °C
SWR200M

% Δ FREQ. vs. TEMP.



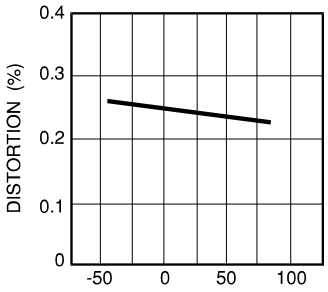
Temperature °C
SWR200C

% Δ FREQ. vs. TEMP.



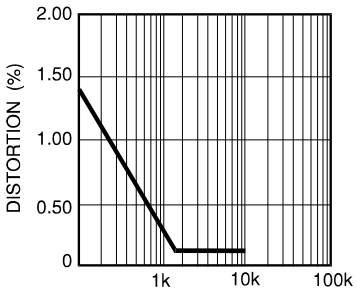
Temperature °C
SWR200M

DISTORTION VS. TEMP



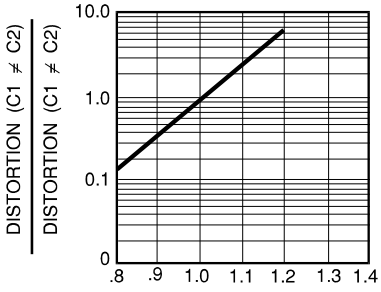
Temperature °C

DISTORTION vs. FREQUENCY



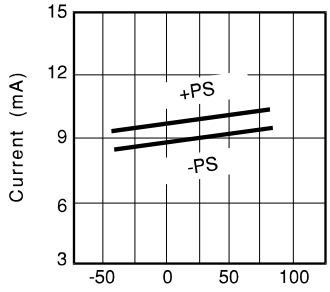
Frequency (Hz)

NORMALIZED DISTORTION vs. C2/C1



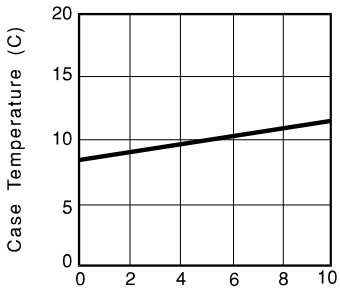
C2/C1

POWER SUPPLY CURRENT vs. TEMP.



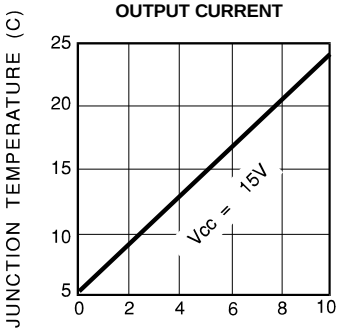
Temperature °C

CASE TEMP. RISE ABOVE AMBIENT vs. OUTPUT CURRENT



Output Current (mA)

JUNCTION TEMP. RISE ABOVE CASE TEMP. vs OUTPUT CURRENT



Output Current (mA)

3. THEORY OF OPERATION

The following refers to the schematic in Figure 1. A1 and A2 are connected as a phase-shift oscillator circuit with the frequency set by the external capacitors C1 and C2. Q4 is included in the feedback loop of A1 as a gain control element.

The oscillator output is fed to the chopper amplifier which develops an absolute value representation of the oscillator output. The chopper output is compared to a precision DC reference in integrator amplifier A3. This DC error signal is used ot control the gain setting FET Q4.

As in all precision zener based DC references, the drift of the zener becomes nonlinear at temperature extremes. The chopper amplifier drift characteristic is complementary to this nonlinearity and compensates for the reference drift.

4. APPLICATION INFORMATION

Figure 1 shows the connections for the SWR200 including the two frequency setting capacitors. The frequency is:

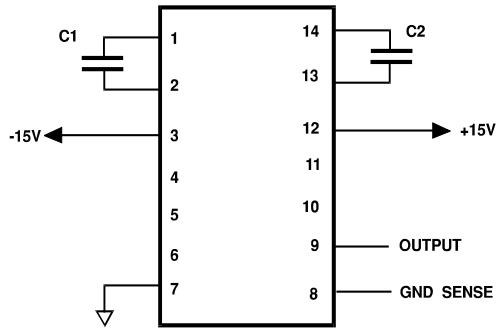
$$f = \frac{10^{-5}}{\sqrt{C_1 C_2}}$$

The frequency stability is directly related to the stability of the capacitors, therefore stable capacitors like NPO ceramic, or polycarbonate or polystyrene film should be used.

Two separate ground pins are provided for accurate ground sensing. This minimizes errors due to drops in the ground pin which can become a significant source of error in sockets.

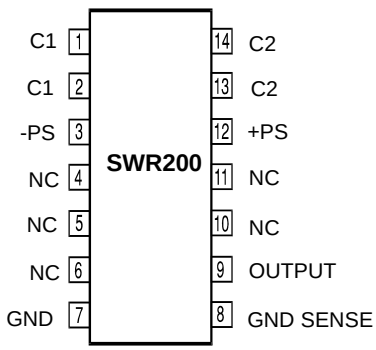
The offset of the SWR200 is fully specified for initial offset and drift and is low enough that it can normally be neglected. In applications which are especially sensitive to offset the output can be AC coupled. Proper capacitor sizing and high impedance sensing will minimize errors due to capacitive coupling.

EXTERNAL CONNECTIONS



PIN CONFIGURATION

TOP VIEW



Precision Voltage Reference

FEATURES

- Very High Accuracy: ±10 V Output, ±0.5 mV
- Extremely Low Drift: 0.5 ppm/ºC (-55ºC to +125ºC)
- Low Warm-up Drift: 1.0 ppm Typical
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 3 ppm/V Typical
- Hermetic 14-pin Ceramic DIP
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

DESCRIPTION

VRE100 Series Precision Voltage References provide ultrastable +10 V (VRE100), -10 V (VRE101) and ±10 V (VRE102) outputs with ±0.5 mV initial accuracy and temperature coefficient as low as 0.5 ppm/°C over the full military temperature range. This improvement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique.

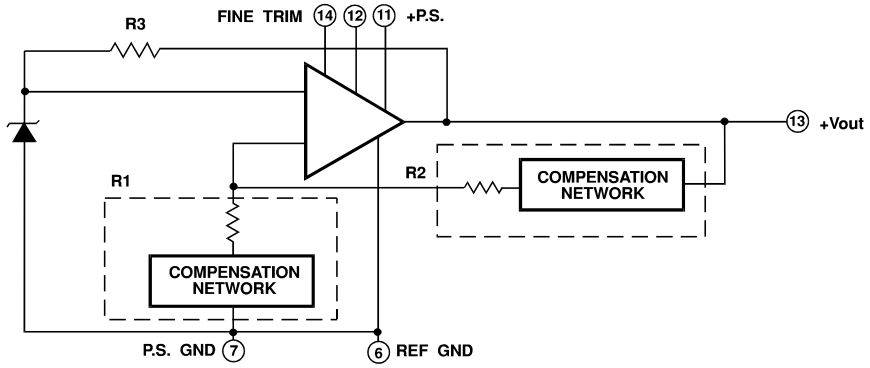
Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE100 series the most accurate and stable 10 V reference available.

VRE100/101/102 devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two performance grades. All devices are packaged in 14-pin hermetic ceramic packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

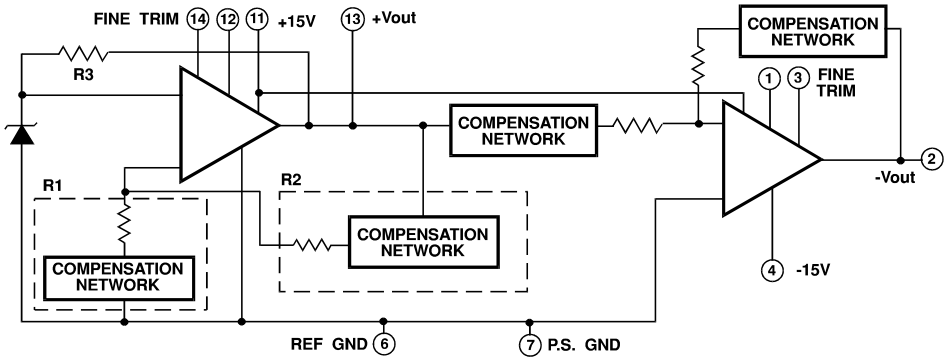
Superior stability, accuracy, and quality make these references ideal for precision applications such as A/D and D/A converters, high-accuracy test and measurement instrumentation, and transducer excitation.

Figure 1. BLOCK DIAGRAMS

VRE100



VRE102



1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25°C, R_L = 10K UNLESS OTHERWISE NOTED.

Grade	C			CA			M			MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS													
Power Supply	±13.5		±22	*		*	*		*	*		*	V
Operating Temperature	-25		+85	*		*	-55		+125	-55		+125	ºC
Storage Temperature	-65		+150	*		*	*		*	*		*	ºC
Short Circuit Protection	Continuous			*			*			*			
OUTPUT VOLTAGE													
VRE100		+10			*			*			*		V
VRE101		-10			*			*			*		V
VRE102		±10			*			*			*		V
OUTPUT VOLTAGE ERRORS													
Initial Error			±1.0			±0.5			±1.5			±0.8	mV
Warmup Drift		2			1			2			1		ppm
T_{MIN} - T_{MAX} (Note1)			0.6			0.3			1.0			0.5	mVz
Long-Term Stability		6			*			*			*		ppm/1000hrs
Noise (0.1 - 10Hz)		6			*			*			*		µVpp
OUTPUT CURRENT													
Range	±10			*			*			*			mA
REGULATION													
Line		3	10		*	*		*	*		*	*	ppm/V
Load		3			*			*			*		ppm/mA
OUTPUT ADJUSTMENT													
Range		20			*			*			*		mV
Temperature Coefficient		4			*			*			*		V/ºC/mV
POWER SUPPLY CURRENT (Note 2)													
VRE100 +PS		5	7		*	*		*	*		*	*	mA
VRE101 -PS		5	7		*	*		*	*		*	*	mA
VRE102 +PS		7	9		*	*		*	*		*	*	mA
VRE102 -PS		4	6		*	*		*	*		*	*	mA

NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE100C	+10	-25°C to +85°C	±0.6mV
VRE100CA	+10	-25°C to +85°C	±0.3mV
VRE100M	+10	-55°C to +125°C	±1.0mV
VRE100MA	+10	-55°C to +125°C	±0.5mV
VRE101C	-10	-25°C to +85°C	±0.6mV
VRE101CA	-10	-25°C to +85°C	±0.3mV
VRE101M	-10	-55°C to +125°C	±1.0mV
VRE100MA	-10	-55°C to +125°C	±0.5mV
VRE102C	±10	-25°C to +85°C	±0.6mV
VRE102CA	±10	-25°C to +85°C	±0.3mV
VRE102M	±10	-55°C to +125°C	±1.0mV
VRE102MA	±10	-55°C to +125°C	±0.5mV

Hermetic 14-pin Ceramic DIP
Package Style HC

2. THEORY OF OPERATION

The following discussion refers to the block diagrams in Figure 1. In operation, approximately 6.3 volts is applied to the noninverting input of the op amp. The voltage is amplified by the op amp to produce a 10.000 V output. The gain is determined by the networks R1 and R2: G=1 + R2/R1. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The zener operating current is derived from the regulated output voltage through R3. This feedback arrangement provides a closely regulated zener current. This current determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, this series produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, we produce a voltage reference that also has very good long term stability.

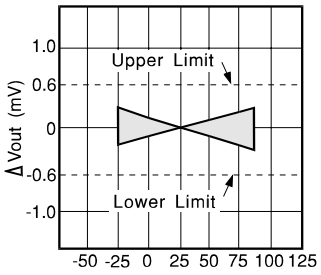
3. APPLICATION INFORMATION

Page 5 shows the proper connection of the VRE100 series voltage reference with the optional trim resistors. When trimming the VRE102, the positive voltage should be trimmed first since the negative voltage tracks the positive side. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE100 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't effect performance. The VRE series voltage references can be connected with or without the use of pin 6 and still provide superior performance.

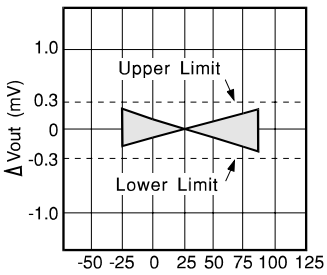
4. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



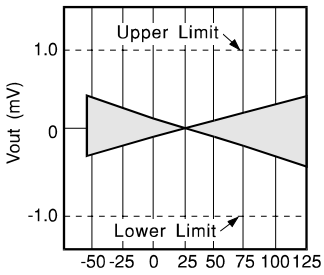
Temperature °C
VRE100/101/102C

V_{OUT} vs. TEMPERATURE



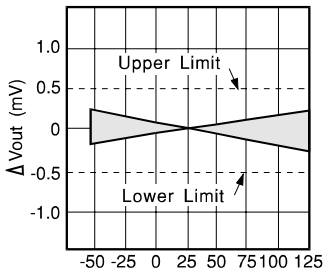
Temperature °C
VRE100/101/102CA

V_{OUT} vs. TEMPERATURE



Temperature °C
VRE100/101/102M

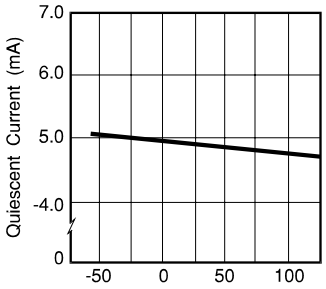
V_{OUT} vs. TEMPERATURE



Temperature °C
VRE100/101/102MA

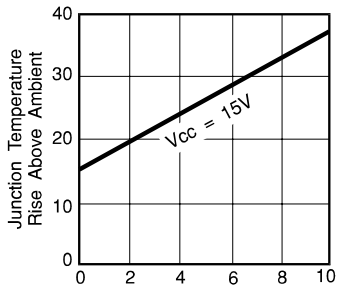
VRE100/101

QUIESCENT CURRENT VS. TEMP



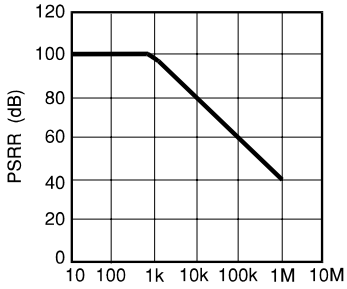
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY

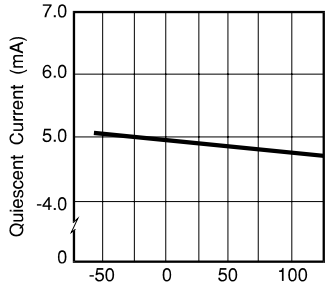


Frequency (Hz)

VRE102

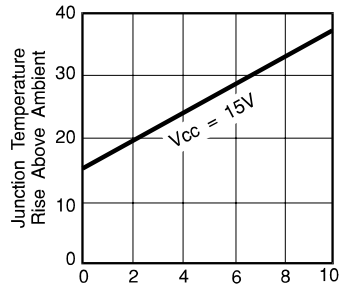
POSITIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



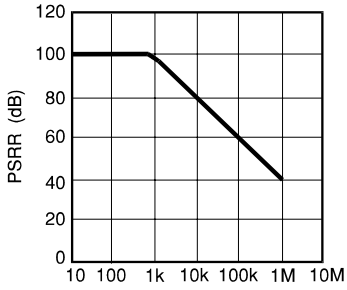
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

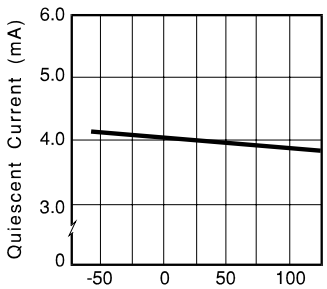
PSRR VS. FREQUENCY



Frequency (Hz)

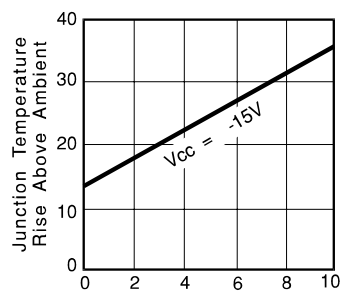
NEGATIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



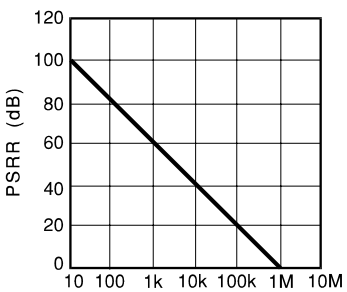
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



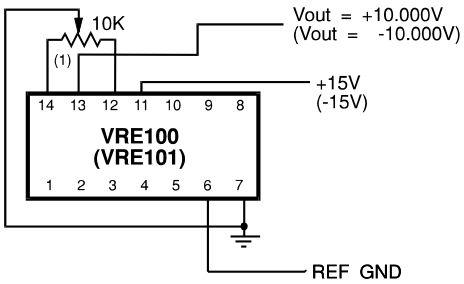
Output Current (mA)

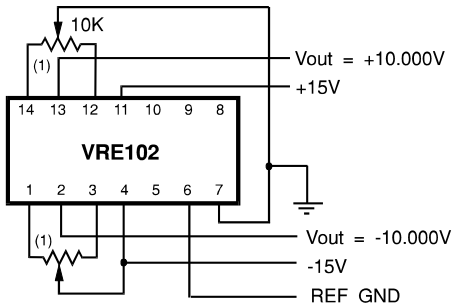
PSRR VS. FREQUENCY



Frequency (Hz)

EXTERNAL CONNECTIONS

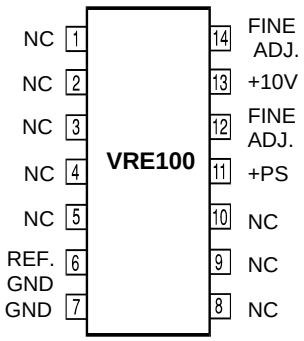




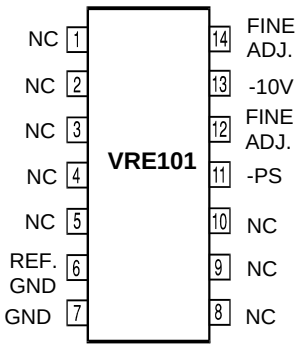
1. Optional Fine Adjust for approximately ±20mV. VRE101 center tap connects to -PS.

PIN CONFIGURATION

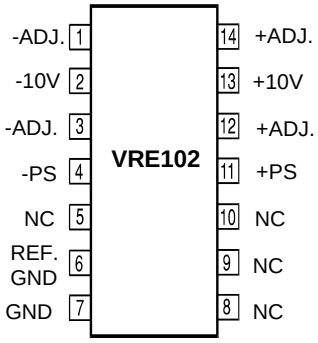
TOP VIEW



TOP VIEW



TOP VIEW



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- Very High Accuracy: +4.5 V Output, ±0.4 mV
- Extremely Low Drift: 0.6 ppm/°C (-55°C to +125°C)
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 6 ppm/V Typical
- Wide Supply Range: ±13.5 to ±22.0 V
- Hermetic 14-pin Ceramic DIP
- Military Processing Options

APPLICATIONS

- Precision A/D And D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

DESCRIPTION

VRE104 Series Precision Voltage References provide ultrastable +4.5 V outputs with up to ±0.4 mV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range.

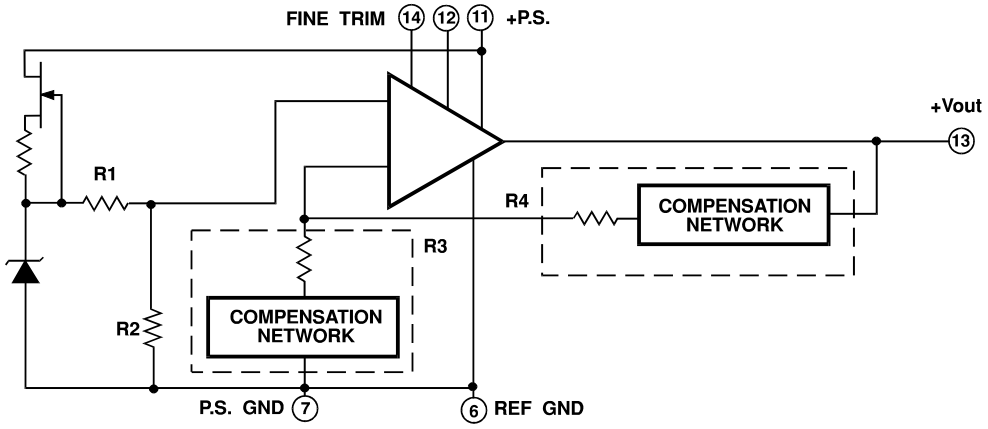
These references are specifically designed to be used with the Crystal Semiconductor line of successive-approximation type Analog to Digital Converters (ADCs). This line of ADCs sets new standards for temperature drift, which can only be as good as the external reference used. The VRE104 combined with an ADC will provide the lowest drift data conversion obtainable.

VRE104 series devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two performance grades. All devices are packaged in 14-pin hermetic ceramic packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

Superior stability, accuracy, and quality make the VRE104 ideal for all precision applications which may require a 4.5 V reference. High-accuracy test and measurement instrumentation, and transducer excitation are some other applications which can benefit from the high accuracy of the VRE104.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE104C VRE104CA	+4.5 +4.5	-25°C to +85°C -25°C to +85°C	±0.4mV ±0.2mV
VRE101M VRE100MA	+4.5 +4.5	-55°C to +125°C -55°C to +125°C	±0.6mV ±0.3mV

Hermetic 14-pin Ceramic DIP
Package Style HC

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =+15V, T = 25°C, R_L = 10K Ω UNLESS OTHERWISE NOTED.

Grade	VRE104C			VRE104CA			VRE104M			VRE104MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS													
Power Supply	±13.5		±22	*		*	*		*	*		*	V
Operating Temperature	-25		+85	*		*	-55		+125	-55		+125	ºC
Storage Temperature	-65		+150	*		*	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*			*		
OUTPUT VOLTAGE													
VRE104		+4.5			*			*			*		V
OUTPUT VOLTAGE ERRORS													
Initial Error			±800			±400			±800			±400	µV
Warmup Drift		2			1			2			1		ppm
T_{MIN} - T_{MAX} (Note1)			400			200			600			300	µV
Long-Term Stability		6			*			*			*		ppm/1000hrs
Noise (0.1 - 10Hz)		3			*			*			*		µVpp
OUTPUT CURRENT													
Range	±10			*			*			*			mA
REGULATION													
Line		6	10		*	*		*	*		*	*	ppm/V
Load		3			*			*			*		ppm/mA
OUTPUT ADJUSTMENT													
Range		10			*			*			*		mV
Temperature Coefficient		4			*			*			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)													
VRE104 +PS		5	7		*	*		*	*		*	*	mA

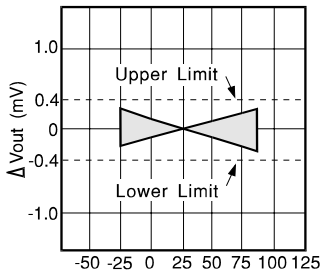
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

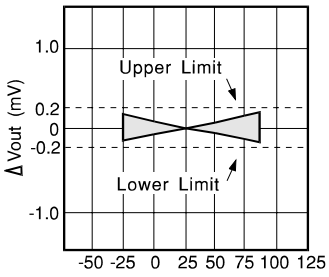
2. TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



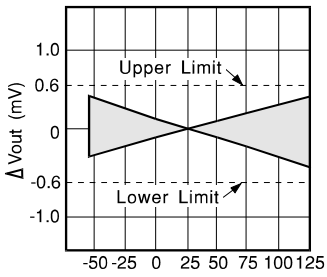
Temperature °C
VRE104C

V_{OUT} vs. TEMPERATURE



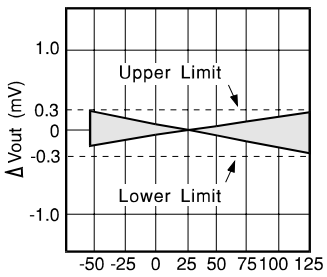
Temperature °C
VRE104CA

V_{OUT} vs. TEMPERATURE



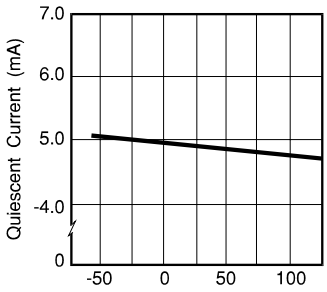
Temperature °C
VRE104M

V_{OUT} vs. TEMPERATURE



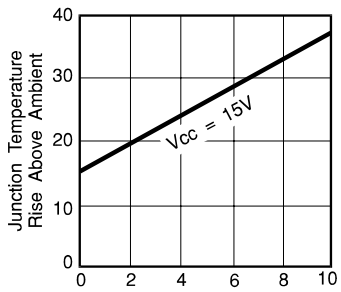
Temperature °C
VRE104MA

QUIESCENT CURRENT VS. TEMP



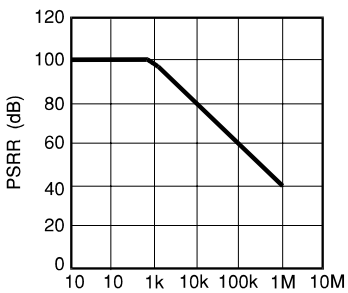
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 4.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear, this method leaves a residual error over wide temperature ranges.

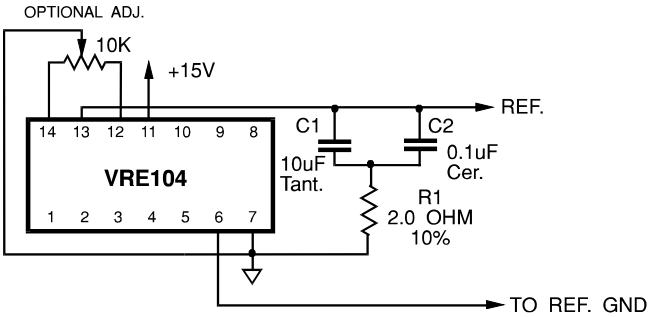
To remove this residual error, a nonlinear compensation network of thermistors and resistors has been developed that is used in the VRE104 series references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, the VRE104 series produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

4. APPLICATION INFORMATION

The proper connection of the VRE104 series voltage references is shown below with the optional trim resistors. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

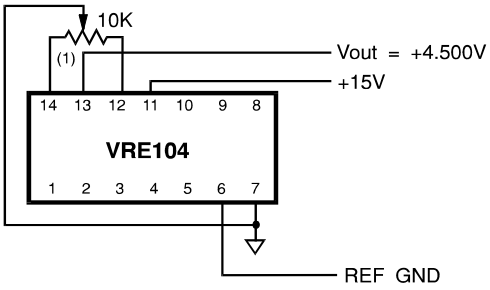
The VRE104 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

VRE104 Used With Crystal Semiconductor ADC



Suggested Reading: Crystal Semiconductor Application Note -
“Voltage References for the CS501X/CS25IIX Series of A/D Converters"

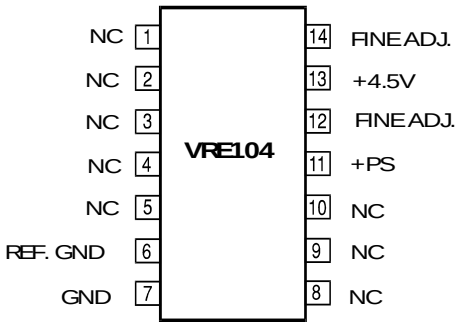
EXTERNAL CONNECTIONS



1. Optional Fine Adjust for approximately ±10mV.

PIN CONFIGURATION

TOP VIEW



Precision Voltage Reference

FEATURES

- Very High Accuracy: ±5 V, ±0.4 mV
- Extremely Low Drift: 0.6 ppm/°C (-55°C to +125°C)
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 6 ppm/V Typical
- Wide Supply Range: ±13.5 V to ±22 V
- Hermetic 14-pin Ceramic DIP
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

DESCRIPTION

VRE107 Series Precision Voltage References provide ultrastable ±5 V outputs with ±0.4 mV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range. This impovement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique.

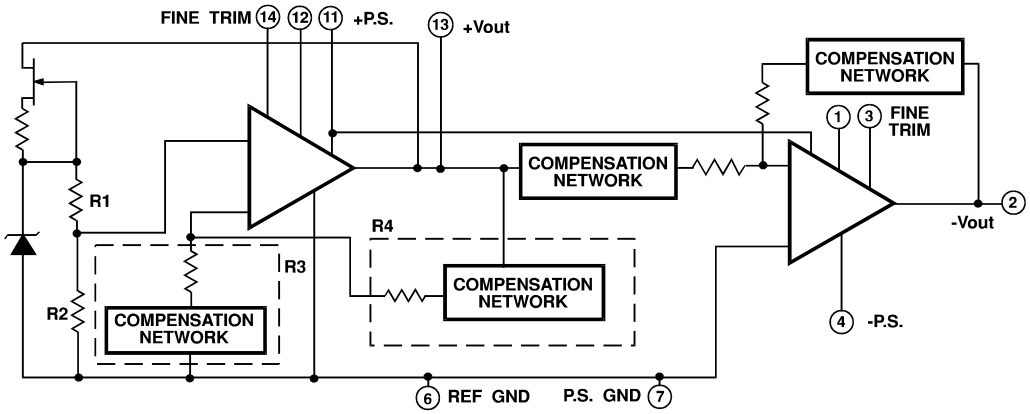
Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE107 series the most accurate and stable 5 V references available.

VRE107 series devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two performance grades. All devices are packaged in 14-pin hermetic ceramic packages for maximum long-term stablity. “M” versions are screened for high reliability and quality.

Superior stability, accuracy, and quality make these references ideal for precision applications such as A/D and D/A converters, high accuracy test and measurement instrumentation, and tranducer excitation.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE107M	±5	-55°C to +125°C	±0.6mV
VRE107MA	±5	-55°C to +125°C	±0.3mV

Hermetic 14-pin Ceramic DIP
Package Style HC

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25°C, R_L = 10K Ω UNLESS OTHERWISE NOTED.

Model	VRE107M			VRE107MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	±13.5		±22	*		*	V
Operating Temperature	-55		+125	*		*	ºC
Storage Temperature	-65		+150	*		*	ºC
Short Circuit Protection		Continuous			*		
OUTPUT VOLTAGE							
VRE107		±5			*		V
OUTPUT VOLTAGE ERRORS							
Initial Error			±800			±400	µV
Warmup Drift		2			1		ppm
T_{MIN} - T_{MAX} (Note1)			600			300	µV
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz)		3			*		µVpp
OUTPUT CURRENT							
Range	±10			*			mA
REGULATION							
Line		6	10		*	*	ppm/V
Load		3			*		ppm/mA
OUTPUT ADJUSTMENT							
Range		10			*		mV
Temperature Coefficient		4			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)							
VRE107 +PS		7	9		*	*	mA
VRE107 -PS		4	6		*	*	mA

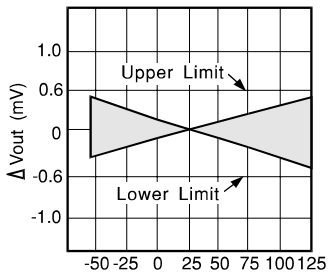
NOTES:

* Same as M Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

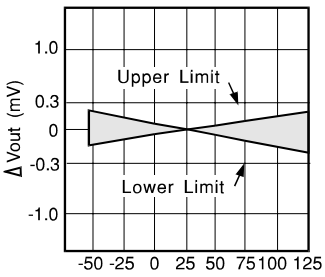
TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



Temperature °C
VRE107M

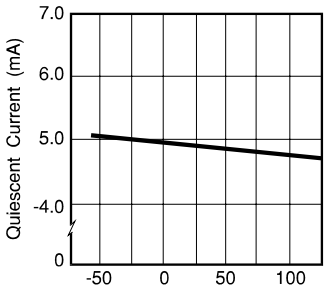
V_{OUT} vs. TEMPERATURE



Temperature °C
VRE107MA

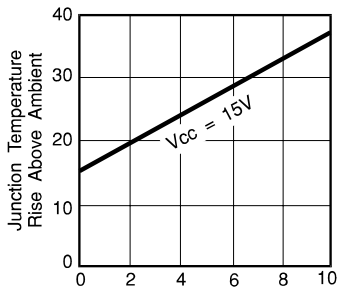
POSITIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



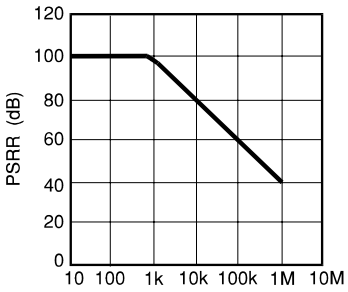
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

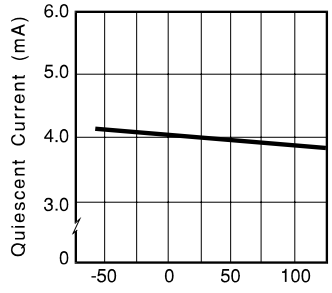
PSRR VS. FREQUENCY



Frequency (Hz)

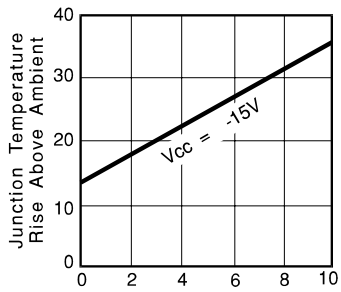
NEGATIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



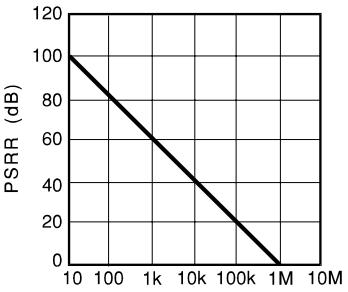
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

2. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the reference's voltage vs. temperature function. By trimming the zener current, a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear, this method leaves a residual error over wide temperature ranges.

To remove this residual error, a nonlinear compensation network of thermistors and resistors is used in the VRE107

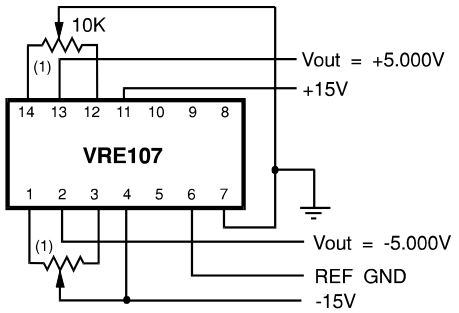
series references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, The VRE107 series produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

3. APPLICATION INFORMATION

The proper connection of the VRE107 series voltage reference is shown below with the optional trim resistors. When trimming the VRE107, the positive voltage should be trimmed first since the negative voltage tracks the positive side. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

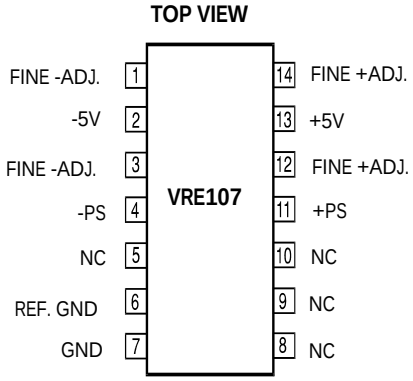
The VRE107 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't effect performance.

EXTERNAL CONNECTIONS



3. Optional Fine Adjust for approximately ±10mV.

PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- Very High Accuracy: ±3 V Output, ±0.2 mV
- Extremely Low Drift: 0.6 ppm/°C (-55°C to +125°C)
- Low Warm-up Drift: 1 ppm Typical
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 3 ppm/V Typical
- Hermetic 14-pin Ceramic DIP
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

DESCRIPTION

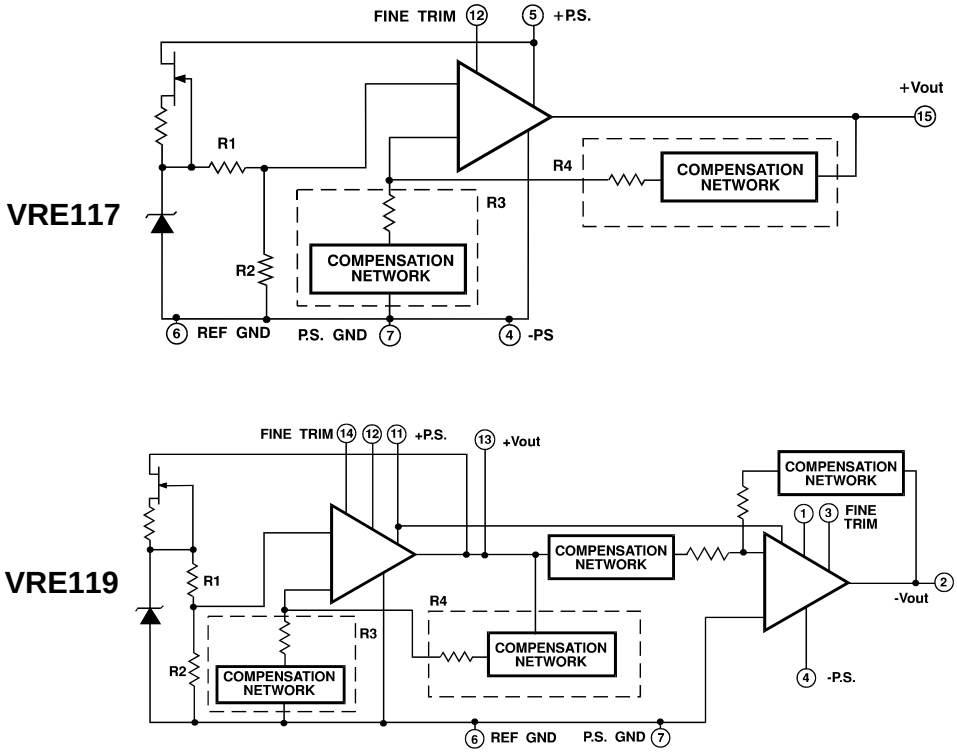
VRE117/119 Series Precision Voltage References provide ultrastable +3 V (VRE117), and ±3 V (VRE119) output with ±0.2 mV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range. This improvement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE117/119 series the most accurate and stable 3 V reference available.

VRE117/119 devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two performance grades. All devices are packaged in 14-pin hermetic ceramic packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

Superior stability, accuracy, and quality make these references ideal for precision applications such as A/D and D/A converters, high-accuracy test and measurement instrumentation, and transducer excitation.

C

Figure 1. BLOCK DIAGRAMS



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE117M VRE117MA	+3 +3	-55°C to +125°C -55°C to +125°C	±400µV ±200µV
VRE119C	±3	-25°C to +85°C	±200µV

Hermetic 14-pin Ceramic DIP
Package Style HC

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25°C, R_L = 10K Ω UNLESS OTHERWISE NOTED.

Model	VRE119C			VRE117M			VRE117MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS										
Power Supply	±13.5		±22	*		*	*		*	V
Operating Temperature	-25		+85	-55		+125	-55		+125	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous			*			*			
OUTPUT VOLTAGE										
VRE117		+3.0			*			*		V
VRE119		±3.0			*			*		V
OUTPUT VOLTAGE ERRORS										
Initial Error			±300			±300			±200	µV
Warmup Drift		2			2			1		ppm
T_{MIN} - T_{MAX} (Note1)			200			400			200	µV
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz)		1.5			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*			*			mA
REGULATION										
Line		3	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
OUTPUT ADJUSTMENT										
Range		5			*			*		mV
Temperature Coefficient		1			*			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)										
VRE117 ±PS		5	7		*	*		*	*	mA
VRE119 +PS		7	9		*	*		*	*	mA
VRE119 -PS		4	6		*	*		*	*	mA

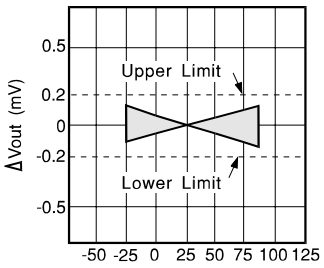
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

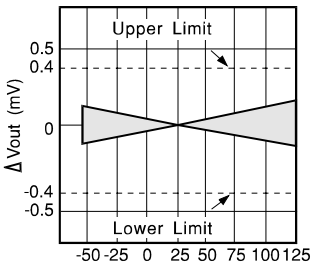
2. TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



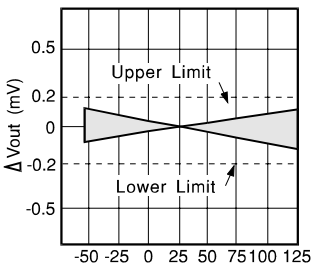
Temperature °C
VRE119C

V_{OUT} vs. TEMPERATURE



Temperature °C
VRE117M

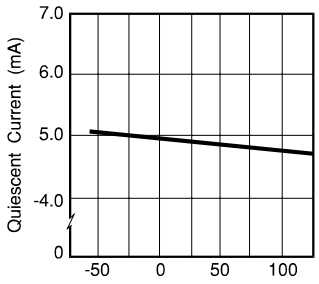
V_{OUT} vs. TEMPERATURE



Temperature °C
VRE117MA

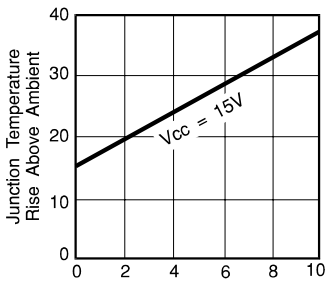
VRE117

QUIESCENT CURRENT VS. TEMP



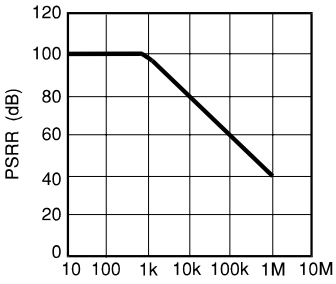
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY

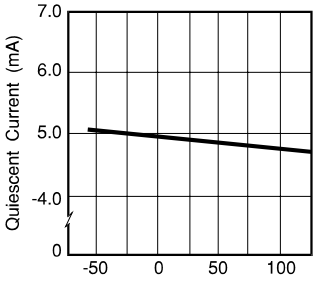


Frequency (Hz)

VRE119

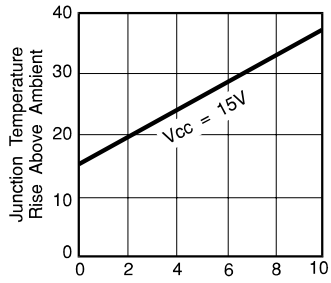
POSITIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



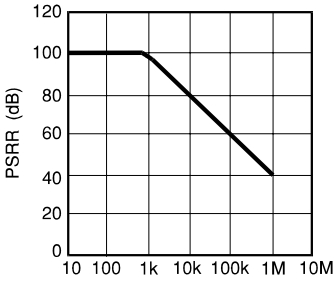
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

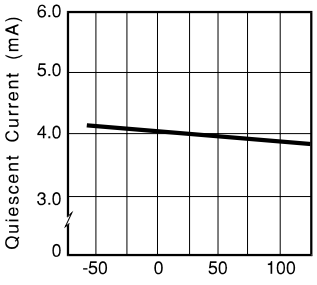
PSRR VS. FREQUENCY



Frequency (Hz)

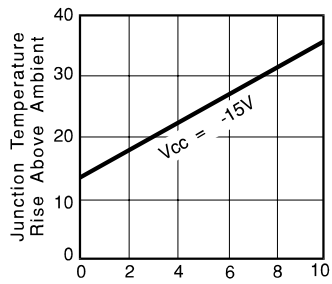
NEGATIVE OUTPUT

QUIESCENT CURRENT VS. TEMP



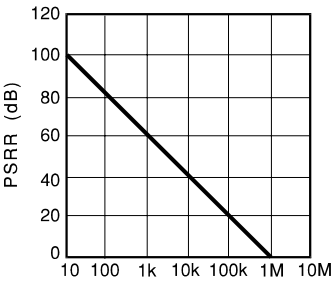
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 3 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the reference's voltage vs. temperature function. By trimming the zener current, a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear, this method leaves a residual error over wide temperature ranges.

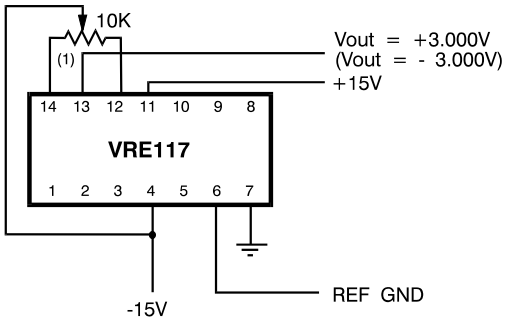
To remove this residual error, a nonlinear compensation network of thermistors and resistors is used in the VRE117/119 series references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, The VRE117/119 series produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

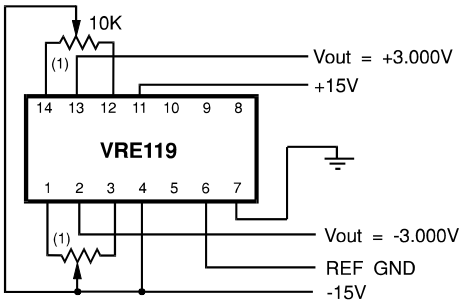
4. APPLICATION INFORMATION

The proper connection of the VRE117 series voltage reference with the optional trim resistors is shown below. When trimming the VRE119, the positive voltage should be trimmed first since the negative voltage tracks the positive side. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE117/119 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't effect performance.

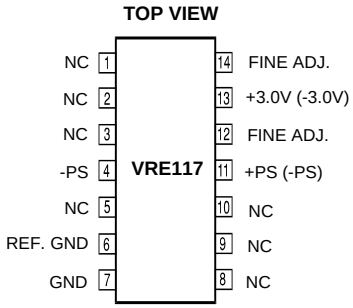
EXTERNAL CONNECTIONS

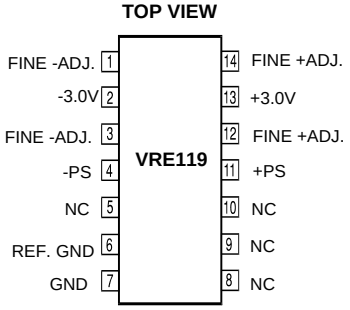




1. Optional Fine Adjust for approximately ±5mV.

PIN CONFIGURATION





Precision Voltage Reference

FEATURES

- Very High Accuracy: +2.5 V Output, ±200 µV
- Extremely Low Drift: 0.6 ppm/°C (25°C to +85°C)
- Low Warm-up Drift: 1 ppm Typical
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 6 ppm/V Typical
- Hermetic 20-Terminal Ceramic LCC
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

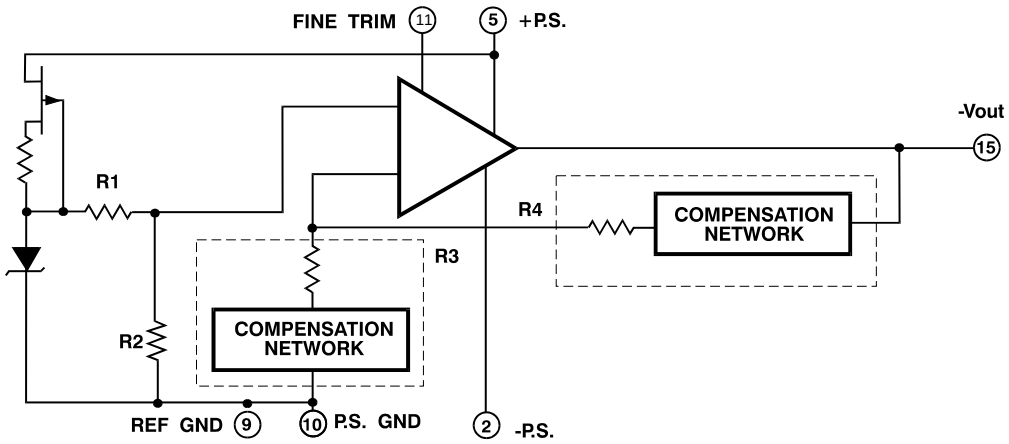
DESCRIPTION

VRE202 Series Precision Voltage References provide ultrastable +2.5 V outputs with ±200 µV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range. This improvement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and longterm stability, making the VRE202 series the most accurate and stable 2.5 V surface mount references available.

VRE202 devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two electrical performance grades. All devices are packaged in 20-terminal ceramic LCC packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE202C	+2.5V	-25°C to +85°C	±200µV
VRE202CA	+2.5V	-25°C to +85°C	±100µV
VRE202M	+2.5V	-55°C to +125°C	±400µV
VRE202MA	+2.5V	-55°C to +125°C	±200µV

20-terminal Ceramic LCC
Package Style HD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =+15V, T = +25°C, R_L = 10KΩ UNLESS OTHERWISE NOTED.

Grade	C			CA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	+13.5		+22	*		*	V
Operating Temperature	-25		+85	*		*	ºC
Storage Temperature	-65		+150	*		*	ºC
Short Circuit Protection		Continuous			*		
OUTPUT VOLTAGE							
VRE202		+2.5			*		V
OUTPUT VOLTAGE ERRORS							
Initial Error			±300			±200	µV
Warmup Drift		2			1		ppm
T_{MIN} - T_{MAX} (Note1)			200			100	µV
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz)		1.5			*		µVpp
OUTPUT CURRENT							
Range	±10			*			mA
REGULATION							
Line		6	10		*	*	ppm/V
Load		3			*		ppm/mA
OUTPUT ADJUSTMENT							
Range		10			*		mV
Temperature Coefficient		4			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)							
VRE202 +PS		5	7		*	*	mA
VRE202 -PS		5	7		*	*	mA

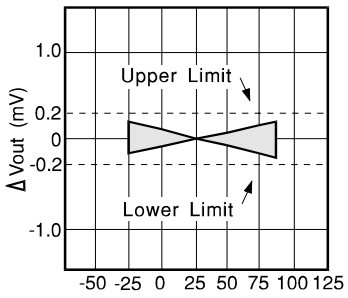
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

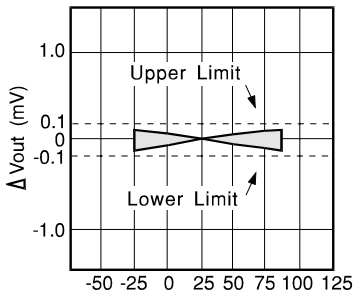
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



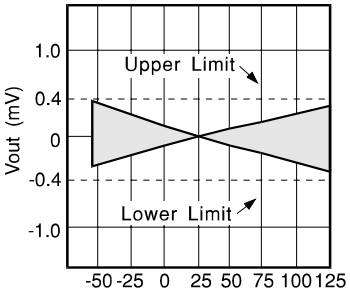
Temperature ºC
VRE202C

V_{OUT} vs. TEMPERATURE



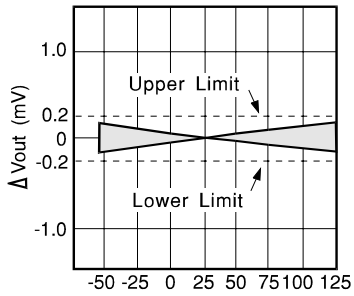
Temperature ºC
VRE202CA

V_{OUT} vs. TEMPERATURE



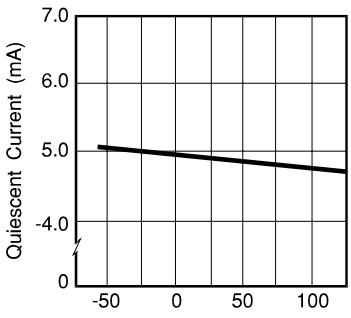
Temperature ºC
VRE202M

V_{OUT} vs. TEMPERATURE



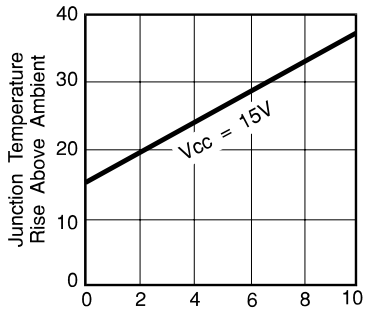
Temperature ºC
VRE202MA

QUIESCENT CURRENT VS. TEMP



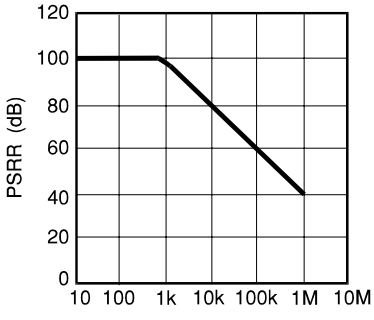
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 2.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

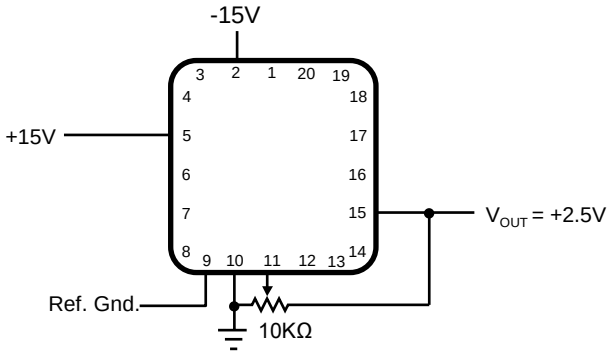
A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. this proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. Then by adjusting the slope, a very stable voltage over wide temperature ranges is produced. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, a voltage reference is produced that also has very good long term stability.

4. APPLICATION INFORMATION

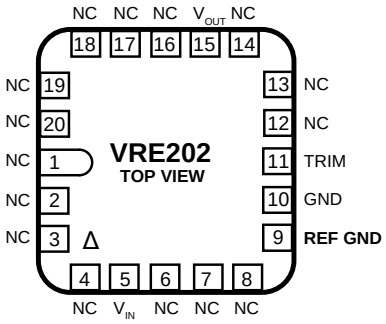
The proper connection of the VRE202 series voltage references with the optional trim resistors is shown below. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE202 series voltage references have the ground terminal brought out on two pins (pin 9 and pin 10) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 10 to the power supply ground and pin 9 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



Precision Voltage Reference

FEATURES

- Very High Accuracy: +4.5 V Output, ±0.4 mV
- Extremely Low Drift: 0.6 ppm/°C (-55°C to +125°C)
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 6 ppm/V Typical
- Wide Supply Range: ±13.5 V to ±22.0 V
- Hermetic 20-terminal Ceramic LCC
- Military Processing Available

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

DESCRIPTION

VRE204 Series Precision Voltage References provide ultrastable +4.5 V outputs with up to ±0.4 mV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range.

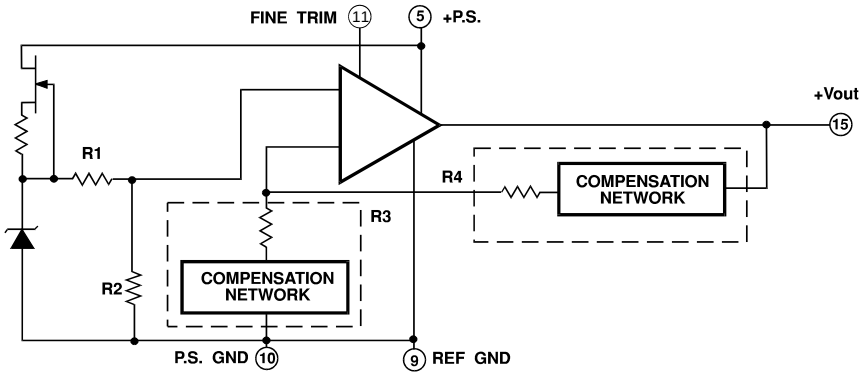
These references are specifically designed to be used with successive-approximation type Analog-to-Digital Converters (ADCs). Specify an ADC with exceptional temperature drift, which can only be as good as the external reference used. The VRE204 combined with the right ADC will provide the lowest drift data conversion obtainable.

The VRE204 series is available in the military operating temperature range -55°C to +125°C, and two performance grades. All devices are packaged in 20-terminal LCC ceramic packages for maximum long-term stability. These “M” versions are screened for high reliability and quality.

Superior stability, accuracy, and quality make the VRE204 ideal for all precision applications which may require a 4.5 V reference. High-accuracy test and measurement instrumentation, and transducer excitation are some other applications which can benefit from the high accuracy of the VRE204.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (MAX)
VRE204M	+4.5V	-55°C to +125°C	±0.6mV
VRE204MA	+4.5V	-55°C to +125°C	±0.3mV

20-terminal Ceramic LCC
Package Style HD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =+15V, T = +25°C, R_L = 10K Ω UNLESS OTHERWISE NOTED.

Model	M			MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	+13.5		+22	*		*	V
Operating Temperature	-55		+125	*		*	ºC
Storage Temperature	-65		+150	*		*	ºC
Short Circuit Protection		Continuous			*		
OUTPUT VOLTAGE							
VRE204		+4.5			*		V
OUTPUT VOLTAGE ERRORS							
Initial Error			±800			±400	µV
Warmup Drift		2			1		ppm
T_{MIN} - T_{MAX} (Note1)			600			300	µV
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz)		3			*		µVpp
OUTPUT CURRENT							
Range	±10			*			mA
REGULATION							
Line		6	10		*	*	ppm/V
Load		3			*		ppm/mA
OUTPUT ADJUSTMENT							
Range		10			*		mV
Temperature Coefficient		4			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)							
VRE204 +PS		5	7		*	*	mA

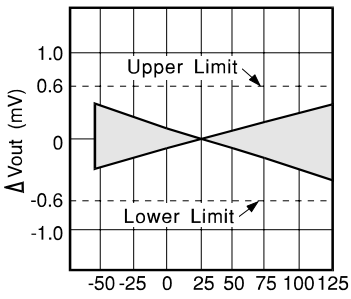
NOTES:

* Same as M Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

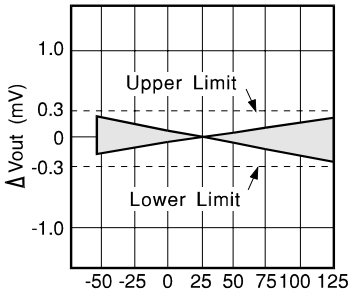
2. TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



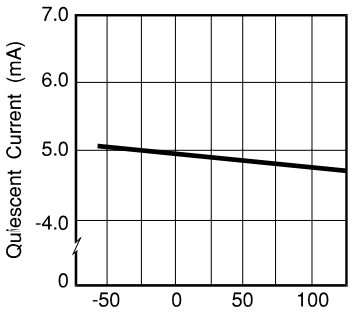
Temperature °C
VRE204M

V_{OUT} vs. TEMPERATURE



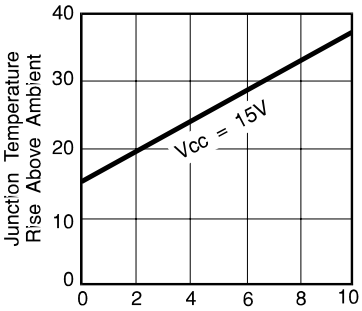
Temperature °C
VRE204MA

QUIESCENT CURRENT VS. TEMP



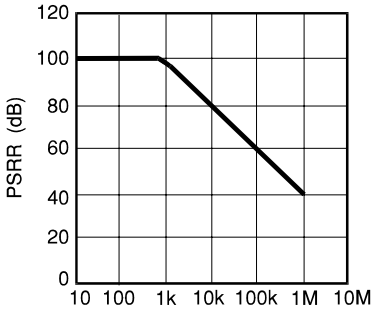
Temperature °C

JUNCTION TEMP. RISE VS OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 4.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

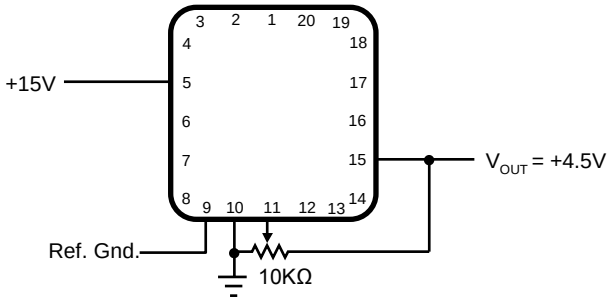
A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, the VRE204 series produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, we produce a voltage reference that also has very good long term stability.

4. APPLICATION INFORMATION

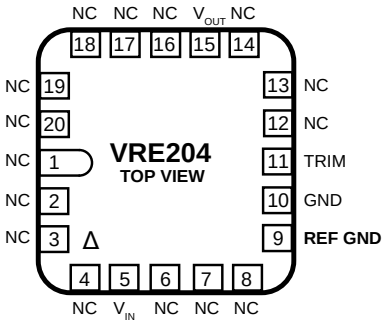
The proper connection of the VRE204 series voltage references with the optional trim resistors is shown below. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE204 series voltage references have the ground terminal brought out on two pins (pin 9 and pin 10) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 10 to the power supply ground and pin 9 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- Very High Accuracy: ±5 V Output, ±0.4 mV
- Extremely Low Drift: 0.6 ppm/°C (-55°C to +125°C)
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 6 ppm/V Typical
- Wide Supply Range: ±13.5 V to ±22 V
- Hermetic 20-terminal Ceramic LCC
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

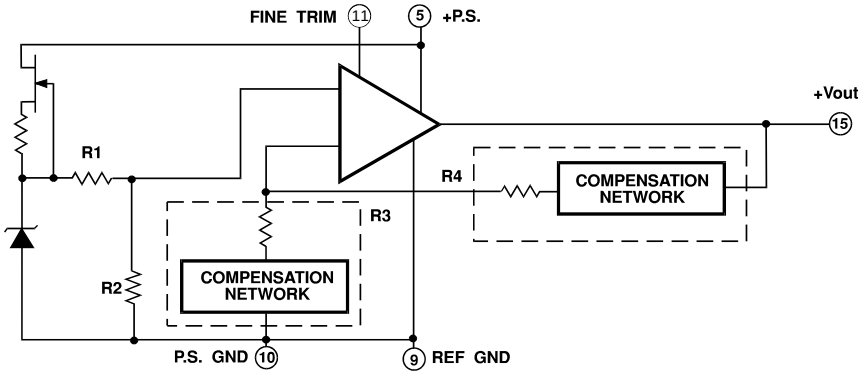
DESCRIPTION

VRE205 Series Precision Voltage References provides ultrastable ±5 V outputs with ±0.4 mV initial accuracy and temperature coefficient as low as 0.6 ppm/°C over the full military temperature range. This improvement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and longterm stability, making the VRE205 series the most accurate and stable 5 V references available.

VRE205 series devices are available in two operating temperature ranges, -25°C to +85°C and -55°C to +125°C, and two performance grades. All devices are packaged in 20-terminal ceramic LCC packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (Max)
VRE205C	±5V	-25°C to +85°C	0.4mV
VRE205CA	±5V	-25°C to +85°C	0.2mV
VRE205M	±5V	-55°C to +125°C	0.6mV
VRE205MA	±5V	-55°C to +125°C	0.3mV

20-terminal Ceramic LCC
Package Style HD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =+15V, T = +25°C, R_L = 10K Ω UNLESS OTHERWISE NOTED.

Model	C			CA			M			MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS													
Power Supply	+13.5		+22	*		*	*		*	*		*	V
Operating Temperature	-25		+85	*		*	-55		+125	-55		+125	ºC
Storage Temperature	-65		+150	*		*	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*			*		
OUTPUT VOLTAGE													
VRE205		±5			*			*			*		V
OUTPUT VOLTAGE ERRORS													
Initial Error			±800			±400			±800			±400	µV
Warmup Drift		2			1			2			1		ppm
T_{MIN} - T_{MAX} (Note1)			400			200			600			300	µV
Long-Term Stability		6			*			*			*		ppm/1000hrs
Noise (0.1 - 10Hz)		3			*			*			*		µVpp
OUTPUT CURRENT													
Range	±10			*			*			*			mA
REGULATION													
Line		6	10		*	*		*	*		*	*	ppm/V
Load		3			*			*			*		ppm/mA
OUTPUT ADJUSTMENT													
Range		10			*			*			*		mV
Temperature Coefficient		4			*			*			*		µV/ºC/mV
POWER SUPPLY CURRENT (Note 2)													
VRE205 +PS		5	7		*	*		*	*		*	*	mA

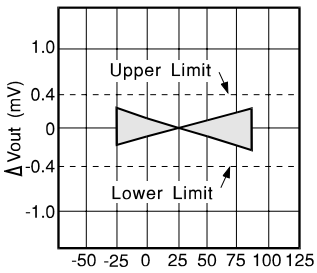
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25°C over the specified operating temperature range.
2. The specified values are unloaded.

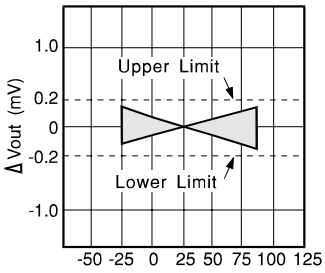
2. TYPICAL PERFORMANCE GRAPHS

V_{OUT} vs. TEMPERATURE



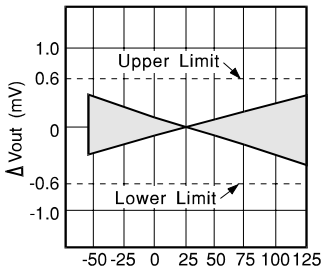
Temperature ºC
VRE205C

V_{OUT} vs. TEMPERATURE



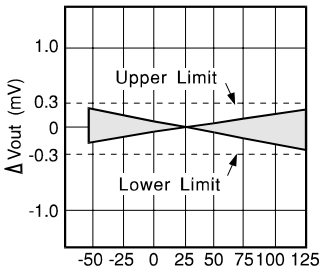
Temperature ºC
VRE205CA

V_{OUT} vs. TEMPERATURE



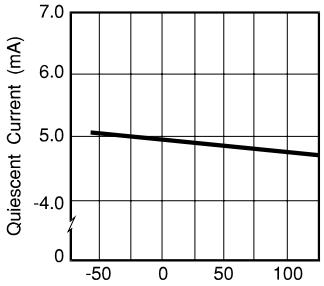
Temperature ºC
VRE205M

V_{OUT} vs. TEMPERATURE



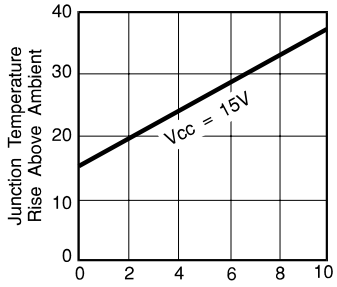
Temperature ºC
VRE205MA

QUIESCENT CURRENT VS. TEMP



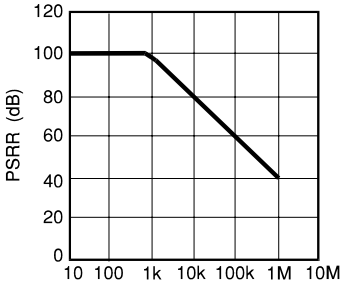
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the schematic in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

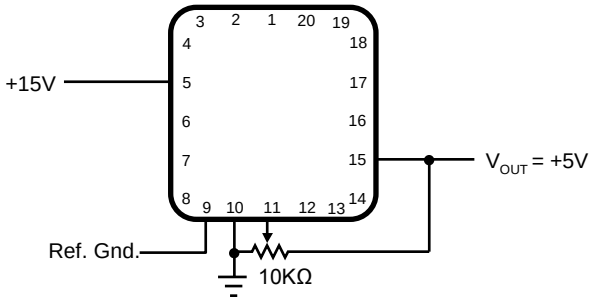
A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage over wide temperature ranges is produced. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, we produce a voltage reference that also has very good long term stability.

4. APPLICATION INFORMATION

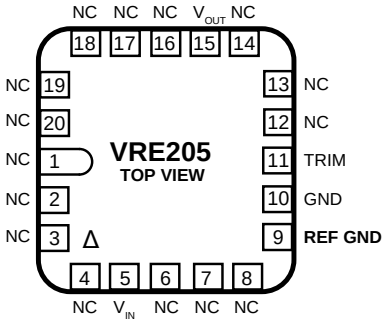
The proper connection of the VRE205 series voltage references with the optional trim resistor is shown below. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE205 series voltage references have the ground terminal brought out on two pins (pin 9 and pin 10) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 10 to the power supply ground and pin 9 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- Very High Accuracy: +10 V Output, ±0.3 mV
- Extremely Low Drift: 0.5 ppm/ºC (-55ºC to +125ºC)
- Low Warm-up Drift: 1 ppm Typical
- Excellent Stability: 6 ppm/1000 Hrs. Typical
- Excellent Line Regulation: 3 ppm/V Typical
- Hermetic 20-terminal Ceramic LCC Package
- Military Processing Option

APPLICATIONS

- Precision A/D and D/A Converters
- Transducer Excitation
- Accurate Comparator Threshold Reference
- High Resolution Servo Systems
- Digital Voltmeters
- High Precision Test and Measurement Instruments

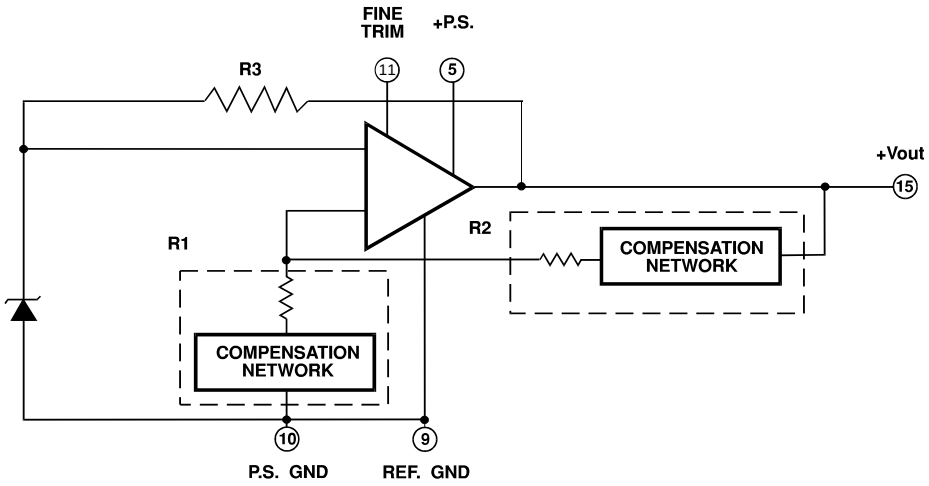
DESCRIPTION

VRE210 Series Precision Voltage References provide ultrastable +10 V outputs with ±0.3 mV initial accuracy and temperature coefficient as low as 0.5 ppm/ºC over the full military temperature range. This improvement in accuracy is made possible by a unique, proprietary multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and longterm stability, making the VRE210 series the most accurate and stable 10 V surface mount references available.

VRE210 devices are available in two operating temperature ranges, -25ºC to +85ºC and -55ºC to +125ºC, and two electrical performance grades. All devices are packaged in 20-terminal ceramic LCC packages for maximum long-term stability. “M” versions are screened for high reliability and quality.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Output (V)	Temperature Operating Range	Volt Deviation (Max)
VRE210C	+10	-25ºC to +85ºC	±0.6mV
VRE210CA	+10	-25ºC to +85ºC	±0.3mV
VRE210M	+10	-55ºC to +125ºC	±1.0mV
VRE210MA	+10	-55ºC to +125ºC	±0.5mV

20-terminal Ceramic LCC Package Style HD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =+15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	VRE210C			VRE210CA			VRE210M			VRE210MA			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS													
Power Supply	+13.5		+22	*		*	*		*	*		*	V
Operating Temperature	-25		+85	*		*	-55		+125	-55		+125	ºC
Storage Temperature	-65		+150	*		*	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*			*		
OUTPUT VOLTAGE													
VRE210		+10			*			*			*		V
OUTPUT VOLTAGE ERRORS													
Initial Error			±500			±300			±800			±400	µV
Warmup Drift		2			1			2			1		ppm
T_{MIN} - T_{MAX} (Note1)			600			300			1000			500	µV
Long-Term Stability		6			*			*			*		ppm/1000hrs
Noise (0.1 - 10Hz)		6			*			*			*		µVpp
OUTPUT CURRENT													
Range	±10			*			*			*			mA
REGULATION													
Line		3	10		*	*		*	*		*	*	ppm/V
Load		3			*			*			*		ppm/mA
OUTPUT ADJUSTMENT													
Range		20			*			*			*		mV
Temperature Coefficient		4			*			*			*		mV/ºC/mV
POWER SUPPLY CURRENT (Note 2)													
VRE210 +PS		5	7		*	*		*	*		*	*	mA

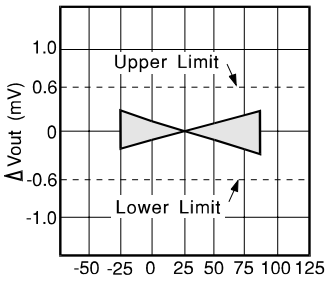
NOTES:

* Same as C Models.

1. Using the box method, the specified value is the maximum deviation from the output voltage at 25ºC over the specified operating temperature range.
2. The specified values are unloaded.

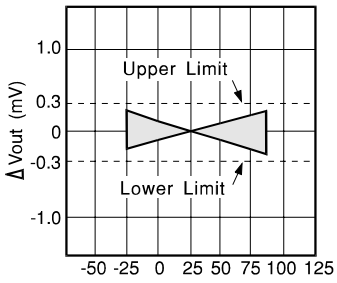
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



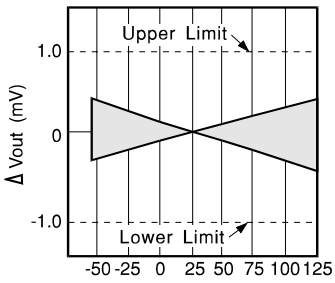
Temperature °C
VRE210C

V_{OUT} vs. TEMPERATURE



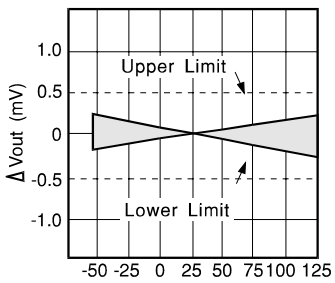
Temperature °C
VRE210CA

V_{OUT} vs. TEMPERATURE



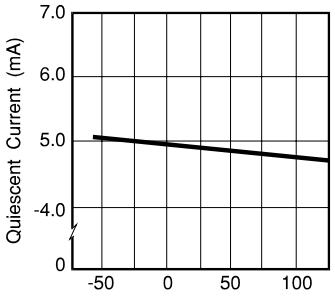
Temperature °C
VRE210M

V_{OUT} vs. TEMPERATURE



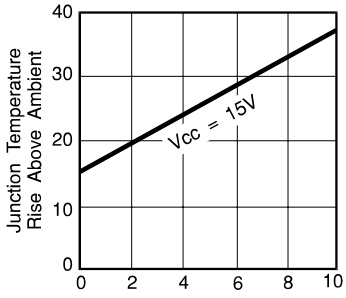
Temperature °C
VRE210MA

QUIESCENT CURRENT VS. TEMP



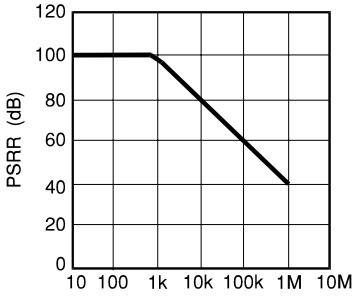
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. In operation, approximately 6.3 volts is applied to the noninverting input of the op amp. The voltage is amplified by the op amp to produce a 10 V output. The gain is determined by the networks R1 and R2: G=1 + R2/R1. The 6.3V zener diode is used because it is the most stable diode over time and temperature.

The zener operating current is derived from the regulated output voltage through R3. This feedback arrangement provides a closely regulated zener current. This current determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

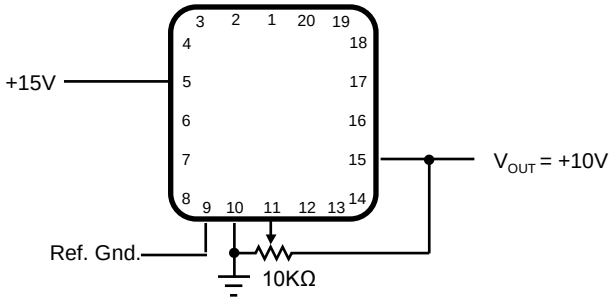
A nonlinear compensation network of thermistors and resistors that is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, Thaler Corporation produces a very stable voltage over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, we produce a voltage reference that also has very good long term stability.

4. APPLICATION INFORMATION

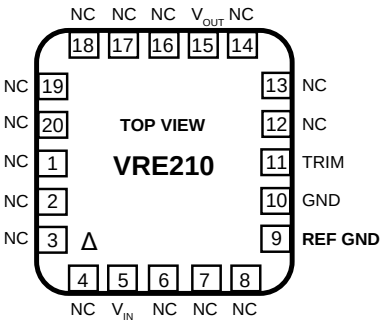
The proper connection of the VRE210 series voltage references with the optional trim resistor is shown below. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The VRE210 series voltage references have the ground terminal brought out on two pins (pin 9 and pin 10) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 10 to the power supply ground and pin 9 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- +2.5 V Output, ± 0.250 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 1.5 μV_{P-P} (0.1-10Hz)
- Industry Standard Pinout: 8-pin DIP or Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability

APPLICATIONS

The VRE302 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE302 offers superior performance over monolithic references.

DESCRIPTION

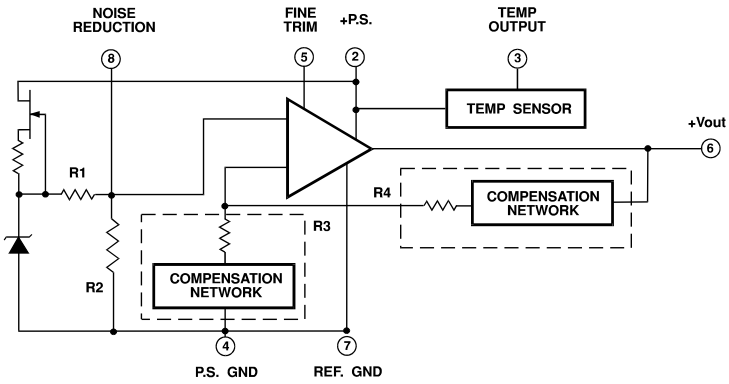
The VRE302 is a low cost, high precision +2.5 V reference. Packaged in the industry standard 8-pin DIP, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +2.5 V output with ±0.25 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/ºC. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE302 series the most accurate reference available in the standard 8-pin DIP package.

For enhanced performance, the VRE302 has an external trim option for users who want less than 0.01% initial error. A reference ground pin is provided to eliminate socket contact resistance errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)	Package Options
VRE302CS	0.50	2.0	0ºC to +70ºC	SMT8 (GD)
VRE302CD	0.50	2.0	0ºC to +70ºC	DIP8 (KD)
VRE302JS	0.25	0.6	-40ºC to +85ºC	SMT8 (GD)
VRE302JD	0.25	0.6	-40ºC to +85ºC	DIP8 (KD)
VRE302KS	0.40	1.0	-40ºC to +85ºC	SMT8 (GD)
VRE302LS	0.50	2.0	-40ºC to +85ºC	SMT8 (GD)
VRE302LD	0.50	2.0	-40ºC to +85ºC	DIP8 (KD)

8-pin Surface Mount Package Style GD

8-pin DIP Package Style KD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	A/J			K			C/L			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS										
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature (A,B)	0		+70	*		*	*		*	ºC
Operating Temperature (K)	-40		+85	*		*	*		*	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*		
OUTPUT VOLTAGE										
VRE302		+2.5			*			*		V
Temp. Sensor Voltage (Note 1)		630			*			*		mV
OUTPUT VOLTAGE ERRORS										
Initial Error (Note 2)			0.25			0.40			0.50	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} (Note3)			0.6			1.0			2.0	ppm/ºC
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		1.5			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*						mA
REGULATION										
Line		6	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
OUTPUT ADJUSTMENT										
Range		10			*			*		mV
POWER SUPPLY CURRENT (Note 5)										
VRE302 +PS		5	7		*	*		*	*	mA

NOTES:

* Same as A Models.

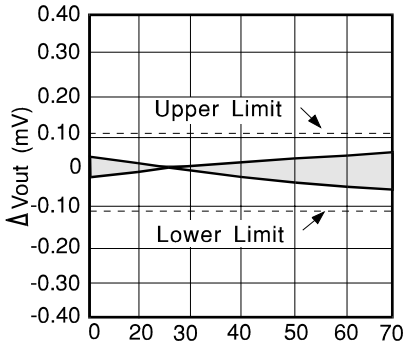
1. The temp. reference TC is 2.1mV/ ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

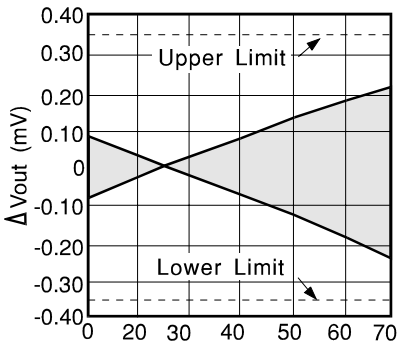
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



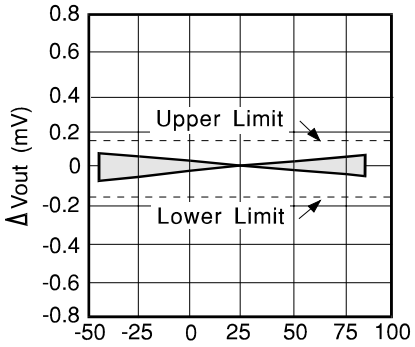
Temperature °C
VRE302A

V_{OUT} vs. TEMPERATURE



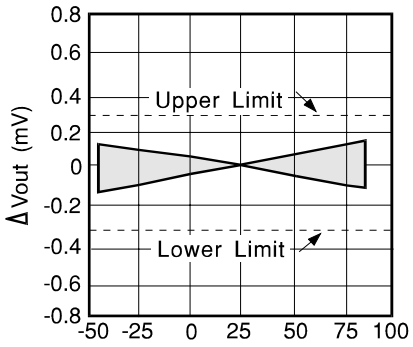
Temperature °C
VRE302C

V_{OUT} vs. TEMPERATURE



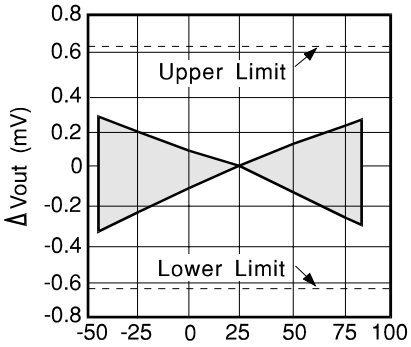
Temperature °C
VRE302J

V_{OUT} vs. TEMPERATURE



Temperature °C
VRE302K

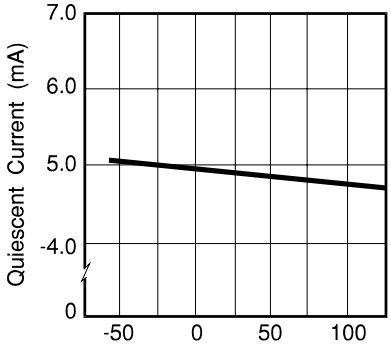
V_{OUT} vs. TEMPERATURE



Temperature °C
VRE302L

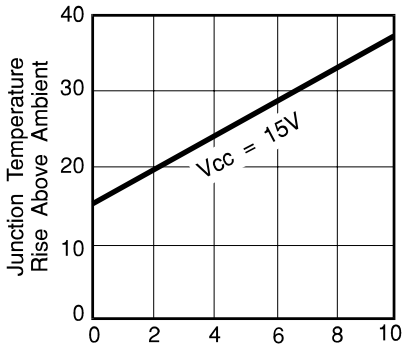
POSITIVE OUTPUT (TYP)

QUIESCENT CURRENT VS. TEMP



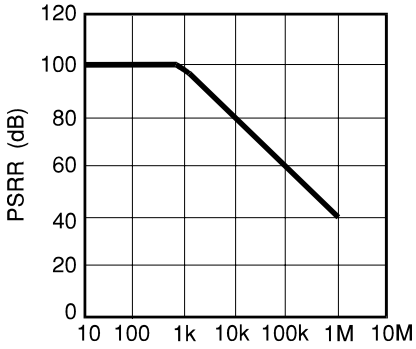
Temperature °C

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the schematic in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 2.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

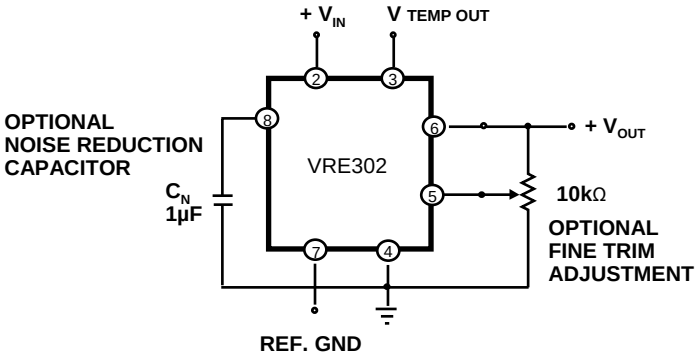
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

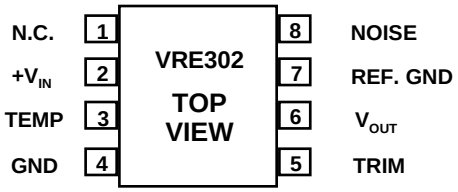
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE302 series voltage references with the optional trim resistor for initial error is shown below. The VRE302 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



Precision Voltage Reference

FEATURES

- +4.5 V Output, ± 0.450 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: $3\mu V_{p-p}$ (0.1-10Hz)
- Industry Standard Pinout: 8-Pin Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability

APPLICATIONS

The VRE304 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE304 offers superior performance over monolithic references.

DESCRIPTION

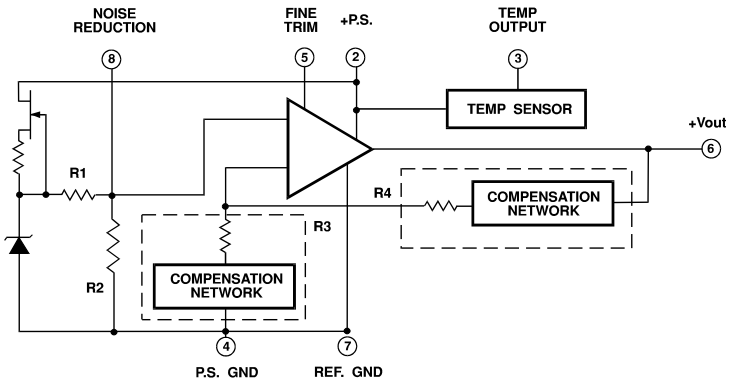
The VRE304 is a low cost, high precision +4.5 V reference. Available in an industry standard 8-pin surface mount package, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +4.5 V output with ±0.45 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability.

For enhanced performance, the VRE304 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE304A	±0.45	0.6	0ºC to +70ºC
VRE304C	±0.90	2.0	0ºC to +70ºC

8-pin Surface Mount Package Style GD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	A			C			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	±13.5	±15	±22	*	*	*	V
Operating Temperature	0		+70	*		*	ºC
Storage Temperature	-65		+150	*		*	ºC
Short Circuit Protection		Continuous			*		
OUTPUT VOLTAGE							
VRE304 (Note 1)		+4.5			*		V
Temp. Sensor Voltage		630			*		mV
OUTPUT VOLTAGE ERRORS							
Initial Error (Note 2)			±0.45			±0.90	mV
Warmup Drift		1			3		ppm
T_{MIN} - T_{MAX} (Note3)			0.6			2.0	ppm/ºC
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		3			*		µVpp
OUTPUT CURRENT							
Range	±10						mA
REGULATION							
Line		6	10		*	*	ppm/V
Load		3			*		ppm/mA
OUTPUT ADJUSTMENT							
Range		10			*		mV
POWER SUPPLY CURRENT (Note 5)							
VRE304 +PS		5	7		*	*	mA

NOTES:

* Same as A Model.

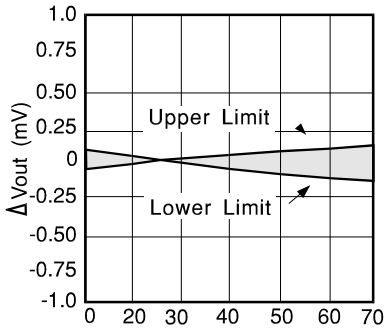
1. The temp. reference TC is 2.1 mV/ ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

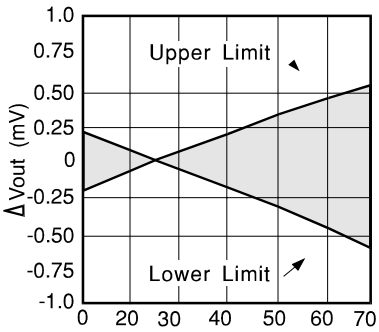
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



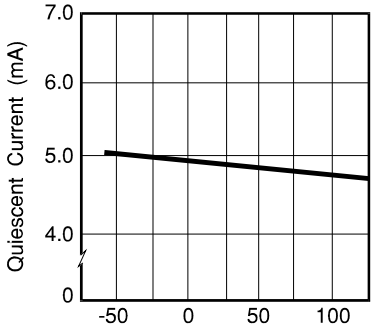
Temperature ºC
VRE304A

V_{OUT} vs. TEMPERATURE



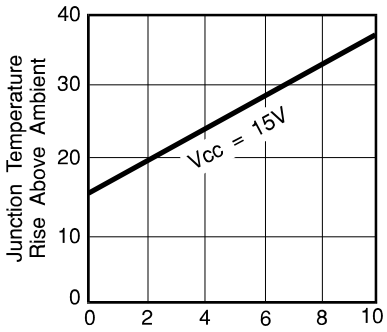
Temperature ºC
VRE304C

QUIESCENT CURRENT VS. TEMP



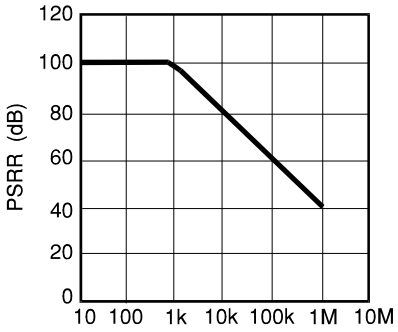
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 4.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

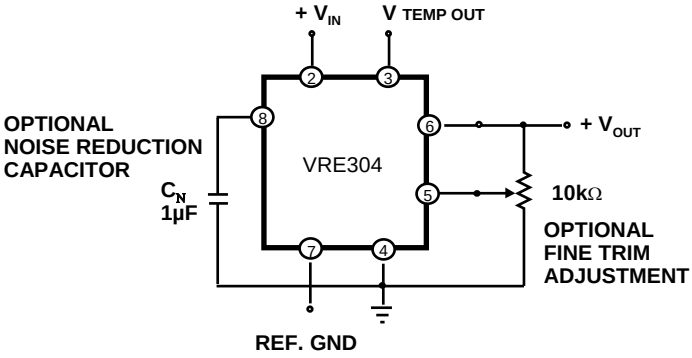
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

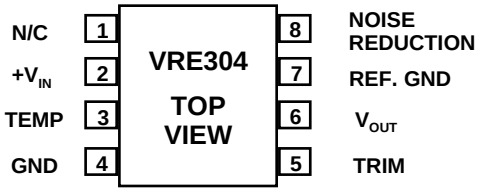
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE304 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below. The VRE304 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- +5 V Output, ± 0.5 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 3 μV_{P-P} (0.1-10Hz)
- Industry Standard Pinout: 8-pin DIP or Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability

APPLICATIONS

The VRE305 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE305 offers superior performance over monolithic references.

DESCRIPTION

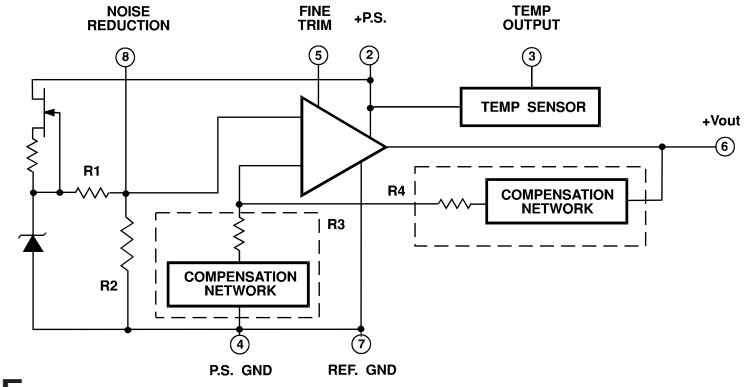
The VRE305 is a low cost, high precision +5 V reference. Packaged in an industry standard 8-pin DIP or SMT, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +5 V output with ±0.5 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE305 series the most accurate reference available in a standard 8-pin DIP or SMT.

For enhanced performance, the VRE305 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)	Package Options
VRE305AS	0.5	0.6	0ºC to +70ºC	SIP8 (GD)
VRE305AD	0.5	0.6	0ºC to +70ºC	DIP8 (KD)
VRE305BS	0.8	1.0	0ºC to +70ºC	SIP8 (GD)
VRE305BD	0.8	1.0	0ºC to +70ºC	DIP8 (KD)
VRE305CS	1.0	2.0	0ºC to +70ºC	SIP8 (GD)
VRE305CD	1.0	2.0	0ºC to +70ºC	DIP8 (KD)
VRE305JS	0.5	0.6	-40ºC to +85ºC	SIP8 (GD)
VRE305JD	0.5	0.6	-40ºC to +85ºC	DIP8 (KD)
VRE305KS	0.8	1.0	-40ºC to +85ºC	SIP8 (GD)
VRE305KD	0.8	1.0	-40ºC to +85ºC	DIP8 (KD)
VRE305LS	1.0	2.0	-40ºC to +85ºC	SIP8 (GD)
VRE305LD	1.0	2.0	-40ºC to +85ºC	DIP8 (KD)

8-pin Surface Mount Package Style GD

8-pin DIP Package Style KD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	A/J			B/K			C/L			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS										
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature (A,B,C)	0		+70	*		*	*		*	ºC
Operating Temperature (J,K,L)	-40		+85	*		*	*		*	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*		
OUTPUT VOLTAGE										
VRE305		+5.0			*			*		V
Temp. Sensor Voltage (Note 1)		630			*			*		mV
OUTPUT VOLTAGE ERRORS										
Initial Error (Note 2)			0.5			0.80			1.00	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} (Note3)			0.6			1.0			2.0	ppm/ºC
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		3			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*						mA
REGULATION										
Line		6	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
OUTPUT ADJUSTMENT										
Range		10			*			*		mV
POWER SUPPLY CURRENT (Note 5)										
VRE305 +PS		5	7		*	*		*	*	mA

NOTES:

* Same as A/J Models.

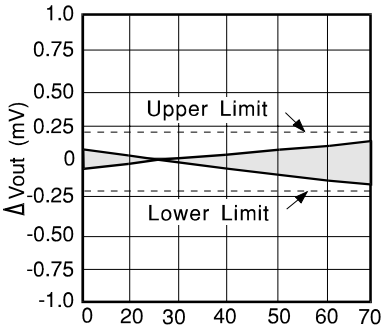
1. The temp. reference TC is 2.1 mV/ ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

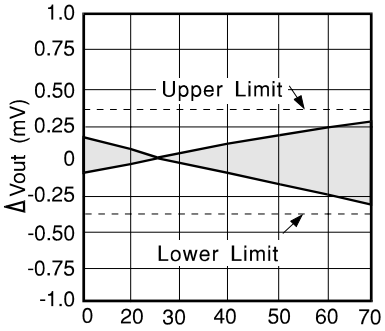
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



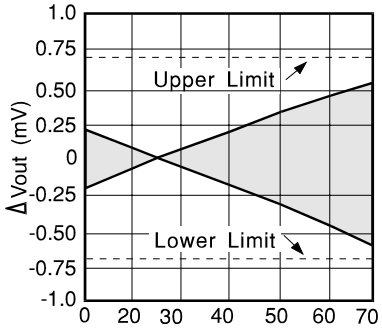
Temperature ºC
VRE305A

V_{OUT} vs. TEMPERATURE



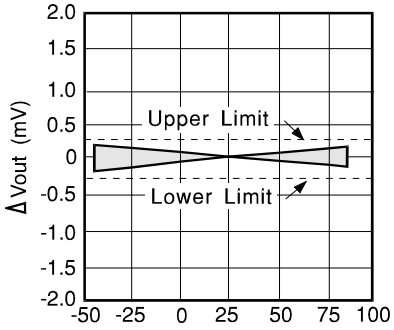
Temperature ºC
VRE305B

V_{OUT} vs. TEMPERATURE



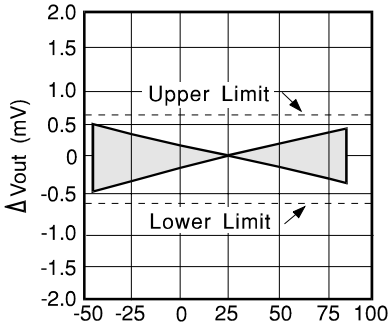
Temperature ºC
VRE305C

V_{OUT} vs. TEMPERATURE



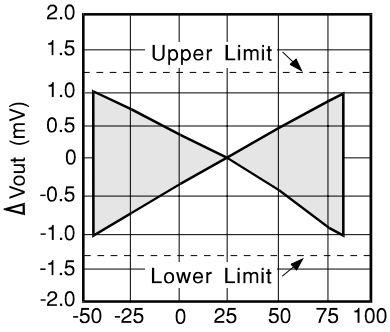
Temperature ºC
VRE305J

V_{OUT} vs. TEMPERATURE



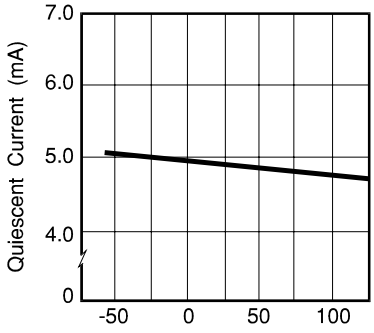
Temperature ºC
VRE305K

V_{OUT} vs. TEMPERATURE



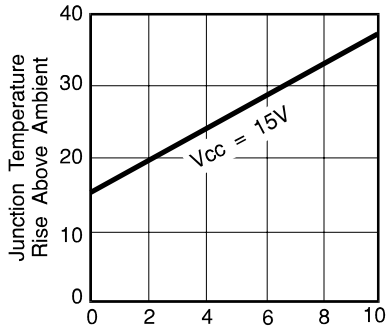
Temperature ºC
VRE305L

QUIESCENT CURRENT VS. TEMP



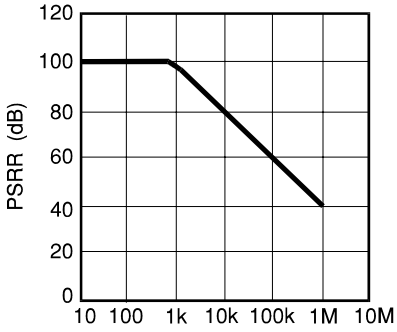
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

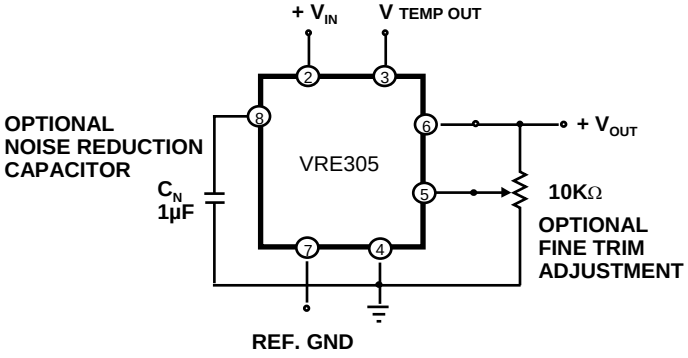
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

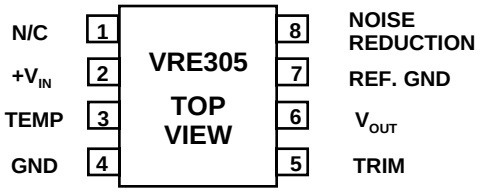
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE305 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below. The VRE305 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



Precision Voltage Reference

FEATURES

- +6 V Output, ± 0.6 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 4 μV_{P-P} (0.1-10Hz)
- Industry Standard Pinout: 8-pin Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability

APPLICATIONS

The VRE306 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE306 offers superior performance over monolithic references.

DESCRIPTION

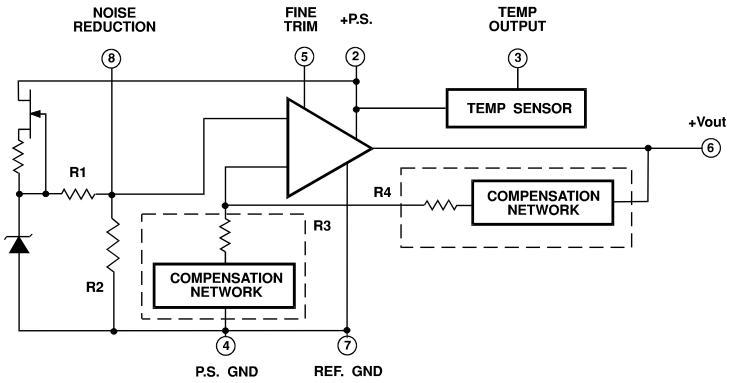
The VRE306 is a low cost, high precision +6 V reference. Available in an industry standard 8-pin surface mount package, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +6 V output with ±0.6 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/ºC. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE306 series the most accurate reference available in a standard 8-pin SMT package.

For enhanced performance, the VRE306 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE306A	±0.6	0.6	0ºC to +70ºC
VRE306C	±1.2	2.0	0ºC to +70ºC

8-pin Surface Mount Package Style GD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	VRE306A			VRE306C			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS							
Power Supply	±14	±15	±16	*	*	*	V
Operating Temperature (A,C)	0		+70	*		*	ºC
Storage Temperature	-65		+150	*		*	ºC
Short Circuit Protection		Continuous			*		
OUTPUT VOLTAGE							
VRE306		+6.0			*		V
Temp. Sensor Voltage (Note 1)		630			*		mV
OUTPUT VOLTAGE ERRORS							
Initial Error (Note 2)			±0.6			±1.2	mV
Warmup Drift		1			3		ppm
T_{MIN} - T_{MAX} (Note3)			0.6			2.0	ppm/ºC
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		4			*		µVpp
OUTPUT CURRENT							
Range	±10						mA
REGULATION							
Line		6	10		*	*	ppm/V
Load		3			*		ppm/mA
OUTPUT ADJUSTMENT							
Range		10			*		mV
POWER SUPPLY CURRENT (Note 5)							
VRE306 +PS		5	7		*	*	mA

NOTES:

* Same as A Models.

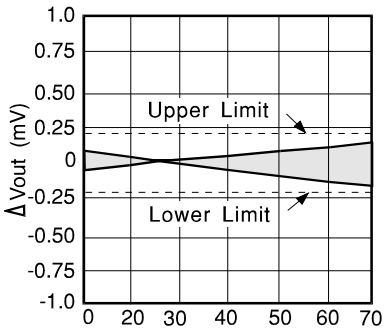
1. The temp. reference TC is 2.1 mV/ ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

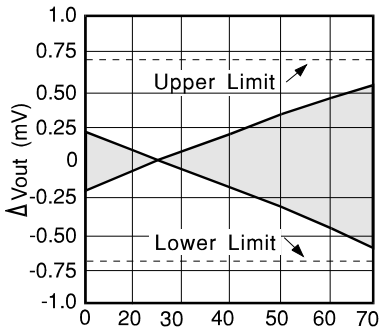
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



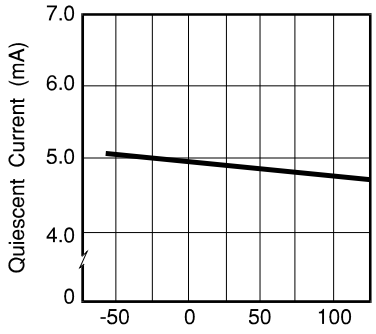
Temperature ºC
VRE306A

V_{OUT} vs. TEMPERATURE



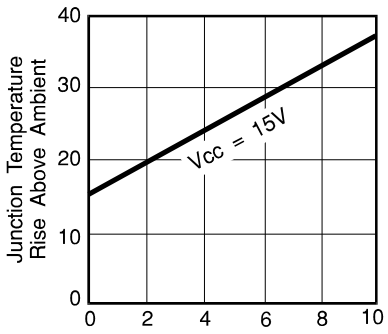
Temperature ºC
VRE306C

QUIESCENT CURRENT VS. TEMP



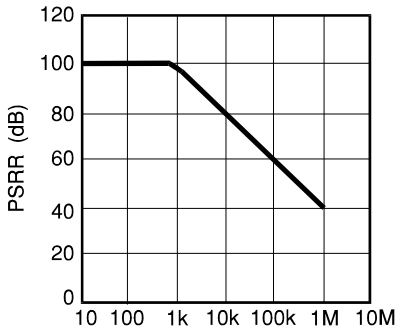
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 6.0V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

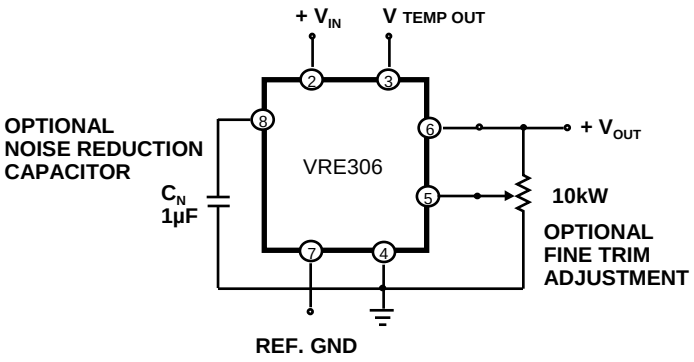
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

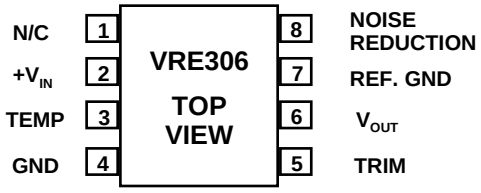
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE306 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below. The VRE306 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- +10 V Output, ±1.0 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 6 μV_{P-P} (0.1-10Hz)
- Industry Standard Pinout: 8-pin DIP or Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability

APPLICATIONS

The VRE310 is recommended for use as a reference for 14, 16, or 18-bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE310 offers superior performance over monolithic references.

DESCRIPTION

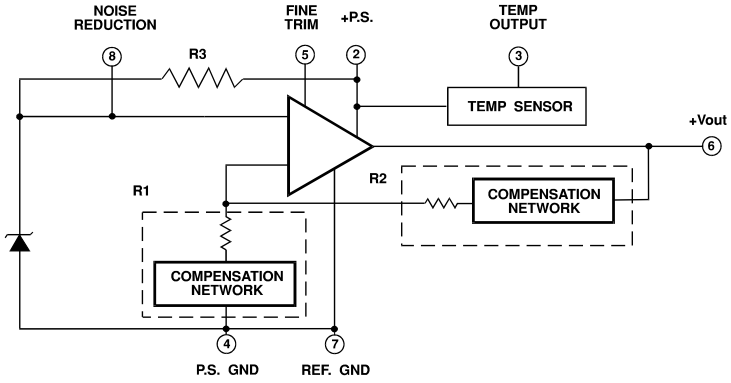
The VRE310 is a low cost, high precision +10 V reference. Available in an industry standard 8-pin DIP or SMT, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +10 V output with ±1.0 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/ºC. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE310 series the most accurate reference available in a standard 8-pin DIP or SMT package.

For enhanced performance, the VRE310 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)	Package Options
VRE310AS	1.0	0.6	0ºC to +70ºC	SMT8 (GD)
VRE310AD	1.0	0.6	0ºC to +70ºC	DIP8 (KD)
VRE310BS	1.6	1.0	0ºC to +70ºC	SMT8 (GD)
VRE310BD	1.6	1.0	0ºC to +70ºC	DIP8 (KD)
VRE310CS	2.0	2.0	0ºC to +70ºC	SMT8 (GD)
VRE310CD	2.0	2.0	0ºC to +70ºC	DIP8 (KD)
VRE310JS	1.0	0.6	-40ºC to +85ºC	SMT8 (GD)
VRE310JD	1.0	0.6	-40ºC to +85ºC	DIP8 (KD)

8-pin Surface Mount Package Style GD

8-pin DIP Package Style KD

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	A/J			B			C			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE MAXIMUM RATINGS										
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature (A,B,C)	0		+70	*		*	*		*	ºC
Operating Temperature (J)	-40		+85	*		*	*		*	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*		
OUTPUT VOLTAGE										
VRE310		+10.0			*			*		V
Temp. Sensor Voltage (Note 1)		630			*			*		mV
OUTPUT VOLTAGE ERRORS										
Initial Error (Note 2)			±1.0			±1.6			±2.0	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} (Note3)			0.6			1.0			2.0	ppm/ºC
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		6			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*						mA
REGULATION										
Line		6	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
OUTPUT ADJUSTMENT										
Range		20			*			*		mV
POWER SUPPLY CURRENT (Note 5)										
VRE310 +PS		5	7		*	*		*	*	mA

NOTES:

* Same as A/J Models.

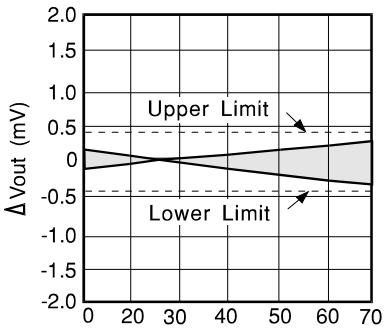
1. The temp. reference TC is 2.1 mV/ ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

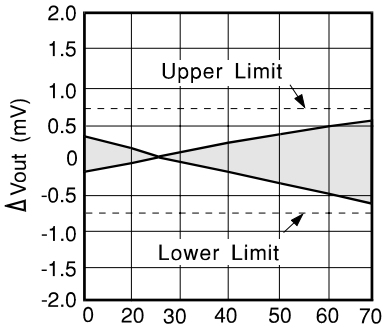
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



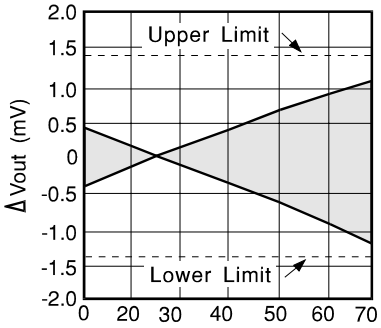
Temperature ºC
VRE310A

V_{OUT} vs. TEMPERATURE



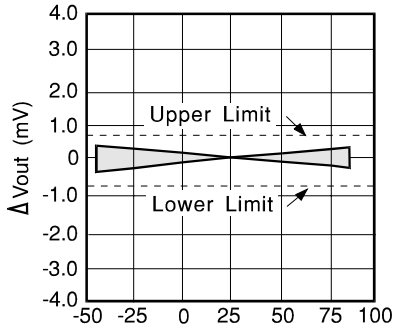
Temperature ºC
VRE310B

V_{OUT} vs. TEMPERATURE



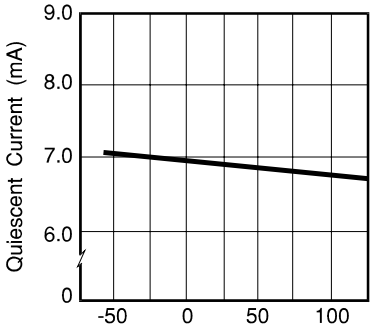
Temperature ºC
VRE310C

V_{OUT} vs. TEMPERATURE



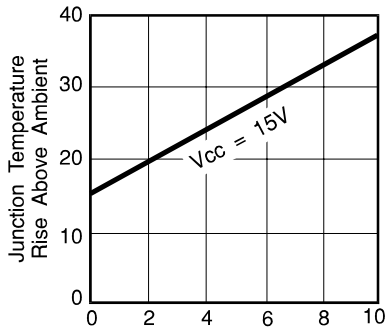
Temperature ºC
VRE310J

QUIESCENT CURRENT VS. TEMP



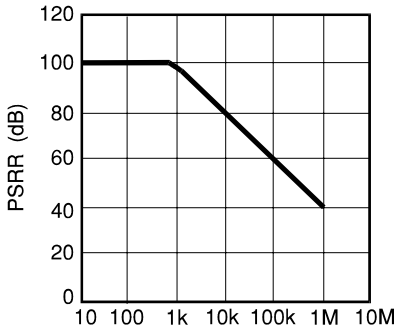
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. In operation, approximately 6.3 V is applied to the noninverting input of the op amp. The voltage is amplified by the op amp to produce a 10 V output. The gain is determined by the networks R1 and R2: G=1 + R2/R1. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

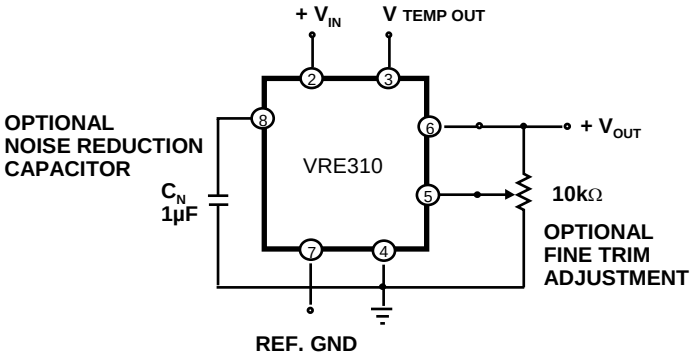
The zener operating current is derived from the regulated output voltage through R3. This feedback arrangement provides a closely regulated zener current. This current determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage is produced over wide temperature ranges.

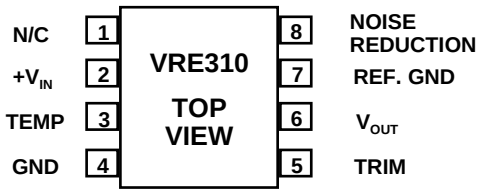
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. By using highly stable resistors in our network, we produce a voltage reference that also has very good long term stability.

The proper connection of the VRE310 series voltage references with the optional trim resistor is shown below. The VRE310 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



Precision Dual Voltage Reference

FEATURES

- ±5 V Output, ± 0.5 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 3 μV_{P-P} (0.1-10hz)
- Tracking Error: 0.3 mV Max.
- Excellent Line Regulation: 6 ppm/V Typical
- Surface Mount and DIP Package Options

APPLICATIONS

The VRE405 is recommended for use as a reference for high precision D/A and A/D converters which require an external precision reference. The device is ideal for calibrating scale factor on high resolution A/D converters. The VRE405 offers superior performance over monolithic references.

DESCRIPTION

The VRE405 is a low cost, high precision, ±5 V reference. Available in 14-pin DIP or SMT packages, the device is ideal for new designs that need a high performance reference.

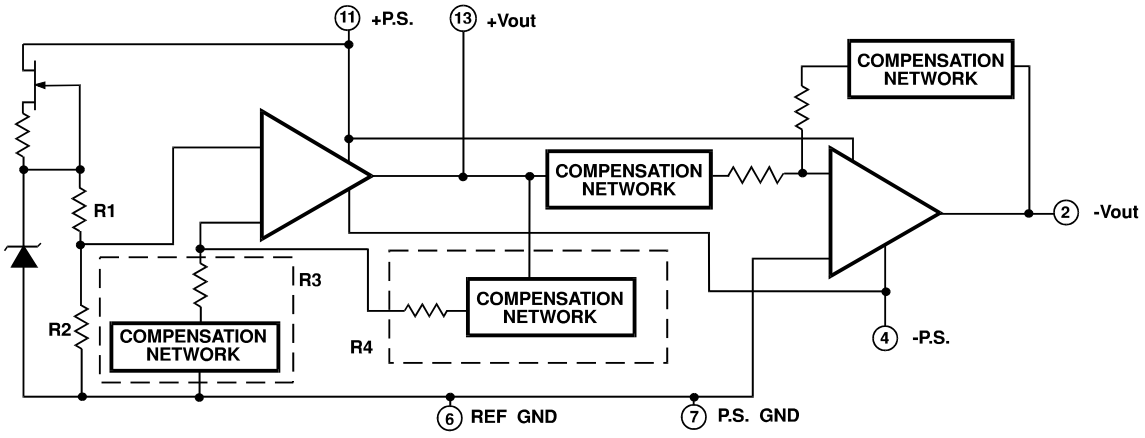
The device provides ultrastable ±5 V output with ±0.5 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique.

Another key feature of this reference is the 0.3 mV maximum tracking error between the positive and negative output voltages over the operating temperature range. This is extremely important in high performance systems for reducing overall system errors.

For designs which use the DIP package in a socket, there is a reference ground pin to eliminate the reference ground errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)	Package Options
VRE405AS	±0.5	0.6	0ºC to +70ºC	SMT14 (GE)
VRE405AD	±0.5	0.6	0ºC to +70ºC	DIP14 (KE)
VRE405BS	±0.8	1.0	0ºC to +70ºC	SMT14 (GE)
VRE405BD	±0.8	1.0	0ºC to +70ºC	DIP14 (KE)
VRE405CS	±1.0	2.0	0ºC to +70ºC	SMT14 (GE)
VRE405CD	±1.0	2.0	0ºC to +70ºC	DIP14 (KE)

14-pin Surface Mount Package Style GE

14-pin DIP Package Style KE

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	VRE405A			VRE405B			VRE405C			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE RATINGS										
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature	0		+70	*		*	*		*	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous			*			*			
OUTPUT VOLTAGE										
VRE405		±5.0			*			*		V
OUTPUT VOLTAGE ERRORS										
Initial Error (Note 1)			±0.05			±0.80			±1.00	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} (Note2)			0.6			1.0			2.0	ppm/ºC
Tracking Error			0.3			0.4			0.5	mV
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 3)		3			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*						mA
REGULATION										
Line		3	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
OUTPUT ADJUSTMENT										
Range		20			*			*		mV
POWER SUPPLY CURRENT (Note 4)										
+PS		7	9		*	*		*	*	mA
-PS		4	6		*	*		*	*	mA

NOTES:

* Same as A Models.

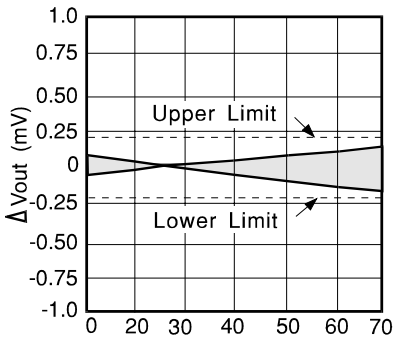
1. The specified values are without external trim.
2. The temperature coefficient (TC) is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The tracking error is the deviation between the positive and negative output over the operating temp. range.
5. The specified values are unloaded.

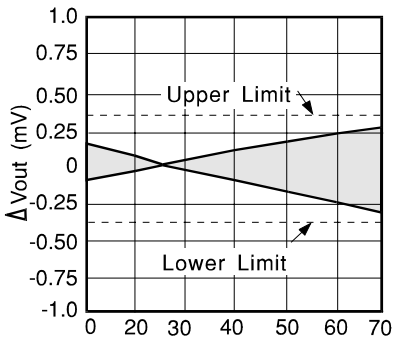
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



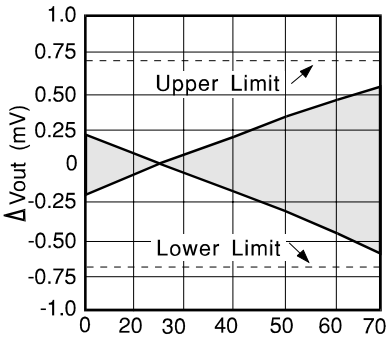
Temperature ºC
VRE405A

V_{OUT} vs. TEMPERATURE



Temperature ºC
VRE405B

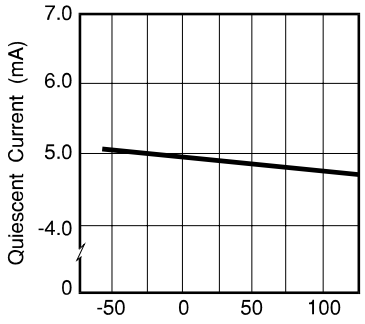
V_{OUT} vs. TEMPERATURE



Temperature ºC
VRE405C

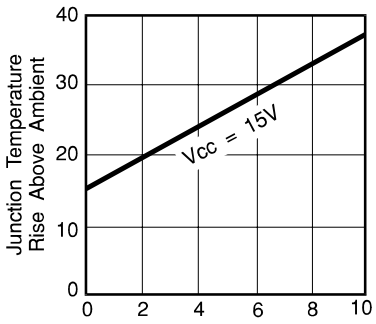
POSITIVE OUTPUT (TYP)

QUIESCENT CURRENT VS. TEMP



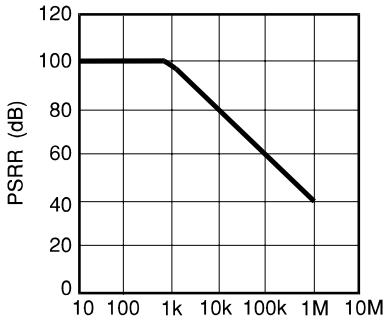
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

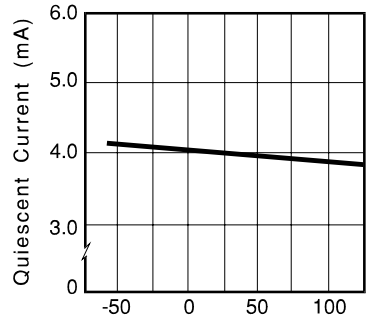
PSRR VS. FREQUENCY



Frequency (Hz)

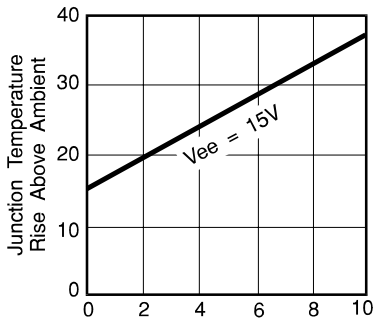
NEGATIVE OUTPUT (TYP)

QUIESCENT CURRENT VS. TEMP



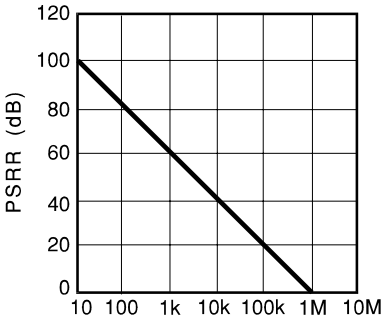
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

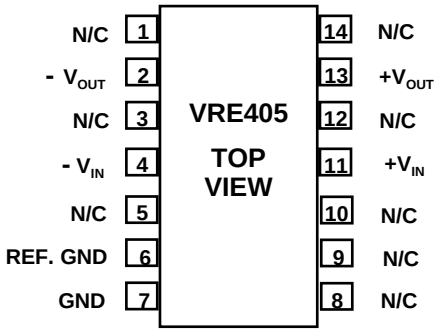
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors that is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The VRE405 reference has it's ground terminal brought out on two pins (pin 6 and 7) which are connected internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance.

PIN CONFIGURATION



Precision Dual Voltage Reference

FEATURES

- ±10 V Output, ± 1.0 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 6 μV_{P-P} (0.1-10Hz)
- Tracking Error: 0.5 mV Max.
- Excellent Line Regulation: 6 ppm/V Typical
- Surface Mount Package

APPLICATIONS

The VRE410 is recommended for use as a reference for high precision D/A and A/D converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE410 offers superior performance over monolithic references.

DESCRIPTION

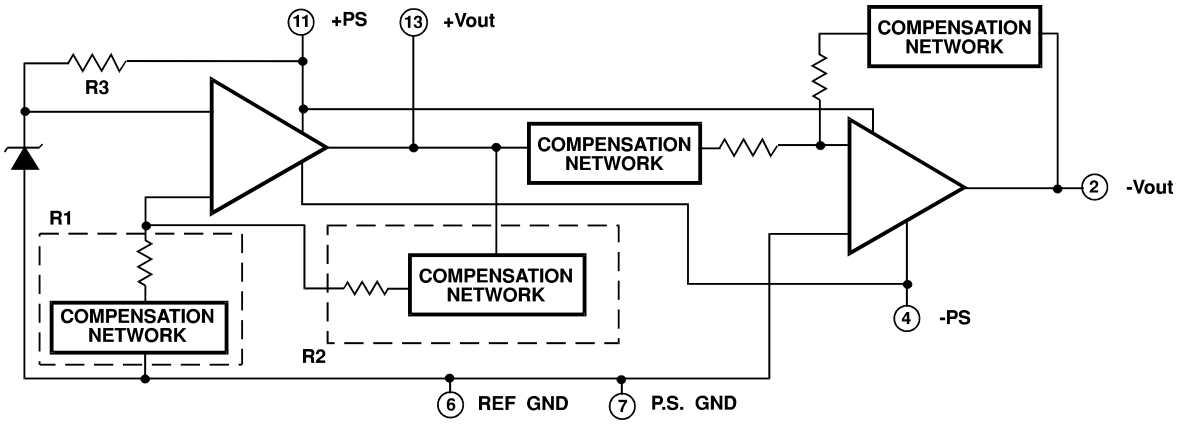
The VRE410 is a low cost, high precision, ±10 V reference. Available in a 14-pin SMT package, the device is ideal for new designs that need a high performance reference.

The device provides ultrastable ±10 V output with ±1.0 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique.

Another key feature of this reference is the 0.5 mV maximum tracking error between the positive and negative output voltages over the full operating temperature range. This is extremely important in high performance systems for reducing overall system errors.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE410A	±1.0	0.6	0ºC to +70ºC
VRE410B	±1.6	1.0	0ºC to +70ºC
VRE410C	±2.0	2.0	0ºC to +70ºC
VRE410J	±1.0	0.6	-40ºC to +85ºC
VRE410L	±2.0	2.0	-40ºC to +85ºC

14-pin Surface Mount
Package Style GE

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Model	A/J			B			C/L			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
ABSOLUTE RATINGS										
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature (A,B,C)	0		+70	*		*	*		*	ºC
Operating Temperature (J,L)	-40		+85	*		*	*		*	ºC
Storage Temperature	-65		+150	*		*	*		*	ºC
Short Circuit Protection	Continuous				*			*		
OUTPUT VOLTAGE										
VRE410		±10.0			*			*		V
OUTPUT VOLTAGE ERRORS										
Initial Error (Note 1)			±1.00			±1.60			±2.00	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} (Note 2)			0.6			1.0			2.0	ppm/ºC
Tracking Error (Note 3)			0.5			0.7			1.0	mV
Long-Term Stability		6			*			*		ppm/1000hrs.
Noise (0.1 - 10Hz)		6			*			*		µVpp
OUTPUT CURRENT										
Range	±10			*						mA
REGULATION										
Line		3	10		*	*		*	*	ppm/V
Load		3			*			*		ppm/mA
POWER SUPPLY CURRENT (Note 4)										
+PS		7	9		*	*		*	*	mA
-PS		4	6		*	*		*	*	mA

NOTES:

* Same as A/J Models.

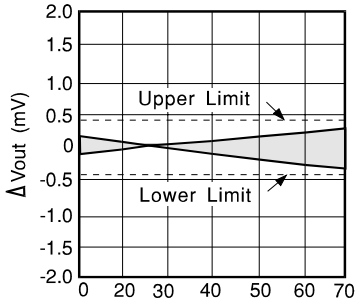
1. The specified values are without external trim.
2. The temperature coefficient (TC) is determined by the box method using the following formula:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The tracking error is the deviation between the positive and negative output over the operating temp. range.
5. The specified values are unloaded.

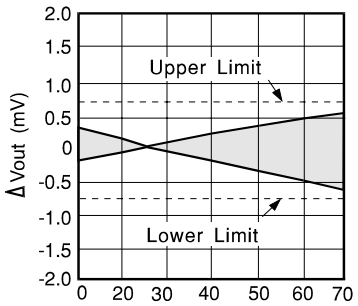
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



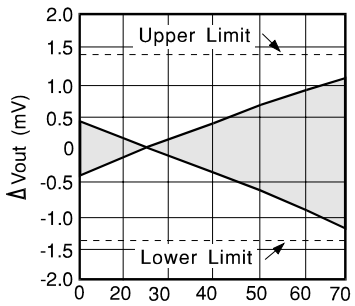
Temperature ºC
VRE410A

V_{OUT} vs. TEMPERATURE



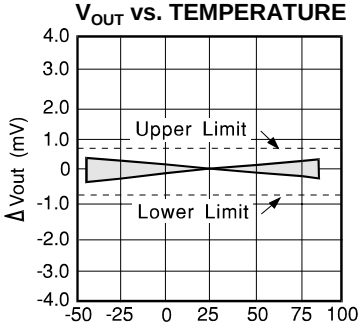
Temperature ºC
VRE410B

V_{OUT} vs. TEMPERATURE



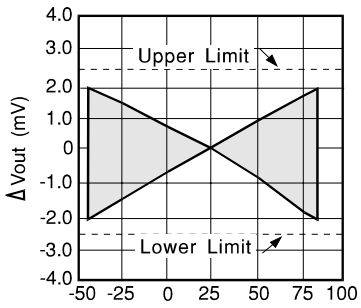
Temperature ºC
VRE410C

V_{OUT} vs. TEMPERATURE



Temperature ºC
VRE410J

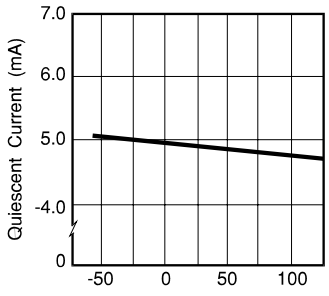
V_{OUT} vs. TEMPERATURE



Temperature ºC
VRE410L

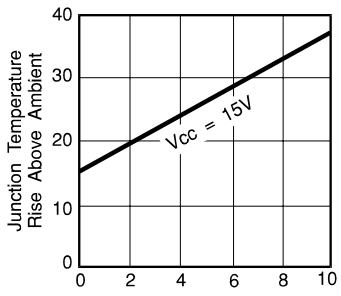
POSITIVE OUTPUT (TYP)

QUIESCENT CURRENT VS. TEMP



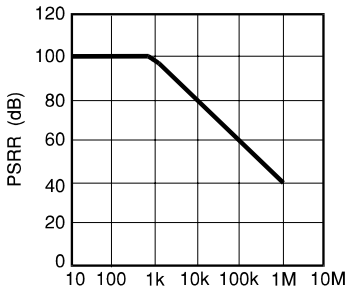
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

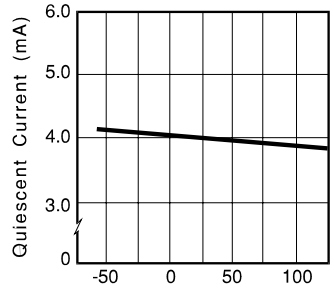
PSRR VS. FREQUENCY



Frequency (Hz)

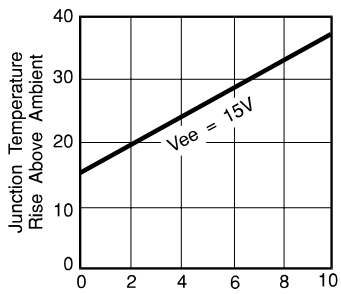
NEGATIVE OUTPUT (TYP)

QUIESCENT CURRENT VS. TEMP



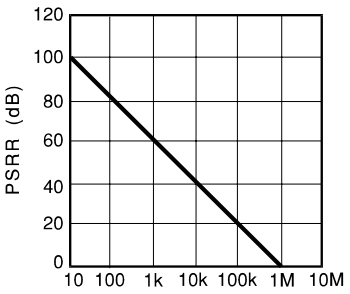
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

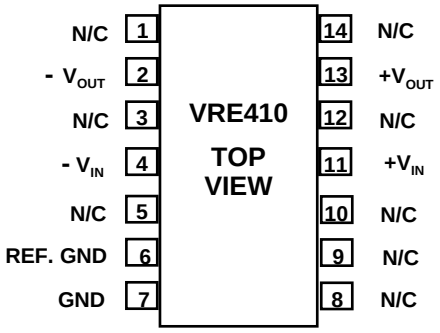
The following discussion refers to the block diagram in Figure 1. In operation, approximately 6.3 V is applied to the noninverting input of the op amp. The voltage is amplified by the op amp to produce a 10 V output. The gain is determined by the networks R1 and R2: G=1 + R2/R1. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The zener operating current is derived from the regulated output voltage through R3. This feedback arrangement provides a closely regulated zener current. This current determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage is produced over wide temperature ranges.

The VRE400 series voltage references have the ground terminal brought out on two pins (pin 6 and 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't effect performance.

PIN CONFIGURATION



Precision Voltage Reference

FEATURES

- +5 V Output, ± 1.0 mV (.02%)
- Temperature Drift: 1 ppm/ºC
- Low Noise: 3 μV_{P-P} (0.1-10 Hz)
- Industry Standard Pinout: 8-pin Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typ.
- Output Trim Capability

DESCRIPTION

The VRE505 is a low cost, high precision +5 V reference. The device is ideal for upgrading systems that use lower performance references.

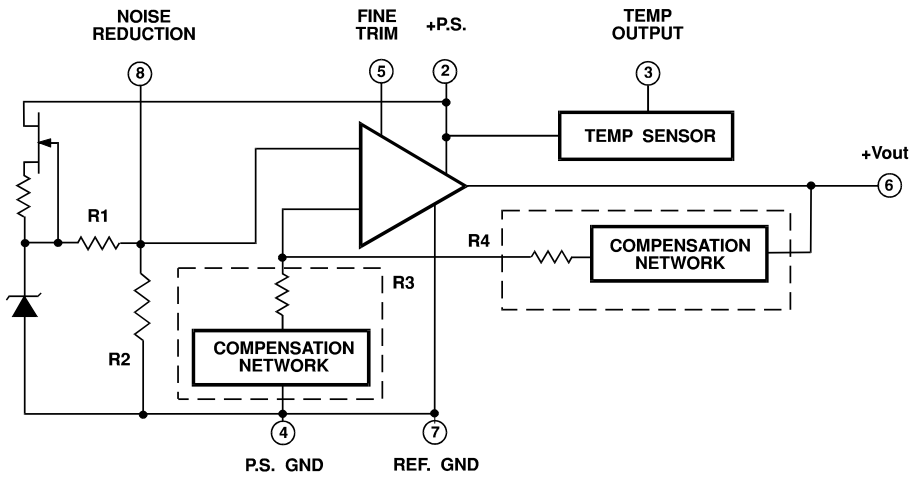
The device provides ultrastable +5 V output with ±0.5 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/ºC. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE505 the most accurate reference available.

For enhanced performance, the VRE505 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

The VRE505 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE505 offers superior performance over monolithic references.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE505K	±1.0	2.0	-40ºC to +85ºC

8-pin Surface Mount Package Style GF

1. CHARACTERISTICS AND SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{PS} = +15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

Parameter	Min	Typ	Max	Units
ABSOLUTE RATINGS				
Power Supply	±13.5	±15	±22	V
Operating Temperature	-40		+85	ºC
Storage Temperature	-65		+150	ºC
Short Circuit Protection		Continuous		
OUTPUT VOLTAGE				
VRE505		+5.0		V
Temperature Sensor Voltage (Note 1)		630		
OUTPUT VOLTAGE ERRORS				
Initial Error (Note 2)			±1.0	mV
Warmup Drift		2		ppm
T_{MIN} - T_{MAX} (Note 3)			2.0	ppm/ºC
Long-Term Stability		6		ppm/1000hrs.
Noise (0.1 - 10Hz) (Note 4)		3		µVpp
OUTPUT CURRENT				
Range	±10			mA
REGULATION				
Line		6	10	ppm/V
Load		3		ppm/mA
OUTPUT ADJUSTMENT				
Range		10		mV
POWER SUPPLY CURRENT (Note 5)				
+PS		5	7	mA

NOTES:

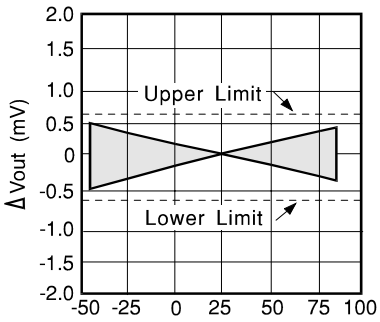
1. The temp. reference T_C is 2.1 mV/ºC
2. The specified values are without external trim.
3. The temperature coefficient is determined by the box method using the following formula:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

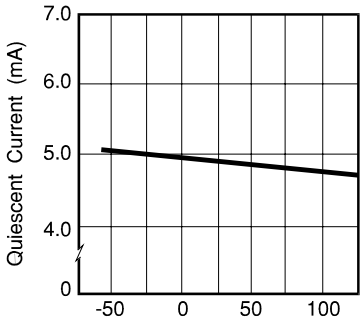
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



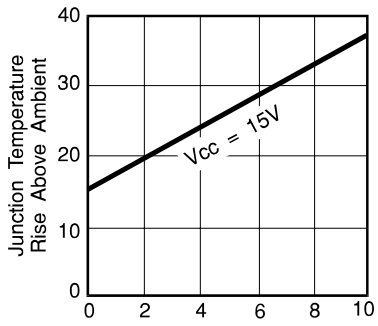
Temperature ºC
VRE505K

QUIESCENT CURRENT VS. TEMP



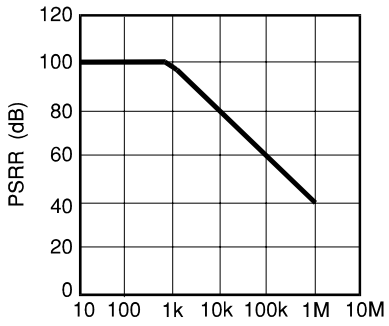
Temperature ºC

JUNCTION TEMP. RISE VS. OUTPUT CURRENT



Output Current (mA)

PSRR VS. FREQUENCY



Frequency (Hz)

3. THEORY OF OPERATION

The following discussion refers to the Block Diagram. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5.0 V output. The gain is determined by the resistor networks R3 and R4: G = 1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

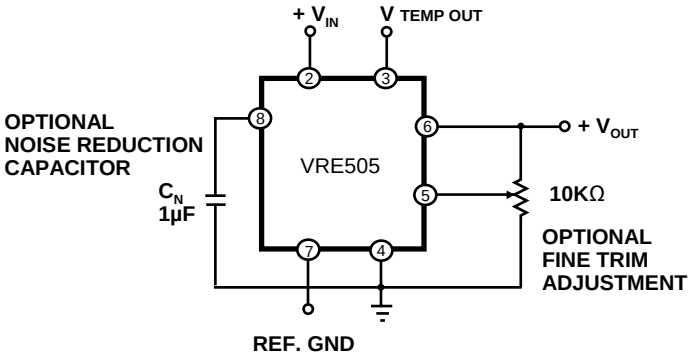
The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, this device produces a very stable voltage over wide temperature ranges.

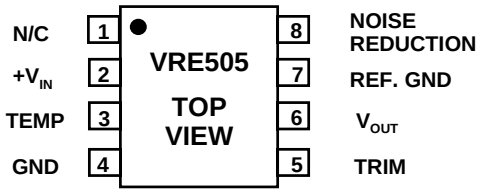
This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE505 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below. The VRE505 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

EXTERNAL CONNECTIONS



PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- +2.5 V Output, ± 0.25 mV (.01%)
- Temperature Drift: 0.6 ppm/ºc
- Low Noise: 1.5 μV_{P-P} (0.1Hz-10Hz)
- Low Thermal Hysteresis: 1 ppm Typical
- ±15 mA Output Source and Sink Current
- Excellent Line Regulation: 5 ppm/V Typical
- Optional Noise Reduction and Voltage Trim
- Industry Standard Pinout: 8-pin DIP or Surface Mount Package

APPLICATIONS

The VRE3025 is recommended for use as a reference for 14, 16, or 18 bit data converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution data converters. The VRE3025 offers superior performance over monolithic references.

DESCRIPTION

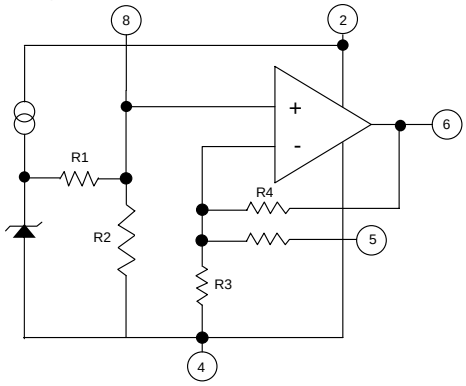
The VRE3025 is a low cost, high precision +2.5 V reference that operates from +10 V. The device features a buried zener for low noise and excellent long term stability. Packaged in either an 8-pin DIP or SMT option, the device is ideal for high resolution data conversion systems.

The device provides ultrastable +2.5 V output with ±0.25 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/ºC. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE3025 series the most accurate reference available.

For enhanced performance, the VRE3025 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)	Package Options
VRE3025AS	0.250	0.6	0ºC to +70ºC	SMT8 (GF)
VRE3025AD	0.250	0.6	0ºC to +70ºC	DIP8 (KD)
VRE3025BS	0.375	1.0	0ºC to +70ºC	SMT8 (GF)
VRE3025BD	0.375	1.0	0ºC to +70ºC	DIP8 (KD)
VRE3025CS	0.500	2.0	0ºC to +70ºC	SMT8 (GF)
VRE3025CD	0.500	2.0	0ºC to +70ºC	DIP8 (KD)
VRE3025JS	0.250	0.6	-40ºC to +85ºC	SMT8 (GF)
VRE3025JD	0.250	0.6	-40ºC to +85ºC	DIP8 (KD)
VRE3025LS	0.500	2.0	-40ºC to +85ºC	SMT8 (GF)

8-pin Surface Mount Package Style GF

8-pin DIP Package Style KD

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... -0.3V to +40V
OUT, TRIM..... -0.3V to +12V
NR ..... -0.3V to +6V
Operating Temp. (A,B,C) ..... 0ºC to +70ºC
Operating Temp. (J,L)..... -40ºC to +85ºC

Out Short Circuit to GND Duration (V_{IN}< 12V)..... Continuous
Out Short Circuit to GND Duration (V_{IN}< 40V).....5 sec
Out Short Circuit to IN Duration (V_{IN}< 12V) ..... Continuous
Continuous Power Dissipation (T_A = +70ºC)..... 300mW
Storage Temperature..... -65ºC to +150ºC
Lead Temperature (soldering,10 sec)..... +250ºC

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

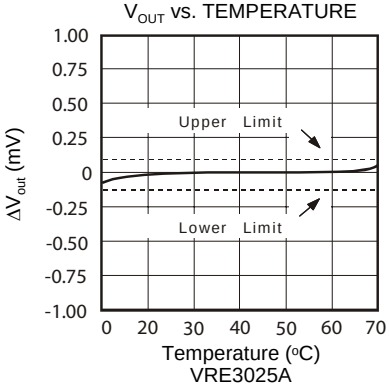
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		+8		+36	V
Output Voltage (Note 1)	V_{OUT}	VRE3025A/J	+2.4998	+2.500	+2.5003	V
		VRE3025B	+2.4996	+2.500	+2.5004	
		VRE3025C/L	+2.4995	+2.500	+2.5005	
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	VRE3025A/J		0.3	0.6	ppm/ºC
		VRE3025B		0.5	1.0	
		VRE3025C/L		1.0	2.0	
Trim Adjustment Range	ΔV_{OUT}	Figure 3		±2.5		mV
Turn-On Settling Time	T_{ON}	To 0.01% of final value		2		µs
Output Noise Voltage	e_n	0.1Hz < f < 10Hz		1.5		µVp-p
		10Hz < f < 1kHz		1.5	3.0	μV_{RMS}
Temperature Hysterisis		Note 4		1		ppm
Long Term Stability	$\Delta V_{OUT/t}$			6		ppm/1000hrs.
Supply Current	I_{IN}			3.5	4.0	mA
Load Regualtion	$\Delta V_{OUT}/ \Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA		8	12	ppm/mA
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA		8	12	
Line Regulation	$\Delta V_{OUT}/ \Delta V_{IN}$	8V ≤ V_{IN} ≤ 10V		25	35	ppm/V
		10V ≤ V_{IN} ≤ 18V		5	10	

NOTES:

1. The specified values are without external trim.
2. The temperature coefficient is determined by the box method. See discussion on temperature performance.
3. Line and load regulation are measured with pulses and do not include voltage changes due to temperature.
4. Hysterisis over the operating temperature range.

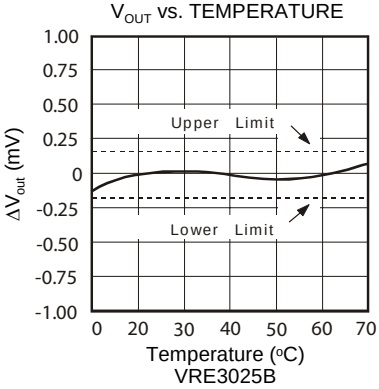
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



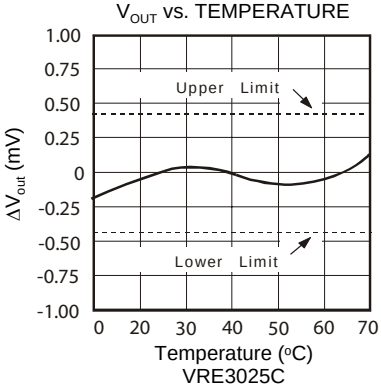
VRE3025A

V_{OUT} vs. TEMPERATURE



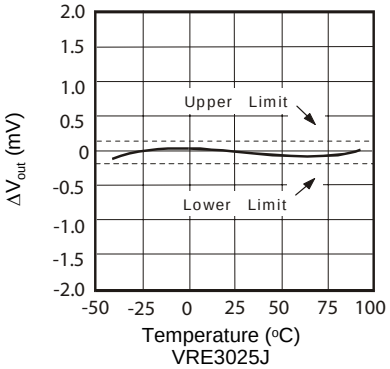
VRE3025B

V_{OUT} vs. TEMPERATURE



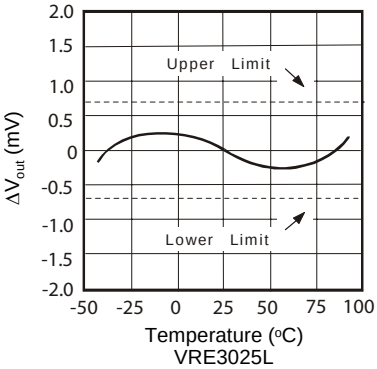
VRE3025C

V_{OUT} vs. TEMPERATURE



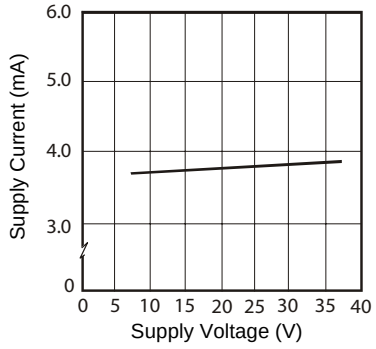
VRE3025J

V_{OUT} vs. TEMPERATURE

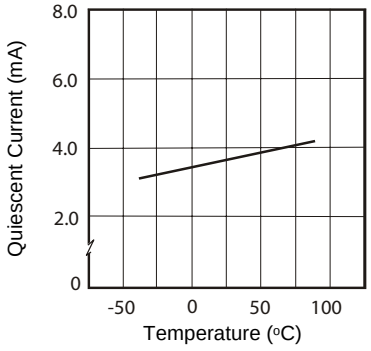


VRE3025L

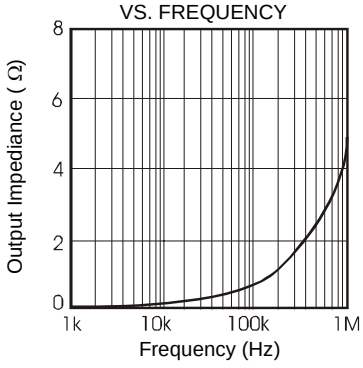
SUPPLY CURRENT VS. SUPPLY VOLTAGE



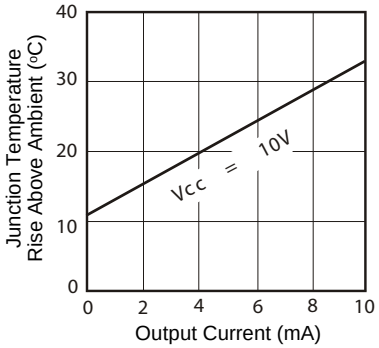
QUIESCENT CURRENT VS. TEMP



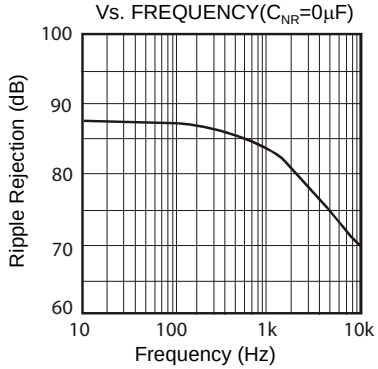
OUTPUT IMPEDIANCE VS. FREQUENCY



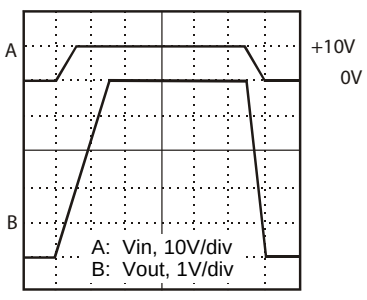
JUNCTION TEMP. RISE VS. OUTPUT CURRENT



RIPPLE REJECTION Vs. FREQUENCY(C_{NR}=0µF)

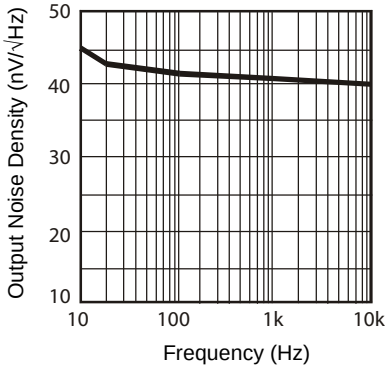


TURN-ON AND TURN-OFF TRANSIENT RESPONSE

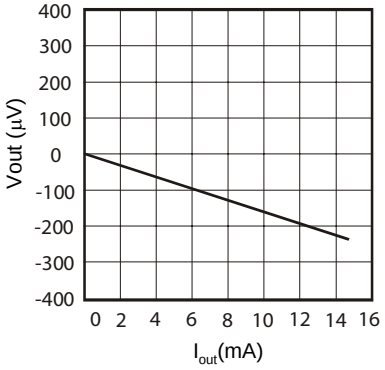


1 µs/div

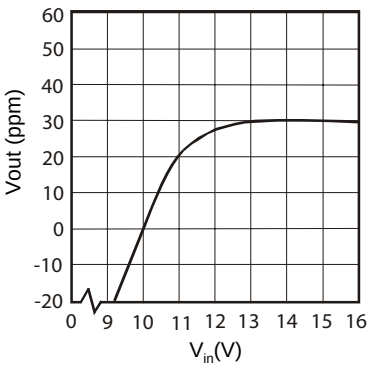
OUTPUT NOISE-VOLTAGE DENSITY vs. FREQUENCY



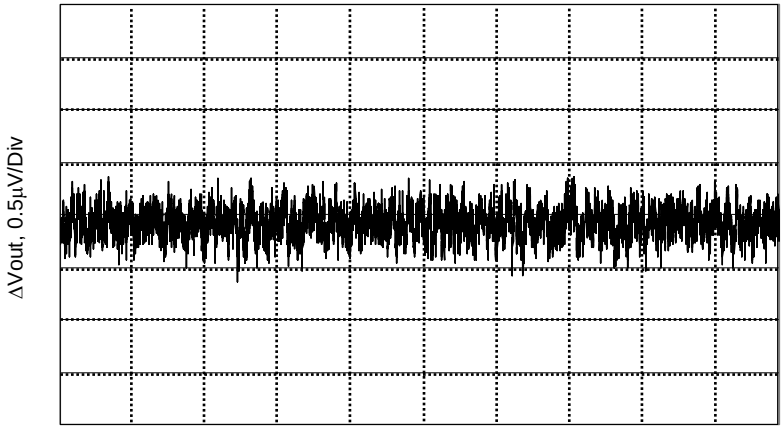
CHANGE IN OUTPUT VOLTAGE VS. OUTPUT CURRENT



CHANGE IN OUTPUT VOLTAGE VS. INPUT VOLTAGE



0.1Hz to 10Hz Noise



3. THEORY OF OPERATION

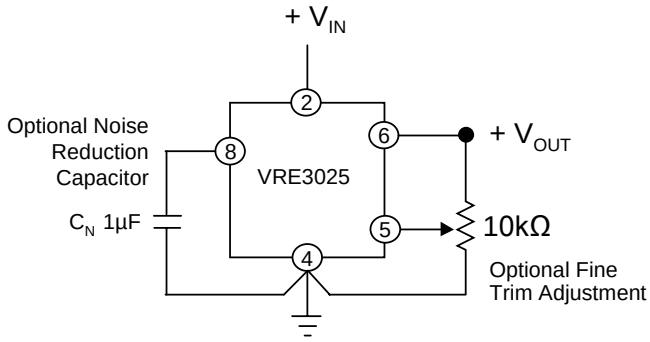
The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 2.5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors that is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. The proper connection of the VRE3025 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below.

EXTERNAL CONNECTIONS



PIN DESCRIPTIONS

1, 3, 7	N. C.	Internally connected. Do not use
2	V_{IN}	Positive power supply input
4	GND	Ground
5	TRIM	External trim input. Leave open if not used.
6	OUT	Voltage reference output
8	NR	Noise Reduction

4. BASIC CIRCUIT CONNECTION

To achieve the specified performance, pay careful attention to the layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected to a single point to minimize interconnect resistances.

5. TEMPERATURE PERFORMANCE

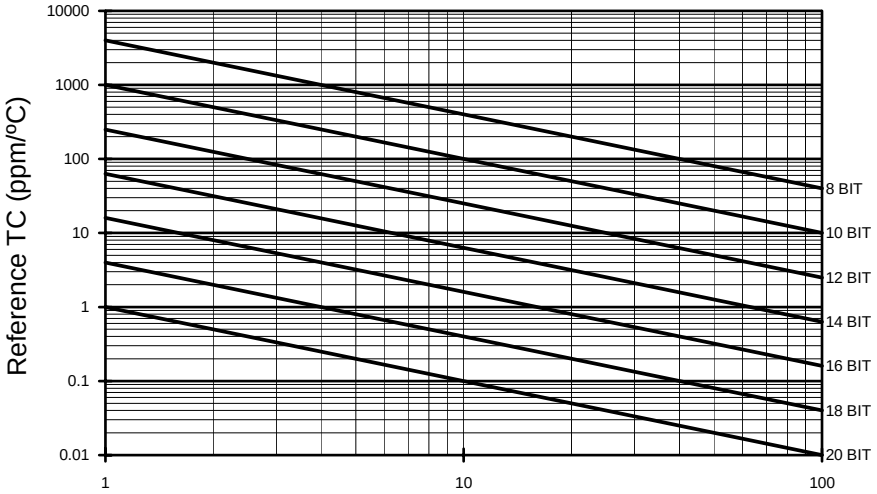
The VRE3025 is designed for applications where the initial error at room temperature and drift over temperature are important to the user. For many instrument manufacturers, a voltage reference with a temperature coefficient less than 1 ppm/°C makes it possible to not have to perform a system temperature calibration, a slow and costly process.

Of the three TC specification methods (slope, butterfly, and box), the box method is used commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape and slope of the device under test.

A designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (-40°C to +85°C), will need a voltage reference with a temperature coefficient (TC) of 1.0 ppm/°C if the reference is allowed to contribute an error equivalent to 1LSB. For 1/2LSB equivalent error from the reference you would need a voltage reference with a temperature coefficient of 0.5 ppm/°C. Figure 4 shows the required reference TC vs. delta T change from 25°C for resolution ranging from 8 bits to 20 bits.

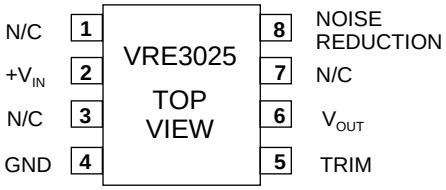


Reference TC vs. ΔT change from 25°C for 1 LSB change

6. THERMAL HYSTERISIS

A change in output voltage as a result of a temperature change. When references experience a temperature change and return to the initial temperature, they do not always have the same initial voltage. Thermal hysterisis is difficult to correct and is a major error source in systems that experience temperature changes greater than 25°C. Reference vendors are starting to include this important specification in their datasheets.

PIN CONFIGURATION



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Precision Voltage Reference

FEATURES

- +5 V Output, ± 0.5 mV (.01%)
- Temperature Drift: 0.6 ppm/ºC
- Low Noise: 3 μV_{P-P} (0.1Hz-10Hz)
- Low Thermal Hysterisis: 1 ppm Typical
- ±15mA Output Source and Sink Current
- Excellent Line Regulation: 5 ppm/V Typical
- Optional Noise Reduction and Voltage Trim
- Industry Standard Pinout: 8-pin Surface Mount Package

APPLICATIONS

The VRE3050 is recommended for use as a reference for 14, 16, or 18 bit data converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution data converters. The VRE3050 offers superior performance over monolithic references.

DESCRIPTION

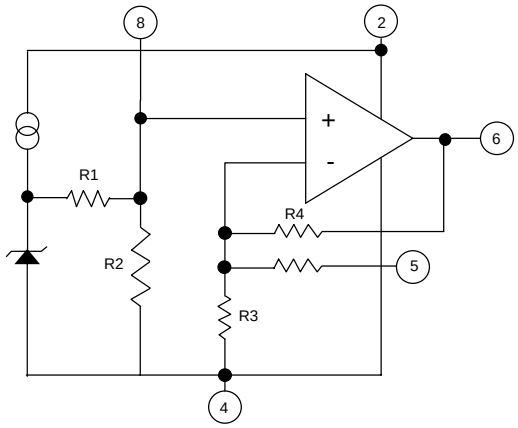
The VRE3050 is a low cost, high precision 5 V reference that operates from +10 V. The device features a buried zener for low noise and excellent long term stability. Packaged in an 8-pin SMT, the device is ideal for high resolution data conversion systems.

The device provides ultrastable +5 V output with ±0.5 mV (.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE3050 series the most accurate reference available.

For enhanced performance, the VRE3050 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin.

C

Figure 1. BLOCK DIAGRAM



SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE3050A	±0.5	0.6	0ºC to +70ºC
VRE3050B	±0.8	1.0	0ºC to +70ºC
VRE3050C	±1.0	2.0	0ºC to +70ºC
VRE3050J	±0.5	0.6	-40ºC to +85ºC
VRE3050K	±0.8	1.0	-40ºC to +85ºC
VRE3050L	±1.0	2.0	-40ºC to +85ºC

8-pin Surface Mount Package Style GF

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... -0.3V to +40V
OUT, TRIM..... -0.3V to +12V
NR ..... -0.3V to +6V
Operating Temp. (A,B,C) ..... 0ºC to +70ºC
Operating Temp. (J,K,L) ..... -40ºC to +85ºC

Out Short Circuit to GND Duration (V_{IN}< 12V)..... Continuous
Out Short Circuit to GND Duration (V_{IN}< 40V).....5 sec
Out Short Circuit to IN Duration (V_{IN}< 12V) ..... Continuous
Continuous Power Dissipation (T_A = +70ºC).....300mW
Storage Temperature..... -65ºC to +150ºC
Lead Temperature (soldering,10 sec)..... +250ºC

ELECTRICAL SPECIFICATIONS

V_{PS} =±15V, T = +25ºC, R_L = 10KΩ Unless Otherwise Noted.

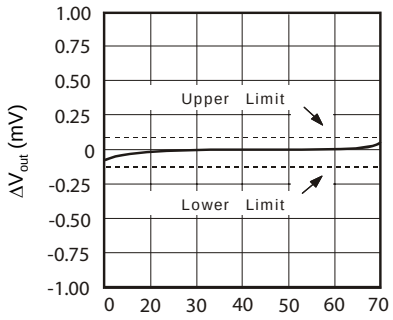
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		+8		+36	V
Output Voltage (Note 1)	V_{OUT}	VRE3050A/J	+2.4995	+5.0000	+5.0005	V
		VRE3050B/K	+2.4992	+5.0000	+5.0008	
		VRE3050C/L	+2.4990	+5.0000	+5.0010	
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	VRE3050A/J		0.3	0.6	ppm/ºC
		VRE3050B/K		0.5	1.0	
		VRE3050C/L		1.0	2.0	
Trim Adjustment Range	ΔV_{OUT}	Figure 3		±5.0		mV
Turn-On Settling Time	T_{ON}	To 0.01% of final value		2.0		µs
Output Noise Voltage	e_n	0.1Hz < f < 10Hz		3.0		µVp-p
		10Hz < f < 1kHz		2.5	5.0	μV_{RMS}
Temperature Hysterisis		Note 4		1		ppm
Long Term Stability	$\Delta V_{OUT/t}$			6		ppm/1000hrs.
Supply Current	I_{IN}			3.5	4.0	mA
Load Regualtion (Note 3)	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA		8	12	ppm/mA
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA		8	12	
Line Regulation (Note 3)	$\Delta V_{OUT}/\Delta V_{IN}$	8V ≤ V_{IN} ≤ 10V		25	35	ppm/V
		10V ≤ V_{IN} ≤ 18V		5	10	

NOTES:

1. The specified values are without external trim.
2. The temperature coefficient is determined by the box method. See discussion on temperature performance.
3. Line and load regulation are measured with pulses and do not include voltage changes due to temperature.
4. Hysterisis over the operating temperature range.

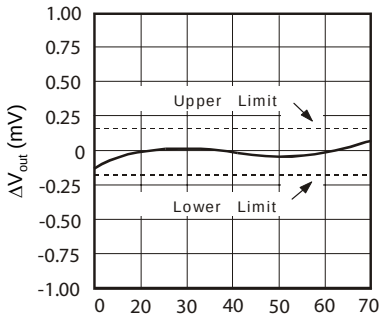
2. TYPICAL PERFORMANCE CURVES

V_{OUT} vs. TEMPERATURE



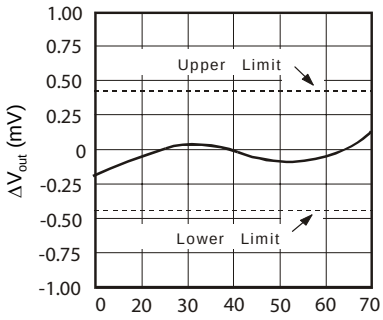
VRE3050A

V_{OUT} vs. TEMPERATURE



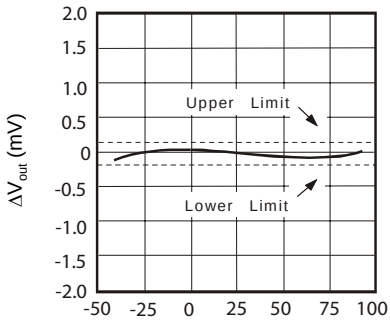
VRE3050B

V_{OUT} vs. TEMPERATURE



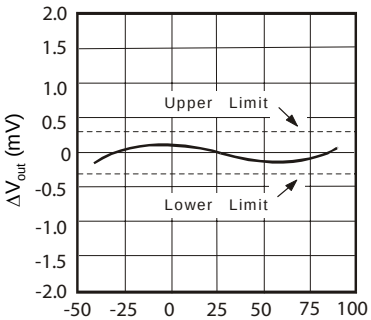
VRE3050C

V_{OUT} vs. TEMPERATURE



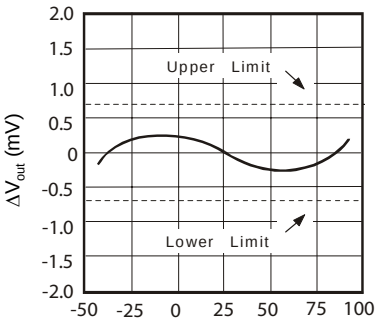
VRE3050J

V_{OUT} vs. TEMPERATURE



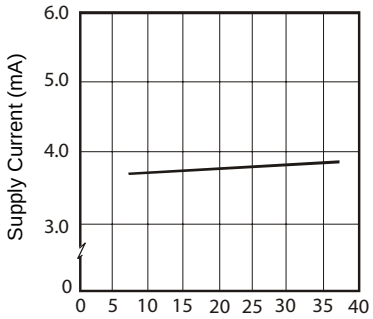
VRE3050K

V_{OUT} vs. TEMPERATURE

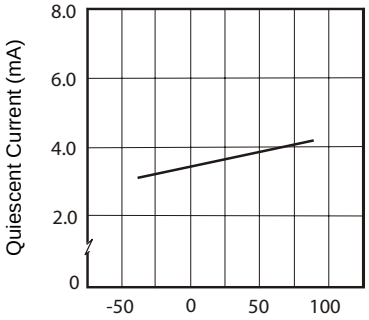


VRE3050L

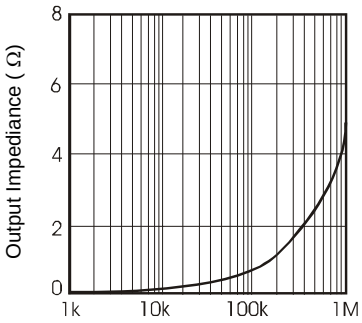
SUPPLY CURRENT VS. SUPPLY VOLTAGE



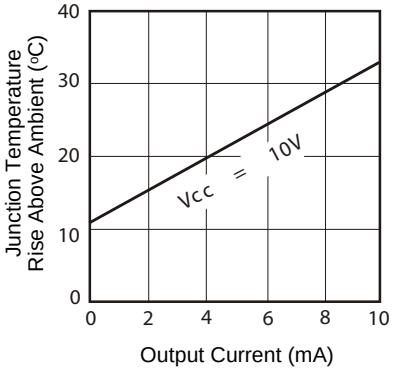
QUIESCENT CURRENT VS. TEMP



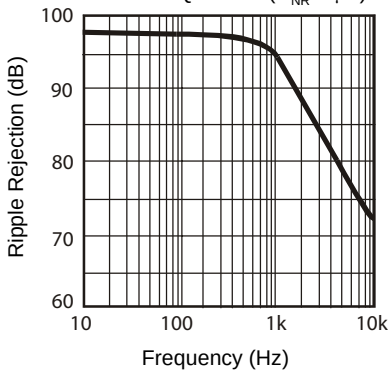
OUTPUT IMPEDIANCE VS. FREQUENCY



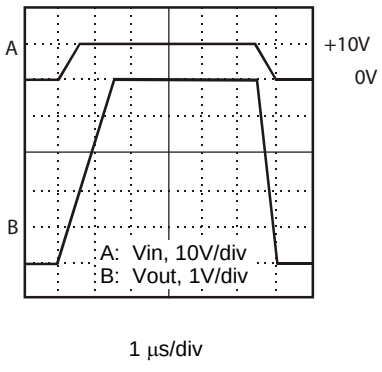
JUNCTION TEMP. RISE VS. OUTPUT CURRENT



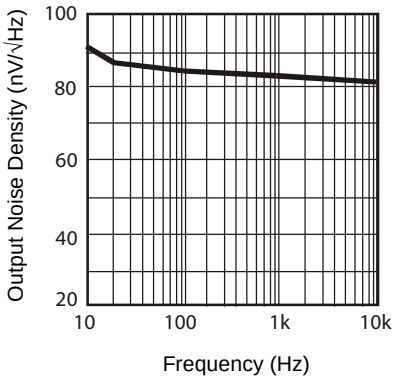
RIPPLE REJECTION Vs. FREQUENCY(C_{NR}=0µF)



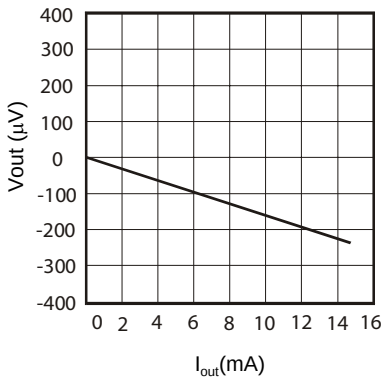
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



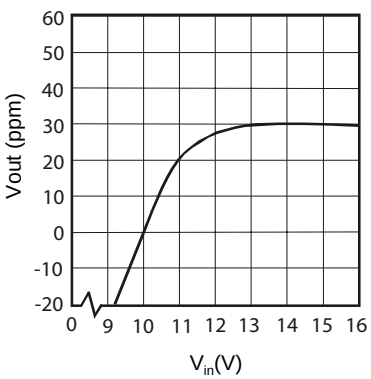
OUTPUT NOISE-VOLTAGE DENSITY vs. FREQUENCY



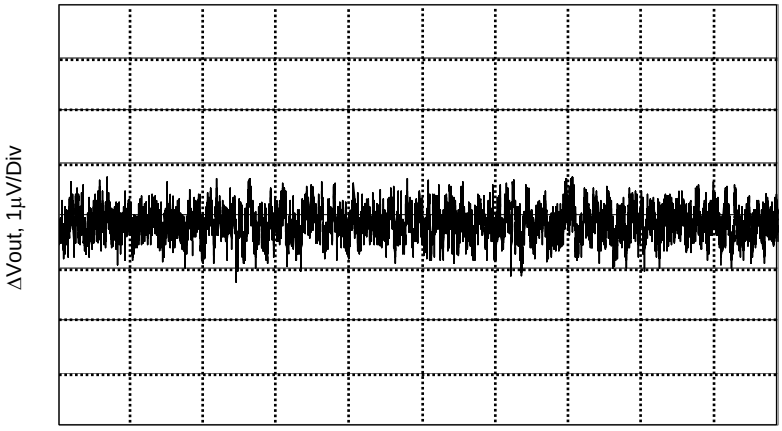
CHANGE IN OUTPUT VOLTAGE VS. OUTPUT CURRENT



CHANGE IN OUTPUT VOLTAGE VS. INPUT VOLTAGE



0.1Hz to 10Hz Noise



1 Sec/Div

3. THEORY OF OPERATION

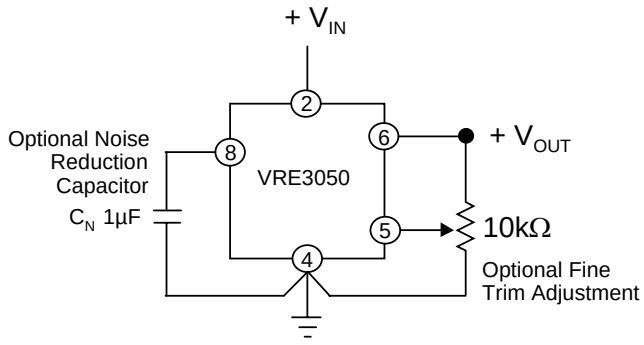
The following discussion refers to the block diagram in Figure 1. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors that is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. The proper connection of the VRE3050 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown below.

EXTERNAL CONNECTIONS



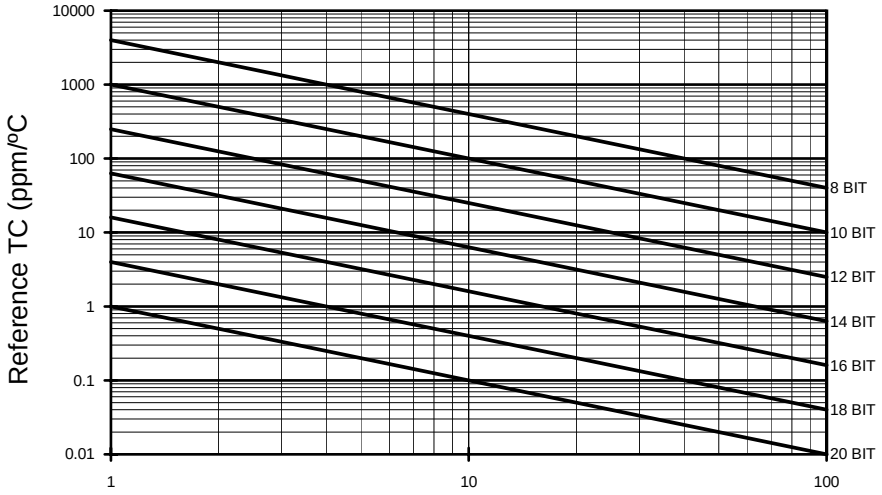
PIN DESCRIPTION

1, 3, 7	N. C.	Internally connected. Do not use
2	V_{IN}	Positive power supply input
4	GND	Ground
5	TRIM	External trim input. Leave open if not used.
6	OUT	Voltage reference output
8	NR	Noise Reduction

4. BASIC CIRCUIT CONNECTION

To achieve the specified performance, pay careful attention to the layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected to a single point to minimize interconnect resistances.

Figure 3.



Reference TC vs. ΔT change from 25°C for 1 LSB change

5. TEMPERATURE PERFORMANCE

The VRE3050 is designed for applications where the initial error at room temperature and drift over temperature are important to the user. For many instrument manufacturers, a voltage reference with a temperature coefficient less than 1 ppm/°C makes it possible to not perform a system temperature calibration, a slow and costly process.

Of the three TC specification methods (slope, butterfly, and box), the box method is most commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows:

$$T.C. = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

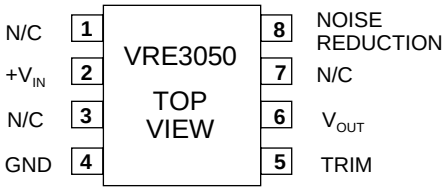
This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape and slope of the device under test.

A designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (-40°C to +85°C), will need a voltage reference with a temperature coefficient (TC) of 1 ppm/°C if the reference is allowed to contribute an error equivalent to 1LSB. For 1/2LSB equivalent error from the reference you would need a voltage reference with a temperature coefficient of 0.5 ppm/°C. Figure 4 shows the required reference TC vs. delta T change from 25°C for resolution ranging from 8 bits to 20 bits.

6. THERMAL HYSTERISIS

A change in output voltage as a result of a temperature change. When references experience a temperature change and return to the initial temperature, they do not always have the same initial voltage. Thermal hysterisis is difficult to correct and is a major error source in systems that experience temperature changes greater than 25°C. Reference vendors are starting to include this important specification in their datasheets.

PIN CONFIGURATION



Product Innovation From CIRRUS LOGIC®

VRE4112 VRE4125 VRE4141

Precision Voltage Reference

FEATURES

- +1.250, +2.500, +4.096 V Output
- Initial Error: ± 0.05% Max.
- Temperature Drift: 1.0 ppm/ºC Max.
- Low Noise: 2.2 μV_{P-P} (0.1 Hz-10 Hz, 1.024 V)
- Low Thermal Hysteresis: 20 ppm
- ±8 mA Output Source
- Power Down Mode
- Industry Standard SOIC 8-pin Package
- Commercial and Industrial Temp Ranges
- Second source for ADR29X, REF19X ,LT1460, LT1461, LT1798, MAX616X, REF102

APPLICATIONS

This series is recommended for use as a reference for 14, 16, or 18-bit data converters which require a precision reference. The series offers superior performance over standard on-chip references commonly found with data converters.

DESCRIPTION

The VRE4112/VRE4125/VRE4141 are low cost, high precision bandgap references that operate from +5 V. These devices feature low noise, digital error correction, and an SOIC-8 package. The ultra stable output is 0.05% accurate with a temperature coefficient as low as 1.0 ppm/ºC. The improvement in overall accuracy is made possible by using EEPROM registers and CMOS DAC's for temperature and initial error correction. The DAC trimming is done after assembly which eliminates assembly related shifts.

C

SELECTION GUIDE

Model	Output (V)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE4112C	+1.250	2.0	0ºC to +70ºC
VRE4112K	+1.250	3.0	-40ºC to +85ºC
VRE4125B	+2.500	1.0	0ºC to +70ºC
VRE4125K	+2.500	3.0	-40ºC to +85ºC
VRE4141B	+4.096	1.0	0ºC to +70ºC
VRE4141K	+4.096	3.0	-40ºC to +85ºC

8-pin SOIC
Package Style FX

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply to any input pin .....-0.3V to +5.6V
Operating Temp. (B,C)..... 0ºC to 70ºC
Operating Temp. (K) .....-40ºC to +85ºC
Storage Temperature Range .....-65ºC to +150ºC

Output Short Circuit Duration ..... Indefinite
ESD Susceptibility Human Body Model..... 2kV
ESD Susceptibility Machine Model..... 200V
Lead Temperature (soldering, 10 sec).....+260ºC

ELECTRICAL SPECIFICATIONS

V_{PS} = +3 V for VRE4112, V_{PS} = +5 V for VRE4125 and VRE4141. T = +25ºC, I_{LOAD} = 1mA, C_{OUT} = 1µF Unless Otherwise Noted.

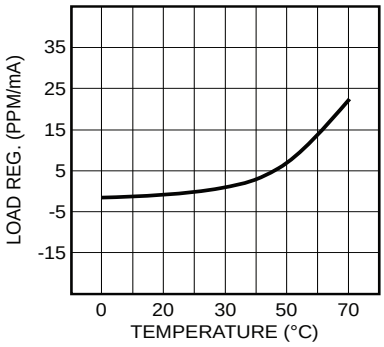
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		+1.8		+5.5	V
Output Voltage Error (Note 1)	V_{OUT}	B Grade		±0.025	±0.050	%
		C/K Grade		±0.040	±0.080	
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	B Grade		+0.5	+1.0	ppm/ºC
		C Grade		+1.0	+2.0	
		K Grade		+1.5	+3.0	
Dropout Voltage (Note 3)	V_{IN} - V_{OUT}	I_L = 8mA		160	235	mV
Turn-On Settling Time	T_{ON}	To 0.01% of final value		2		µs
Output Noise Voltage (Note 4)	E_n	0.1Hz < f < 10Hz		2.2		µVp-p
Temperature Hysteresis		Note 5		20		ppm
Long Term Stability	$\Delta V_{OUT/T}$	1000 Hours		50		ppm
Supply Current	I_{IN}	V_{LOAD} = 0mA		230	320	µA
Load Regulation (Note 6)	$\Delta V_{OUT}/ \Delta I_{OUT}$	1mA ≤ I_{LOAD} ≤ 8mA		1	20	ppm/mA
Line Regulation (Note 6)	$\Delta V_{OUT}/ \Delta V_{IN}$	V_{REF} + 200mV ≤ V_{IN} ≤ 5.5V		20	200	ppm/V
Logic High Input Voltage	V_H		0.8			V
Logic High Input Current	I_H			2		nA
Logic Low Input Voltage	V_L				0.4	V
Logic Low Input Current	I_L			1		nA

NOTES:

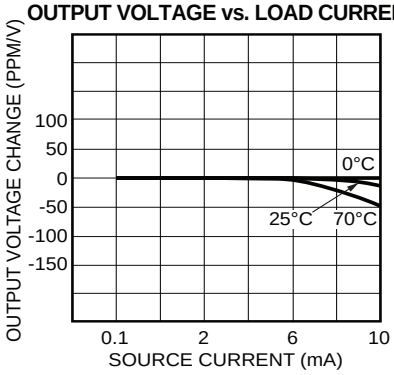
1. High temperature and mechanical stress can effect the initial accuracy of this reference series.See discussion on output accuracy.
2. The temperature coefficient is determined by the box method. See discussion on temperature performance. All units are 100% tested over temperature.
3. The minimum input to output differential voltage at which the output voltage drops by 0.5% from nominal.
4. Based on 1.024 V output. Noise is linearly proportional to V_{REF}.
5. Defined as change in 25ºC output voltage after cycling device over operating temperature range.
6. Line and load regulation are measured with pulses and do not include output voltage changes due to self heating.

2. TYPICAL PERFORMANCE CURVES

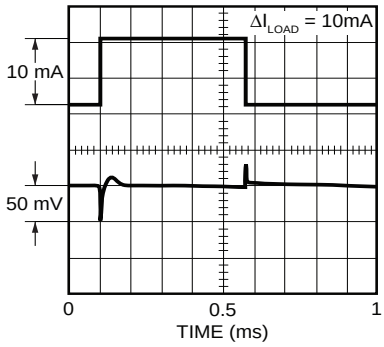
LOAD REGULATION vs. TEMPERATURE



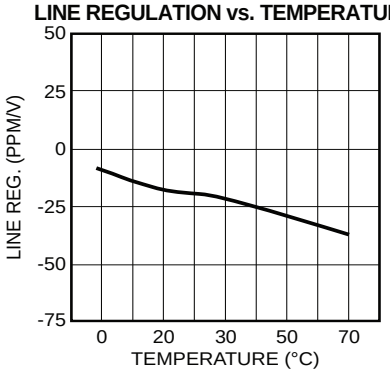
OUTPUT VOLTAGE vs. LOAD CURRENT



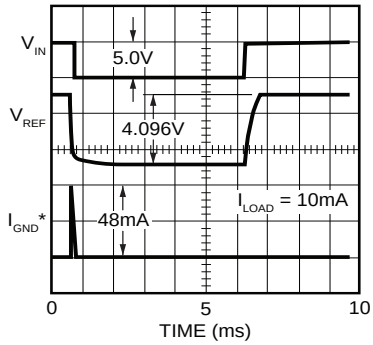
LOAD TRANSIENT RESPONSE



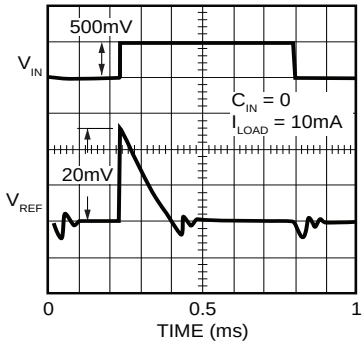
LINE REGULATION vs. TEMPERATURE



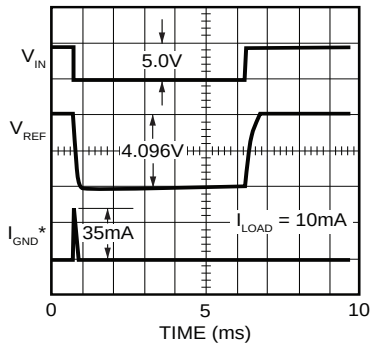
POWER UP/DOWN GROUND CURRENT



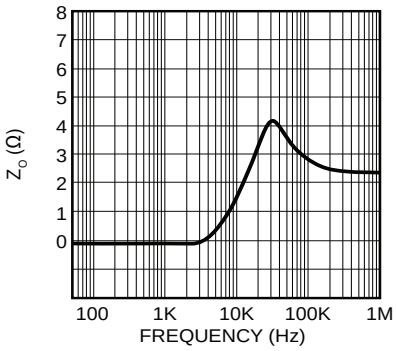
LINE TRANSIENT RESPONSE



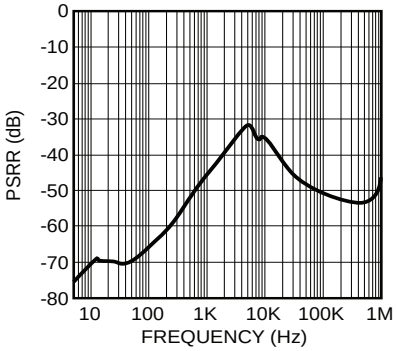
ENABLE RESPONSE



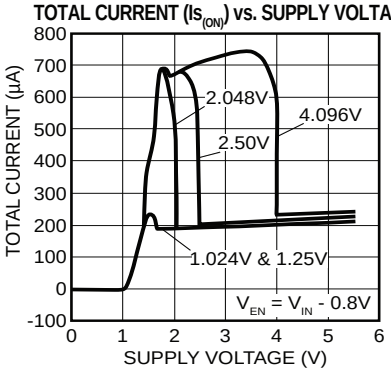
OUTPUT IMPEDANCE



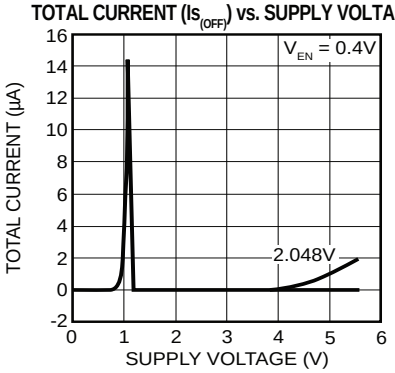
POWER SUPPLY REJECTION RATIO



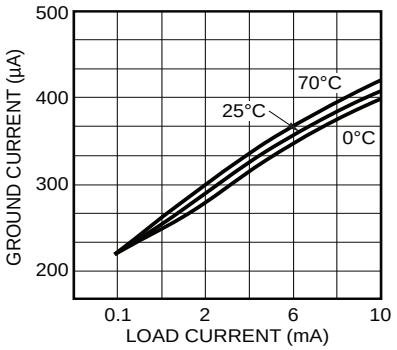
TOTAL CURRENT ($Is_{(ON)}$) vs. SUPPLY VOLTAGE



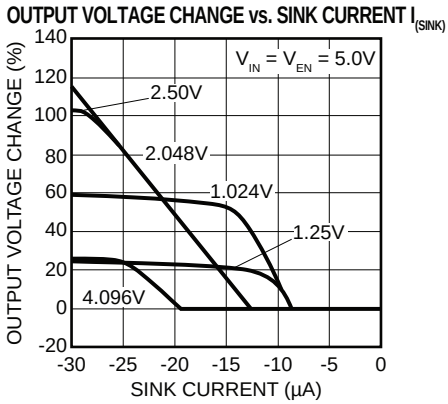
TOTAL CURRENT ($Is_{(OFF)}$) vs. SUPPLY VOLTAGE

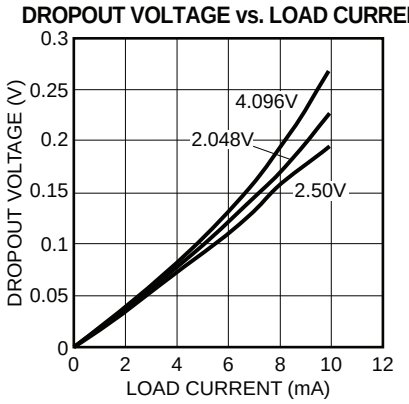


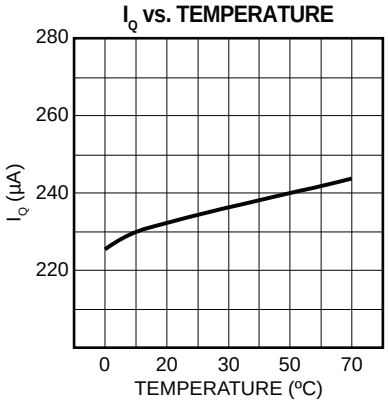
GROUND CURRENT vs. LOAD CURRENT

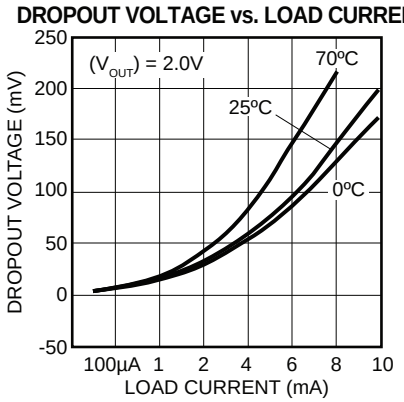


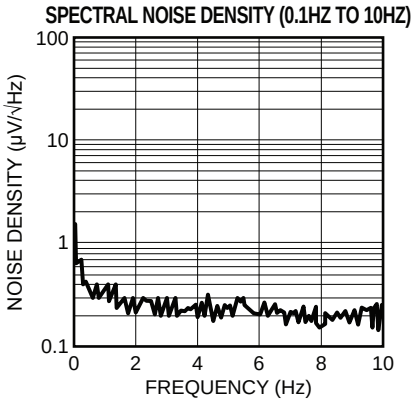
2. TYPICAL PERFORMANCE CURVES, Cont.

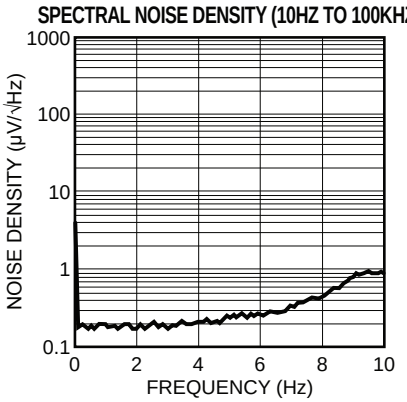












3. TEMPERATURE PERFORMANCE

This series is designed for applications where the initial error at room temperature and drift over temperature are important to the user. For many instrument manufacturers, a voltage reference with a temperature coefficient of 1ppm/ºC makes it possible to eliminate a system temperature calibration, a slow and costly process.

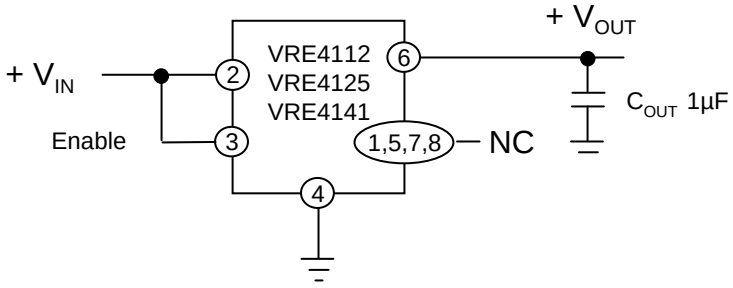
Of the three TC specification methods (slope, butterfly, and box), the box method is most commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape or slope of the device under test.

4. BASIC CIRCUIT CONNECTION

The proper connection for the VRE4112/VRE4125/ VRE4141 series voltage references is shown here. To achieve the specified performance, pay careful attention to the layout. Commons should be connected to a single point to minimize interconnect resistances. This will reduce voltage errors, noise pickup, and noise coupled from the power supply.

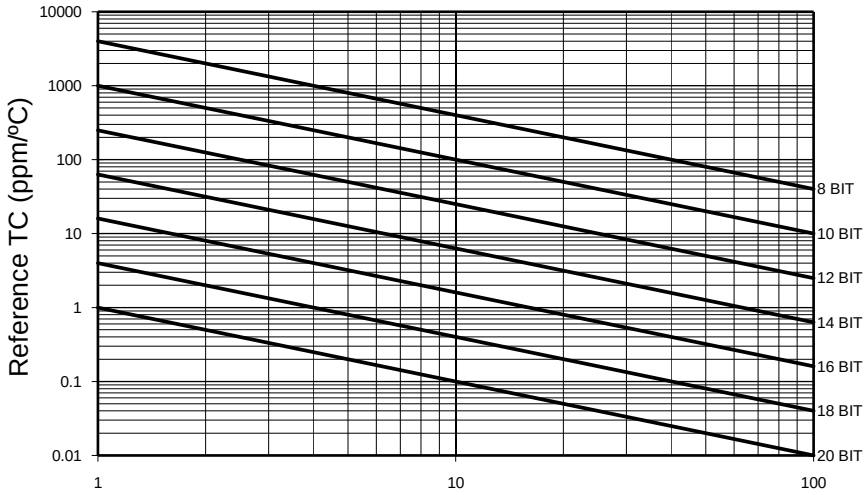


PIN DESCRIPTION

4	GND	These must be connected to ground
2	V_{IN}	Positive power supply input
3	Enable	Pulled to V_{IN} for nominal operation
1,5,7,8	NC	This pin must be left open
6	V_{OUT}	Reference output

EXTERNAL CONNECTIONS

For example a designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (-40ºC to +85ºC), will need a voltage reference with a temperature coefficient (TC) of 1.0ppm/ºC if the reference is allowed to contribute an error equivalent to 1LSB. The required reference TC vs. ΔT change from 25ºC for resolution ranging from 8 bits to 20 bits is shown below.



Reference TC vs. ΔT change from 25°C for 1 LSB change

5. OPERATIONAL NOTES

INPUT CAPACITOR

An input capacitor is recommended for the VRE4112/VRE4125/VRE4141. A supply bypass capacitor on the input will assure that the reference is working from a low impedance source which will improve stability. It can improve the transient response when the load current is suddenly increased.

OUTPUT CAPACITOR

This series requires a 1 µF output capacitor for loop stabilization (compensation) as well as transient response. When the load current changes, the output capacitor must source or sink current during the time it takes the control loop of the device to respond.

The output capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR) range. See Capacitor Selection below.

CAPACITOR SELECTION

A minimum value of 0.2 µF over the operating temperature range is recommended. For a 0.22 µF capacitor the ESR range for 0°C to +70°C is 0.9 to 6.0; 1.0 µF is 0.8 to 6.0; and 10 µF is 0.4 to 7.0.

Surface mount tantalum capacitors offer small size for the value and ESR in the range required for this series. The optimum performance for the output capacitor is achieved with a 1.0 µF value.

Aluminum electrolytic capacitors have a relatively large size for the value. They meet the ESR requirements at 1.0 µF as long as the temperature is above 0°C. Below 0°C, the ESR increases and it may exceed the limits indicated in the figures.

ultilayer ceramic capacitors have a small size for the value, are available in surface mount, and have excellent RF characteristics. They may not meet the minimum ESR requirements and have a large change in value with temperature.

REVERSE CURRENT PATH

The P-channel pass transistor used in this series has an inherent diode connected between the Vin and VOUT pins. Forcing the output to voltages higher than the input or pulling Vin below the voltage stored in the output capacitor by more than the Vbe will forward bias this diode and current will flow from the Vout pin to Vin. This will not damage the device as long as the current does not exceed 50 mA.

ON/OFF OPERATION

This series features a sleep mode that is activated by pulling the enable pin low. To turn the reference on, the enable pin is pulled high. If this feature is not used, the enable pin should be tied to Vin to keep the reference on at all times. The enable pin must not be left unconnected (floating).

When powered off, these devices will quickly reduce both Vout and IQ to zero. During power down, the charge across the output capacitor is discharged to ground through the internal circuitry. On power up, the Vout is restored in less than 200 µs.

The signal source used to drive the enable pin can come from either a totem-pole output or an open collector output with a pull-up resistor to the input voltage. The signal source must be able to swing above and below the voltage thresholds to guarantee an ON or OFF state. It must not exceed the absolute maximum rating for the enable pin.

OUTPUT ACCURACY

The output accuracy after assembly at room temperature is made up of three components: initial accuracy of the device, thermal hysteresis, and mechanical stress. The initial accuracy is measured at the factory and may not reflect the actual output voltage when the devices are mounted to a PCB. The effects of mechanical stress and thermal hysteresis can shift the output voltage.

THERMAL HYSTERESIS

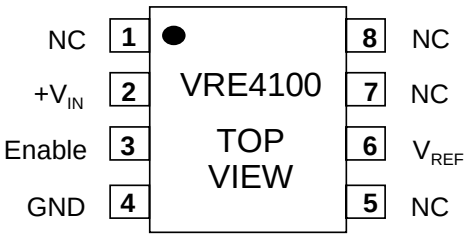
Thermal hysteresis is a change in output voltage as a result of a temperature change. When references experience a temperature change and return to the initial temperature, they do not always have the same initial voltage. Thermal hysteresis is difficult to correct and is a major error source in systems that experience temperature changes greater than 25°C. Reference vendors are starting to include this important specification in their datasheets

MECHANICAL HYSTERESIS

Recommendations to minimize mechanical stress:

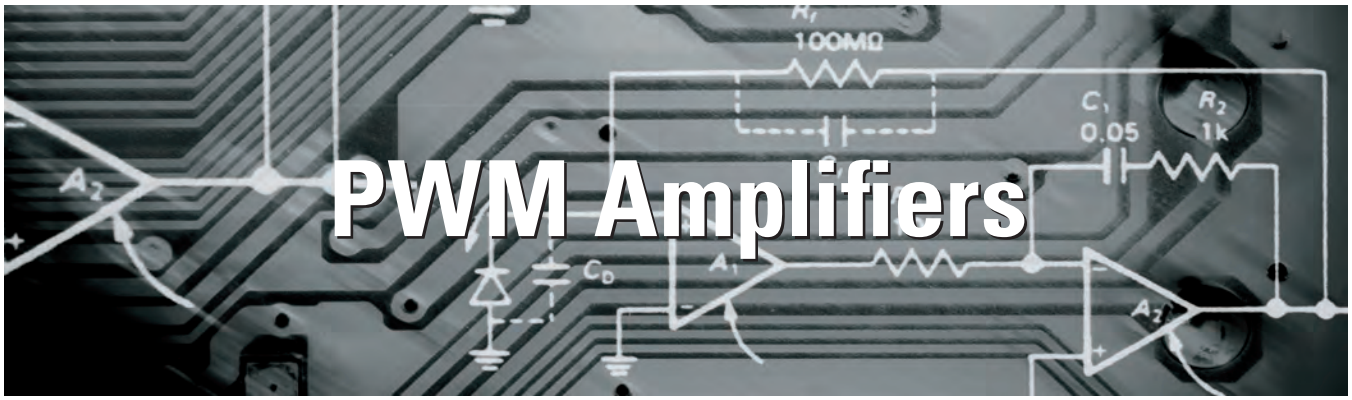
1) Mount the VRE4112/VRE4125/VRE4141 near the edges or corners of the PCB. The center of the board generally has the highest mechanical and thermal stress.
2) Mechanically isolate the device by cutting a U shaped slot around the package. This provides some mechanical and thermal isolation from the rest of the circuit.

PIN CONFIGURATION



NOTES: _____

NOTES: _____

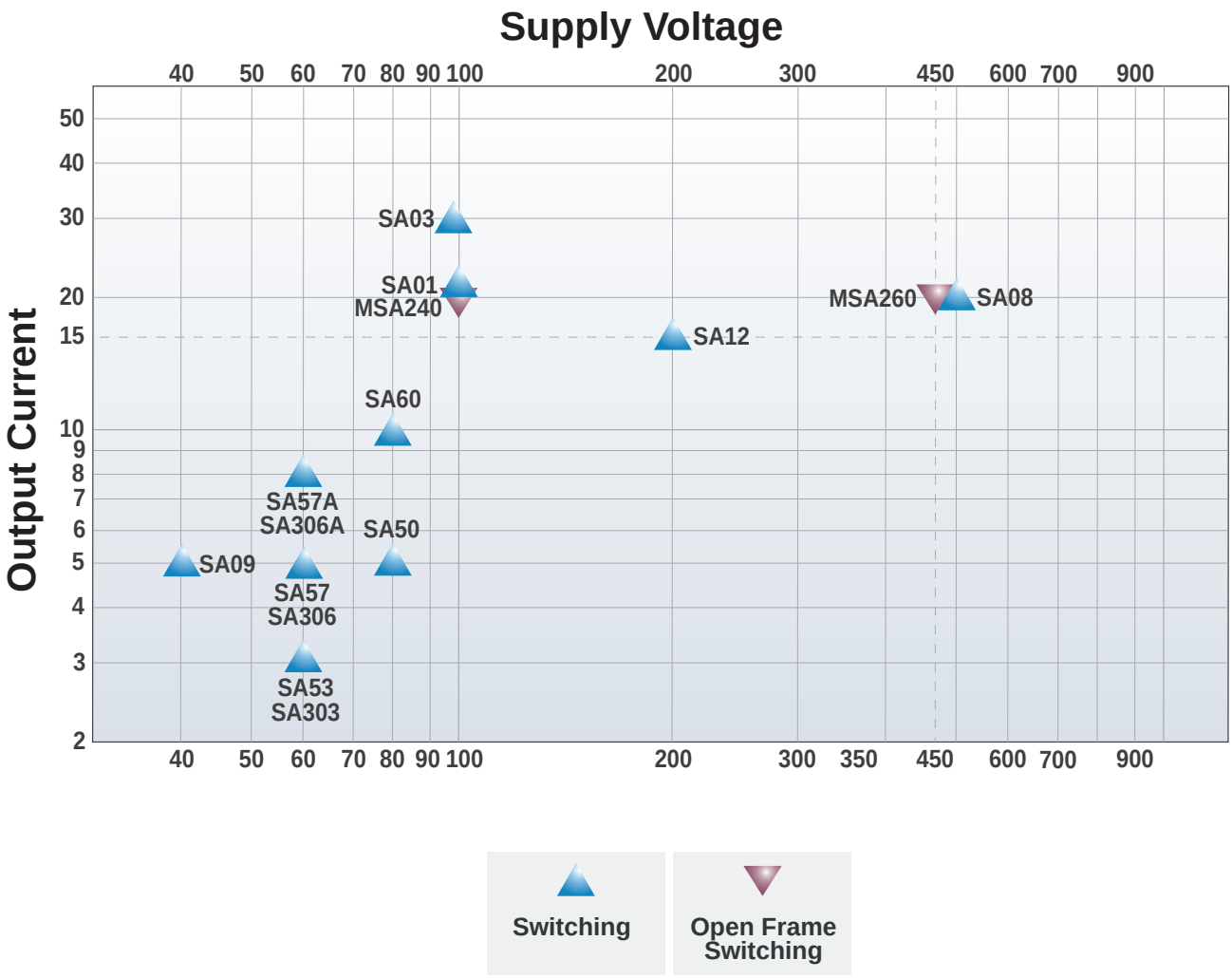


PWM Amplifiers

D

CIRRUS LOGIC®

PRODUCT SELECTOR MATRIX - PWM (SWITCHING)



Pulse Width Modulation Amplifiers

FEATURES

- LOW COST
- HIGH VOLTAGE - 100 VOLTS
- HIGH OUTPUT CURRENT - 20 AMPS
- 2kW OUTPUT CAPABILITY
- VARIABLE SWITCHING FREQUENCY

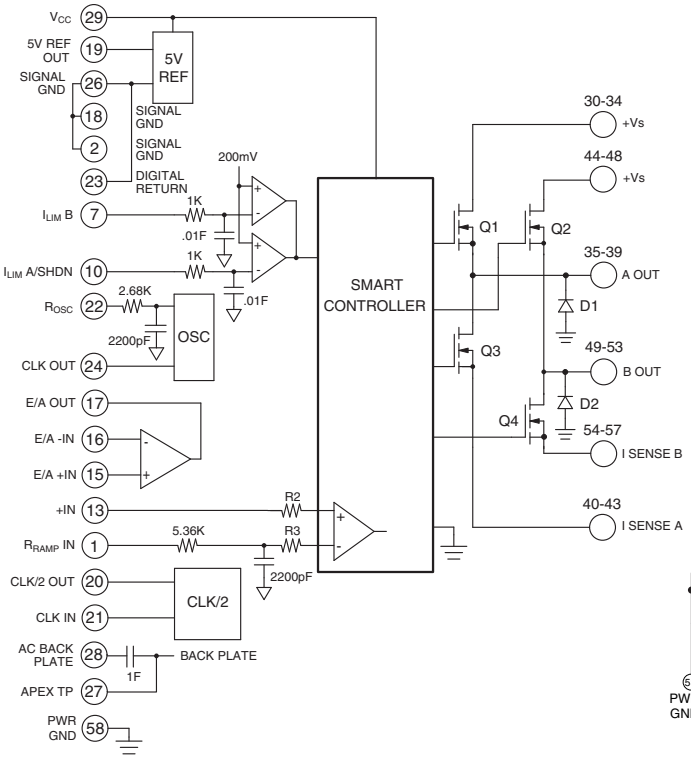
APPLICATIONS

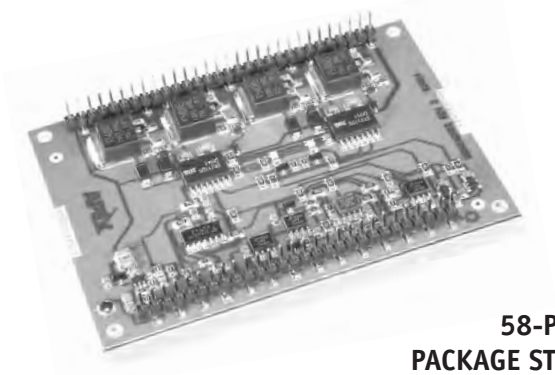
- BRUSH MOTOR CONTROL
- MRI
- MAGNETIC BEARINGS
- CLASS D SWITCHMODE AMPLIFIER

DESCRIPTION

The MSA240 is a surface mount constructed PWM amplifier that provides a cost effective solution in many industrial applications. The MSA240 offers outstanding performance that rivals many much more expensive hybrid components. The MSA240 is a complete PWM amplifier including an oscillator, comparator, error amplifier, current limit comparators, 5V reference, a smart controller and a full bridge output circuit. The switching frequency is user programmable up to 50 kHz. The MSA240 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heatsink.

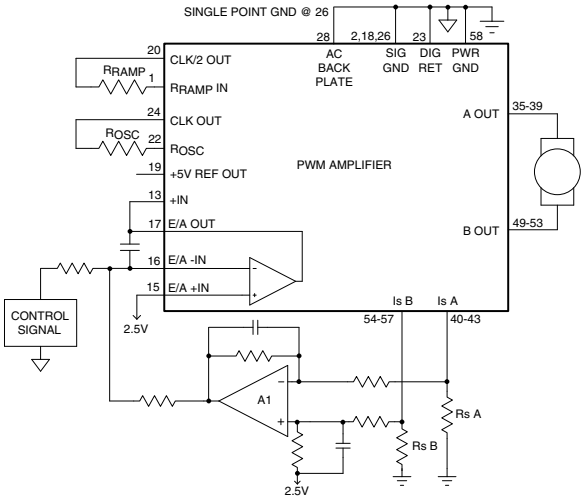
EQUIVALENT CIRCUIT DIAGRAM





58-PIN DIP
PACKAGE STYLE KC

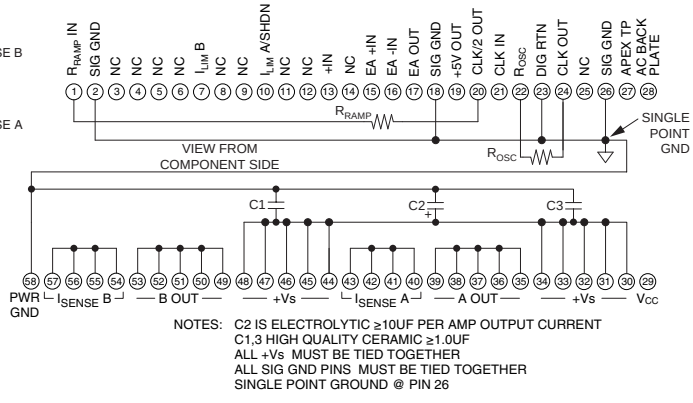
TYPICAL APPLICATION



TORQUE MOTOR CONTROL

With the addition of a few external components the MSA240 becomes a motor torque controller. In the MSA240 the source terminal of each low side MOSFET driver is brought out for current sensing via R_SA and R_SB. A1 is a differential amplifier that amplifies the difference in currents of the two half bridges. This signal is fed into the internal error amplifier that mixes the current signal and the control signal. The result is an input signal to the MSA240 that controls the torque on the motor.

EXTERNAL CONNECTIONS



NOTES: C2 IS ELECTROLYTIC ≥10UF PER AMP OUTPUT CURRENT
C1,3 HIGH QUALITY CERAMIC ≥1.0UF
ALL +Vs MUST BE TIED TOGETHER
ALL SIG GND PINS MUST BE TIED TOGETHER
SINGLE POINT GROUND @ PIN 26

ABSOLUTE MAXIMUM RATINGS

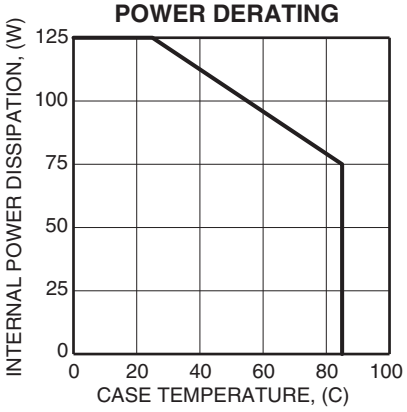
SUPPLY VOLTAGE, VS	100V
SUPPLY VOLTAGE, VCC	16V
OUTPUT CURRENT, peak	30A, within SOA
POWER DISSIPATION, internal, DC	250W[3]
SIGNAL INPUT VOLTAGES	5.4V
TEMPERATURE, pin solder, 10s	225°C.
TEMPERATURE, junction[2]	175°C.
TEMPERATURE RANGE, storage	-40° to 105°C.
OPERATING TEMPERATURE, case	-40° to 85°C.

SPECIFICATIONS

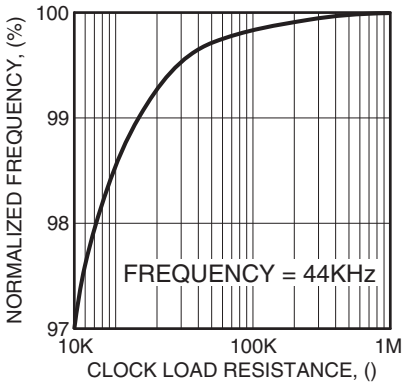
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
OFFSET VOLTAGE	Full temperature range			9	mV
BIAS CURRENT	Full temperature range			500	nA
OFFSET CURRENT	Full temperature range			150	nA
COMMON MODE VOLTAGE RANGE	Full temperature range	0		4	V
SLEW RATE	Full temperature range		1		V/µS
OPEN LOOP GAIN	R_L = 2KΩ		96		dB
UNITY GAIN BANDWIDTH			1		MHz
CLOCK					
LOW LEVEL OUTPUT VOLTAGE	Full temperature range			.2	V
HIGH LEVEL OUTPUT VOLTAGE	Full temperature range	4.8			V
RISE TIME			7		nS
FALL TIME			7		nS
BIAS CURRENT, pin 22	Full temperature range			0.6	µA
5V REFERENCE OUTPUT					
VOLTAGE		4.85		5.15	V
LOAD CURRENT				2	mA
OUTPUT					
TOTAL R_{ON}, both MOSFETs[4]	I_O = 20A , T_J = 85°C			155	mΩ
CURRENT, continuous				20	A
CURRENT, peak	100mS			30	A
OUTPUT MOSFET BODY DIODE					
CONTINUOUS CURRENT				20	A
FORWARD VOLTAGE	I = 16A		1.3		V
REVERSE RECOVERY	I_F = 16A		250		nS
POWER SUPPLY					
VOLTAGE, V_S		3	60	100	V
VOLTAGE, V_{CC}		14	15	16	V
CURRENT, V_S, quiescent	22kHz switching		4	28	mA
CURRENT, V_{CC}, quiescent	22kHz switching			18	mA
CURRENT, V_{CC}, shutdown				10	mA
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range			1.2	°C/W
RESISTANCE, junction to air	Full temperature range			14	°C/W
TEMPERATURE RANGE, case		-40		85	°C/W

NOTES:
1. Unless otherwise noted: T_C=25°C, V_{CC} = 15V, V_S = 60V
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Each of the two output transistors on at any one time can dissipate 125W.
4. Maximum specification guaranteed but not tested.

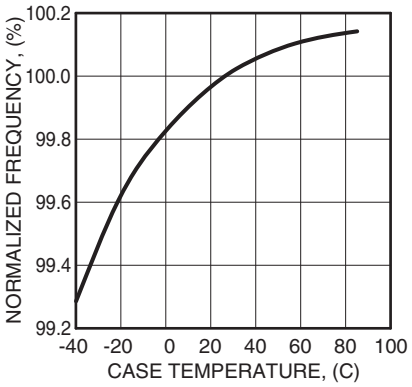
POWER DERATING



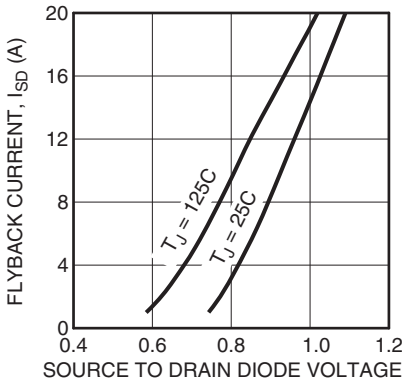
CLOCK LOADING



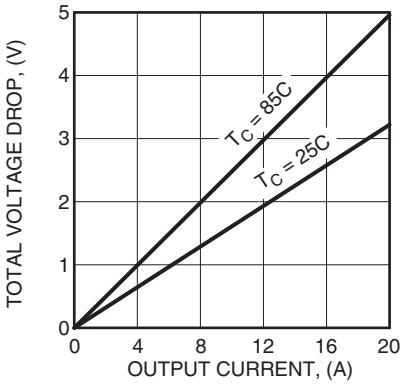
CLOCK FREQUENCY OVER TEMP.



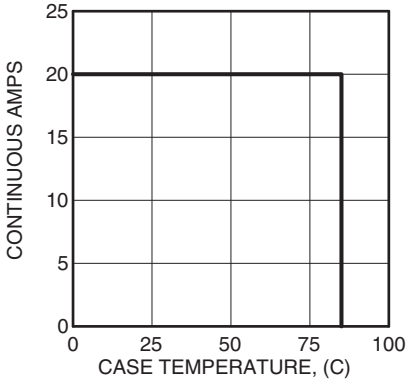
REVERSE DIODE



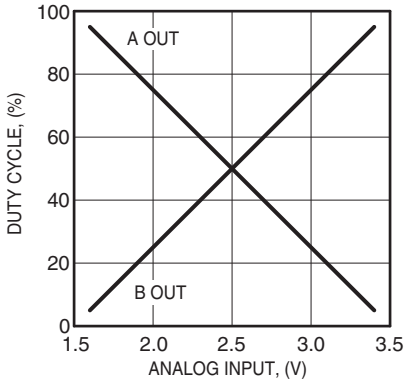
TOTAL VOLTAGE DROP



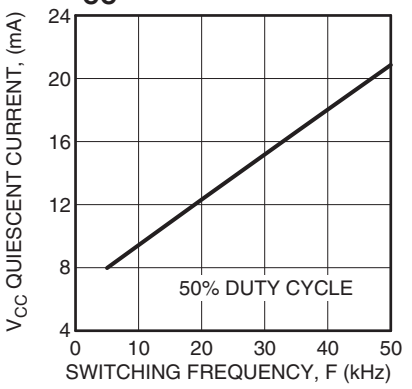
CONTINUOUS OUTPUT



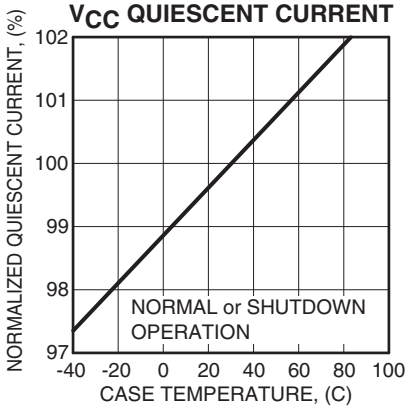
DUTY CYCLE VS. ANALOG INPUT



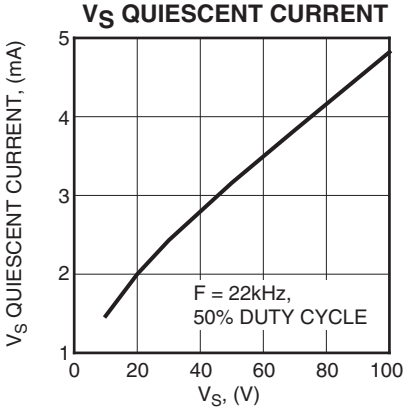
V_{CC} QUIESCENT CURRENT



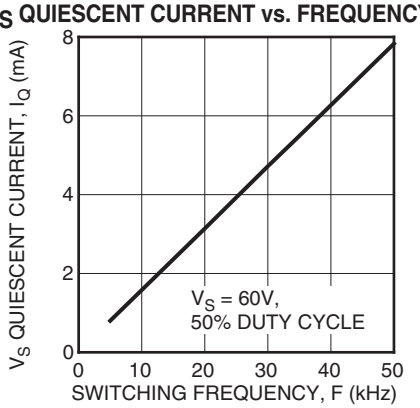
V_{CC} QUIESCENT CURRENT



V_S QUIESCENT CURRENT



V_S QUIESCENT CURRENT vs. FREQUENCY



D

GENERAL

Please read Application Note 30 “PWM Basics”. Refer also to Application Note 1 “General Operating Considerations” for helpful information regarding power supplies, heat sinking, mounting, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power’s complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

OSCILLATOR

The MSA240 includes a user frequency programmable oscillator. The oscillator determines the switching frequency of the amplifier. The switching frequency of the amplifier is 1/2 the oscillator frequency. Two resistor values must be chosen to properly program the switching frequency of the amplifier. One resistor, R_{OSC}, sets the oscillator frequency. The other resistor, R_{RAMP}, sets the internal ramp amplitude. In all cases the ramp voltage will oscillate between 1.5V and 3.5V. See Figure 1. If an external oscillator is applied use the equations to calculate R_{RAMP} .

To program the oscillator, R_{OSC} is given by:

$$R_{OSC} = (1.32X10^8 / F) - 2680$$

where F is the desired **switching frequency** and:

$$R_{RAMP} = 2 \times R_{OSC}$$

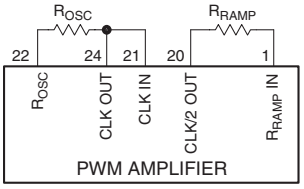
Use 1% resistors with 100ppm drift (RN55C type resistors, for example). Maximum **switching frequency** is 50kHz.

Example:

If the desired switching frequency is 22kHz then R_{OSC} = 3.32K and R_{RAMP} = 6.64K. Choose the closest standard 1% values:

$$R_{OSC} = 3.32K \text{ and } R_{RAMP} = 6.65K.$$

FIGURE 1. EXTERNAL OSCILLATOR CONNECTIONS



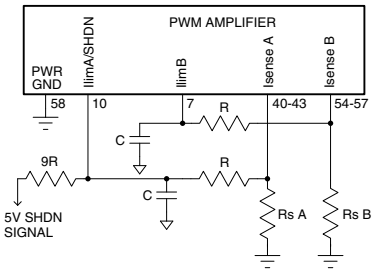
SHUTDOWN

The MSA240 output stage can be turned off with a shutdown command voltage applied to Pin 10 as shown in Figure 2. The shutdown signal is OR’ed with the current limit signal and simply overrides it. As long as the shutdown signal remains high the output will be off.

CURRENT SENSING

The low side drive transistors of the MSA240 are brought out for sensing the current in each half bridge. A resistor from each sense line to PWR GND (pin 58) develops the current sense voltage. Choose R and C such that the time constant is equal to 10 periods of the selected switching frequency. The internal current limit comparators trip at 200mV. Therefore, current limit occurs at $I = 0.2/R_{SENSE}$ for each half bridge. See Figure 2. Accurate milliohm power resistors are required and there are several sources for these listed in the Accessories Vendors section of the Databook.

FIGURE 2. CURRENT LIMIT WITH OPTIONAL SHUTDOWN



POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ must be connected physically close to the pins to prevent local parasitic oscillation and overshoot. All $+V_S$ pins must be connected together. Place an electrolytic capacitor of at least 10µF per output amp required midpoint between these sets of pins. In addition place a ceramic capacitor 1µF or greater directly at each set of pins for high frequency bypassing. V_{CC} is bypassed internally.

GROUNDING AND PCB LAYOUT

Switching amplifiers combine millivolt level analog signals and large amplitude switching voltages and currents with fast rise times. As such grounding is crucial. Use a single point ground at SIG GND (pin 26). Connect signal ground pins 2 and 18 directly to the single point ground on pin 26. Connect the digital return pin 23 directly to pin 26 as well. Connect PWR GND pin 58 also to pin 26. Connect AC BACKPLATE pin 28 also to the single point ground at pin 26. Connect the ground terminal of the V_{CC} supply directly to pin 26 as well. Make sure no current from the load return to PWR GND flows in the analog signal ground. Make sure that the power portion of the PCB layout does not pass over low-level analog signal traces on the opposite side of the PCB. Capacitive coupling through the PCB may inject switching voltages into the analog signal path. Further, make sure that the power side of the PCB layout does not come close to the analog signal side. Fast rising output signal can couple through the trace-to-trace capacitance on the same side of the PCB.

DETERMINING THE OUTPUT STATE

The input signal is applied to +IN (Pin 13) and varies from 1.5 to 3.5 volts, zero to full scale. As +IN varies from 1.5 to 2.5 volts the A output "high" duty cycle (relative to ground) is greater than the B output "high" duty cycle. The reverse occurs as the input signal varies from 2.5 to 3.5 volts. When +IN = 2.5 volts the duty cycles of both A and B outputs are 50%. Consequently, when the input voltage is 1.5V the A output is close to 100% duty cycle and the B output is close to 0% duty cycle. The reverse occurs with an input voltage of 3.5V. The output duty cycle extremes vary somewhat with switching frequency and are internally limited to approximately 5% to 95% at 10kHz and 7% to 93% at 50kHz.

Pulse Width Modulation Amplifier

FEATURES

- LOW COST
- HIGH VOLTAGE - 450 VOLTS
- HIGH OUTPUT CURRENT - 20 AMPS
- 9kW OUTPUT CAPABILITY
- VARIABLE SWITCHING FREQUENCY
- IGBT FULL BRIDGE OUTPUT

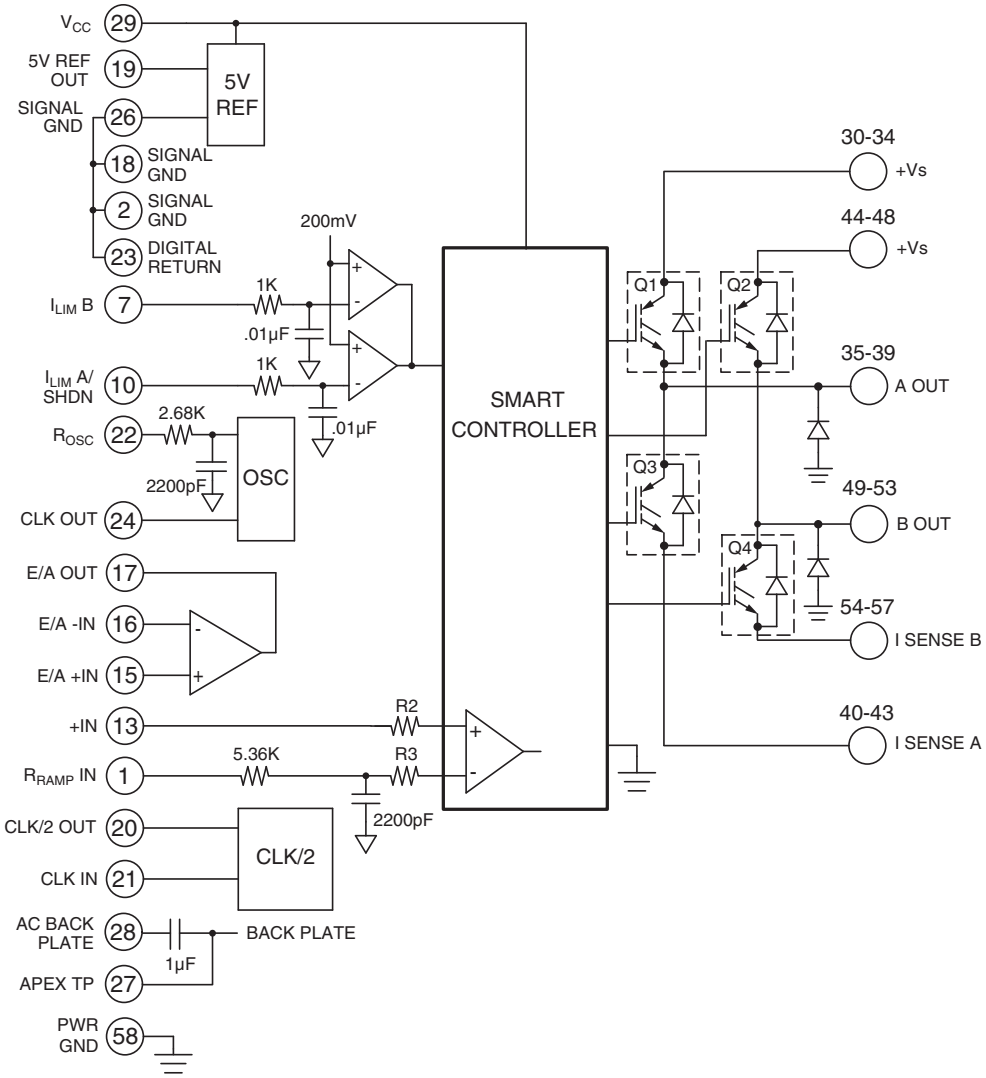
APPLICATIONS

- BRUSH MOTOR CONTROL
- MRI
- MAGNETIC BEARINGS
- CLASS D SWITCHMODE AMPLIFIER

GENERAL DESCRIPTION

The MSA260 is a surface mount constructed PWM amplifier that provides a cost effective solution in many industrial applications. The MSA260 offers outstanding performance that rivals many much more expensive hybrid components. The MSA260 is a complete PWM amplifier including an oscillator, comparator, error amplifier, current limit comparators, 5V reference, a smart controller and a full bridge IGBT output circuit. The switching frequency is user programmable up to 50 kHz. The MSA260 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heatsink.

EQUIVALENT CIRCUIT DIAGRAM



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_S		450	V
SUPPLY VOLTAGE	V_{CC}		16	V
OUTPUT CURRENT, peak, within SOA			30	A
POWER DISSIPATION, internal, DC (Note 3)			250	W
SIGNAL INPUT VOLTAGES			5.4	V
TEMPERATURE, pin solder, 10s			225	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	105	°C
OPERATING TEMPERATURE, case		−40	85	°C

SPECIFICATIONS

Parameter	Test Conditions (Note 1)	Min	Typ	Max	Units
ERROR AMPLIFIER					
OFFSET VOLTAGE	Full temperature range			9	mV
BIAS CURRENT, initial (Note 3)	Full temperature range			500	nA
OFFSET CURRENT, initial	Full temperature range			150	nA
COMMON MODE VOLTAGE RANGE, pos.	Full temperature range	0		4	V
SLEW RATE	Full temperature range		1		V/µs
OPEN LOOP GAIN	R_L = 2KΩ		96		dB
UNITY GAIN BANDWIDTH			1		MHz
CLOCK					
LOW LEVEL OUTPUT VOLTAGE	Full temperature range			0.2	V
HIGH LEVEL OUTPUT VOLTAGE	Full temperature range	4.8			V
RISE TIME			7		nS
FALL TIME			7		nS
BIAS CURRENT, pin 22	Full temperature range			0.6	µA
5V REFERENCE OUTPUT					
VOLTAGE		4.85		5.15	V
LOAD CURRENT				2	mA
OUTPUT (Note 4)					
$V_{CE(ON)}$, each active IGBT	I_{CE} = 15A			2.25	V
CURRENT, continuous	V_S = 400V, F = 22kHz			20	A
CURRENT, peak	1mS, V_S = 400V, F = 22kHz			30	A
FLYBACK DIODE					
CONTINUOUS CURRENT			44	20	A
FORWARD VOLTAGE	I_F = 15A		200	1.5	V
REVERSE RECOVERY	I_F = 15A	0.2	0.7	150	nS

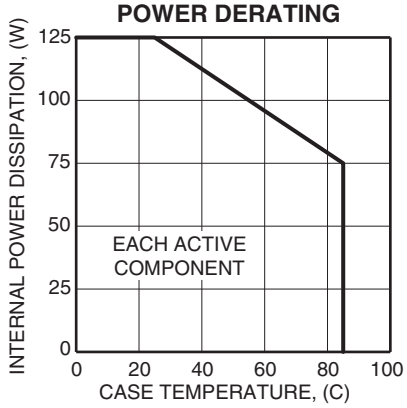
Parameter	Test Conditions (Note 1)	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE, V_S		5	400	450	V
VOLTAGE, V_{CC}		14	15	16	V
CURRENT, V_S, quiescent	22kHz switching		9	28	mA
CURRENT, V_{CC}, quiescent	22kHz switching			18	mA
CURRENT, V_{CC}, shutdown				10	mA
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range			1	°C/W
RESISTANCE, junction to air	Full temperature range			14	°C/W
TEMPERATURE RANGE, case		-40		85	°C

NOTES:

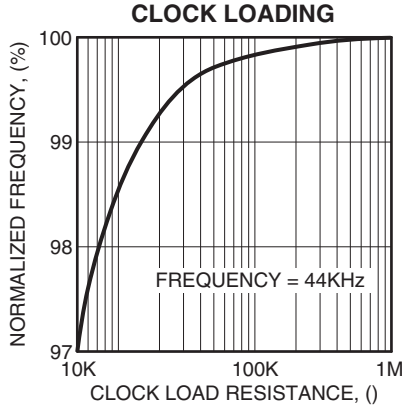
1. Unless otherwise noted: T_C=25°C, V_{CC} = 15V, V_S = 400V, F = 22kHz.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Each of the two output transistors on at any one time can dissipate 125W.
4. Maximum specification guaranteed but not tested.

D

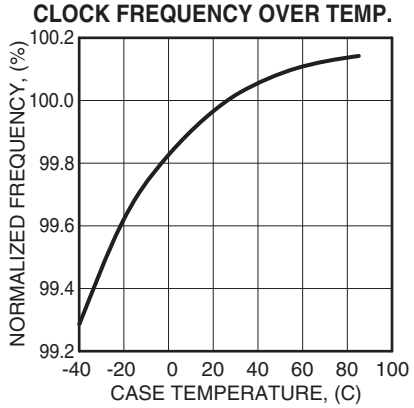
POWER DERATING



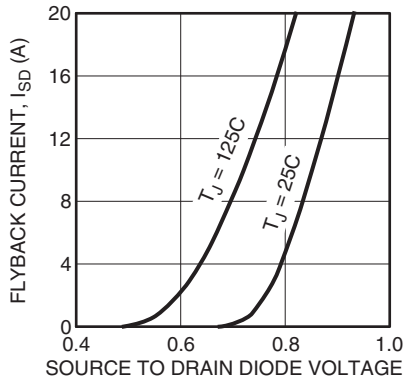
CLOCK LOADING



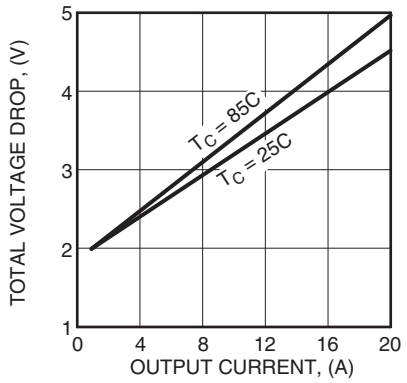
CLOCK FREQUENCY OVER TEMP.

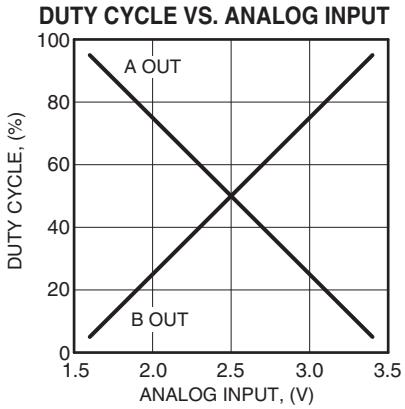


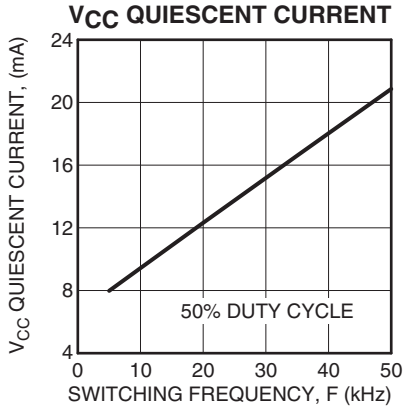
REVERSE DIODE

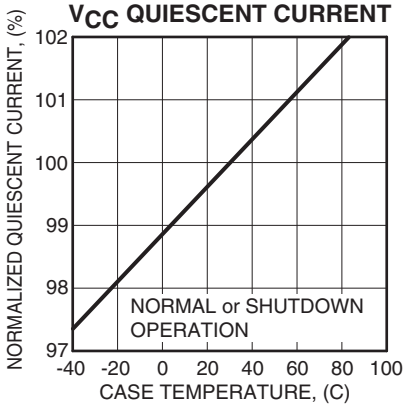


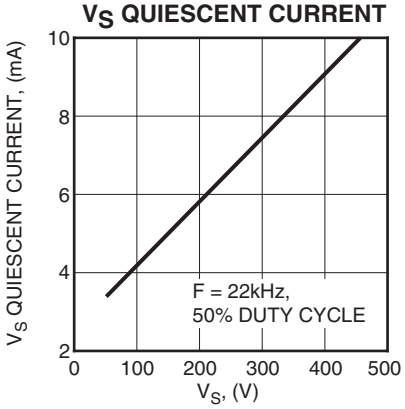
TOTAL VOLTAGE DROP

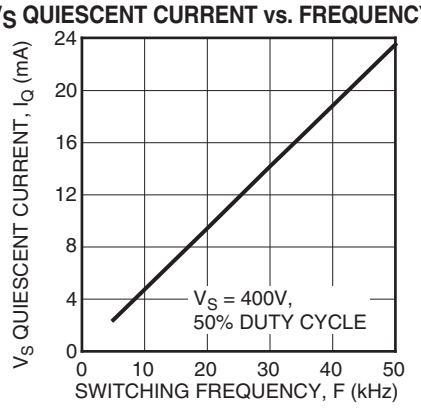




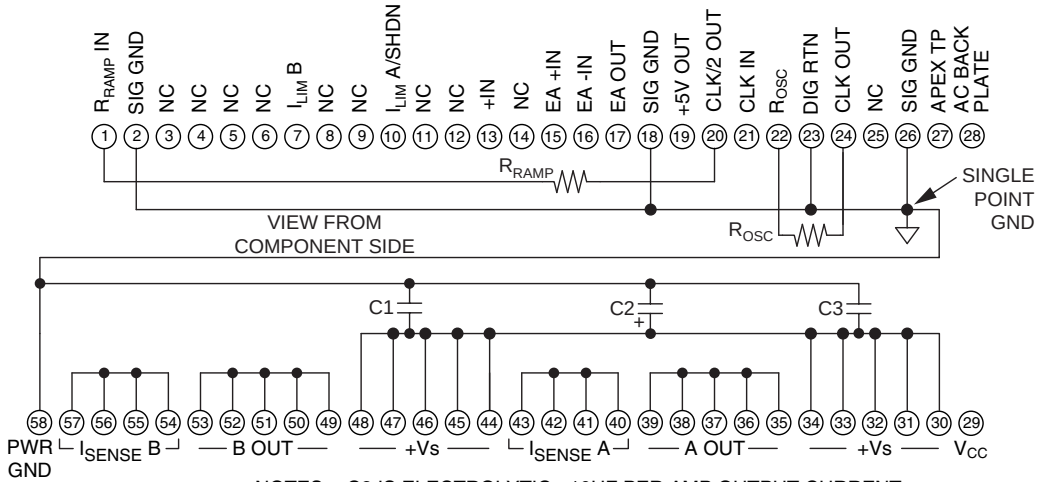




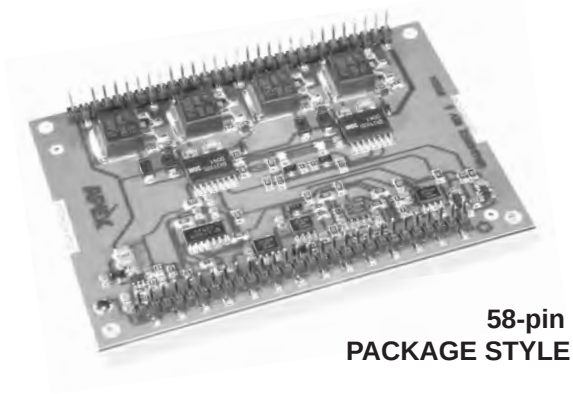




EXTERNAL CONNECTIONS



NOTES: C2 IS ELECTROLYTIC ≥10UF PER AMP OUTPUT CURRENT
C1,3 HIGH QUALITY CERAMIC ≥1.0UF
ALL +Vs MUST BE TIED TOGETHER
ALL SIG GND PINS MUST BE TIED TOGETHER
SINGLE POINT GROUND @ PIN 26

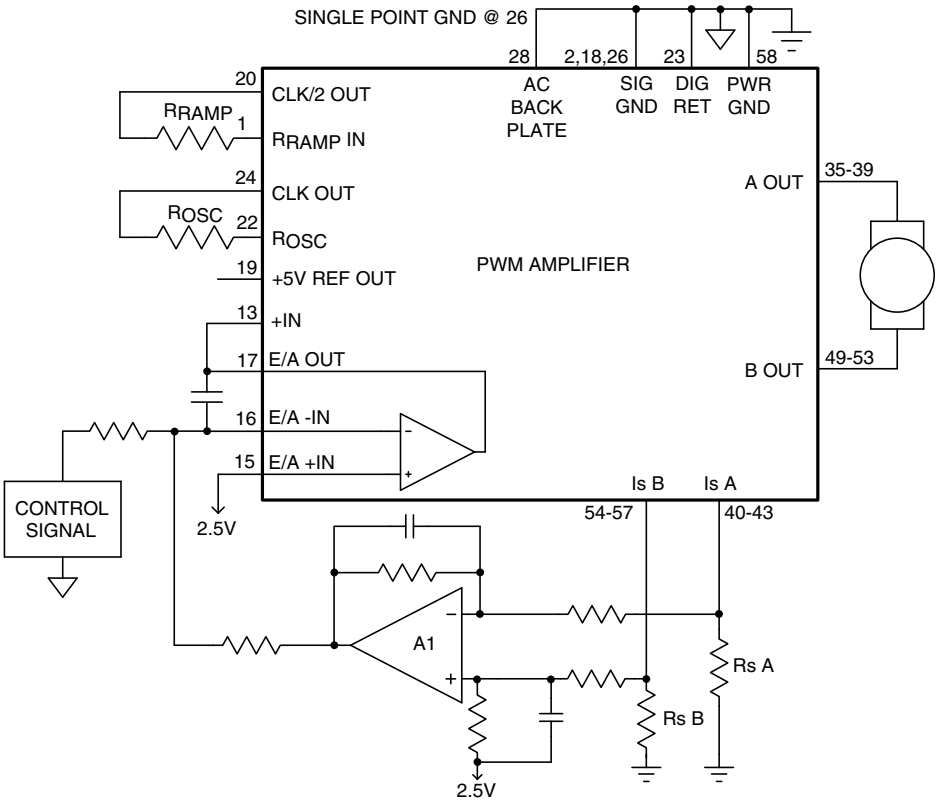


58-pin DIP
PACKAGE STYLE KC

TYPICAL APPLICATION

TORQUE MOTOR CONTROL

With the addition of a few external components the MSA260 becomes a motor torque controller. In the MSA260 the source terminal of each low side IGBT driver is brought out for current sensing via R_SA and R_SB. A1 is a differential amplifier that amplifies the difference in currents of the two half bridges. This signal is fed into the internal error amplifier that mixes the current signal and the control signal. The result is an input signal to the MSA260 that controls the torque on the motor.



GENERAL

Please read Application Note 30 “PWM Basics”. Refer also to Application Note 1 “General Operating Considerations” for helpful information regarding power supplies, heat sinking, mounting, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power’s complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

OSCILLATOR

The MSA260 includes a user frequency programmable oscillator. The oscillator determines the switching frequency of the amplifier. The switching frequency of the amplifier is 1/2 the oscillator frequency. Two resistor values must be chosen to properly program the switching frequency of the amplifier. One resistor, R_{OSC}, sets the oscillator frequency. The other resistor, R_{RAMP}, sets the ramp amplitude. In all cases the ramp voltage will oscillate between 1.5V and 3.5V. See Figure 1. If an external oscillator is applied use the equations to calculate R_{RAMP} .

To program the oscillator, R_{OSC} is given by:

$$R_{OSC} = (1.32X10^8 / F) - 2680$$

where F is the desired **switching frequency** and:

$$R_{RAMP} = 2 X R_{OSC}$$

Use 1% resistors with 100ppm drift (RN55C type resistors, for example). Maximum **switching frequency** is 50kHz.

Example:
If the desired **switching frequency** is 22kHz then R_{OSC} = 3.32K and R_{RAMP} = 6.64K. Choose the closest standard 1% values: R_{OSC} = 3.32K and R_{RAMP} = 6.65K or simply use two of selected R_{OSC} in series for R_{RAMP}.

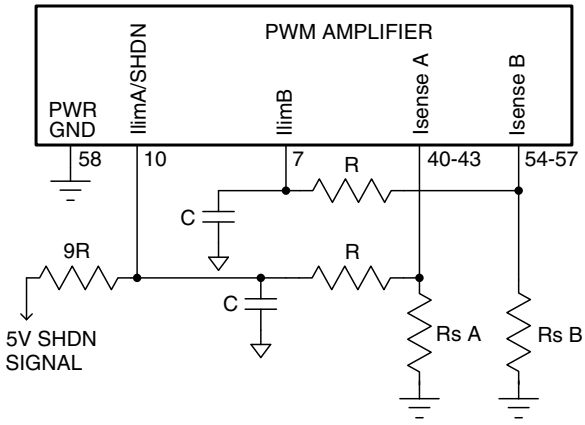


FIGURE 1. EXTERNAL OSCILLATOR CONNECTIONS

SHUTDOWN

The MSA260 output stage can be turned off with a shutdown command voltage applied to Pin 10 as shown in Figure 2. The shutdown signal is OR'ed with the current limit signal and simply overrides it. As long as the shutdown signal remains high the output will be off.

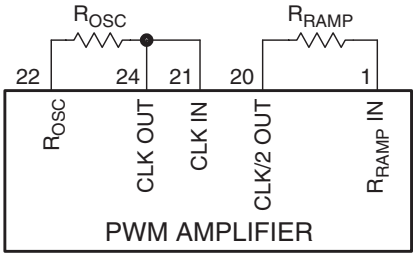


FIGURE 2. CURRENT LIMIT WITH OPTIONAL SHUTDOWN

CURRENT SENSING

The low side drive transistors of the MSA260 are brought out for sensing the current in each half bridge. A resistor from each sense line to PWR GND (pin 58) develops the current sense voltage. Choose R and C such that the time constant is equal to 10 periods of the selected switching frequency. The internal current limit comparators trip at 200mV. Therefore, current limit occurs at $I = 0.2/R_{SENSE}$ for each half bridge. See Figure 2. Accurate milliohm power resistors are required and there are several sources for these listed in the Accessories Vendors section of the Databook.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ must be connected physically close to the pins to prevent local parasitic oscillation and overshoot. All $+V_S$ must be connected together. Place and electrolytic capacitor of at least 10µF per output amp required midpoint between these sets of pins. In addition place a ceramic capacitor 1.0µF or greater directly at **each** set of pins for high frequency bypassing. V_{CC} is bypassed internally.

GROUNDING AND PCB LAYOUT

Switching amplifiers combine millivolt level analog signals and large amplitude switching voltages and currents with fast rise times. As such grounding is crucial. Use a single point ground at SIG GND (pin 26). Connect signal ground pins 2 and 18 directly to the single point ground on pin 26. Connect the digital return pin 23 directly to pin 26 as well. Connect PWR GND pin 58 also to pin 26. Connect AC BACKPLATE pin 28 also to the single point ground at pin 26. Connect the ground terminal of the V_{CC} supply directly to pin 26 as well. Make sure no current from the load return to PWR GND flows in the analog signal ground. Make sure that the power portion of the PCB layout does not pass over low-level analog signal traces on the opposite side of the PCB. Capacitive coupling through the PCB may inject switching voltages into the analog signal path. Further, make sure that the power side of the PCB layout does not come close to the analog signal side. Fast rising output signal can couple through the trace-to-trace capacitance on the same side of the PCB.

DETERMINING THE OUTPUT STATE

The input signal is applied to +IN (Pin 13) and varies from 1.5 to 3.5 volts, zero to full scale. The ramp also varies over the same range. When:

$$\text{Ramp} > +\text{IN } A_{OUT} > B_{OUT}$$

The output duty cycle extremes vary somewhat with switching frequency and are internally limited to approximately 5% to 95% at 10kHz and 7% to 93% at 50kHz.

CALCULATING INTERNAL POWER DISSIPATION

Detailed calculation of internal power dissipation is complex but can be approximated with simple equations. Conduction loss is given by:

$$W = I \cdot 2.5 + I^2 \cdot 0.095$$

where I = output current

Switching loss is given by:

$$W = 0.00046 \cdot I \cdot V_{supply} \cdot F_{switching\ (in\ kHz)}$$

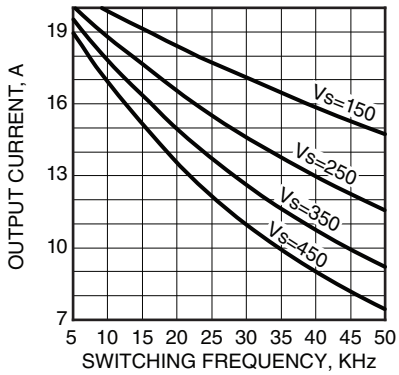
Combine these two losses to obtain total loss. Calculate heatsink ratings and case temperatures as would be done for a linear amplifier. For calculation of junction temperatures, assume half the loss is dissipated in each of two switches:

$$T_j = T_a + W_{total} \cdot R\text{Øhs} + 1/2 W_{total} \cdot R\text{Øjc}, \text{ where:}$$

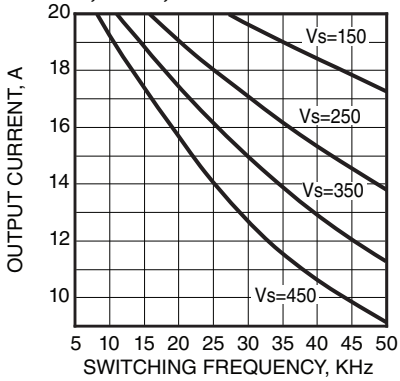
RØhs = heatsink rating
RØjc = junction-to-case thermal resistance of the MSA260.

The SOA typical performance graphs below show performance with the MSA260 mounted with thermal grease on the Apex Precision Power HS26. The Free Air graph assumes vertical orientation of the heatsink and no obstruction to air flow in an ambient temperature of 30°C. The other two graphs show performance with two levels of forced air. Note that air velocity is given in linear feet per minute. As fans are rated in cubic delivery capability, divide the cubic rating by the square area this air flows through to find velocity. As fan delivery varies with static pressure, these calculations are approximations, and heatsink ratings vary with amount of power dissipated, there is no substitute for temperature measurements on the heatsink in the center of the amplifier footprint as a final check.

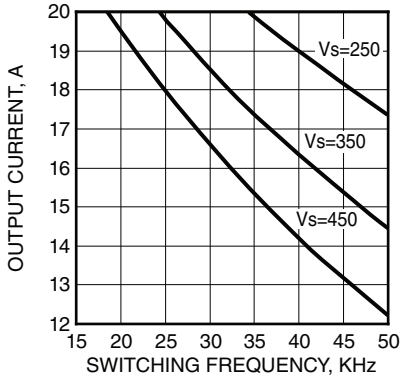
SOA, HS26, FREE AIR



SOA, HS26, 150LFM FORCED AIR



SOA, HS26, 500LFM FORCED AIR



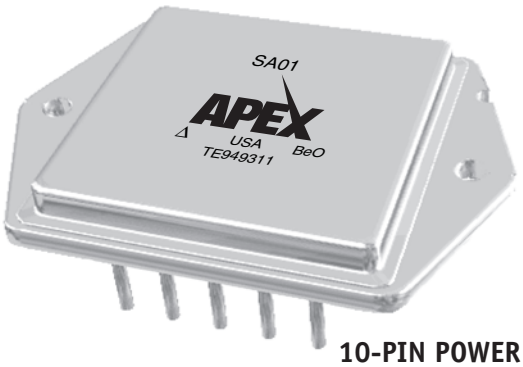
SA01 • SA01-6

Pulse Width Modulation Amplifier

RoHS COMPLIANT

FEATURES

- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE — 16-100V
- 20A CONTINUOUS OUTPUT
- PROGRAMMABLE CURRENT LIMIT
- SHUTDOWN CONTROL
- HERMETIC PACKAGE
- 2 IN² FOOTPRINT



10-PIN POWER DIP
PACKAGE STYLE DE

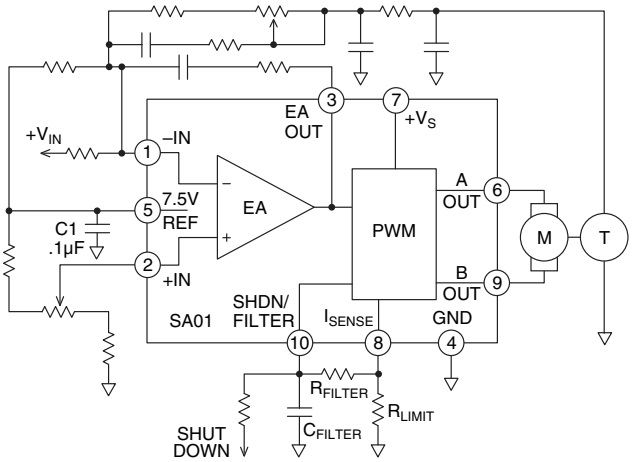
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- PELTIER CONTROL
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

DESCRIPTION

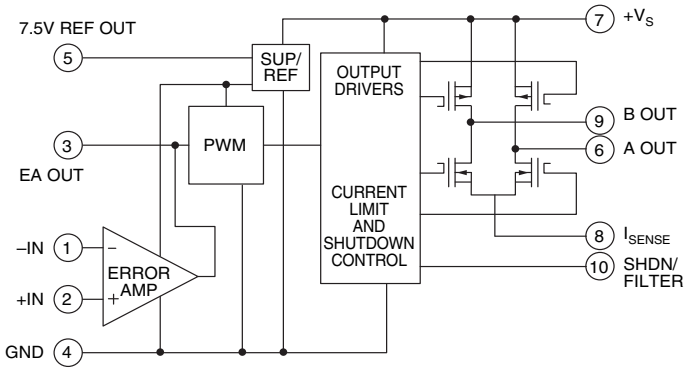
The SA01 amplifier is a pulse width modulation amplifier that can supply 2KW to the load. The full bridge output amplifier can be operated from a single power supply over a wide range of voltages. An error amplifier is included which can provide gain for the velocity control loop in brush type motor control applications. Current limit is programmable by a single resistor. A shutdown input turns off all four drivers of the H bridge output. A precision reference output is provided for use in offsetting the error amplifier. The error amplifier can then be scaled for standard input signals. The amplifier is protected from shorts to supply or ground. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 10-pin hermetic power package occupies only 2 square inches of board space and is isolated.

TYPICAL APPLICATION



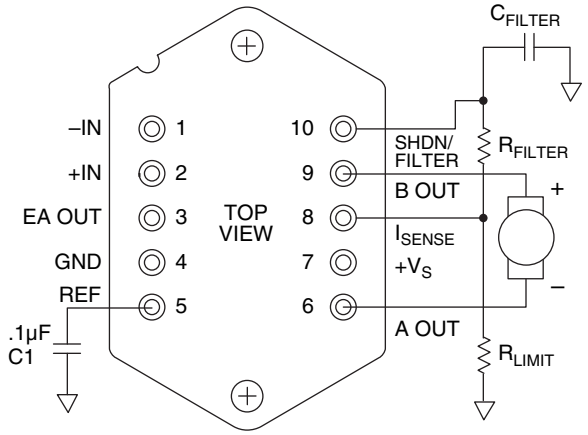
Motor Driver With Tach Feedback

BLOCK DIAGRAM



AS EA OUT (3) GOES MORE POSITIVE, HIGH STATE OF A OUT (6) INCREASES AND HIGH STATE OF B OUT (9) DECREASES.

EXTERNAL CONNECTIONS



$$R_{LIMIT} = \frac{.2}{I_{LIMIT}}$$

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
OUTPUT CURRENT, peak	30A
POWER DISSIPATION, internal	185W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE	10V
REFERENCE LOAD CURRENT	10mA
ERROR AMP INPUT ±	0 to +12V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	SA01 MIN	SA01 TYP	SA01 MAX	SA01-6 MIN	SA01-6 TYP	SA01-6 MAX	UNITS
ERROR AMP								
OFFSET VOLTAGE, initial	T_C = 25°C			10			*	mV
OFFSET VOLTAGE, vs. temperature	Full Temperature Range[5]			50			50	µV/°C
BIAS CURRENT, initial	T_C = 25°C			5			*	µA
BIAS CURRENT, vs. temperature	Full Temperature Range[5]			400			400	nA/°C
OFFSET CURRENT, initial	T_C = 25°C			1			*	µA
OFFSET CURRENT, vs. temperature	Full Temperature Range[5]			80			80	nA/°C
COMMON MODE VOLTAGE RANGE[4]		2		8	*		*	V
COMMON MODE REJECTION, DC[4]		75			*			dB
SLEW RATE			15			*		V/µS
OPEN LOOP GAIN[4]		75			*			dB
GAIN BANDWIDTH PRODUCT			2			*		MHz
OUTPUT								
TOTAL R_{ON}			.25			*		Ω
EFFICIENCY, 10A OUTPUT	V_S = 100V		97			*		%
SWITCHING FREQUENCY	Full temperature range[5]	35.3	42	48.7	35	42	49	KHz
CURRENT, continuous[4]		20			*			A
CURRENT, peak[4]		30			*			A
REFERENCE								
VOLTAGE	I_{REF} = 5mA	7.46	7.50	7.54	*	*	*	V
VOLTAGE VS. TEMP	Full temperature range[5]			50			50	PPM/°C
OUTPUT CURRENT				5			5	mA
LOAD REGULATION[4]			20	50		*	*	PPM/mA
LINE REGULATION			1			*		PPM/V
POWER SUPPLY								
VOLTAGE	Full temperature range[5]	16	50	100	16	50	100	V
CURRENT	I_{OUT} = 0, I_{REF} = 0, Full temperature range[5]		76	90		76	93	mA
CURRENT, shutdown	I_{REF} = 0			25			*	mA
SHUTDOWN								
TRIP POINT		.18		.22	*		*	V
INPUT CURRENT				100			*	nA
THERMAL[2]								
RESISTANCE, junction to case[4]	Full temp range, for each transistor			1.0			*	°C/W
RESISTANCE, junction to air[4]	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications[5]	–25		+85	–55		125	°C

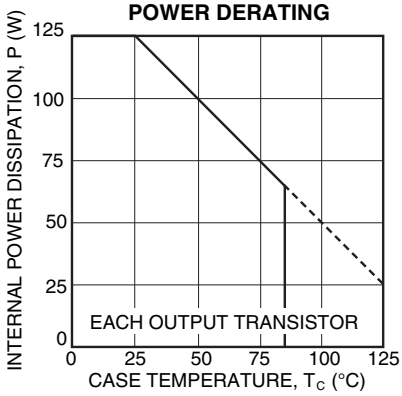
NOTES:
1. Each of the two active output transistors can dissipate 125W, however the N-channel will be about 1/3 of the total dissipated power. Internal connection resistance is .05Ω.
2. Unless otherwise noted: T_C = 25°C.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. Full temperature range specifications apply to the operating case temperature range as specified under THERMAL. For the SA01 these specifications are guaranteed but not tested. For the SA01-6 these specifications are tested over the SA01-6 operating case temperature range.

CAUTION

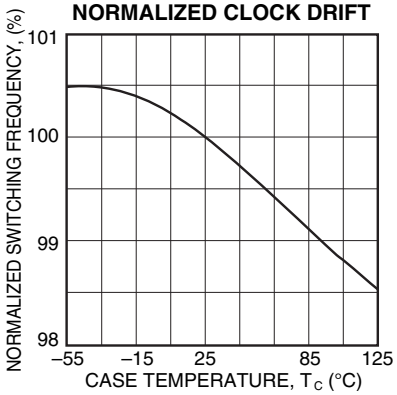
The SA01 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

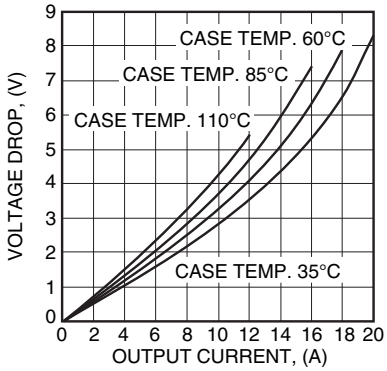
POWER DERATING



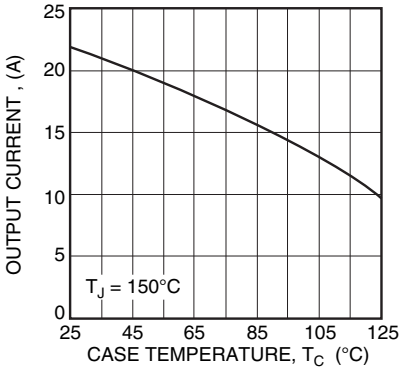
NORMALIZED CLOCK DRIFT



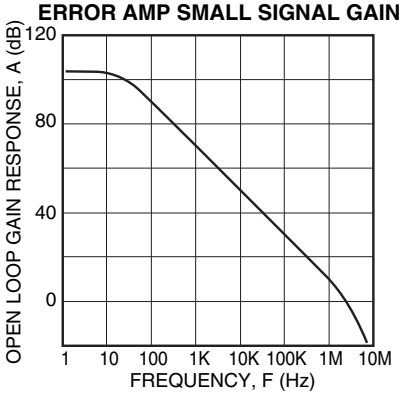
VOLTAGE DROP



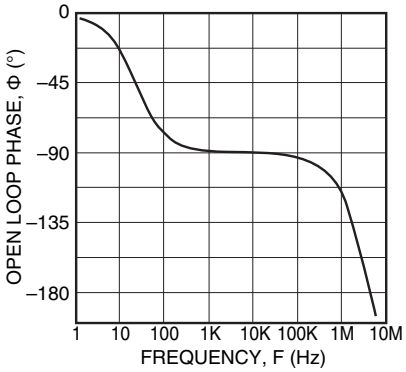
MAXIMUM CONTINUOUS OUTPUT



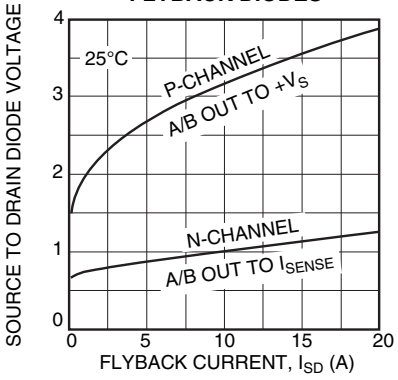
ERROR AMP SMALL SIGNAL GAIN



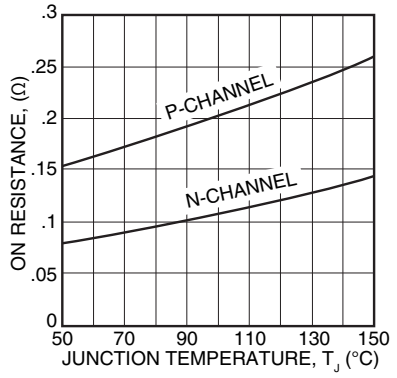
ERROR AMP SMALL SIGNAL PHASE



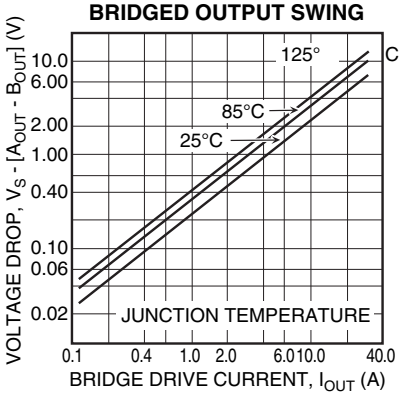
FLYBACK DIODES



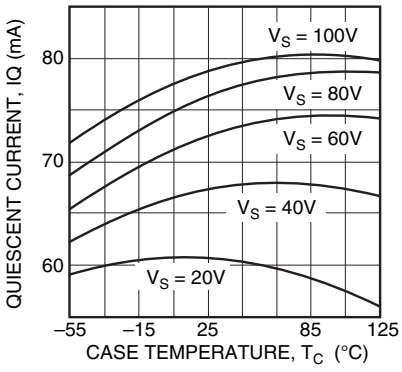
FET ON RESISTANCE



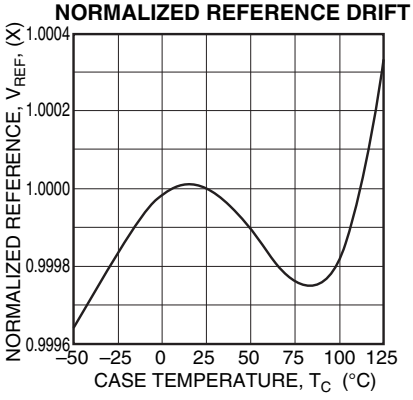
BRIDGED OUTPUT SWING



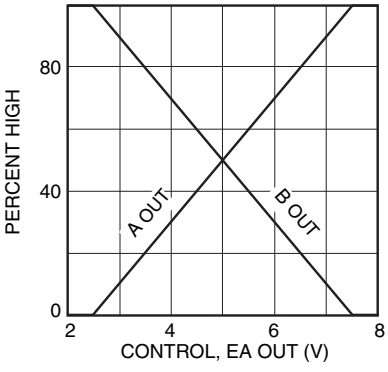
QUIESCENT CURRENT DRIFT



NORMALIZED REFERENCE DRIFT



DUTY CYCLE



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The current limit function sets a peak limit on current flow in pin 8 (Isense). This limits load current and also limits current in the event of a short of either output to +Vs. This circuit can trip anytime during the conduction period and will hold the output transistors off for the remainder of that conduction period.

For proper operation the current limit sense resistor must be connected as shown in the external connection diagram. It is recommended that the resistor be a non-inductive type. Load current flows in pin 8. No current flows in pin 10 (Shutdown/filter) so no error will be introduced by the length of the connection to pin 10. However, the voltage at pin 10 is compared to GND (pin 4) and an error could be introduced if the grounded end of R_{LIMIT} is not directly tied to pin 4. Good circuit board layout practice would be to connect R_{LIMIT} directly between pins 8 and 4.

Switching noise spikes will invariably be found at pin 8. The amplitude and duration will be load dependent. The noise spikes could trip the current limit threshold which is only 200 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 200 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. Suggested starting values are C_{FILTER} = .01µF, R_{FILTER} = 5k.

The required value of R_{LIMIT} may be calculated by:

$$R_{LIMIT} = .2\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined as shown below in Figure 1. R_{LIMIT} will normally be a very low value resistor and can be considered zero for this application. R_{SD} and R_{FILTER} form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit adjust the value of R_{SD} to give 317 mV of shutdown signal at pin 10 when the shutdown signal is high. This means pin 10 will reach the 200 mV trip point in about one time constant with low output current and less time as output current increases. The voltage at pin 10 is referenced to pin 4 (GND). C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

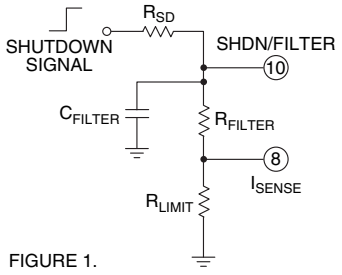


FIGURE 1.

PROTECTION CIRCUITS

There are two conditions which will latch all the output transistors off. The first of these conditions is activation of the high side current limit. Specifically, current in pin 7 ($+V_S$) is monitored. The DC trip level is about 35A and response time about 5us. As actual currents increase the response time decreases. The external fault generally associated with this condition is shorting one of the outputs to ground. However, a load fault can also activate this high side current limit if the current rise time is less than the response time of the filter discussed under "Current Limit". The second of these conditions is activation of any of the four output transistor over-temperature sensors at about 165°C. Ambient temperature, air flow, amplifier mounting problems and all the previously mentioned high current faults contribute to junction temperature. When either of these protection circuits are activated, the root fault must be corrected and power cycled to restore normal operation.

DEAD TIME

There is a dead time between the on and off of each output. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge output during the switching interval. During the dead time all output transistors are off. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

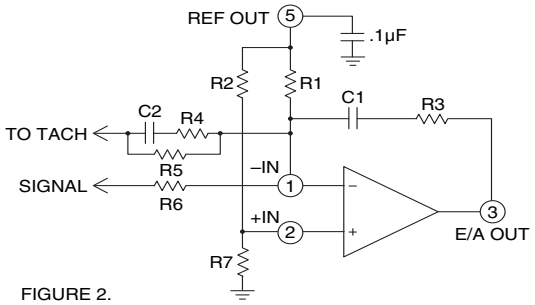


FIGURE 2.

ERROR AMPLIFIER

The internal error amplifier is an operational amplifier. For highest loop accuracy it is best to configure the op amp as an integrator (See Figure 2). Feedback can be adjusted with appropriate poles and zeroes to properly compensate the velocity loop for optimum stability.

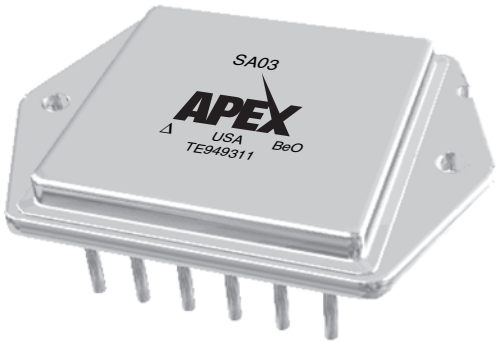
The op amp is operated from a single supply voltage generated internally. The non-inverting input of the op amp does not have a common mode range which includes ground. R2 and R7 are used with the reference voltage provided at pin 5 to bias the non-inverting input to +5 volts, which is approximately half of the voltage supplied internally to the op amp. Similarly, R1 and the parallel combination of R5 R6 are selected to bias the inverting input also at +5 volts. Resistors R1 R2 must be matched. Likewise the parallel combination of R5 R6 must be matched with R7. The source impedances of the tach and the signal source may affect the matching and should be considered in the design.

Pulse Width Modulation Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE—16-100V
- 30A CONTINUOUS TO 60°C case
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL



12-PIN POWER DIP
PACKAGE STYLE CR

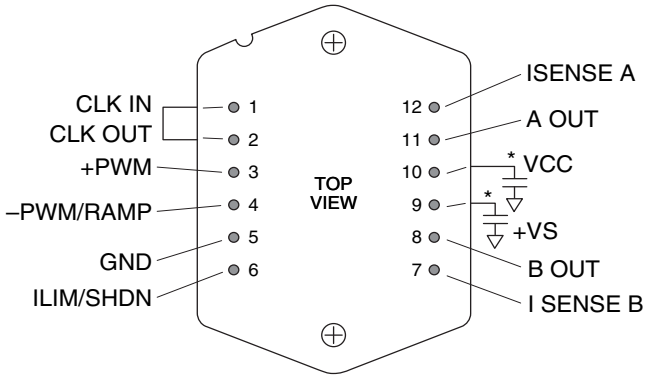
APPLICATIONS

- MOTORS TO 4HP
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA03 is a pulse width amplifier that can supply 3000W to the load. An internal 45kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the basic switching of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS

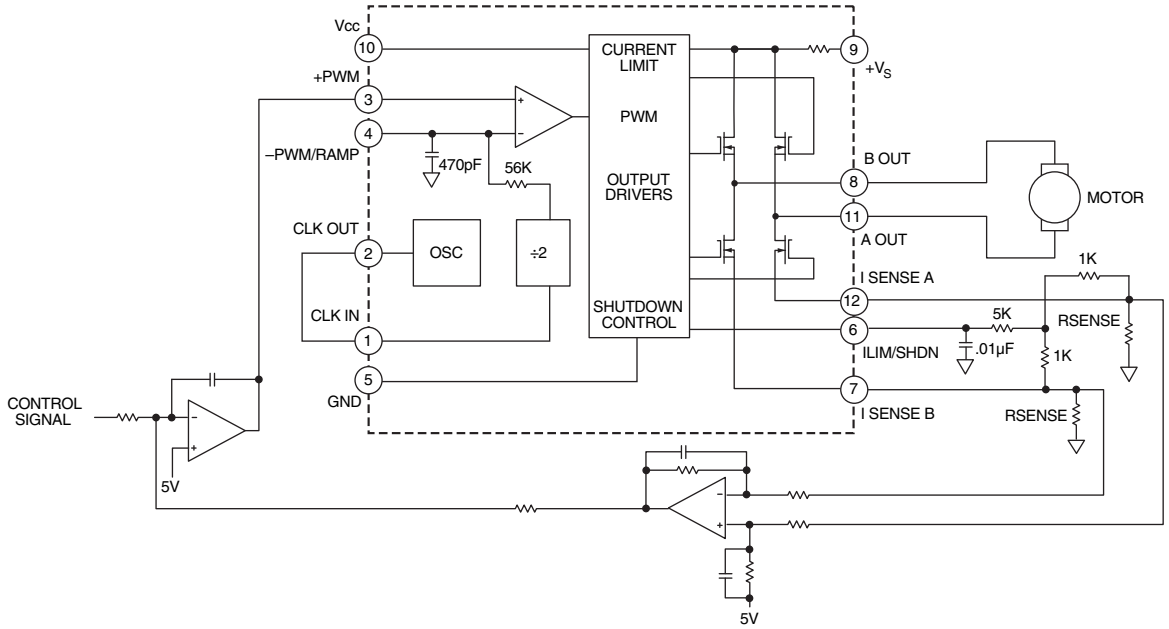


Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT.

* See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	300W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

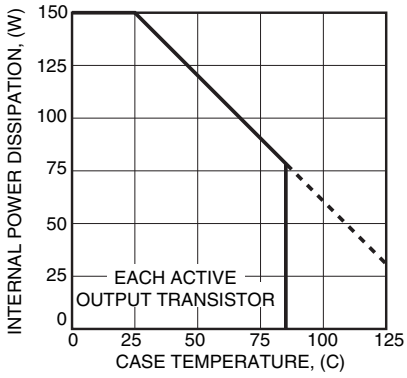
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \le 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \le 1mA$	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}				.16	Ω
EFFICIENCY, 10A output	V_S = 100V		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22	22.5	23	kHz
CURRENT, continuous[4]	60°C case	30			A
CURRENT, peak[4]		40			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	60	100	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 150W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)}$ = 0V.

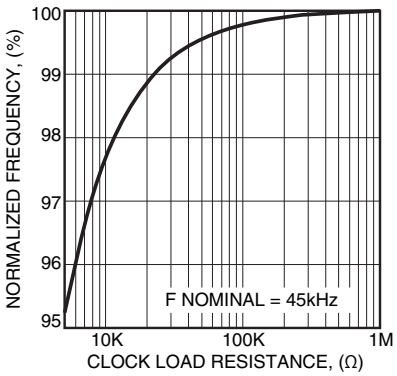
CAUTION The SA03 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

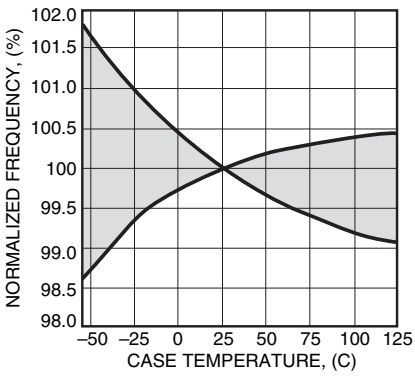
POWER DERATING



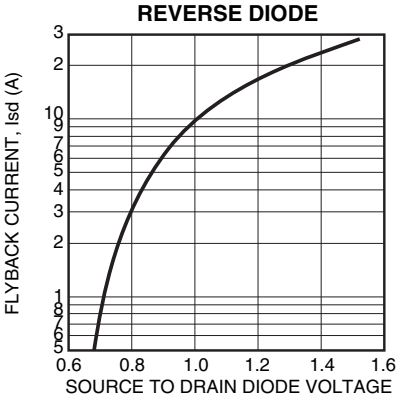
CLOCK LOADING



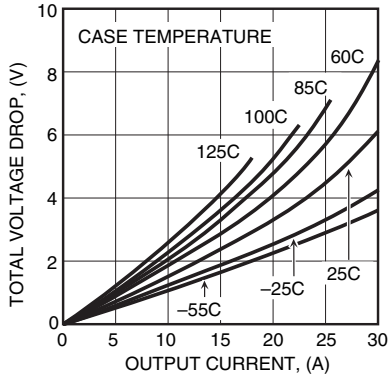
CLOCK FREQUENCY OVER TEMP



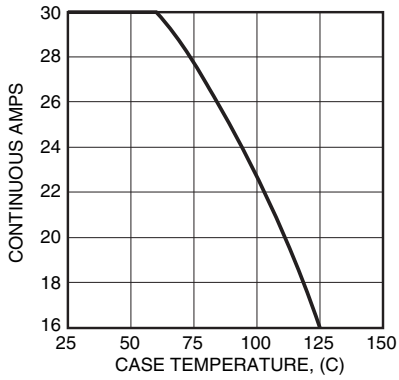
REVERSE DIODE



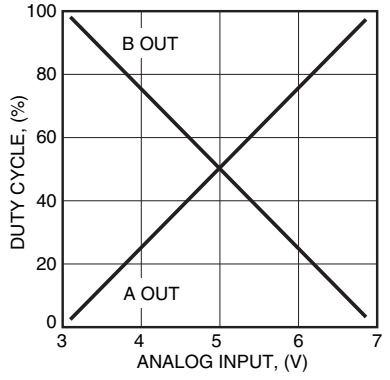
TOTAL VOLTAGE DROP



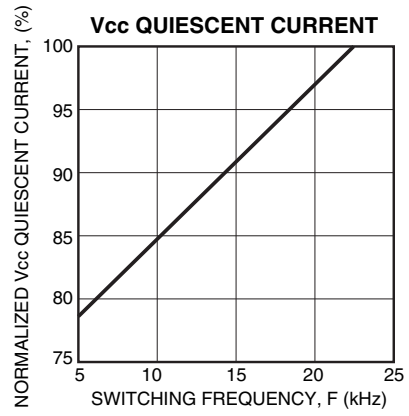
CONTINUOUS OUTPUT



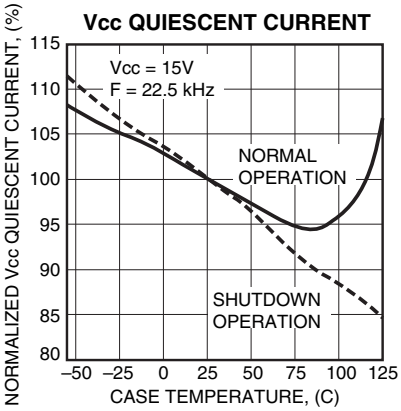
DUTY CYCLE VS ANALOG INPUT



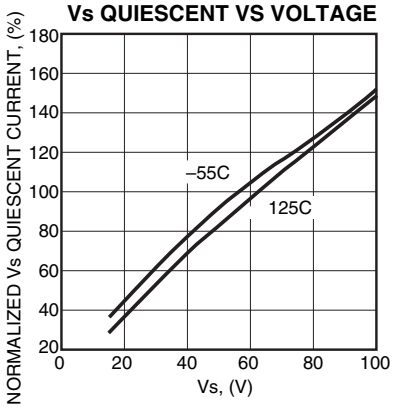
Vcc QUIESCENT CURRENT



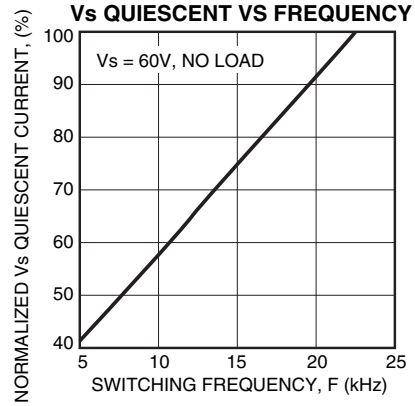
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the high side current. It is nominally set to 140% of the continuous rated output current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. Also, the temperature of the output transistors is continually monitored. Should a fault condition occur which raises the temperature of the output transistors to 165°C the thermal protection circuit will activate and also latch off the output transistors. In either case, it will be necessary to remove the fault condition and recycle power to V_{CC} to restart the circuit.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

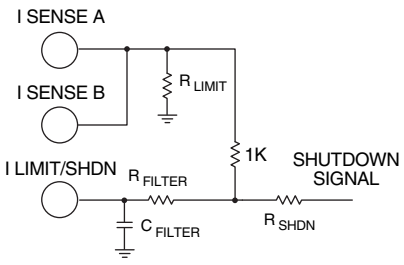


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

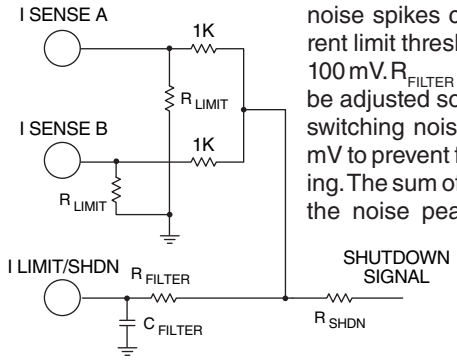


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA03 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

D

Pulse Width Modulation Amplifiers

RoHS COMPLIANT

FEATURES

- IGBT OUTPUTS
- WIDE SUPPLY RANGE—16-450V
- 20A TO 100°C CASE
- 3 PROTECTION CIRCUITS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

12-PIN POWER DIP
PACKAGE STYLE CR

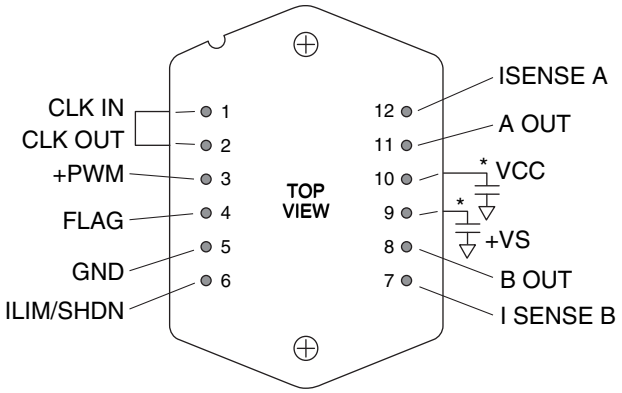
APPLICATIONS

- MOTORS
- REACTIVE LOADS
- MAGNETIC BEARINGS
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA08 is a pulse width modulation amplifier that can supply 9KW to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. The oscillator may also be used to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output IGBTs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS

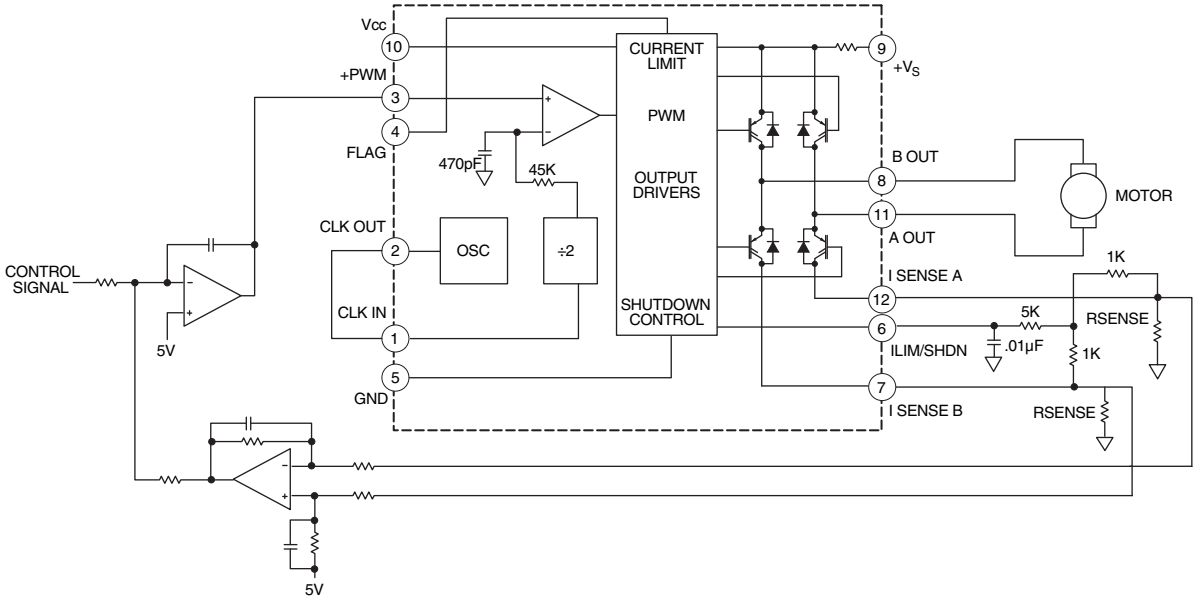


Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

*See text. As +PWM goes more positive, A OUT duty cycle increases.

BLOCK DIAGRAM AND TYPICAL APPLICATION

MOTOR TORQUE CONTROL



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	450V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal[1]	250W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 TO +11V
INPUT VOLTAGE, I_{LIM}	0 TO +10V

SPECIFICATIONS

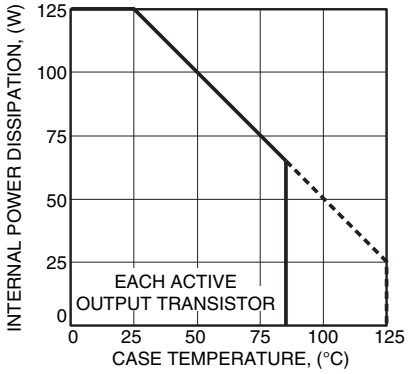
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \le 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \le 1mA$	0		.4	V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
FREQUENCY		44.10	45.00	46.90	kHz
ANALOG INPUT (+PWM)					
center voltage			5		V
P-P voltage	0/100% modulation		4		V
FLAG					
FLAG, high level			10		V
FLAG, low level			0		V
OUTPUT					
TOTAL DROP	I = 20A			5.4	V
EFFICIENCY, 20A output	V_S = 380V		98		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	100°C case	20			A
CURRENT, peak[4]		28			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	450	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)}$ = 0V.

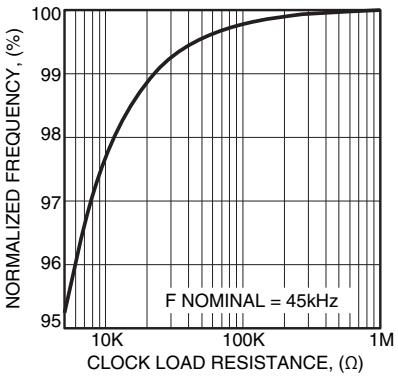
CAUTION The SA08 is constructed from static sensitive components. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

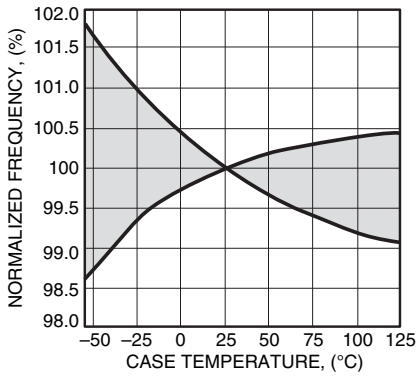
POWER DERATING



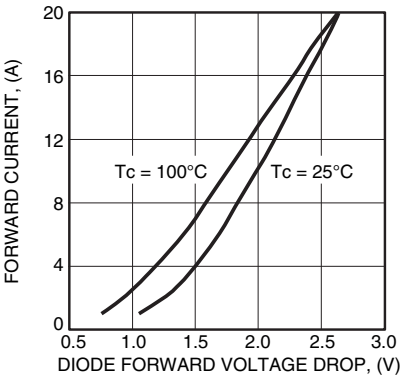
CLOCK LOADING



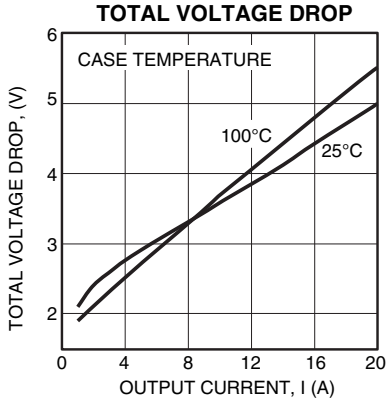
CLOCK FREQUENCY OVER TEMP



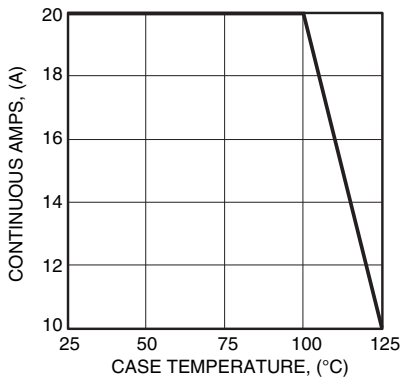
REVERSE DIODE



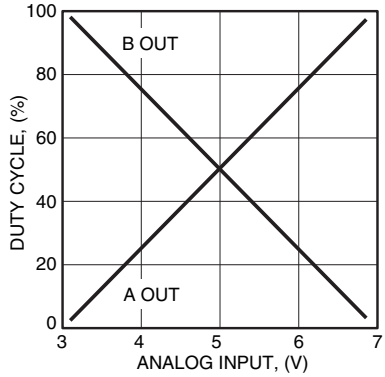
TOTAL VOLTAGE DROP



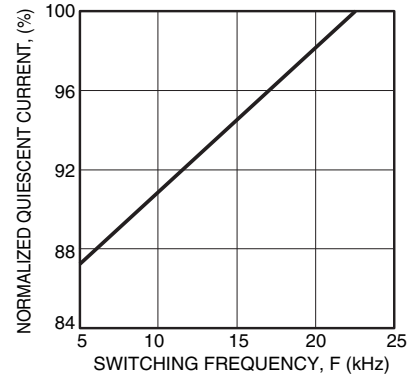
CONTINUOUS AMPS



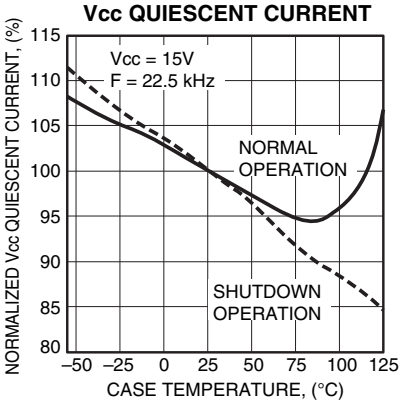
DUTY CYCLE VS ANALOG INPUT



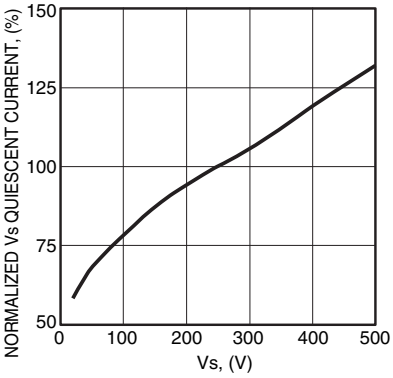
Vcc QUIESCENT CURRENT



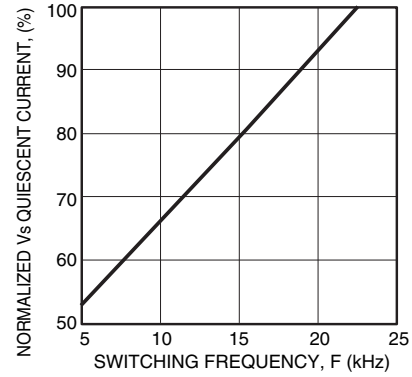
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal. An external clock signal can be applied to the CLK IN pin for synchronization purposes, but must be 45 kHz +/- 2%.

FLAG OUTPUT

Whenever the SA08 has detected a fault condition, the flag output is set high (10V). When the programmable low side current limit is exceeded, the FLAG output will be set high. The FLAG output will be reset low on the next clock cycle. This reflects the pulse-by-pulse current limiting feature. When the internally-set high side current limit is tripped or the thermal limit is reached, the FLAG output is latched high. See PROTECTION CIRCUITS below.

PROTECTION CIRCUITS

A fixed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

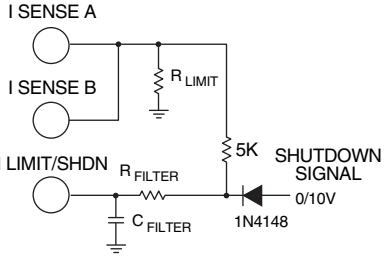


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .1uF, R_{FILTER} = 5k .

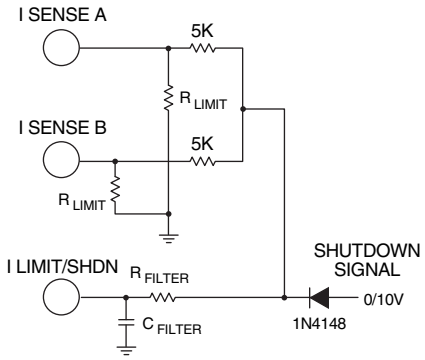


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the IGBT output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA08 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

Pulse Width Modulation Amplifiers

RoHS COMPLIANT

FEATURES

- 500kHz SWITCHING
- FULL BRIDGE OUTPUT 5-40V (80V P-P)
- 5A OUTPUT
- 1 IN^2 FOOTPRINT
- FAULT PROTECTION
- SHUTDOWN CONTROL
- SYNCHRONIZABLE CLOCK
- HERMETIC PACKAGE

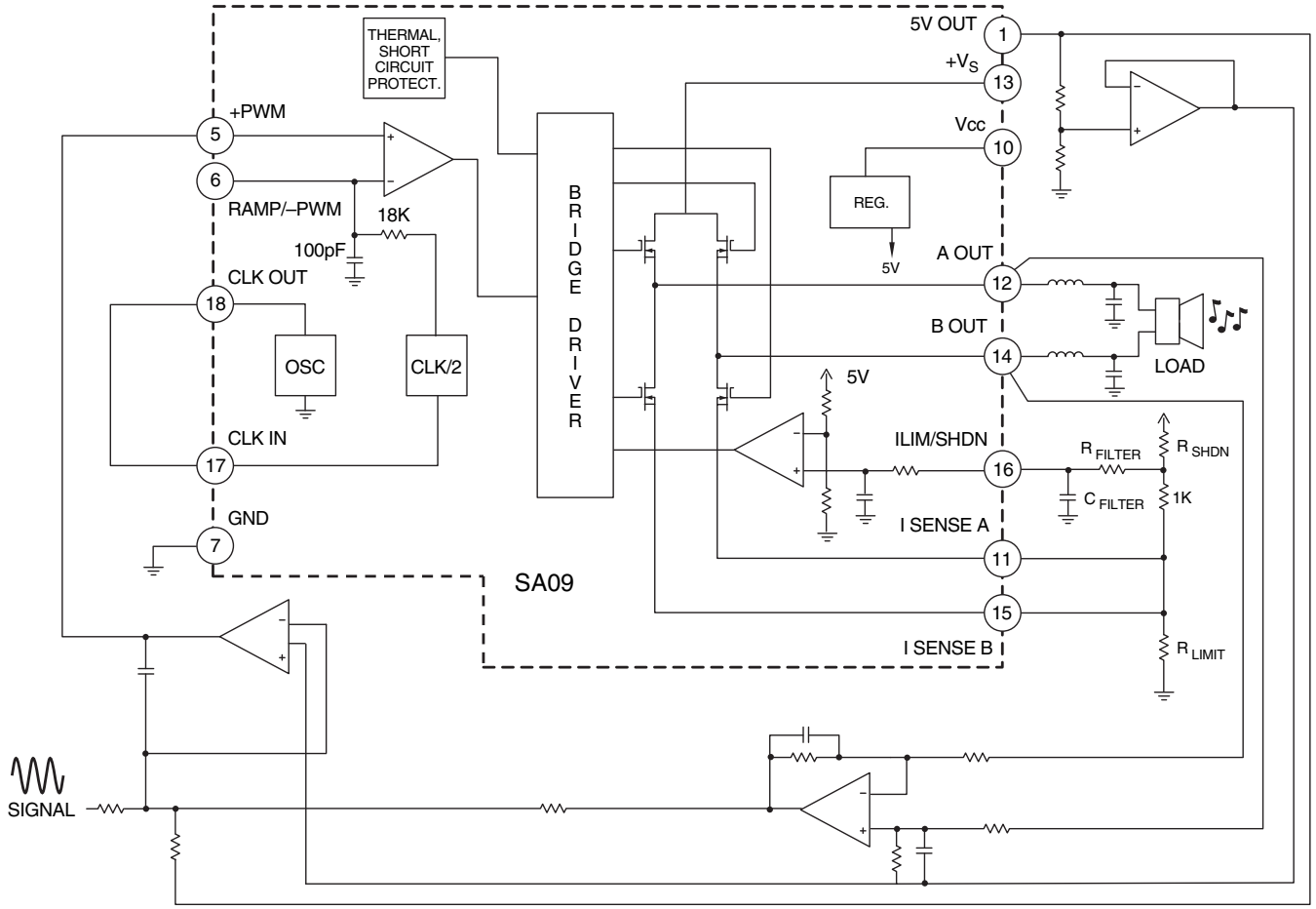
APPLICATIONS

- HIGH FIDELITY AUDIO AMPLIFIER
- BRUSH TYPE MOTOR CONTROL
- VIBRATION CANCELLING AMPLIFIER

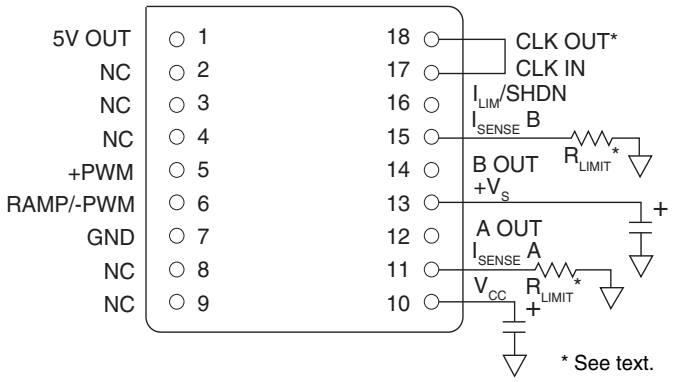
DESCRIPTION

The SA09 amplifier is a 40 volt, 500kHz PWM amplifier. The full bridge output circuit provides 5 amps of continuous drive current for applications as diverse as high fidelity audio and brush type motors. Clock output and input pins can be used for synchronization with other amplifiers or an externally generated clock. Direct access to the pwm input is provided for connection to digital motion control circuits. Protection circuits guard against thermal overloads as well as shorts to supply or ground. The current limit is programmable with one or two external resistors depending on the application. A shutdown input disables all output bridge drivers. The 18 pin steel package is hermetically sealed.

BLOCK DIAGRAM
AND TYPICAL APPLICATION CONNECTIONS HIGH FIDELITY AUDIO



EXTERNAL CONNECTIONS



18-pin DIP
PACKAGE STYLE EL

Case tied to Pin 7. Allow no current in case. Bypassing of supplies is required. If +PWM > RAMP then A OUT > B OUT.

D

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, +Vs to GND, 10mS surge			60	V
SUPPLY VOLTAGE, $+V_{CC}$ to GND			16	V
OUTPUT CURRENT, peak			7.5	A
POWER DISSIPATION, internal (Note 3)			80	W
TEMPERATURE, pin solder, 10s			300	°C
TEMPERATURE, junction (Note 1)			150	°C
TEMPERATURE, storage		−65	150	°C
OPERATING TEMPERATURE RANGE, case		−55	125	°C
INPUTS		−0.4	+5.4	V

CAUTION The SA09 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

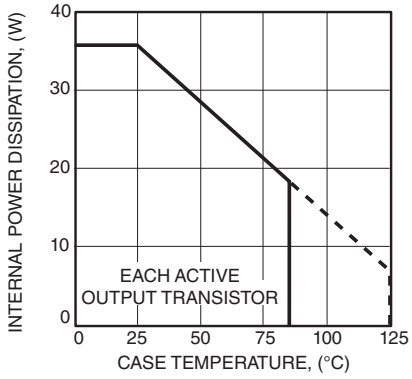
SPECIFICATIONS

Parameter (Note 1)	Test Conditions	Min	Typ	Max	Units
CLOCK OUT		0.98	1	1.02	MHz
CLOCK OUT, high level		4.7		5.3	V
CLOCK OUT, low level		0		0.2	V
5V OUT	LOAD ≤ 5mA	4.988	5	5.012	V
OUTPUT					
EFFICIENCY, 5A output	V_S = 40V		94		%
SWITCHING FREQUENCY			500		kHz
CURRENT, continuous		5			A
CURRENT, peak (Note 4)	100 ms, 10% duty cycle	7			A
$R_{DS(ON)}$ (Note 4)				0.55	Ω
POWER SUPPLY					
VOLTAGE, V_{CC}	Full temperature range	10	12	16	V
VOLTAGE, V_S	Full temperature range	5		40	V
CURRENT, V_{CC}	Switching			50	mA
CURRENT, V_S	Switching, no load			90	mA
INPUTS (Note 4)					
I_{LIM}/SHDN, trip point		90		110	mV
–PWM, +PWM, low level		0		0.8	V
–PWM, +PWM, high level		2.7		V_{CC}	V
CLOCK IN, low level		0		0.3	V
CLOCK IN, high level		3		5.6	V
THERMAL (Note 2)					
RESISTANCE, junction to case	Full temperature range			3.5	°C/W
RESISTANCE, junction to air	Full temperature range		15		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		85	°C

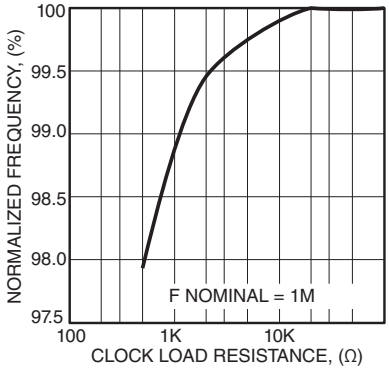
NOTES:

1. All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink datasheet.
3. 40W in each of the two active output transistors on at any one time.
4. Min max values guaranteed but not tested.

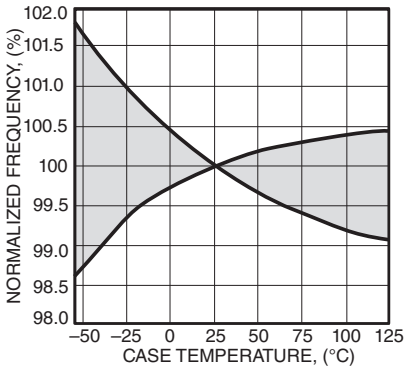
POWER DERATING



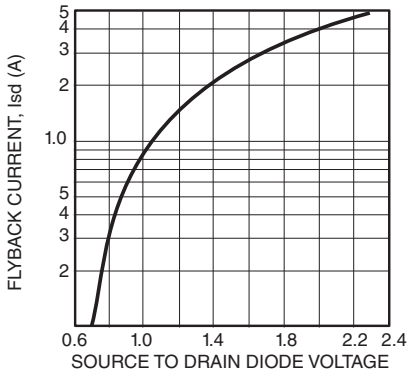
CLOCK LOADING



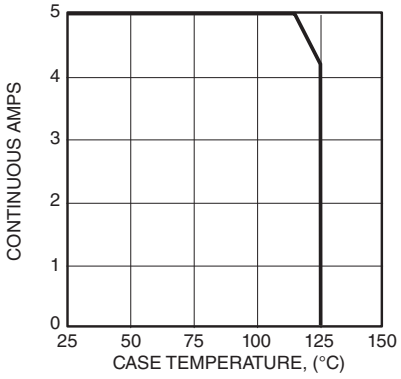
CLOCK FREQUENCY OVER TEMP



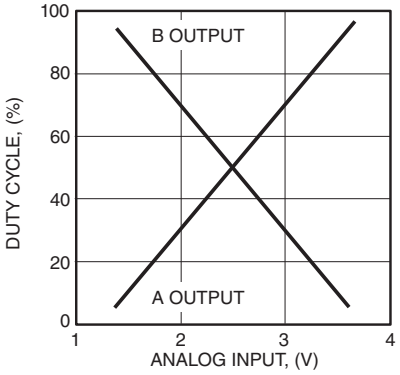
REVERSE DIODE



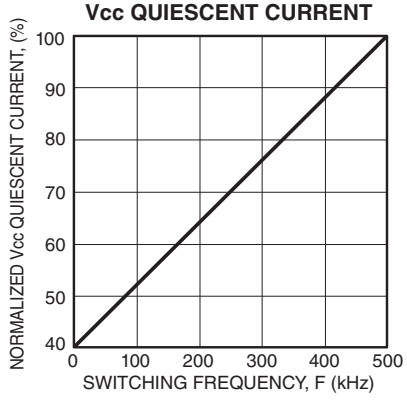
CONTINUOUS OUTPUT



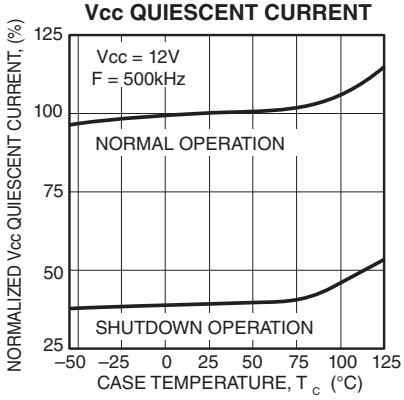
DUTY CYCLE VS ANALOG INPUT



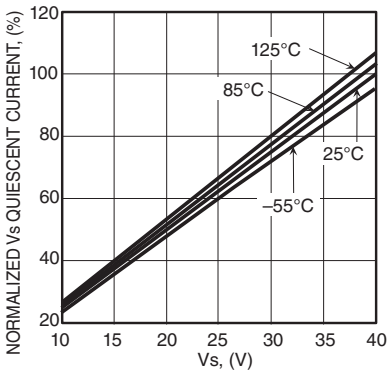
Vcc QUIESCENT CURRENT



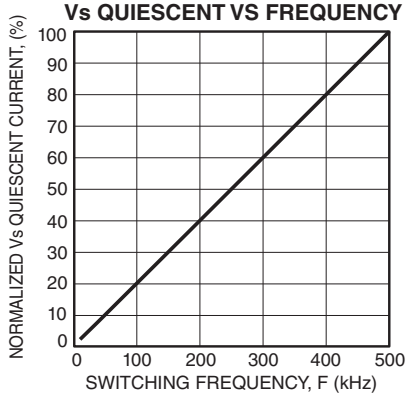
Vcc QUIESCENT CURRENT



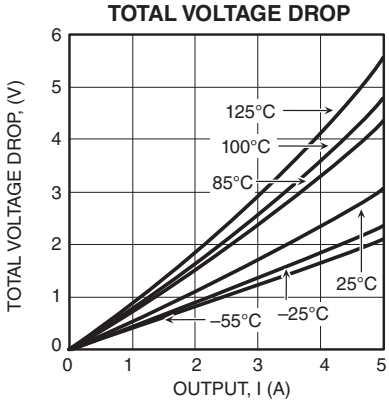
Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



TOTAL VOLTAGE DROP



D

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 1MHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 1MHz is chosen an external capacitor must be tied to the RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 2.5 volts p-p with the lower peak 1.25 volts above ground.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the V_{CC} supply are less stringent, but still necessary. A 0.1µF to 0.47µF ceramic capacitor connected directly to the V_{CC} pin will suffice.

NOISE FILTERING

Switching noise can enter the SA09 through the external error amp to +PWM connection. A wise precaution is to low pass filter this connection. Adjust the pass band of the filter to 10 times the bandwidth required by the application. Keep the resistor value to 100 ohms or less since this resistor becomes part of the hysteresis circuit on the pwm comparator.

PCB LAYOUT

The designer needs to appreciate that the SA09 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA09:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Make all ground connections with a star pattern at pin 7.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 11-16).
5. Do not allow high currents to flow into the ground plane.
6. Separate switching and analog grounds and connect the two only at pin 7 as part of the star pattern.

INTEGRATOR

The integrator provides the inverted signal for negative feedback and also the open loop gain for the overall application circuit accuracy. Recommended value of C_{INT} is 10 pF for stability. However, poles and zeroes can be added to the circuit for overall loop stability as required.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin. Do not connect R_{LIMIT} sense resistors to the ground plane.

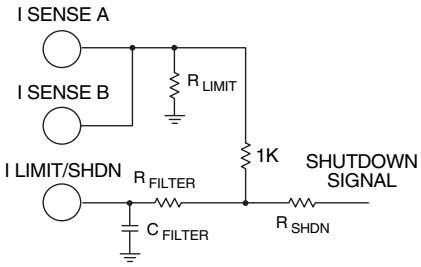


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

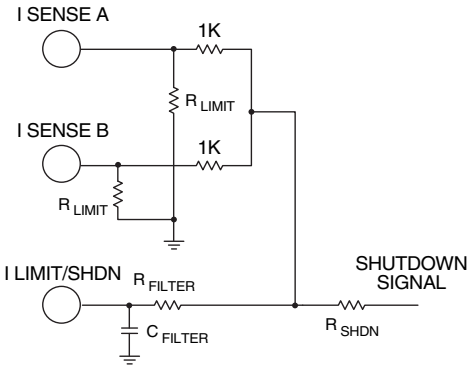


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = 0.001uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by: $R_{LIMIT} = 0.1\ V / I_{LIMIT}$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined in voltage and current modes as shown below in Figures A and B. The R_{LIMIT} resistors will normally be very low values and can be considered zero for this application. In Figure A, R_{SHDN} and 1K form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit, adjust the value of R_{SHDN} to give a minimum 110 mV of shutdown signal at the I LIMIT/SHDN pin when the shutdown signal is high. Note that C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

PROTECTION CIRCUITS

Circuits monitor the temperature and load on each of the bridge output transistors. On each cycle should any fault condition be detected all output transistors in the bridge are shut off. Faults protected against are: shorts across the outputs, shorts to ground, and over temperature conditions. Should any of these faults be detected, the output transistors will be latched off *. In addition there is a built in dead time during which all the output transistors are off. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge during the switching interval. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

* To restart the SA09 remove the fault and recycle V_{CC} or, alternatively, toggle the I LIMIT/SHDN (pin16) with a shut down pulse.

Pulse Width Modulation Amplifiers

RoHS COMPLIANT

FEATURE

- HIGH FREQUENCY SWITCHING — 200 kHz
- WIDE SUPPLY RANGE—16-200V
- 15A CONTINUOUS TO 65°C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

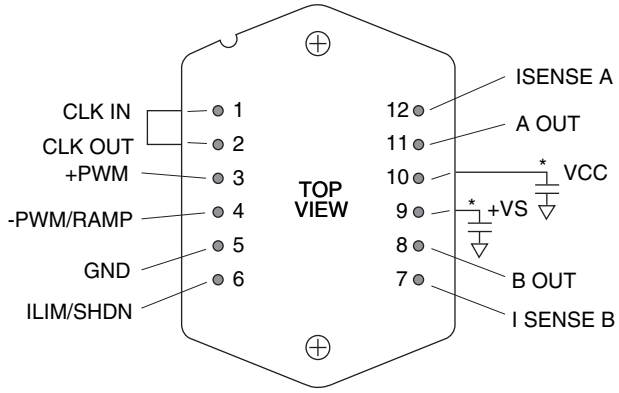
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA12 is a pulse width modulation amplifier that can supply 3000W to the load. An internal 400kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the 200 kHz switching frequency. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the H-bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

12-PIN POWER DIP
PACKAGE STYLE CR

EXTERNAL CONNECTIONS

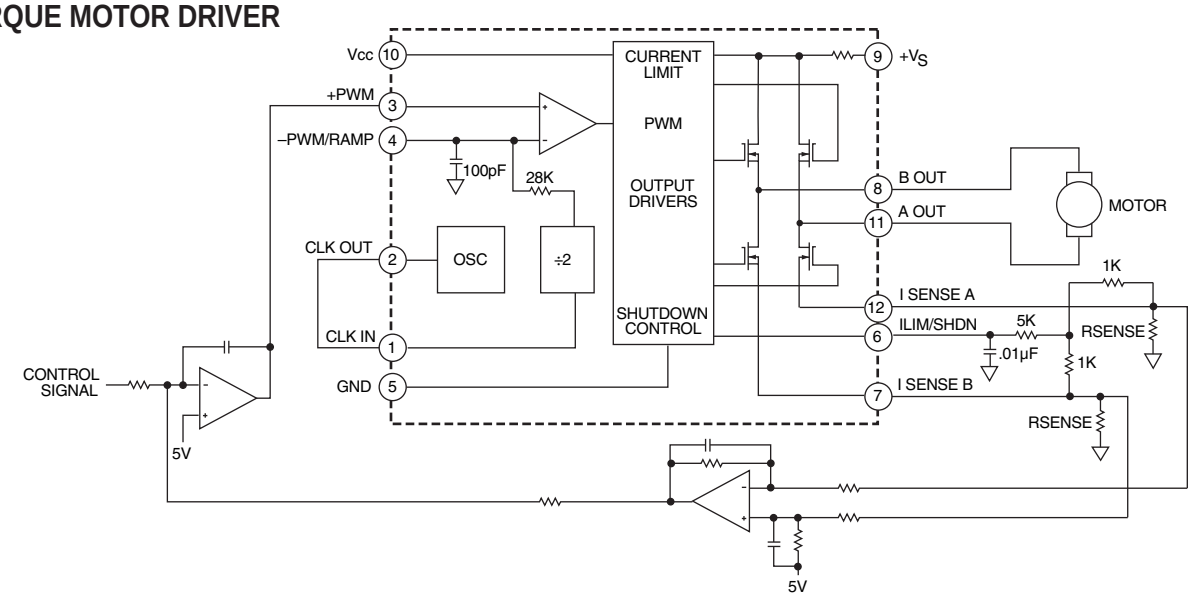


Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

*See text. As +PWM goes more positive, A OUT duty cycle increases.

BLOCK DIAGRAM AND TYPICAL APPLICATION

TORQUE MOTOR DRIVER



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	200V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	250W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

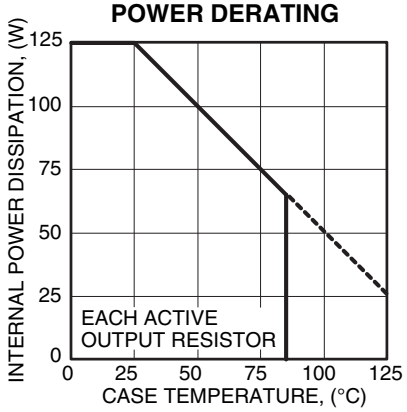
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		392	400	408	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}[4]				.4	Ω
EFFICIENCY, 10A output	V_S = 200V		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	196	200	204	kHz
CURRENT, continuous[4]	65°C case	15			A
CURRENT, peak[4]		20			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16	120	200	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			125	mA
CURRENT, V_{CC}, shutdown				80	mA
CURRENT, V_S	No Load			200	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

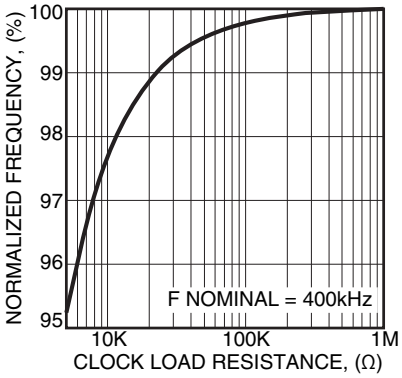
CAUTION The SA12 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

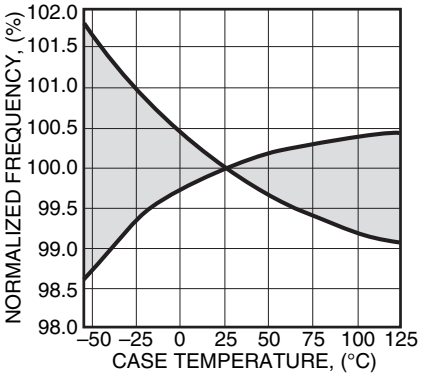
POWER DERATING



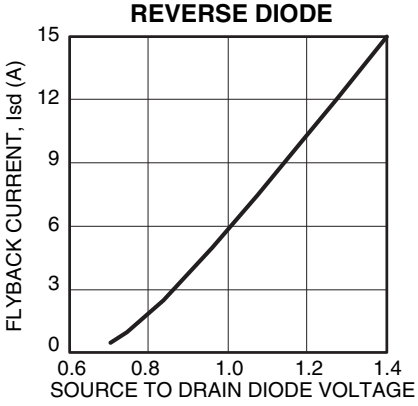
CLOCK LOADING



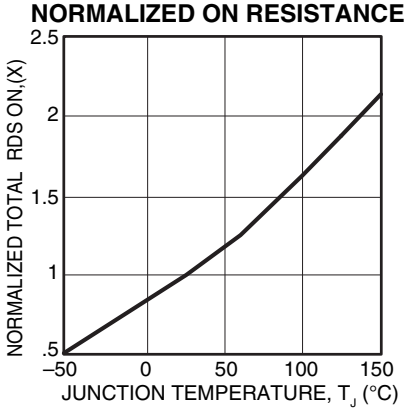
CLOCK FREQUENCY OVER TEMP



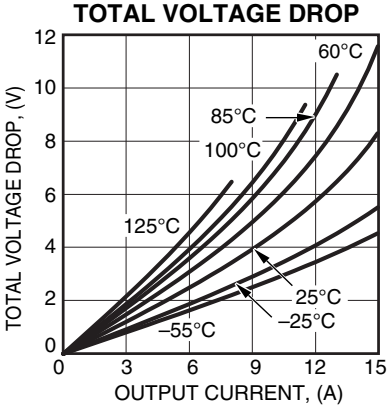
REVERSE DIODE



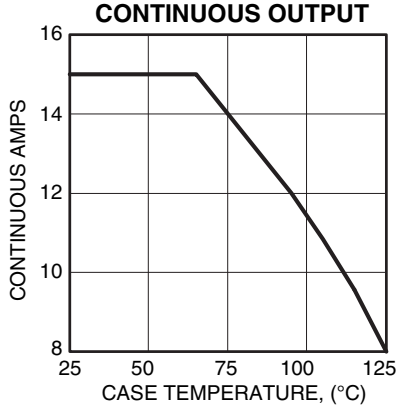
NORMALIZED ON RESISTANCE



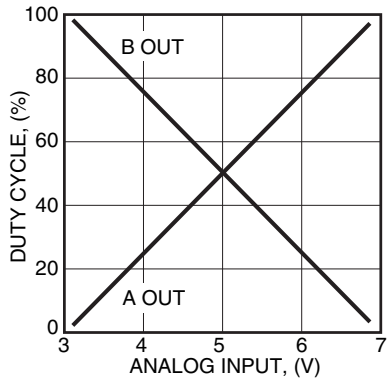
TOTAL VOLTAGE DROP



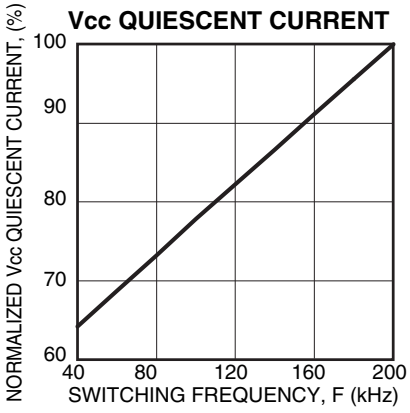
CONTINUOUS OUTPUT



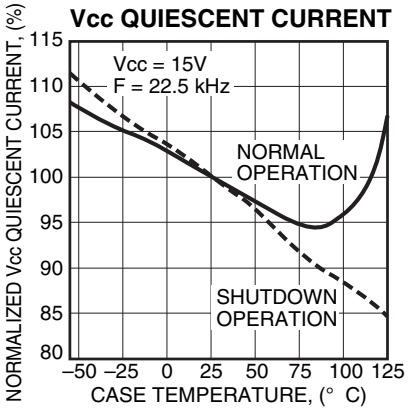
DUTY CYCLE VS ANALOG INPUT



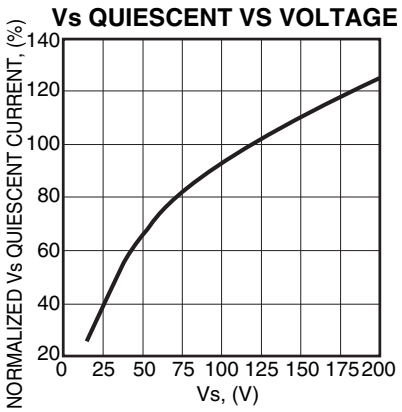
Vcc QUIESCENT CURRENT



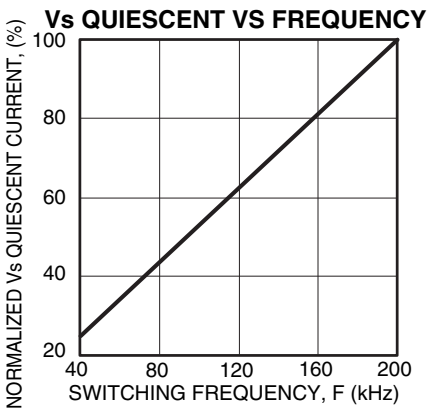
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 400kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 400kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

A fixed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit will latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

When supply voltage is over 100V, these circuits may not protect the FET switches in the case of short circuits directly at the pins of the amplifier. However, a small inductance between the amplifier and the short circuit will limit current rise time and the protection circuits will be effective. A pair of 12 inch wires is adequate inductance.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

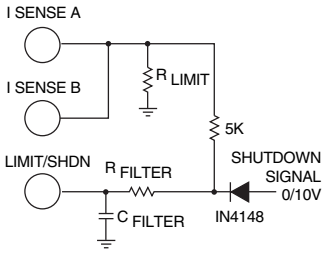


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

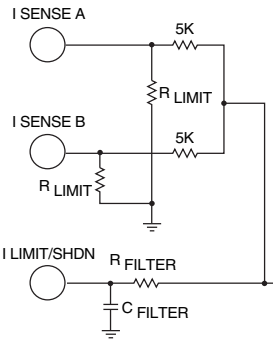


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

MODULATION RANGE

The high side of the all N channel H-bridge is driven by a bootstrap circuit. For the output circuit to switch high, the low side circuit must have previously been switched on in order to charge the bootstrap capacitor. Therefore, if the input signal to the SA12 demands a 100% duty cycle upon start-up the output will not follow and will be in a tri-state (open) condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal one time the output state will be correct thereafter. In addition, if during normal operation the input signal drives the SA12 beyond its linear modulation range (approximately 95%) the output will jump to 100% modulation.

H-Bridge Motor Driver/Amplifiers

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- SINGLE ENDED SUPPLY OPERATION
- WIDE SUPPLY RANGE: UP TO 80V
- 5A CONTINUOUS OUTPUT
- HERMETIC SEALED PACKAGE
- HIGH EFFICIENCY: 95% TYPICAL
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL PWM GENERATION

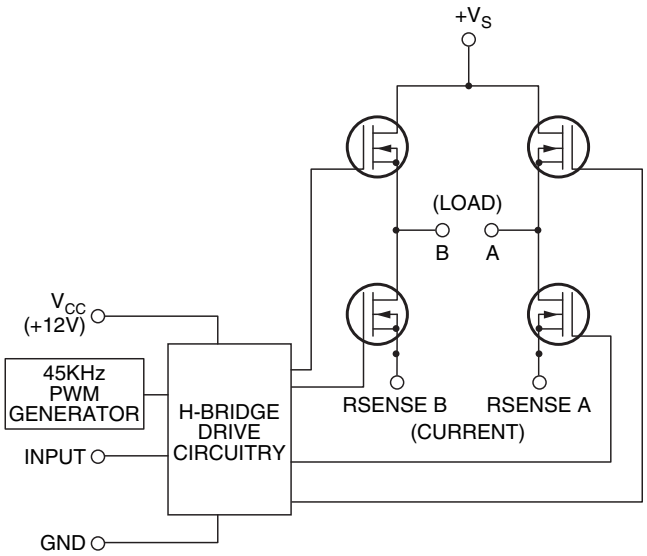
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

DESCRIPTION

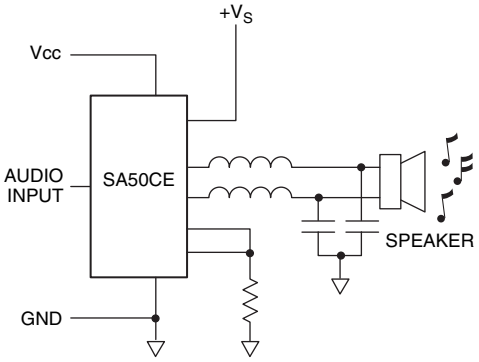
The SA50CE is a pulse width modulation amplifier that can continuously supply 5A to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and high side switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed and direction, or audio signal for switchmode audio amplification. The SA50CE is packaged in a space efficient isolated 8-pin TO-3 that can be directly connected to a heatsink.

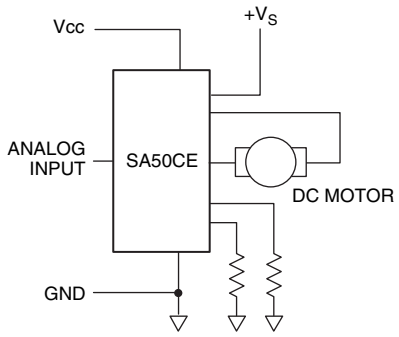
BLOCK DIAGRAM



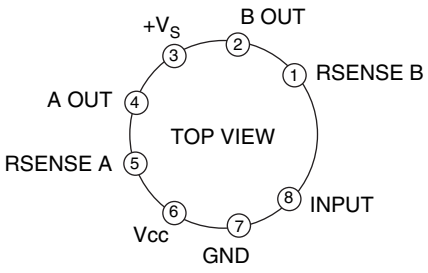
8-PIN TO-3
PACKAGE STYLE CE

TYPICAL APPLICATIONS





EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V[5]
OUTPUT CURRENT, peak	7A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	72W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–65 to +125°C
INPUT VOLTAGE	+1V to Vcc – 1.5 Vdc

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
ANALOG INPUT VOLTAGES	Vcc = 9.5V to 15V				
MOTOR A, B = 50% Duty Cycle			$V_{CC}/2$		V
MOTOR A = 100% Duty Cycle High[6]			$2V_{CC}/3$		V
MOTOR B = 100% Duty Cycle High[6]			$V_{CC}/3$		V
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 5A		1.0	1.3	Vdc
TOTAL Ron, both MOSFETs			0.4		Ω
EFFICIENCY, 5A OUTPUT	$+V_S$ = 80V		95		%
SWITCHING FREQUENCY		40	45	50	kHz
CURRENT, continuous		5			A
CURRENT, peak	t = 100 m-sec	7			A
SWITCHING CHARACTERISTICS[4]	$+V_S$ = 28V, Vcc = 12V, Ic =2A				
RISE TIME			36	54	ns
FALL TIME			170	250	ns
DEAD TIME			100		ns
POWER SUPPLY					
$+V_S$ VOLTAGE[5]	$+V_S$ I = Load I			80	V
Vcc VOLTAGE		9.5	12	15	V
Vcc CURRENT	Vcc = 12Vdc		20	30	mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor		2.0		°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–40		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 36W. This is an output FET rating only; normal operation at worst case conditions and maximum duty cycle only causes 19 watts internal heat generation in each active output FET. Use 40 watts maximum to size heatsink.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. Derate linearly to 70V at – 40°C from T_C = +25°C.

CAUTION

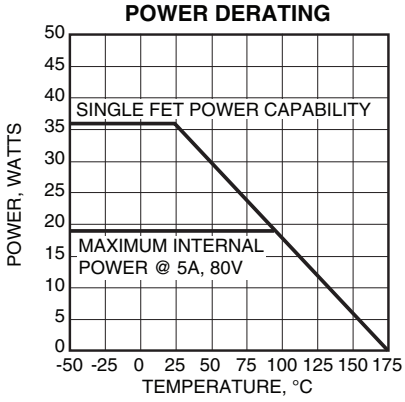
The SA50CE is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

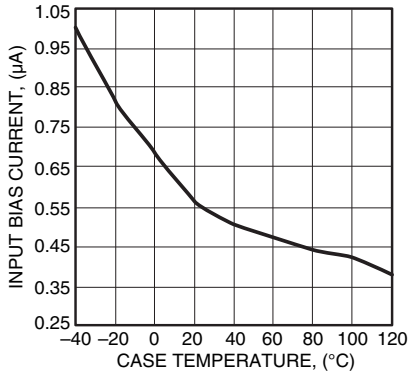
WARNING—AMPLIFIER PROTECTION

The SA50CE contains an internal logic chip that turns on and turns off output MOSFET drivers at a certain sequence. Noises or oscillation caused by external wiring inductance, lack of proper power supply bypass capacitors, ground, supply and local internal loops, may be fed back to this logic chip and cause it to turn on one or more MOSFET drivers at the wrong time, thus destroying the SA50CE. A well laid out PC board with low impedance copper ground plane and excellent bypassing is necessary for the SA50CE to function properly. A low ESR high frequency bypass capacitor, such as a 0.1 µf 100V X7R ceramic, or better, should be mounted as close to the Vs and ground pins as possible to avoid radiation of high frequency transients on the power supply wiring. The Apex Precision Power EK-SA50CE evaluation board is recommended for fast and easy breadboarding of circuits using the SA50CE.

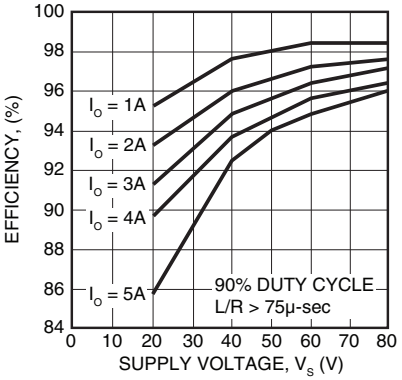
POWER DERATING



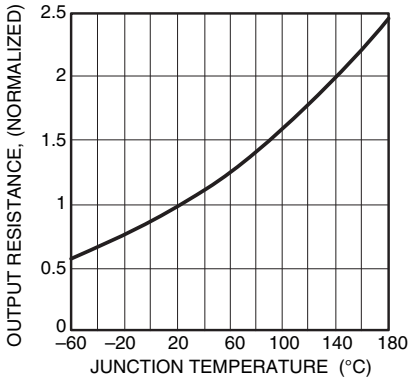
INPUT CURRENT VS TEMP



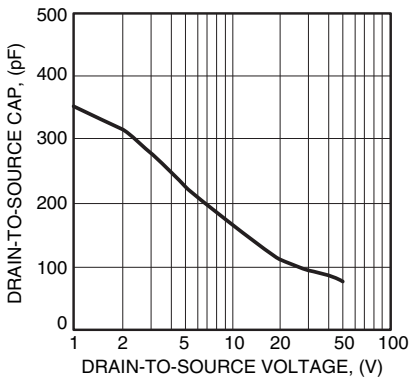
EFFICIENCY vs. POWER SUPPLY VOLTAGE



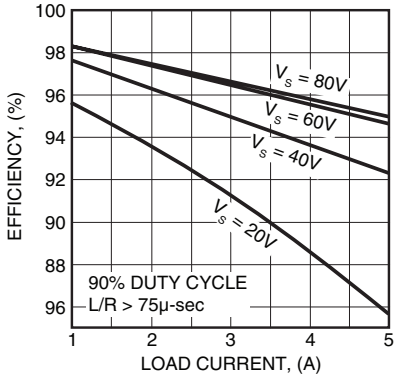
OUTPUT RESISTANCE DRIFT



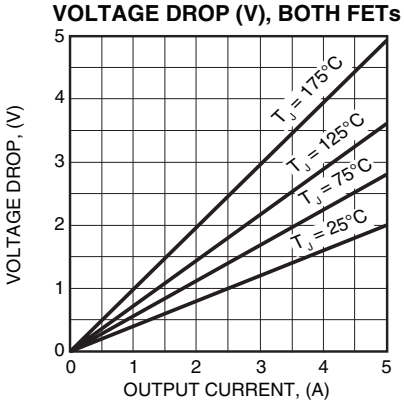
H-BRIDGE FET CAPACITANCE



EFFICIENCY vs. LOAD CURRENT



VOLTAGE DROP (V), BOTH FETs



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

PIN DESCRIPTION

V_{CC} - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. Proper by-passing to GND with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

A OUT - is the output pin for one half of the bridge. Increasing the input voltage causes increasing duty cycle at this output.

B OUT - is the output pin for the other half of the bridge. Decreasing the input voltage causes increasing duty cycles at this point.

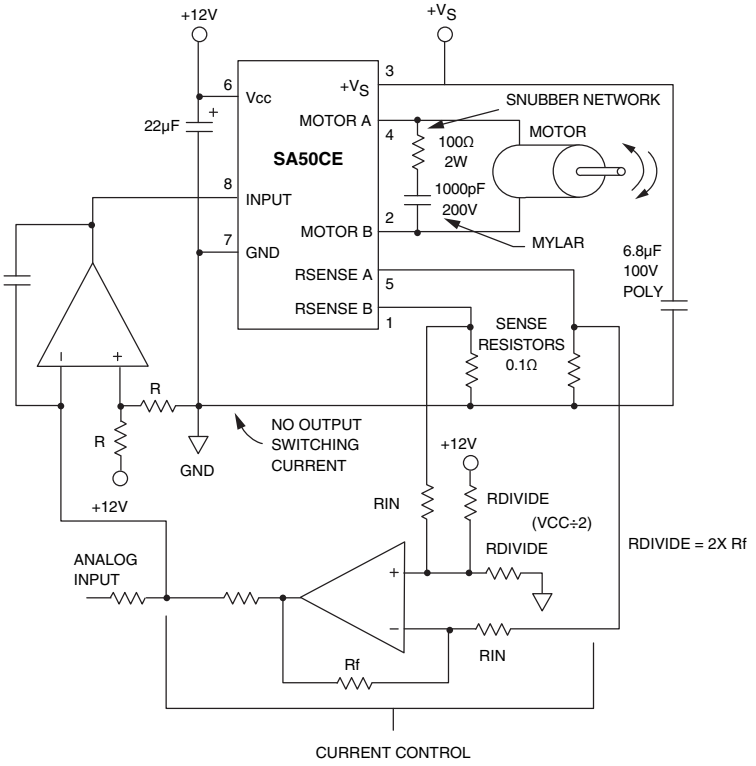
RSENSE A - This is the connection for the bottom of the A half bridge. This can have a sense resistor connected to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

GND - is the return connection for the input logic and V_{CC}.

RSENSE B - This is the connection for the bottom of the B half bridge. This can have a sense resistor connection to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than V_{CC}/2 will produce greater than 50% duty cycle pulses out of A OUT. A voltage lower than V_{CC}/2 will produce greater than 50% duty cycle pulses out of B OUT.

TYPICAL SYSTEM OPERATION



This is a diagram of a typical application of the SA50CE. The design Vcc voltage is +12 volts. V_{CC} is internally bypassed with a good low ESR ceramic capacitor. A higher ESR bulk capacitor, such as a tantalum electrolytic, may be used externally in parallel. The analog input can be an analog speed control voltage from a potentiometer, other analog circuitry or by microprocessor and a D/A converter. This analog input gets pulled by the current control circuitry in the proper direction to reduce the current flow in the bridge if it gets too high. The gain of the current control amplifier will have to be set to obtain the proper amount of current limiting required by the system.

Current sensing is done in this case by a 0.1Ω sense resistor to sense the current from both legs of the bridge separately. It is important to make the high current traces as big as possible to keep inductance down. The storage capacitor connected to the V_S and the hybrid GND should be large enough to provide the high energy pulse without the voltage sagging too far. A low ESR capacitor will be required. Mount capacitor as close to the hybrid as possible. The connection between GND and the V_S return should not be carrying any motor current. The sense resistor signal is common mode filtered as necessary to feed the limiting circuitry. This application will allow full four quadrant torque control for a closed loop servo system.

A snubber network is usually required, due to the inductance in the power loop. It is important to design the snubber network to suppress any positive spikes above $+V_S$ and negative spikes below –2V with respect to pin 7 (GND).

Switching Amplifier

RoHS COMPLIANT

FEATURES

- Low Cost Intelligent Switching Amplifier
- Directly Connects to Most Embedded Microcontrollers and Digital Signal Controllers
- Integrated Gate Driver Logic with Dead-time Generation and Shoot-through Prevention
- Wide Power Supply Range (8.5 V To 60 V)
- Over 10A Peak Output Current per Phase
- 3A Continuous Output Current per Phase
- Independent Current Sensing for each Output
- User Programmable Cycle-by-cycle Current Limit Protection
- Over-Current and Over-Temperature Warning Signals

APPLICATIONS

- Bidirectional DC Brush Motors
- 2 Unidirectional DC Brush Motors
- 2 Independent Solenoid Actuators
- Stepper Motors

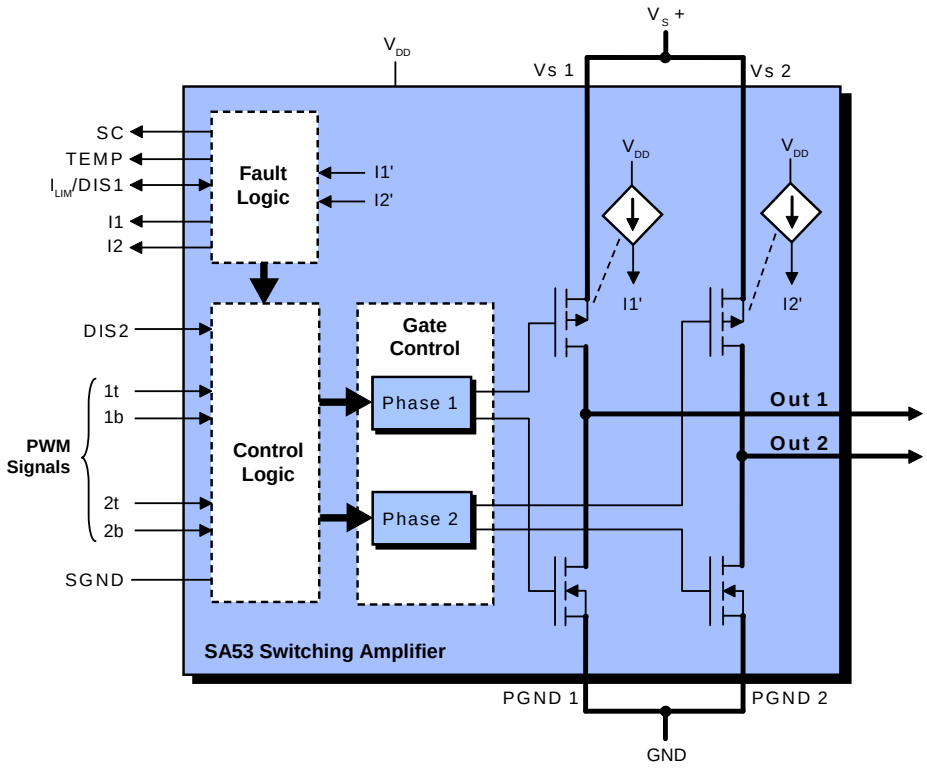
DESCRIPTION

The SA53 is a fully integrated switching amplifier designed primarily to drive DC brush motors. Two independent half bridges provide over 10 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram is provided in Figure 1.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA53 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

The Power Quad surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

FIGURE 1. BLOCK DIAGRAM



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_S		60	V
SUPPLY VOLTAGE	V_{DD}		5.5	V
LOGIC INPUT VOLTAGE		(-0.5)	(V_{DD}+0.5)	V
OUTPUT CURRENT, peak, 10ms (NOTE 2)	I_{OUT}		10	A
POWER DISSIPATION, avg, 25ºC (NOTE 2)	P_D		100	W
TEMPERATURE, solder, 10sec	T_S		260	°C
TEMPERATURE, junction (NOTE 2)	T_J		150	°C
TEMPERATURE RANGE, storage	T_{STG}	−55	125	°C
OPERATING TEMPERATURE, case	T_A	−40	125	°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
LOGIC					
INPUT LOW				1	V
INPUT HIGH		1.8			V
OUTPUT LOW				0.3	V
OUTPUT HIGH		3.7			V
OUTPUT CURRENT (SC, Temp, I_{LIM}/DIS1)			50		mA
POWER SUPPLY					
V_S		UVLO	50	60	V
V_S UNDERVOLTAGE LOCKOUT, (UVLO)			8.3		V
V_{DD}		4.5		5.5	V
SUPPLY CURRENT, V_S	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		25	30	mA
SUPPLY CURRENT, V_{DD}	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		5	6	mA
CURRENT LIMIT					
CURRENT LIMIT THRESHOLD (Vth)			3.75		V
Vth HYSTERESIS			100		mV
OUTPUT					
CURRENT, CONTINUOUS	25ºC Case Temperature	3			A
RISING DELAY, TD (RISE)	See Figure 10		270		ns
FALLING DELAY, TD (FALL)	See Figure 10		270		ns
DISABLE DELAY, TD (DIS)	See Figure 10		200		ns
ENABLE DELAY, TD ($\overline{DIS}$)	See Figure 10		200		ns
RISE TIME, T (RISE)	See Figure 11		50		ns
FALL TIME, T (FALL)	See Figure 11		50		ns
ON RESISTANCE SOURCING (P-CHANNEL)	3A Load		400		mΩ
ON RESISTANCE SINKING (N-CHANNEL)	3A Load		400		mΩ

SPECIFICATIONS, continued

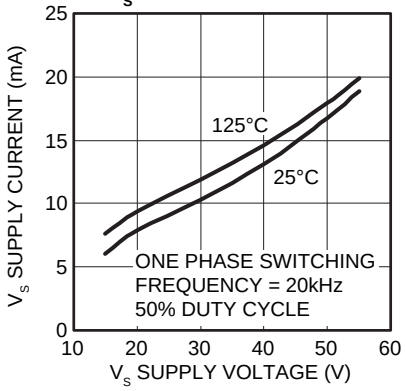
PARAMETER	TEST CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
THERMAL					
THERMAL WARNING			135		ºC
THERMAL WARNING HYSTERESIS			40		ºC
RESISTANCE, junction to case	Full temperature range		1.25	1.5	ºC/W
TEMPERATURE RANGE, case	Meets Specifications	-40		85	ºC

NOTES:

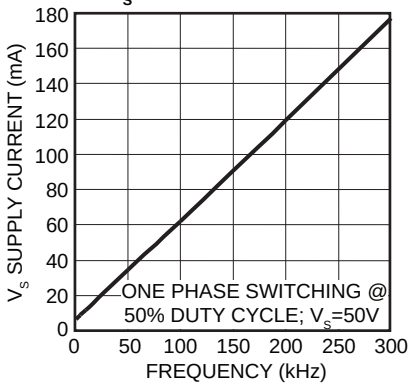
1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.
3. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

FIGURE 2. 64-pin QFP, Package Style HQ

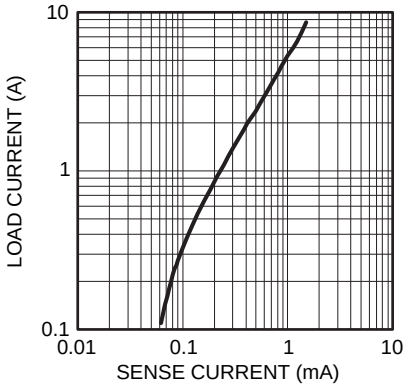
V_S SUPPLY CURRENT



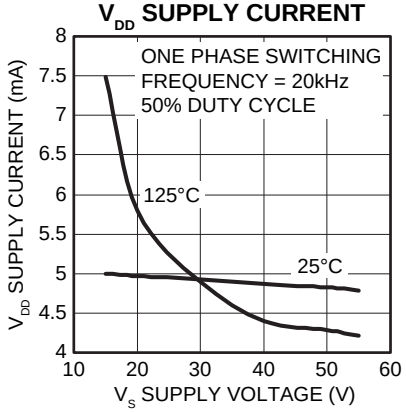
V_S SUPPLY CURRENT



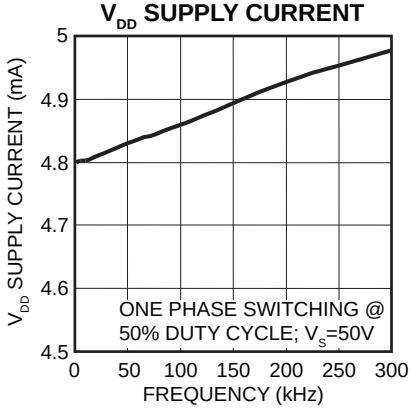
CURRENT SENSE



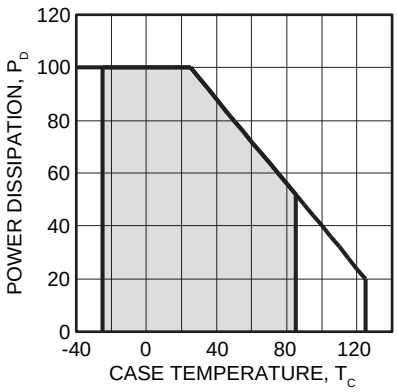
V_{DD} SUPPLY CURRENT



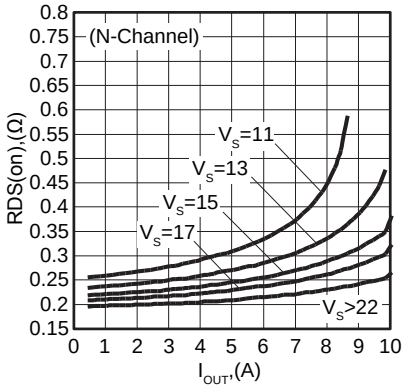
V_{DD} SUPPLY CURRENT



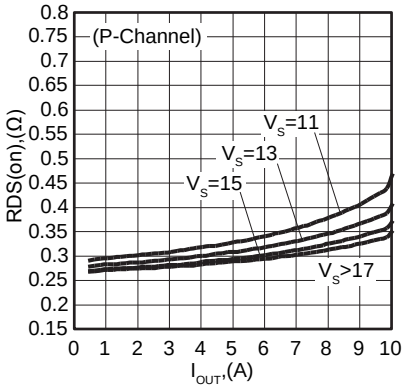
POWER DERATING



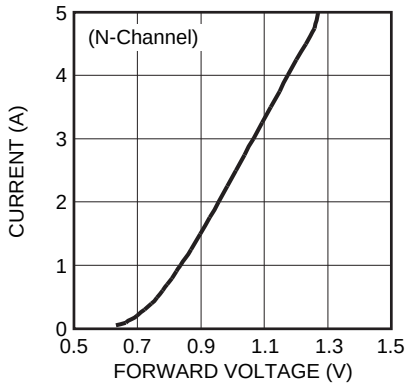
ON RESISTANCE - BOTTOM FET



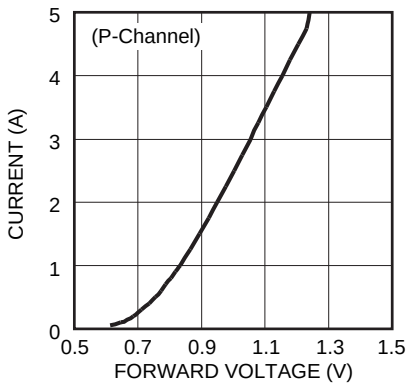
ON RESISTANCE - TOP FET



DIODE FORWARD VOLTAGE - BOTTOM FET



DIODE FORWARD VOLTAGE - TOP FET



D

FIGURE 3. EXTERNAL CONNECTIONS

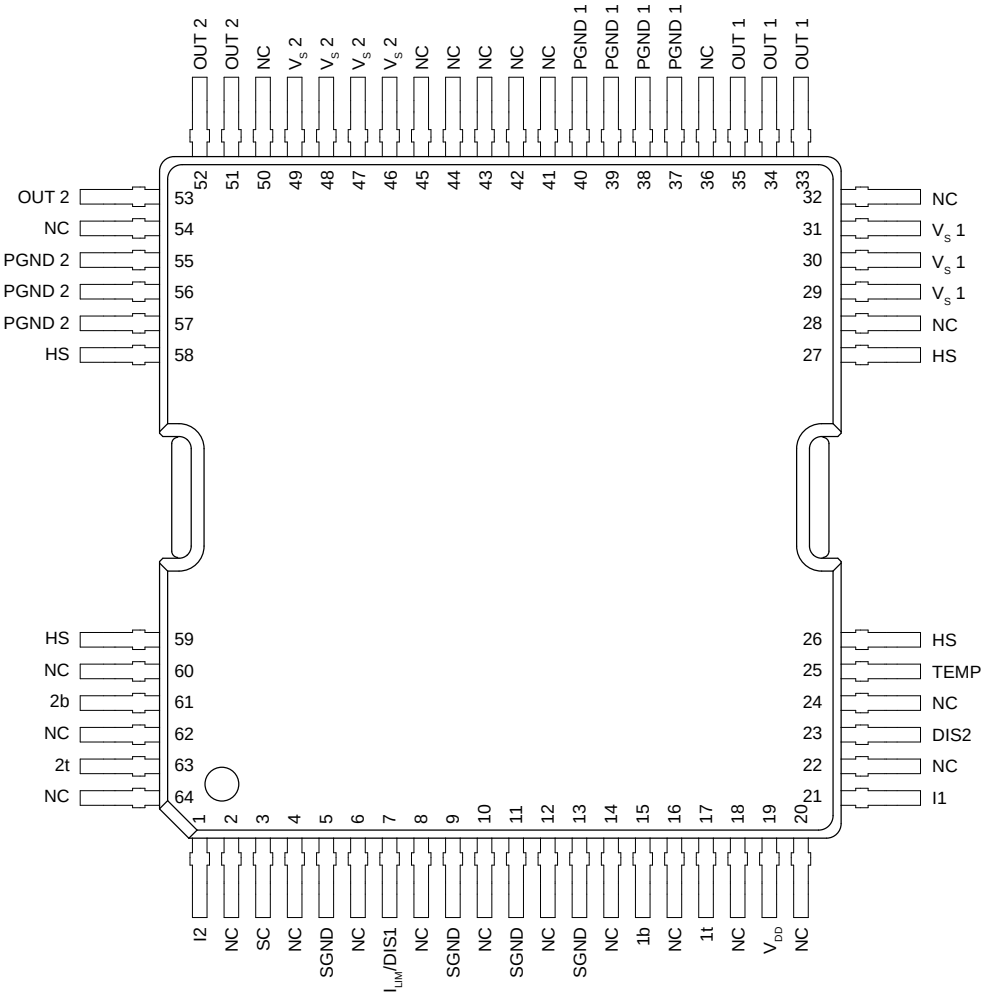


TABLE 1. PIN DESCRIPTIONS			
Pin #	**Pin Name**	**Signal Type**	**Simplified Pin Description**
29,30,31	V_S (phase 1)	Power	High Voltage Supply (8.5-60V) supplies phase 1 only
51,52,53	OUT 2	Power Output	Half Bridge 2 Power Output
55,56,57	PGND (phase 2)	Power	High Current GND Return Path for Power Output 2
3	SC	Logic Output	Indication of a short of an output to supply, GND or another phase
61	2b	Logic Input	Logic high commands 2 phase lower FET to turn on
63	2t	Logic Input	Logic high commands 2 phase upper FET to turn on
1	I2	Analog Output	Phase 2 current sense output
7	I_{LIM}/DIS1	Logic Input/Output	As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function.
5,9,11,13	SGND	Power	Analog and digital GND – internally connected to PGND
15	1b	Logic Input	Logic high commands 1 phase lower FET to turn on
17	1t	Logic Input	Logic high commands 1 phase upper FET to turn on
19	V_{DD}	Power	Logic Supply (5V)
21	I1	Analog Output	Phase 1 current sense output
23	DIS2	Logic Input	Logic high places all outputs in a high impedance state

TABLE 1. PIN DESCRIPTIONS			
Pin #	**Pin Name**	**Signal Type**	**Simplified Pin Description**
25	TEMP	Logic Output	Thermal indication of die temperature above 135ºC
46,47,48,49	V_S (phase 2)	Power	High Voltage Supply phase 2
33,34,35	OUT 1	Power Output	Half Bridge 1 Power Output
37,38,39,40	PGND (phase 1)	Power	High Current GND Return Path for Power Outputs 1&2
26,27,58,59	HS	Mechanical	Pins connected to the package heat slug
2,4,6,8,10, 12,14,16,18, 20,22,24,28, 32,36,41,42, 43,44,45,50, 54,60,62,64	NC	---	Do Not Connect

1.2 Pin Descriptions

V_S: Supply voltage for the output transistors. These pins require decoupling (1µF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V_S and PGND pins as possible. Additional capacitance will be required at the V_S pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that V_S pins 29-31 carry only the phase 1 supply current. Pins 46-49 carry supply current for phase 2. Phase 1 may be operated at a different supply voltage from phase 2. Both V_S voltages are monitored for undervoltage conditions.

OUT 1, OUT 2: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t_{RR} specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs. (See Section 2.6)

PGND: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

SC: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor.

1b, 2b: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If 2b or 2b is high at the same time that a corresponding 1t or 2t input is high, protection circuitry will turn off both FETs in order to prevent shoot-through on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

1t, 2t: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

I1, I2: Current sense pins. The SA53 supplies a positive current to these pins which is proportional to the current flowing through the top side P-channel FET for that phase. Commutating currents flowing through the backbody diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.

The current sense pins are also internally compared with the current limit threshold voltage reference, Vth. If the voltage on any current sense pin exceeds Vth, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

I_{LIM}/DIS1: This pin is directly connected to the disable circuitry of the SA53. Pulling this pin to logic high places OUT 1 and OUT 2 in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

SGND: This is the ground return connection for the V_{DD} logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms,. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

V_{DD}: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA53. This pin requires decoupling (at least 0.1µF capacitor with good high frequency characteristics is recommended) to the SGND pin.

DIS2: The DIS2 pin is a Schmitt triggered logic level input that places OUT 1 and OUT 2 in a high impedance state when pulled high. DIS2 has an internal 12kΩ pull-down resistor and may therefore be left unconnected.

TEMP: This logic level output goes high when the die temperature of the SA53 reaches approximately 135ºC. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor.

HS: These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

NC: These “no-connect” pins should be left unconnected.

2. SA53 OPERATION

The SA53 is designed primarily to drive DC brush motors. However, it can be used for any application requiring two high current outputs. The signal set of the SA53 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for both phases provide performance information which can be used to regulate or limit torque.

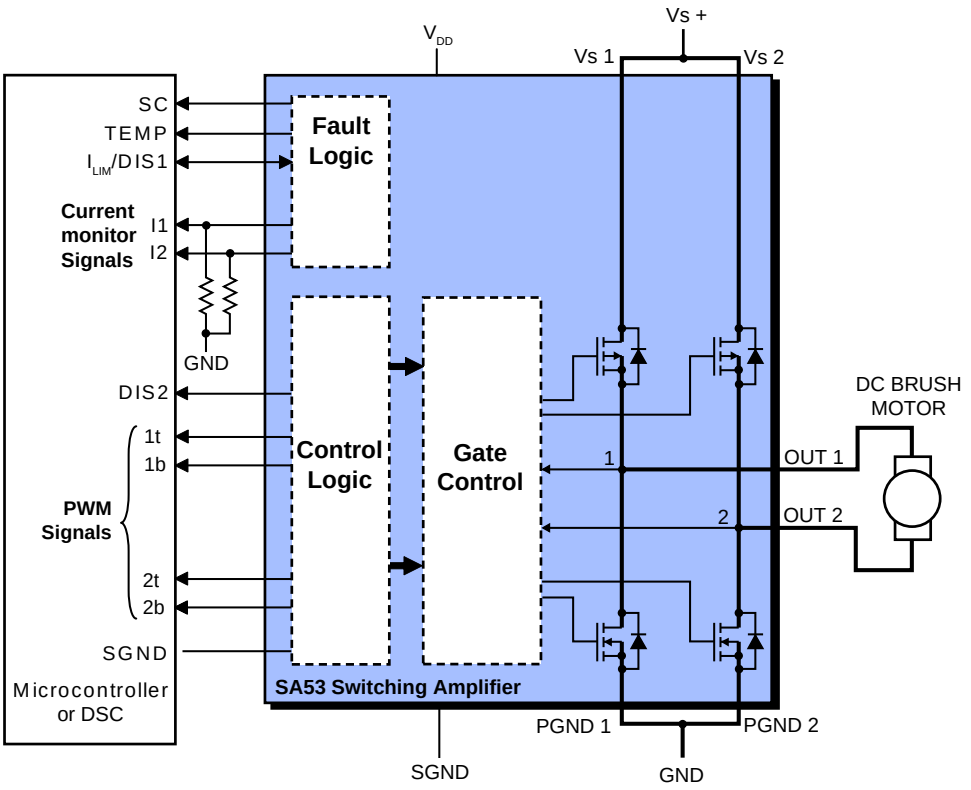


FIGURE 4. SYSTEM DIAGRAM

The block diagram in Figure 5 illustrates the features of the input and output structures of the SA53. For simplicity, a single phase is shown.

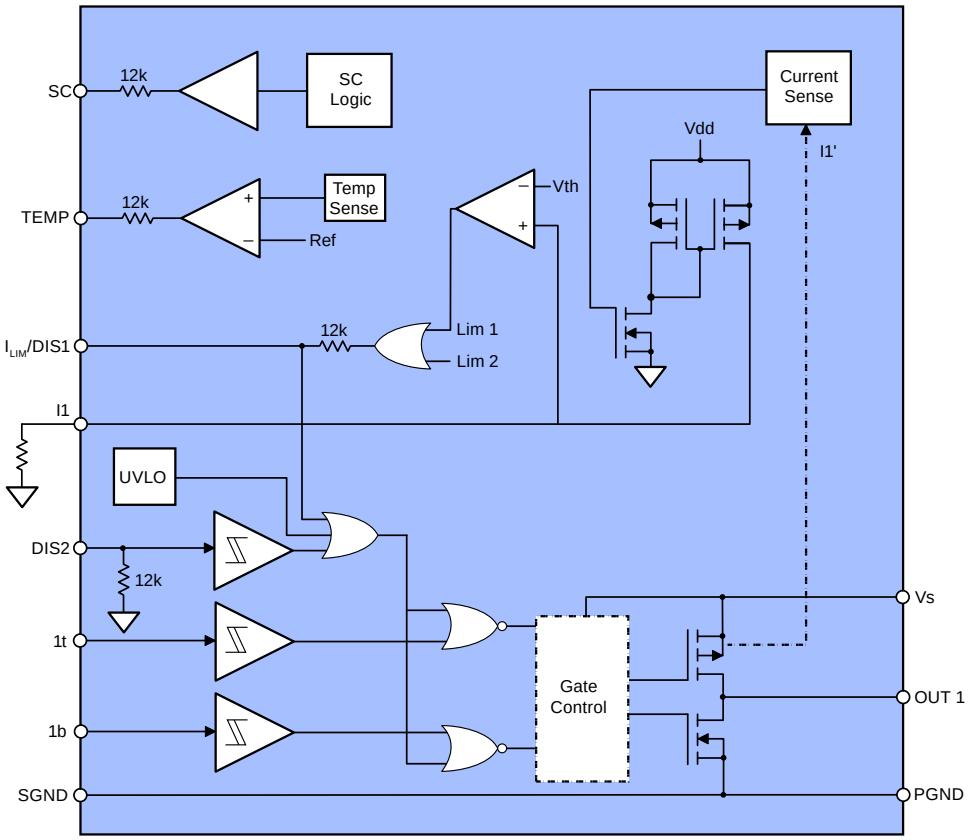


FIGURE 5. INPUT AND OUTPUT STRUCTURES FOR A SINGLE PHASE

TABLE 2. TRUTH TABLE

1t, 2t	1b, 2b	I1, I2	I_{LIM}/DIS1	DIS2	OUT 1 OUT 2	Comments
0	0	X	X	X	High-Z	Top and Bottom output FETs for that phase are turned off.
0	1	$<V_{th}$	0	0	PGND	Bottom output FET for that phase is turned on.
1	0	$<V_{th}$	0	0	VS	Top output FET for that phase is turned on.
1	1	X	X	X	High-Z	Both output FETs for that phase are turned off.
X	X	$>V_{th}$	1	X	High-Z	Voltage on I1 or I2 has exceeded Vth, which causes I_{LIM}/DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases.
X	X	X	X	1	High-Z	DIS2 pin pulled high, which disables all outputs.
X	X	X	Pulled High	X	High-Z	Pulling the I_{LIM}/DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.
X	X	X	Pulled Low	0	Determined by PWM inputs	Pulling the DIS2 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.
X	X	X	X	X	High-Z	If V_S is below the UVLO threshold all output FETs will be disabled.

2.1 LAYOUT CONSIDERATIONS

Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25µF per ampere of output current should be placed near the SA53 as well. Capacitor types rated for switching applications are the only types that should be considered.

The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1µF to 0.47µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

2.2 FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA53 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA53.

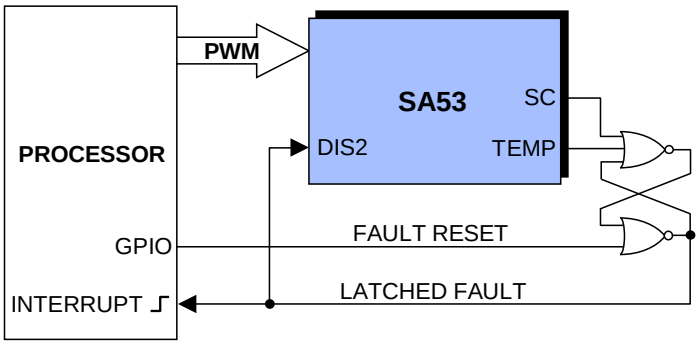


FIGURE 6. EXTERNAL FAULT LATCH CIRCUIT

Figure 6 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA53 will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

2.3 UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA53 unilaterally disabling all output FETs until VS is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lock- out condition is in progress. The SA53 has two V_S connections: one for phase 1 and another for phase 2. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

2.4 CURRENT SENSE

External power shunt resistors are not required with the SA53. Forward current in each top, Pchannel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the V_{DD} supply. Headroom required for the current sense circuit is approximately 0.5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 4 of this datasheet.

2.5 CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at startup.

Because the output current of each upper output FET is measured, the SA53 is able to provide a very robust current limit scheme. This enables the SA53 to safely and easily drive virtually any DC brush motor through a startup inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 7 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the two current sense pins exceeds the current limit threshold voltage (Vth), all outputs are disabled. After all current sense pins fall below the Vth threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (1t or 2t). With most commutation schemes, the current limit will reset each pwm cycle. This scheme regulates the peak current in each phase during each pwm cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

Figure 8 illustrates the current limit trigger and reset sequence. Current limit engages and I_{LIM}/DIS1 goes high when any current sense pin exceeds Vth. Notice that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a sub-cycle oscillation.

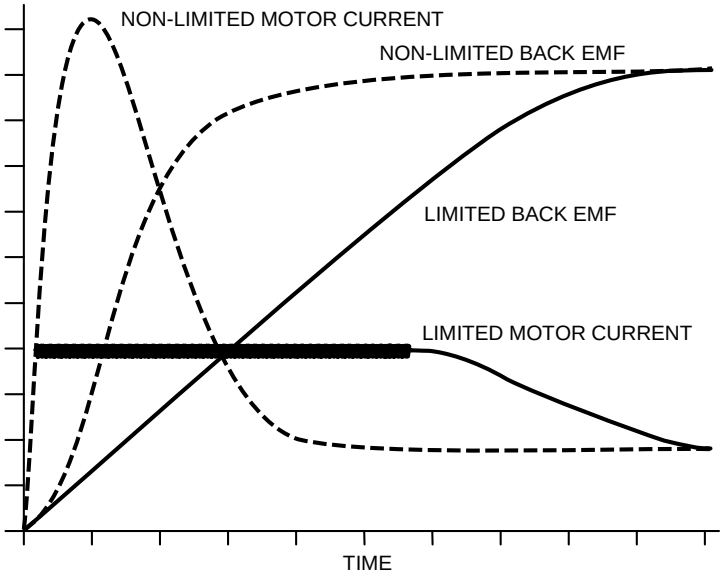


FIGURE 7. START-UP VOLTAGE AND CURRENT

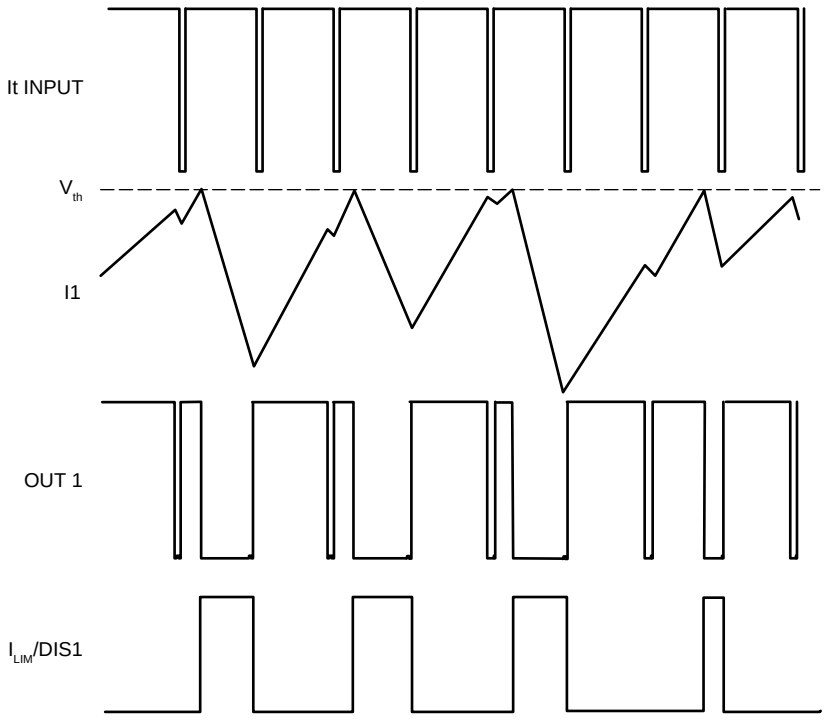


FIGURE 8. CURRENT LIMIT WAVEFORMS

This oscillation can be seen on the I_{LIM}/DIS1 pin waveform in Figure 8. Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of 1t and 2t except when commutating phases. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

The current limit feature may be disabled by tying the I_{LIM}/Dis1 pin to GND. The current sense pins will continue to provide top FET output current information.

Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

2.6 EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

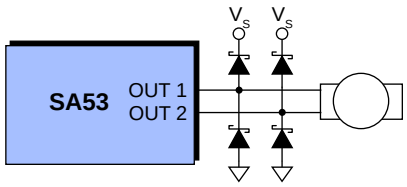


FIGURE 9. SCHOTTKY DIODES

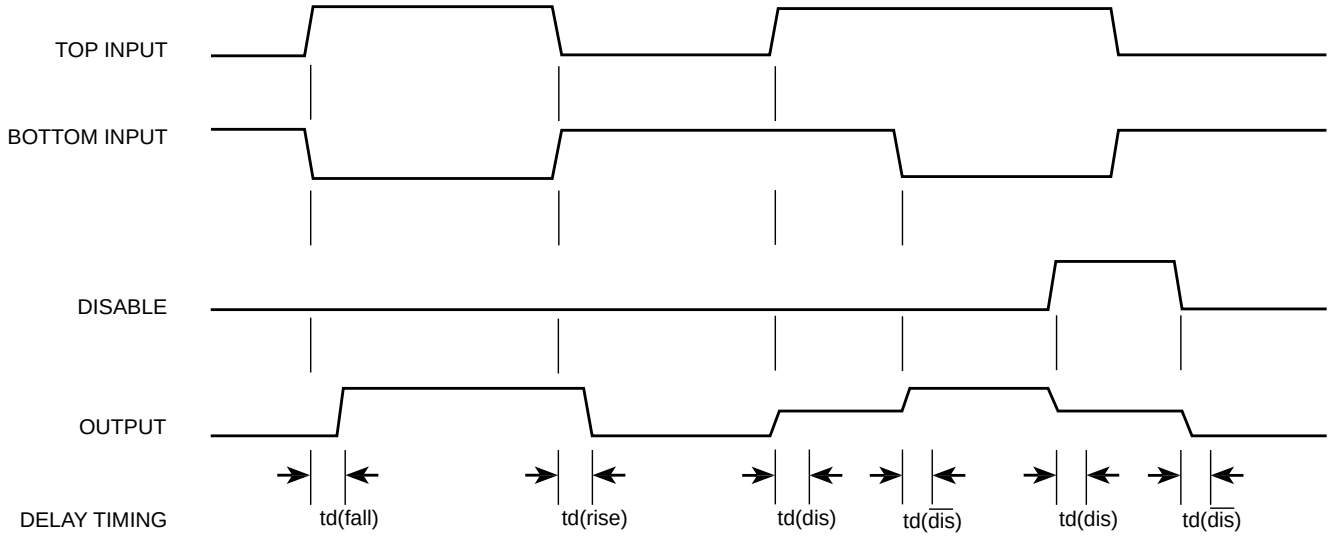


FIGURE 10. TIMING DIAGRAMS

3. POWER DISSIPATION

The thermally enhanced package of the SA53 allows several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents. Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA53. Applications vary widely and various thermal techniques are available to match the required performance. The patent pending mounting technique shown in Figure 12, with the SA53 inverted and suspended through a cutout in the PCB is adequate for power dissipation up to 17W with the HS33, a 1.5 inch long aluminum extrusion with four fins. In free air, mounting the PCB perpendicular to the ground, such that the heated air flows upward along the channels of the fins can provide a total Θ_{JA} of less than 14 ºC/W (9W max average PD). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a Θ_{JA} of 16.66 ºC/W (7.5W max average P_D). In applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance.

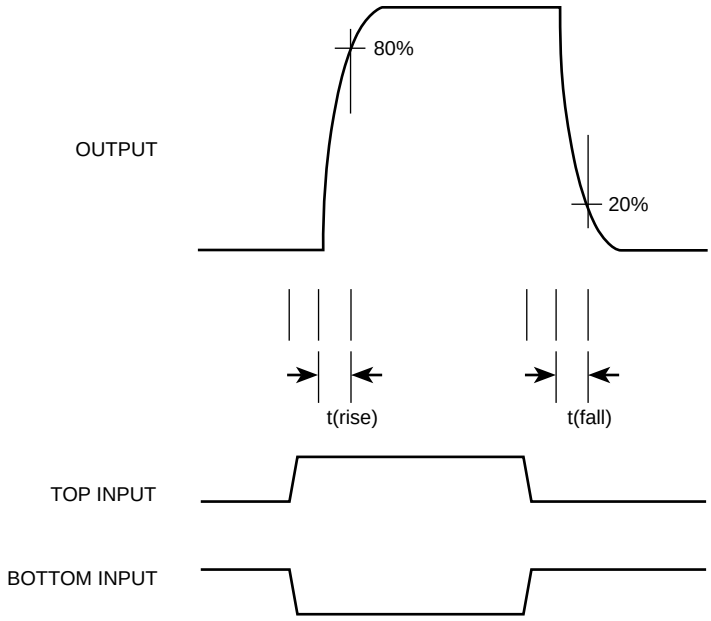
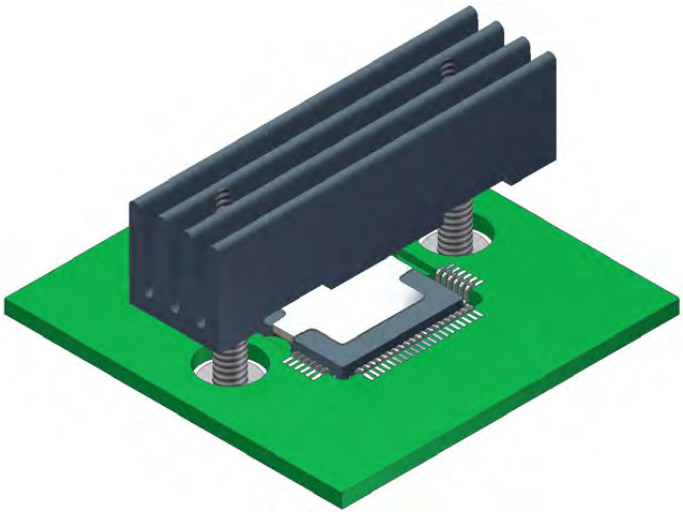


FIGURE 11. OUTPUT RESPONSE

FIGURE 12. HEATSINK TECHNIQUE

PATENT PENDING



4. ORDERING AND PRODUCT STATUS INFORMATION

MODEL	TEMPERATURE	PACKAGE	PRODUCTION STATUS
SA53-IHZ	-25 to 85ºC	64 pin Power QFP (HQ package drawing)	Samples Available 1Q09

SA57 • SA57A

Switching Amplifier

RoHS COMPLIANT

FEATURES

- Low cost intelligent switching amplifier
- Directly connects to most embedded Microcontrollers and Digital Signal Controllers
- Integrated gate driver logic with dead-time generation and shoot-through prevention
- Wide power supply range (8.5V to 60V)
- Over 15A peak output current per phase
- 5A continuous output current per phase
  8A continuous for A-Grade (SA57A)
- Independent current sensing for each output
- User programmable cycle-by-cycle current limit protection
- Over-current and over-temperature warning signals

APPLICATIONS

- Bidirectional DC brush motors
- 2 unidirectional DC brush motors
- 2 independent solenoid actuators
- Stepper motors

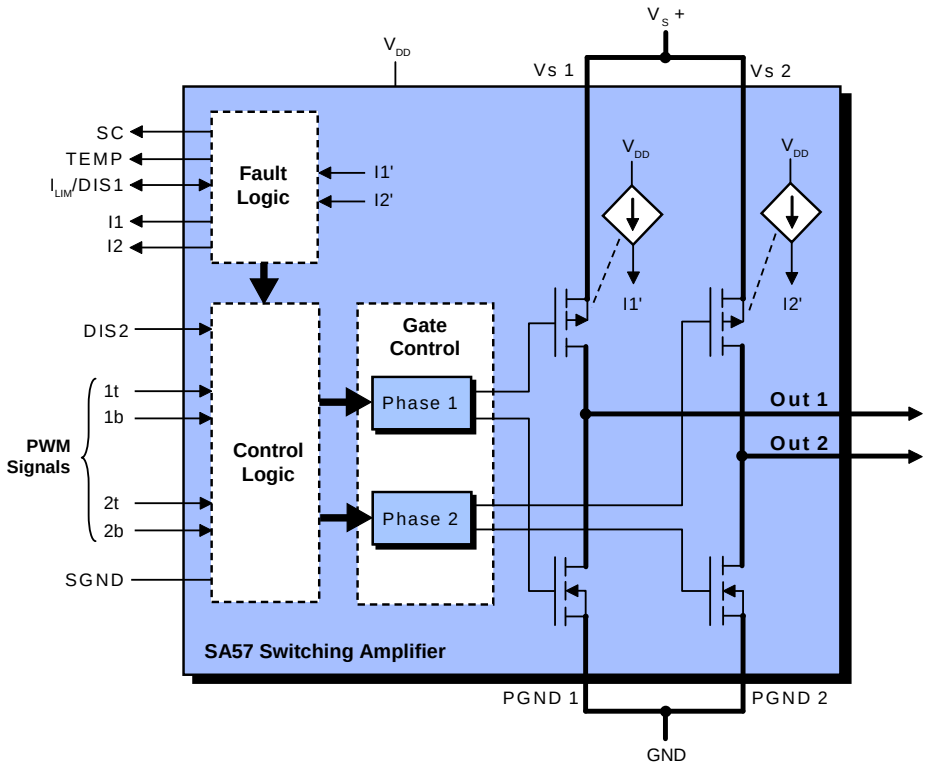
DESCRIPTION

The SA57 is a fully integrated switching amplifier designed primarily to drive DC brush motors. Two independent half bridges provide over 15 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram is provided in Figure 1.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA57 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

The Power Quad surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

Figure 1. BLOCK Diagram



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_S		60	V
SUPPLY VOLTAGE	V_{DD}		5.5	V
LOGIC INPUT VOLTAGE		(-0.5)	(V_{DD}+0.5)	V
OUTPUT CURRENT, peak, 10ms[2]	I_{OUT}		17	A
POWER DISSIPATION, avg, 25ºC[2]	P_D		100	W
TEMPERATURE, junction[3]	T_J		150	°C
TEMPERATURE RANGE, storage	T_{STG}	−55	125	°C
OPERATING TEMPERATURE, case	T_A	−40	125	°C

SPECIFICATIONS

Parameter	Test Conditions[2]	SA57			SA57A			Units
		Min	Typ	Max	Min	Typ	Max	
LOGIC								
INPUT LOW				1			*	V
INPUT HIGH		1.8			*			V
OUTPUT LOW				0.3			*	V
OUTPUT HIGH		3.7			*			V
OUTPUT CURRENT (SC, Temp, I_{LIM}/DIS1)			50			*		mA
POWER SUPPLY								
V_S		UVLO	50	60			55	V
V_S UNDERVOLTAGE LOCKOUT, (UVLO)			9			*	*	V
V_{DD}		4.5		5.5	*		*	V
SUPPLY CURRENT, V_S	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		25	30		*	*	mA
SUPPLY CURRENT, V_{DD}	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		5	6		*	*	mA
CURRENT LIMIT								
CURRENT LIMIT THRESHOLD (Vth)			3.95			*		V
Vth HYSTERESIS			100			*		mV
OUTPUT								
CURRENT, CONTINUOUS	25ºC Case Temperature	5			8			A
RISING DELAY, TD (RISE)	See Figure 10		270			*		ns
FALLING DELAY, TD (FALL)	See Figure 10		270			*		ns
DISABLE DELAY, TD (DIS)	See Figure 10		200			*		ns
ENABLE DELAY, TD ($\overline{DIS}$)	See Figure 10		200			*		ns
RISE TIME, T (RISE)	See Figure 11		50			*		ns
FALL TIME, T (FALL)	See Figure 11		50			*		ns

SPECIFICATIONS, continued

Parameter	Test Conditions[2]	SA57			SA57A			Units
		Min	Typ	Max	Min	Typ	Max	
ON RESISTANCE SOURCING (P-CHANNEL)	5A Load		300	750		300	600	mΩ
ON RESISTANCE SINKING (N-CHANNEL)	5A Load		250	750		250	600	mΩ
THERMAL								
THERMAL WARNING			135			*		ºC
THERMAL WARNING HYSTERESIS			40			*		ºC
RESISTANCE, junction to case	Full temperature range		1.25	1.5		*	*	ºC/W
TEMPERATURE RANGE, case	Meets Specifications	-25		85	-40		125	ºC

NOTES:

* The specification of SA57A is identical to the specification for SA57 in applicable column to the left.

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.
3. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

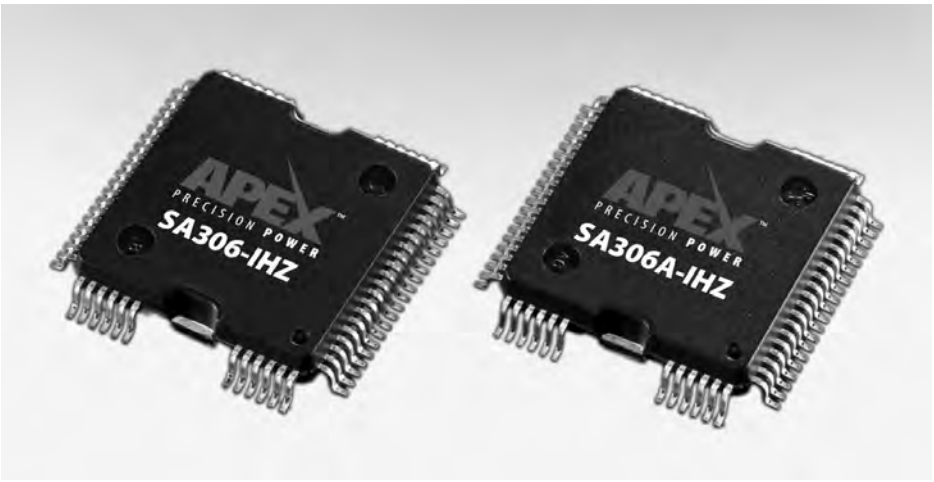
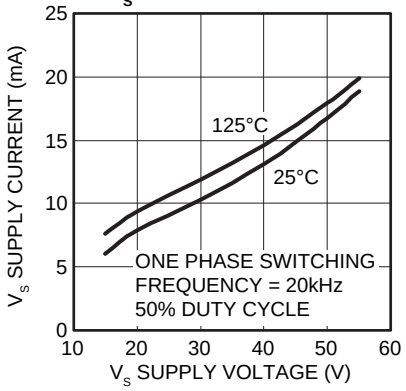
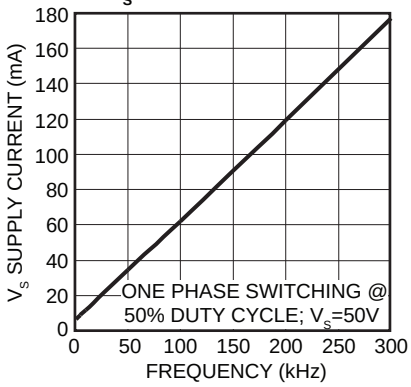


Figure 2. 64-Pin QFP, Package Style HQ

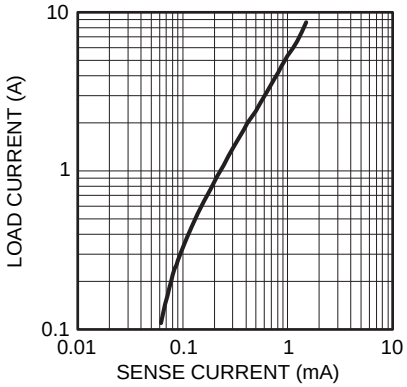
V_S SUPPLY CURRENT



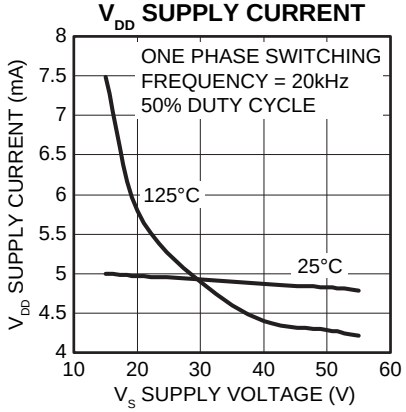
V_S SUPPLY CURRENT



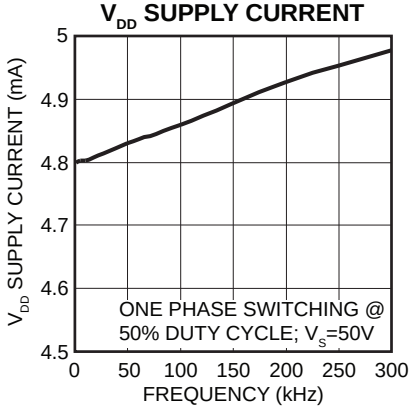
CURRENT SENSE



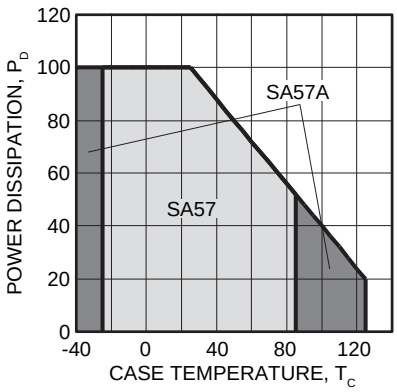
V_{DD} SUPPLY CURRENT



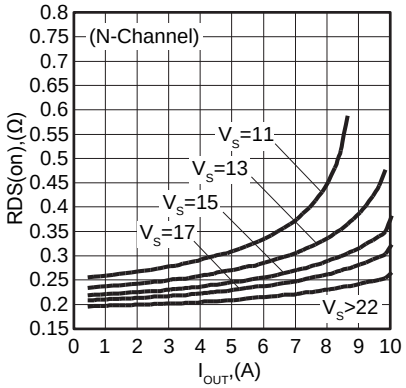
V_{DD} SUPPLY CURRENT



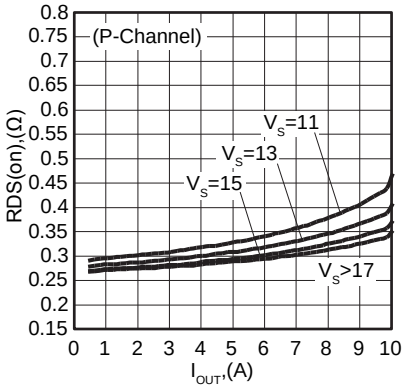
POWER DERATING



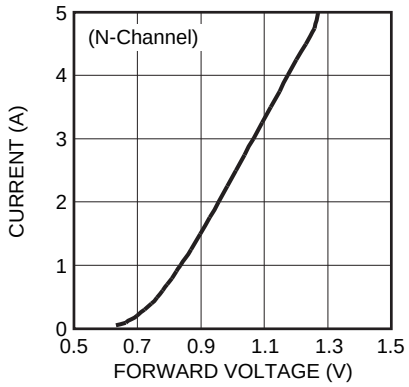
ON RESISTANCE - BOTTOM FET



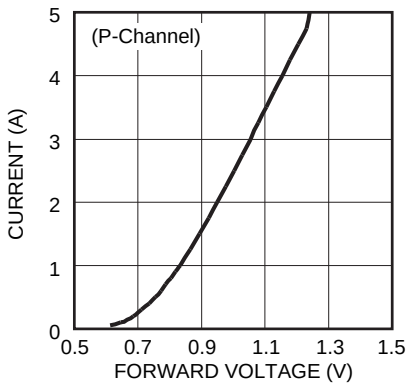
ON RESISTANCE - TOP FET



DIODE FORWARD VOLTAGE - BOTTOM FET



DIODE FORWARD VOLTAGE - TOP FET



D

Figure 3. External Connections

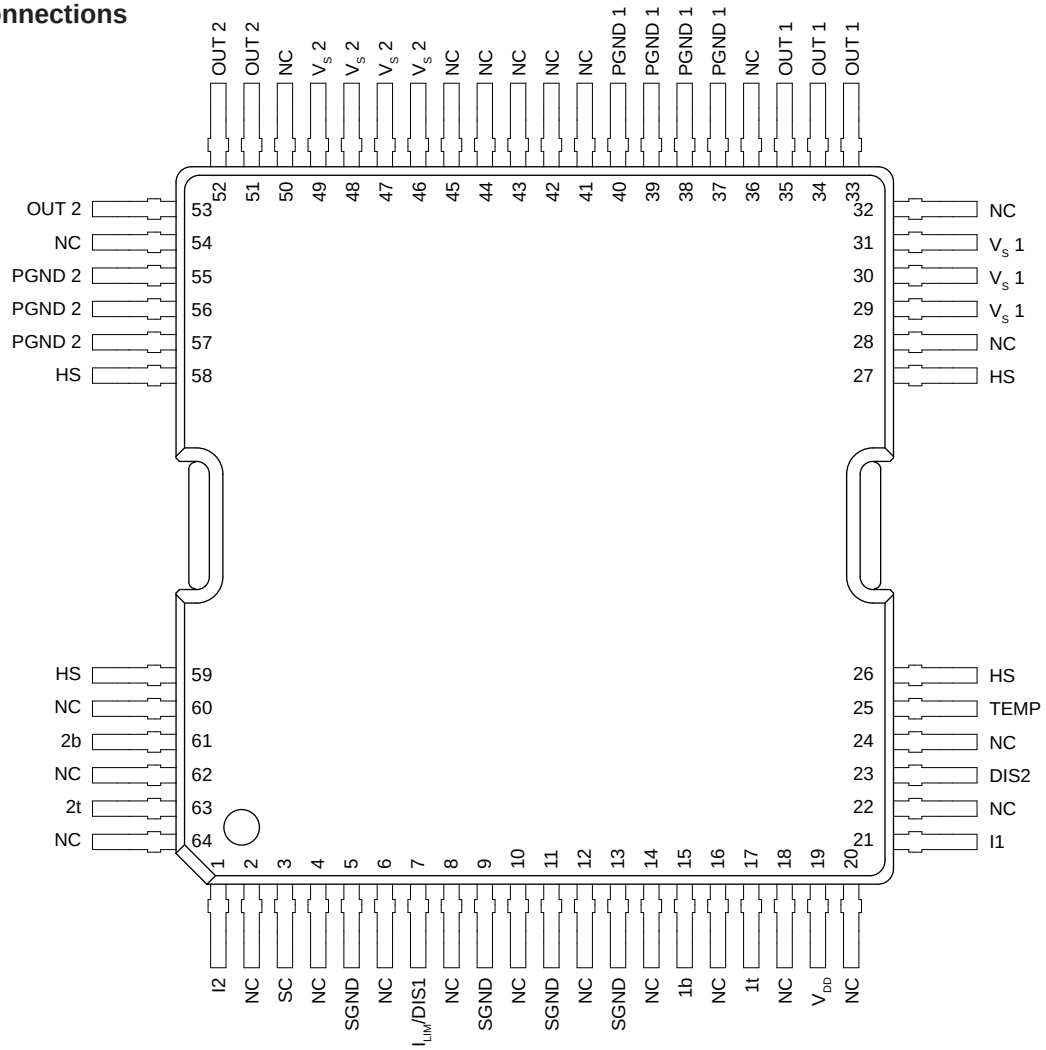


TABLE 1. PIN DESCRIPTIONS			
Pin #	**Pin Name**	**Signal Type**	**Simplified Pin Description**
29,30,31	V_S (phase 1)	Power	High Voltage Supply (8.5-60V) supplies phase 1 only
51,52,53	OUT 2	Power Output	Half Bridge 2 Power Output
55,56,57	PGND (phase 2)	Power	High Current GND Return Path for Power Output 2
3	SC	Logic Output	Indication of a short of an output to supply, GND or another phase
61	2b	Logic Input	Logic high commands 2 phase lower FET to turn on
63	2t	Logic Input	Logic high commands 2 phase upper FET to turn on
1	I2	Analog Output	Phase 2 current sense output
7	I_{LIM}/DIS1	Logic Input/Output	As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function.
5,9,11,13	SGND	Power	Analog and digital GND – internally connected to PGND
15	1b	Logic Input	Logic high commands 1 phase lower FET to turn on
17	1t	Logic Input	Logic high commands 1 phase upper FET to turn on
19	V_{DD}	Power	Logic Supply (5V)
21	I1	Analog Output	Phase 1 current sense output
23	DIS2	Logic Input	Logic high places all outputs in a high impedance state

TABLE 1. PIN DESCRIPTIONS			
Pin #	**Pin Name**	**Signal Type**	**Simplified Pin Description**
25	TEMP	Logic Output	Thermal indication of die temperature above 135ºC
46,47,48,49	V_S (phase 2)	Power	High Voltage Supply phase 2
33,34,35	OUT 1	Power Output	Half Bridge 1 Power Output
37,38,39,40	PGND (phase 1)	Power	High Current GND Return Path for Power Outputs 1&2
26,27,58,59	HS	Mechanical	Pins connected to the package heat slug
2,4,6,8,10, 12,14,16,18, 20,22,24,28, 32,36,41,42, 43,44,45,50, 54,60,62,64	NC	---	Do Not Connect

1.2 PIN DESCRIPTIONS

V_S: Supply voltage for the output transistors. These pins require decoupling (1µF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V_S and PGND pins as possible. Additional capacitance will be required at the V_S pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that Vs pins 29-31 carry only the phase 1 supply current. Pins 46-49 carry supply current for phase2. Phase 1 may be operated at a different supply voltage from phase 2. Only the B & C supply pins (46-49) are monitored for undervoltage conditions.

OUT 1, OUT 2: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t_{RR} specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs. (See Section 2.6)

PGND: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

SC: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor.

1b, 2b: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If 1b or 2b is high at the same time that a corresponding 1t or 2t input is high, protection circuitry will turn off both FETs in order to prevent shoot-through current on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

1t, 2t: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

I1, I2: Current sense pins. The SA57 supplies a positive current to these pins which is proportional to the current flowing through the top side P-channel FET for that phase. Commutating currents flowing through the back-body diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.
The current sense pins are also internally compared with the current limit threshold voltage reference, Vth. If the voltage on any current sense pin exceeds Vth, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

I_{LIM}/DIS1: This pin is directly connected to the disable circuitry of the SA57. Pulling this pin to logic high places OUT 1 and OUT 2 in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

SGND: This is the ground return connection for the V_{DD} logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms,. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

V_{DD}: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA57. This pin requires decoupling (at least 0.1µF capacitor with good high frequency characteristics is recommended) to the SGND pin.

DIS2: The DIS2 pin is a Schmitt triggered logic level input that places OUT 1 and OUT 2 in a high impedance state when pulled high. DIS2 has an internal 12kΩ pull-down resistor and may therefore be left unconnected.

TEMP: This logic level output goes high when the die temperature of the SA57 reaches approximately 135ºC. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor.

HS: These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

NC: These “no-connect” pins should be left unconnected.

2. SA57 OPERATION

The SA57 is designed primarily to drive DC brush motors. However, it can be used for any application requiring two high current outputs. The signal set of the SA57 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for both phases provide performance information which can be used to regulate or limit torque.

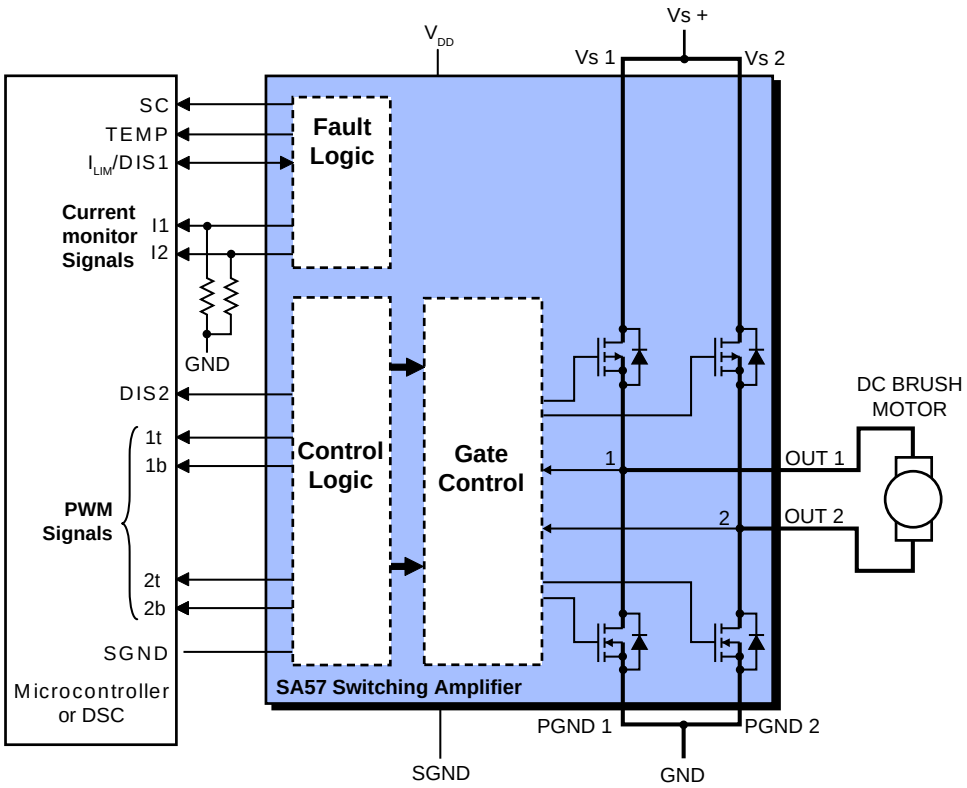


Figure 4. System Diagram

The block diagram in Figure 5 illustrates the features of the input and output structures of the SA57. For simplicity, a single phase is shown.

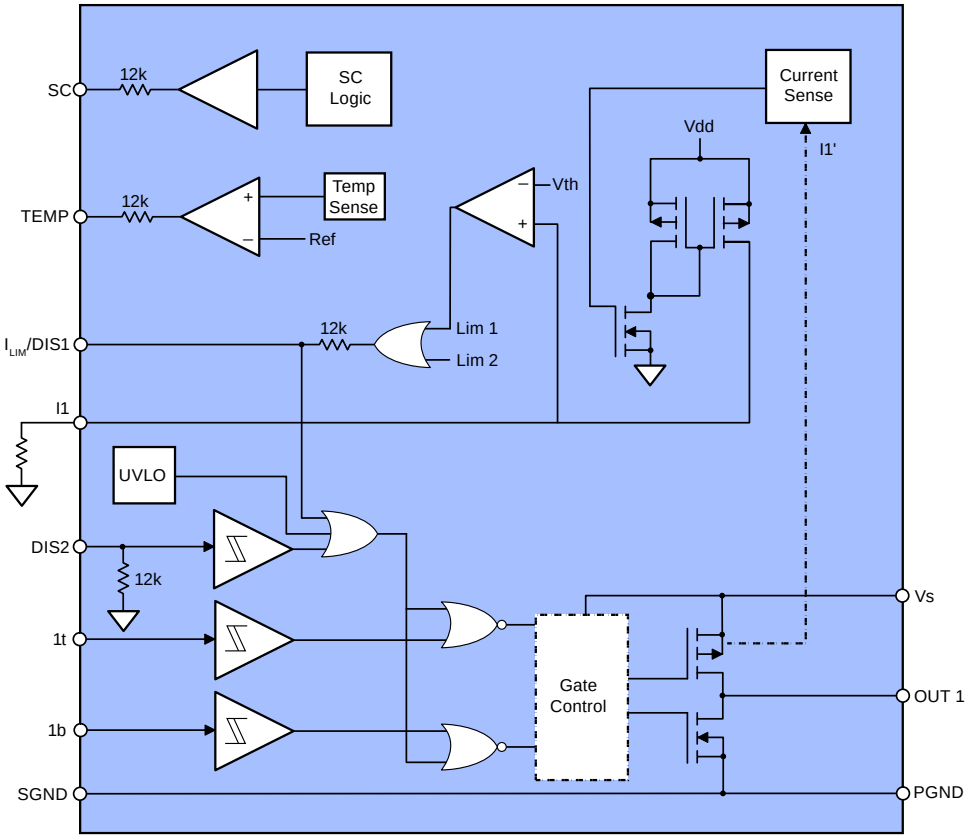


Figure 5. Input and output structures for a single phase

TABLE 2. TRUTH TABLE

1t, 2t	1b, 2b	I1, I2	I_{LIM}/DIS1	DIS2	OUT 1 OUT 2	Comments
0	0	X	X	X	High-Z	Top and Bottom output FETs for that phase are turned off.
0	1	<V_{th}	0	0	PGND	Bottom output FET for that phase is turned on.
1	0	<V_{th}	0	0	VS	Top output FET for that phase is turned on.
1	1	X	X	X	High-Z	Both output FETs for that phase are turned off.
X	X	>V_{th}	1	X	High-Z	Voltage on I1 or I2 has exceeded Vth, which causes I_{LIM}/DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases.
X	X	X	X	1	High-Z	DIS2 pin pulled high, which disables all outputs.
X	X	X	Pulled High	X	High-Z	Pulling the I_{LIM}/DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.
X	X	X	Pulled Low	0	Determined by PWM inputs	Pulling the DIS2 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.
X	X	X	X	X	High-Z	If V_S is below the UVLO threshold all output FETs will be disabled.

2.1 LAYOUT CONSIDERATIONS

Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25µF per ampere of output current should be placed near the SA57 as well. Capacitor types rated for switching applications are the only types that should be considered.

The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1µF to 0.47µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

2.2 FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA57 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA57.

Figure 6 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

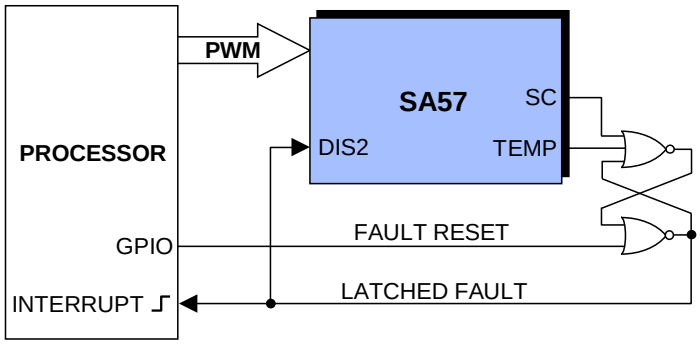


Figure 6. External Fault Latch Circuit

In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA57 will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

2.3 UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA57 unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lockout condition is in progress. The SA57 has two V_S connections: one for phase 1 and another for phase 2. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

2.4 CURRENT SENSE

External power shunt resistors are not required with the SA57. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, I1 and I2. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the V_{DD} supply. Headroom required for the current sense circuit is approximately 0.5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 4 of this datasheet.

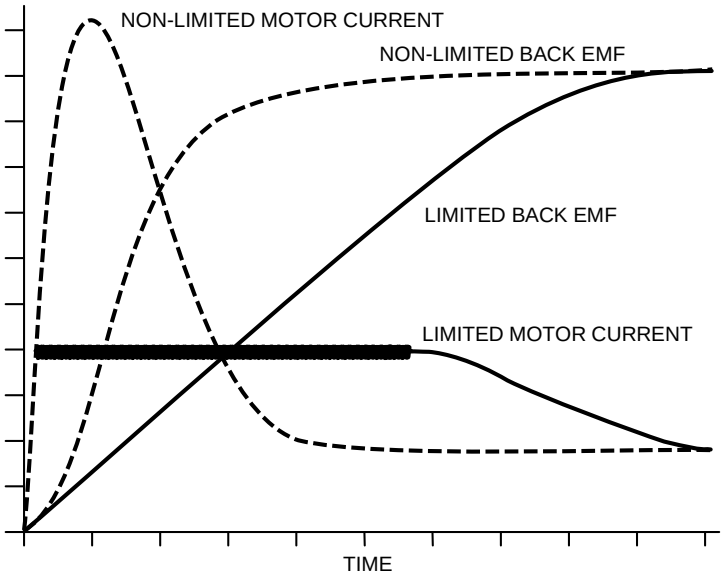


Figure 7. Start-up Voltage and Current

2.5 CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at start-up.

Because the output current of each upper output FET is measured, the SA57 is able to provide a very robust current limit scheme. This enables the SA57 to safely and easily drive virtually any DC brush motor through a start-up inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 7 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the two current sense pins exceeds the current limit threshold voltage (Vth), all outputs are disabled. After all current sense pins fall below the Vth threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (1t or 2t). With most commutation schemes, the current limit will reset each PWM cycle. This scheme regulates the peak current in each phase during each PWM cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

Figure 8 illustrates the current limit trigger and reset sequence. Current limit engages and I_{LIM}/DIS1 goes high when any current sense pin exceeds Vth. Notice that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will

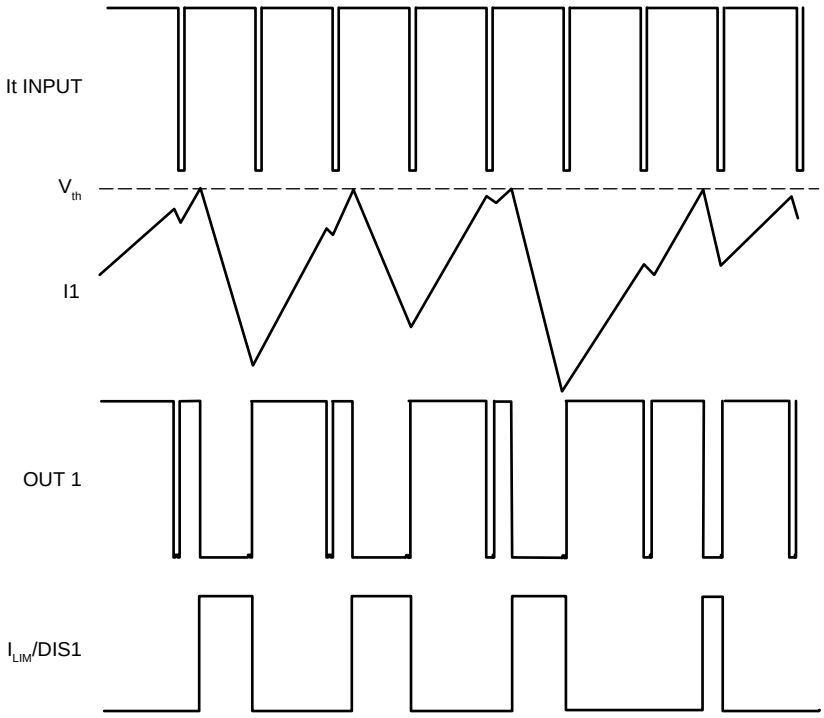


Figure 8. Current Limit Waveforms

often result in an audible beat frequency sometimes called a sub-cycle oscillation. This oscillation can be seen on the I_{LIM}/DIS1 pin waveform in Figure 8.

Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of 1t and 2t. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

The current limit feature may be disabled by tying the I_{LIM}/DIS1 pin to GND. The current sense pins will continue to provide top FET output current information.

Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

2.6 EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

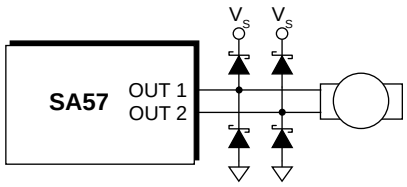


Figure 9. Schottky Diodes

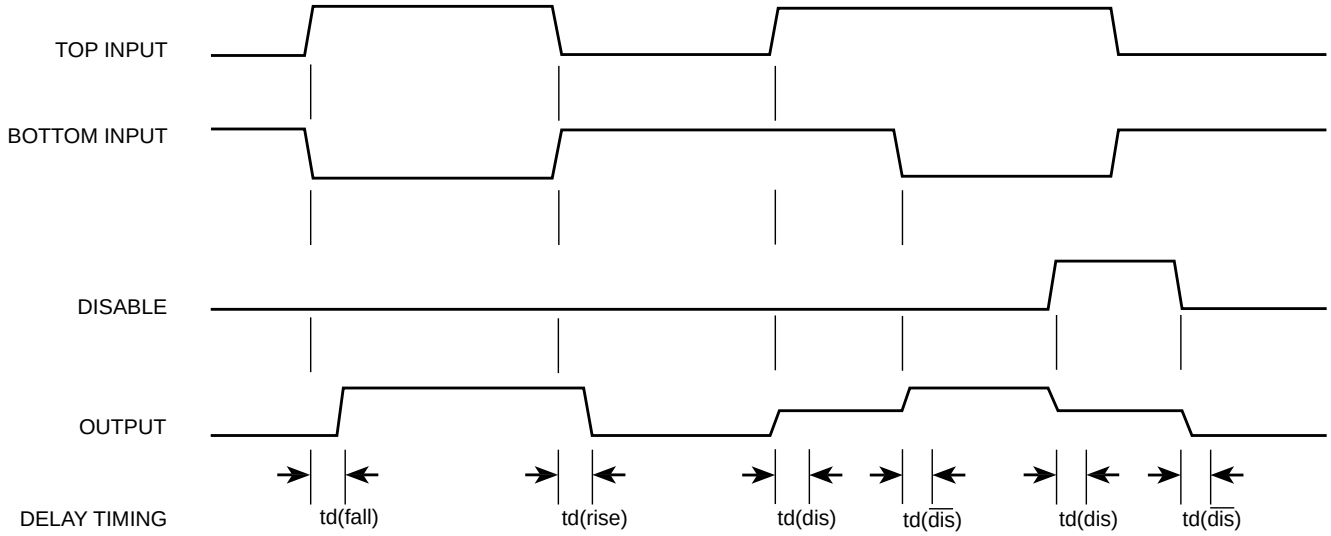


Figure 10. Timing Diagrams

3. POWER DISSIPATION

The thermally enhanced package of the SA57 allows several options for managing the power dissipated in the two output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents. Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA57. Applications vary widely and various thermal techniques are available to match the required performance. The pat-

ent pending mounting technique shown in Figure 12, with the SA57 inverted and suspended through a cutout in the PCB is adequate for power dissipation up to 17W with the HS33, a 1.5 inch long aluminum extrusion with four fins. In free air, mounting the PCB perpendicular to the ground, such that the heated air flows upward along the channels of the fins can provide a total Θ_{JA} of less than 14 ºC/W (9W max average P_D). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a Θ_{JA} of 16.66 ºC/W (7.5W max average P_D). In applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance.

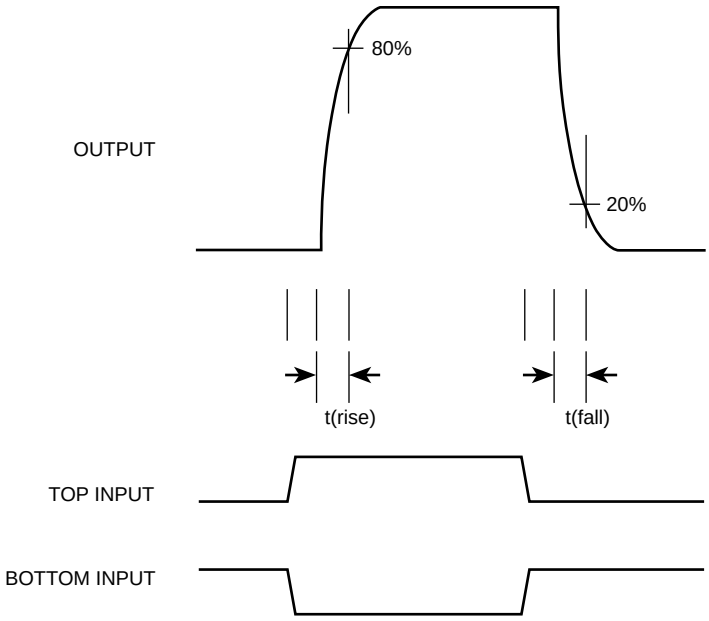


Figure 11. Output Response

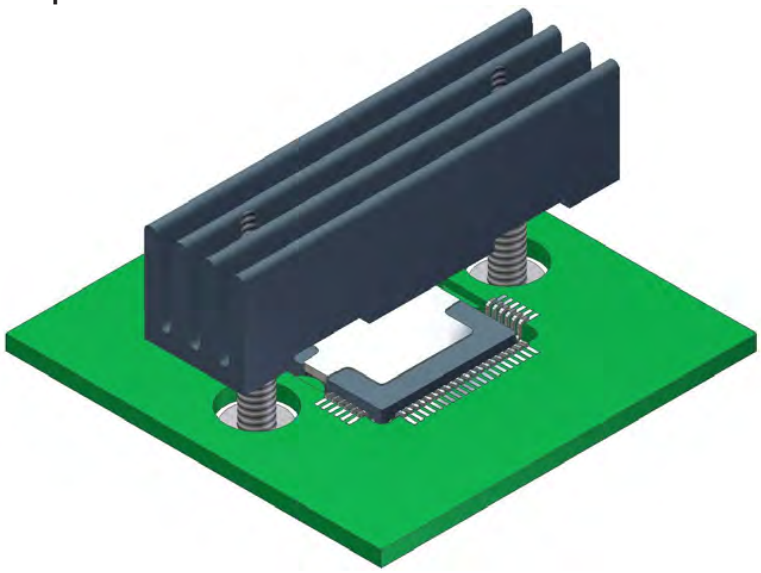
D

4. ORDERING AND PRODUCT STATUS INFORMATION

MODEL	TEMPERATURE	PACKAGE	PRODUCTION STATUS
SA57-IHZ	-25 to 85ºC	64 pin Power QFP (HQ package drawing)	Samples Available
SA57A-FHZ	-40 to +125ºC	64 pin Power QFP (HQ package drawing)	Samples Available

Figure 12. Heatsink Technique

PATENT PENDING



SA60

H-Bridge Motor Driver/Amplifiers

RoHS COMPLIANT

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/ HIGHSIDE DRIVE CIRCUITRY
- WIDE SUPPLY RANGE: UP TO 80V
- 10A CONTINUOUS OUTPUT
- ISOLATED CASE ALLOWS DIRECT HEATSINKING
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL/PROGRAMMABLE PWM FREQUENCY GENERATION

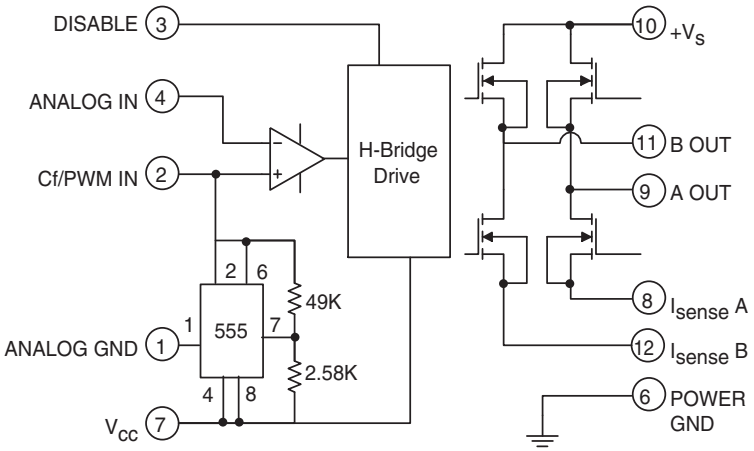
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

DESCRIPTION

The SA60 is a pulse width modulation amplifier that can supply 10A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed/direction, or audio signal for switchmode audio amplification. The internal PWM frequency can be programmed by an external integrator capacitor. Alternatively, the user may provide an external TTL-compatible PWM signal for simultaneous amplitude and direction control for four quadrant mode.

BLOCK DIAGRAM



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ (Note 4)			80	V
OUTPUT CURRENT, peak			15	A
LOGIC SUPPLY VOLTAGE, V_{CC}			16	V
POWER DISSIPATION, internal (Note 3)			156	W
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The SA60 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

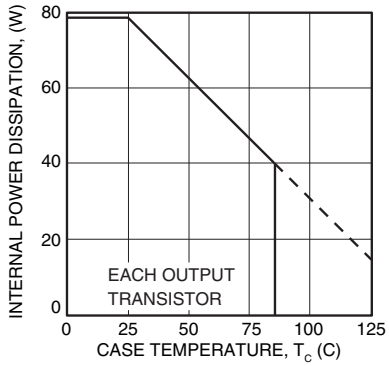
SPECIFICATIONS

Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
ANALOG INPUT VOLTAGES	V_{CC} = 12V				
A,B OUT = 50% Duty Cycle			1/2 V_{CC}		VDC
A OUT = 100% Duty Cycle High			1/3 V_{CC}		VDC
B OUT = 100% Duty Cycle High			2/3 V_{CC}		VDC
PWM INPUT					
PWM PULSE LOW VOLTAGE		0		0.8	VDC
PWM PULSE HIGH VOLTAGE		2.7		5.0	VDC
PWM FREQUENCY			45	250	KHz
DISABLE ON		2.7		V_{CC}	VDC
DISABLE OFF		0		0.8	VDC
OUTPUT					
V_{DS} (ON) VOLTAGE, each MOSFET	I_{DS} = 10A		1.7	2.5	VDC
TOTAL R_{ON}, both MOSFETs				0.45	Ω
EFFICIENCY, 10A OUTPUT	$+V_S$ = 80A		91		%
CURRENT, continuous		10			A
CURRENT, peak	t = 100 msec	15			A
SWITCHING FREQUENCY	C_F = 270pF		45		KHz
DEAD TIME			90		nS
POWER SUPPLY					
$+V_S$ VOLTAGE (Note 4)	$+V_S$ Current = Load Current			80	VDC
V_{CC} VOLTAGE		9.5	12	15	VDC
V_{CC} CURRENT	V_{CC} = 12VDC		28	36	mA
$+V_S$ CURRENT	Switching, no load, V_S = 50V		5		mA

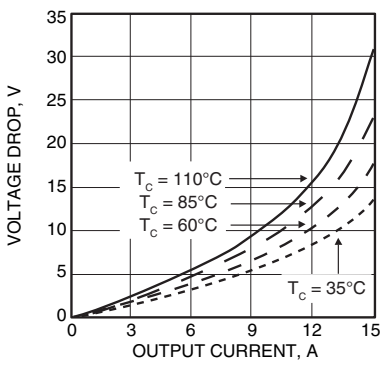
Parameter	Test Conditions[1]	Min	Typ	Max	Units
THERMAL (Note 3)					
RESISTANCE, junction to case	Full temperature range, for each transistor			1.6	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		-25		+85	°C

NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C, V_{CC} = 12VDC).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Each of the two active output transistors can dissipate 78W.
4. Derate to 70V below T_C = +25°C.

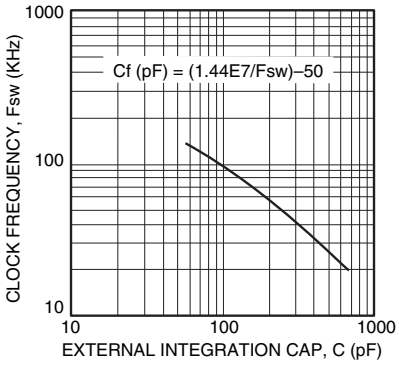
POWER DERATING



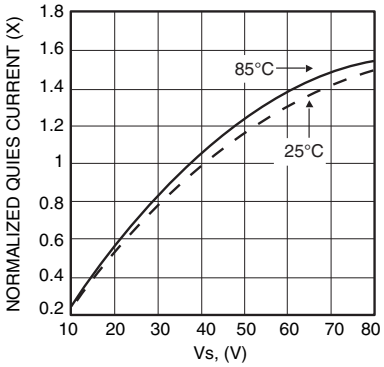
TOTAL VOLTAGE DROP



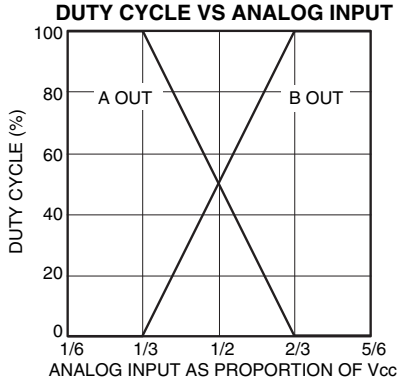
PWM FREQ VS EXT INT CAP



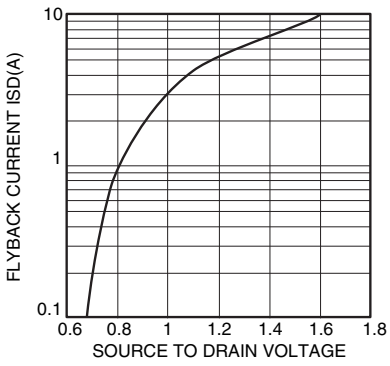
Vs QUIESCENT VS VOLTAGE



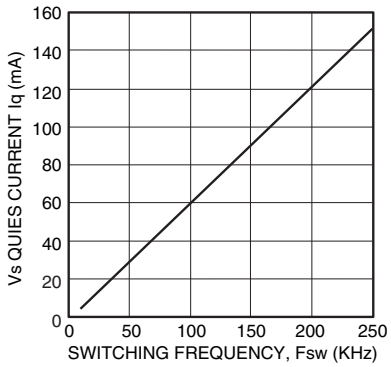
DUTY CYCLE VS ANALOG INPUT



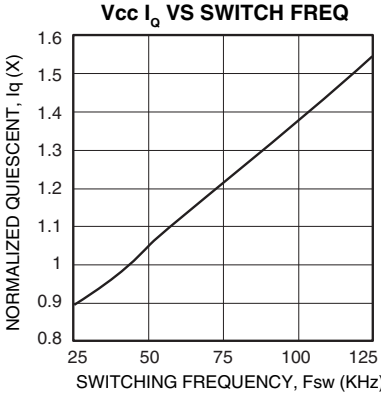
REVERSE DIODES



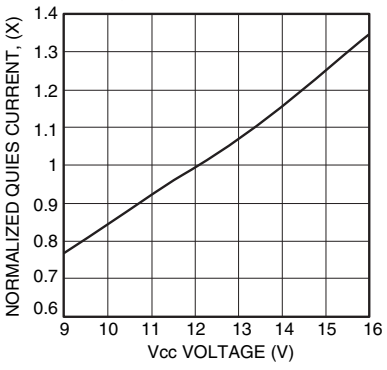
Vs QUIESCENT VS SWITCH FREQ



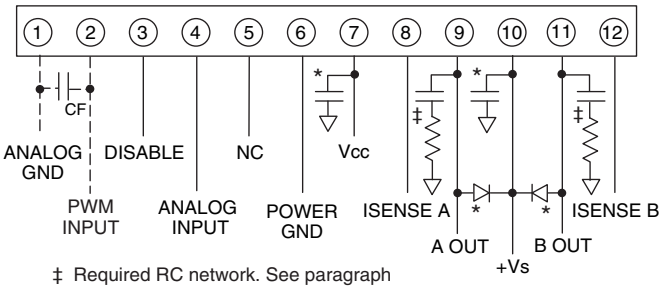
Vcc I_Q VS SWITCH FREQ



Vcc QUIESCENT VS VOLTAGE



EXTERNAL CONNECTIONS



‡ Required RC network. See paragraph on transient shutdown.

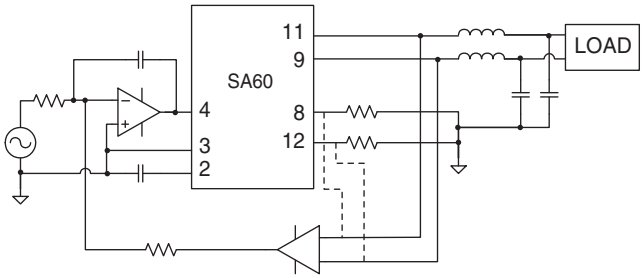
* Protection diodes are recommended for applications where +Vs exceeds 50V.

12-pin Power SIP
PACKAGE
STYLE DP

Formed Leads Available
See package style EE

TYPICAL APPLICATION

A wide variety of loads can be driven in either the voltage mode or the current mode. The most common applications use three external blocks: a low pass filter converting pulse width data to an analog output, a difference amplifier to monitor voltage or current and an error amplifier. Filter inductors must be suitable for square waves at the switching frequency (laminated steel is generally not acceptable). Filter capacitors must be low ESR and rated for the expected ripple current. A difference amplifier with gain of less than one translates the differential output voltage to a single feedback voltage. Dashed line connections and a higher gain difference amplifier would be used for current control. The error amplifier integrates the difference between the input and feedback voltages to close the loop.



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

PWM OSCILLATOR – INTERNAL OR EXTERNAL

The SA60 contains an internal PWM oscillator whose frequency is determined by an external capacitor connected between pin 1 and pin 2. Maximum frequency is 125 kHz. The user may also disregard the internal PWM oscillator and supply the SA60 with an external TTL pulse generator up to 250KHZ.

PIN DESCRIPTION

V_{cc} - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts.

ISENSE A & B - These are tied to power gnd directly or through sense resistors.

ANALOG GND - is the reference for the internal PWM oscillator. Connect this pin to pin 6. Connect low side of Vcc supply and any other supply used to generate analog input signals to ANALOG GND.

ANALOG INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than Vcc/2 will produce greater than 50% duty cycle pulses out of B OUT. A voltage lower than Vcc/2 will produce greater than 50% duty cycle pulses out of A OUT. If using in the digital mode, bias this point at 1/2 the logic high level.

DISABLE - Is the connection for disabling all 4 output switches. DISABLE high overrides all other inputs. When taken low, everything functions normally. An internal pullup to Vcc will keep DISABLE high if pin left open.

PWM INPUT - Is the TTL compatible digital input for controlling the PWM pulse width of the bridge. A duty cycle greater than 50% will produce greater than 50% duty cycle pulses out of the A out. A duty cycle less than 50% will produce greater than 50% duty cycle from the B out. For analog inputs, the integration capacitor for the internal clock must be connected between this pin and analog ground. The internal switching frequency is programmable up to 125 kHz by selection of the integration capacitor. The formula is:

$$C_F\,(pF) = \left(\frac{1.44 \times 10^7}{Fsw}\right) - 50$$

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The 1µF ceramic capacitor must be physically connected directly to the Vs and POWER GND pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc and ANALOG GND pins will suffice.

PCB LAYOUT

The designer needs to appreciate that the SA60 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA60:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Connect ANALOG GND to POWER GND with a conductor having no intermediate connections. Connect all Vs power supply, filter and load related ground connections to POWER GND keeping these conductors separate until reaching pin 6. Connect all Vcc power supply and input signal related ground connections to ANALOG GND keeping conductors separate until reaching pin 1. Do not allow ground loops to form by making additional ground connections at the low side of the physical power supplies. If ground plane is used do not allow more than 1mA to flow through it.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 8-12).

CURRENT SENSE

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted to POWER GND in the voltage mode connection but both must be used in the current mode connection. It is recommended that R SENSE resistors be non-inductive. Load current flows in the I SENSE pins. The SA60 has no internal current limit.

TRANSIENT SUPPRESSION

An RC network of a 100 pF Capacitor and a one ohm resistor is required as shown in the external connection diagram on page 1. This network assures proper operation under various loads. Minimal power is dissipated in the resistor.

3 Phase Switching Amplifier

RoHS COMPLIANT

FEATURES

- Low Cost 3 Phase Intelligent Switching Amplifier
- Directly Connects to Most Embedded Micro-controllers and Digital Signal Controllers
- Integrated Gate Driver Logic with Dead-Time Generation and Shoot-through Prevention
- Wide Power Supply Range (8.5V To 60V)
- Over 10A Peak Output Current per Phase
- 3A Continuous Output Current per Phase
- Independent Current Sensing for each Output
- User Programmable Cycle-by-cycle Current Limit Protection
- Over-Current and Over-Temperature Warning Signals

APPLICATIONS

- 3 phase brushless DC motors
- Multiple DC brush motors
- 3 independent solenoid actuators

DESCRIPTION

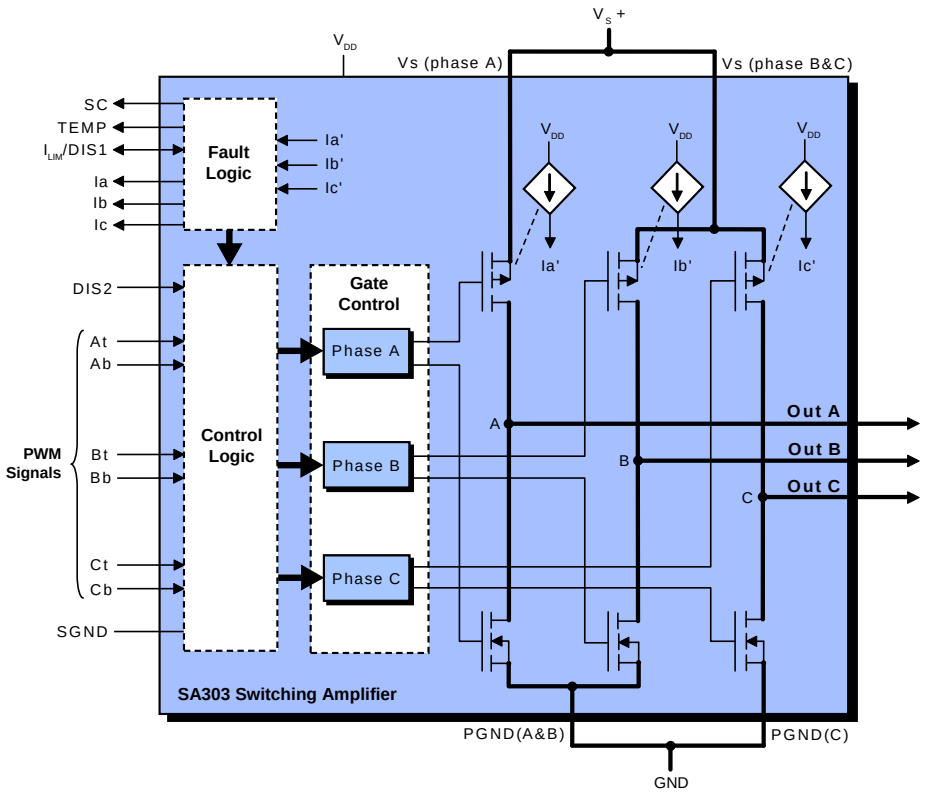
The SA303 is a fully integrated switching amplifier designed primarily to drive three-phase Brushless DC (BLDC) motors. Three independent half bridges provide over 10 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram is provided in Figure 1.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA303 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

The Power Quad surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

D

Figure 1. BLOCK Diagram



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_S		60	V
SUPPLY VOLTAGE	V_{DD}		5.5	V
LOGIC INPUT VOLTAGE		(-0.5)	(V_{DD}+0.5)	V
OUTPUT CURRENT, peak, 10ms (Note 2)	I_{OUT}		10	A
POWER DISSIPATION, avg, 25ºC (Note 2)	P_D		100	W
TEMPERATURE, solder, 10sec	T_S		260	°C
TEMPERATURE, junction (Note 2)	T_J		150	°C
TEMPERATURE RANGE, storage	T_{STG}	−55	125	°C
OPERATING TEMPERATURE, case	T_A	−40	125	°C

SPECIFICATIONS

Parameter	Test Conditions (Note 1)	Min	Typ	Max	Units
LOGIC					
INPUT LOW				1	V
INPUT HIGH		1.8			V
OUTPUT LOW				0.3	V
OUTPUT HIGH		3.7			V
OUTPUT CURRENT (SC, Temp, I_{LIM}/DIS1)			50		mA
POWER SUPPLY					
V_S		UVLO	50	60	V
V_S UNDERVOLTAGE LOCKOUT, (UVLO)			8.3		V
V_{DD}		4.5		5.5	V
SUPPLY CURRENT, V_S	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		25	30	mA
SUPPLY CURRENT, V_{DD}	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		5	6	mA
CURRENT LIMIT					
CURRENT LIMIT THRESHOLD (Vth)			3.75		V
Vth HYSTERESIS			100		mV
OUTPUT					
CURRENT, CONTINUOUS	25ºC Case Temperature	3			A
RISING DELAY, TD(RISE)	See Figure 10		270		ns
FALLING DELAY, TD(FALL)	See Figure 10		270		ns
DISABLE DELAY, TD(DIS)	See Figure 10		200		ns
ENABLE DELAY, TD($\overline{DIS}$)	See Figure 11		200		ns
RISE TIME, T(RISE)	See Figure 11		50		ns
FALL TIME, T(FALL)			50		ns
ON RESISTANCE SOURCING (P-CHANNEL)	3A Load		400		mΩ
ON RESISTANCE SINKING (N-CHANNEL)	3A Load		400		mΩ

SPECIFICATIONS, continued

Parameter	Test Conditions (Note 1)	Min	Typ	Max	Units
THERMAL					
THERMAL WARNING			135		ºC
THERMAL WARNING HYSTERESIS			40		ºC/W
RESISTANCE, junction to case	Full temperature range		1.25	1.5	ºC/W
TEMPERATURE RANGE, case	Meets Specifications	-40		85	ºC

NOTES:

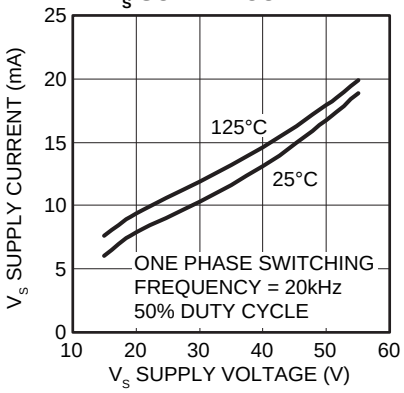
* The specification of SA303A is identical to the specification for SA303 in applicable column to the left.

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.
3. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

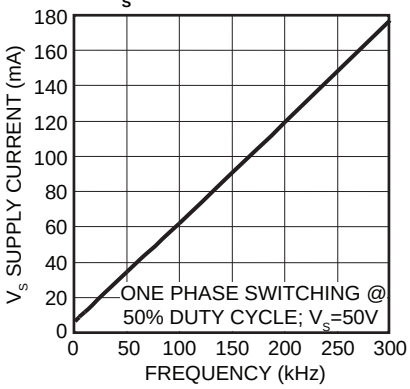
D

Figure 2. 64-Pin QFP, Package Style HQ

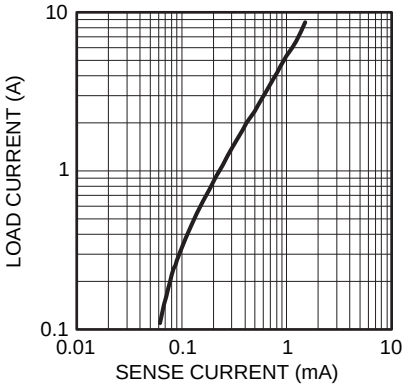
V_S SUPPLY CURRENT



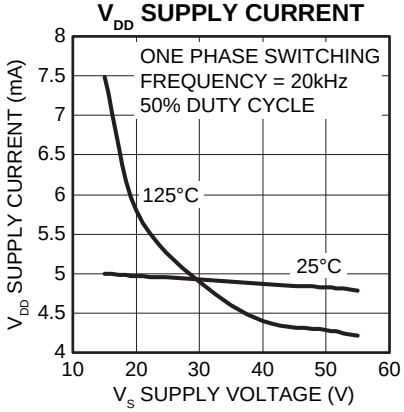
V_S SUPPLY CURRENT



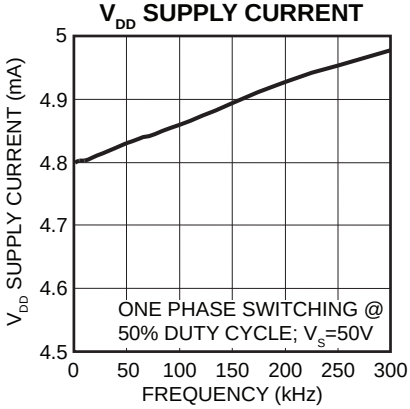
CURRENT SENSE



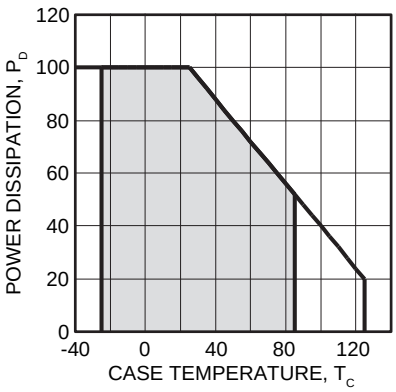
V_{DD} SUPPLY CURRENT



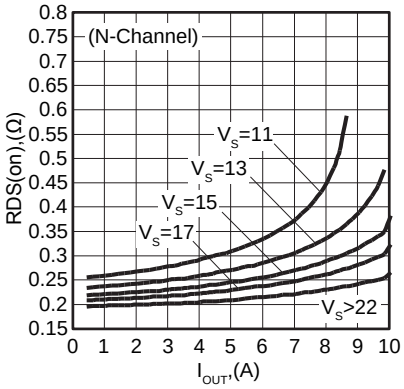
V_{DD} SUPPLY CURRENT



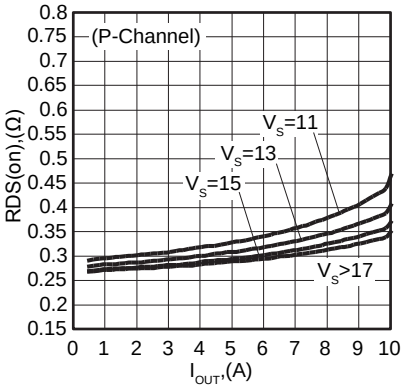
POWER DERATING



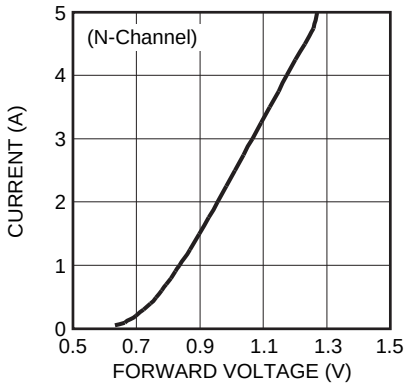
ON RESISTANCE - BOTTOM FET



ON RESISTANCE - TOP FET



DIODE FORWARD VOLTAGE - BOTTOM FET



DIODE FORWARD VOLTAGE - TOP FET

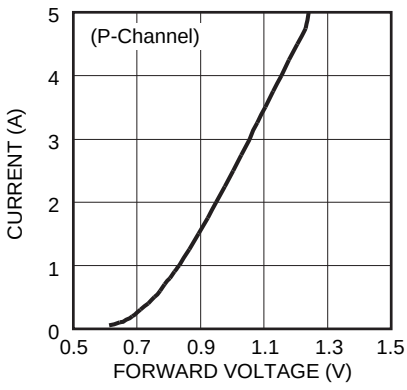


Figure 3. External Connections

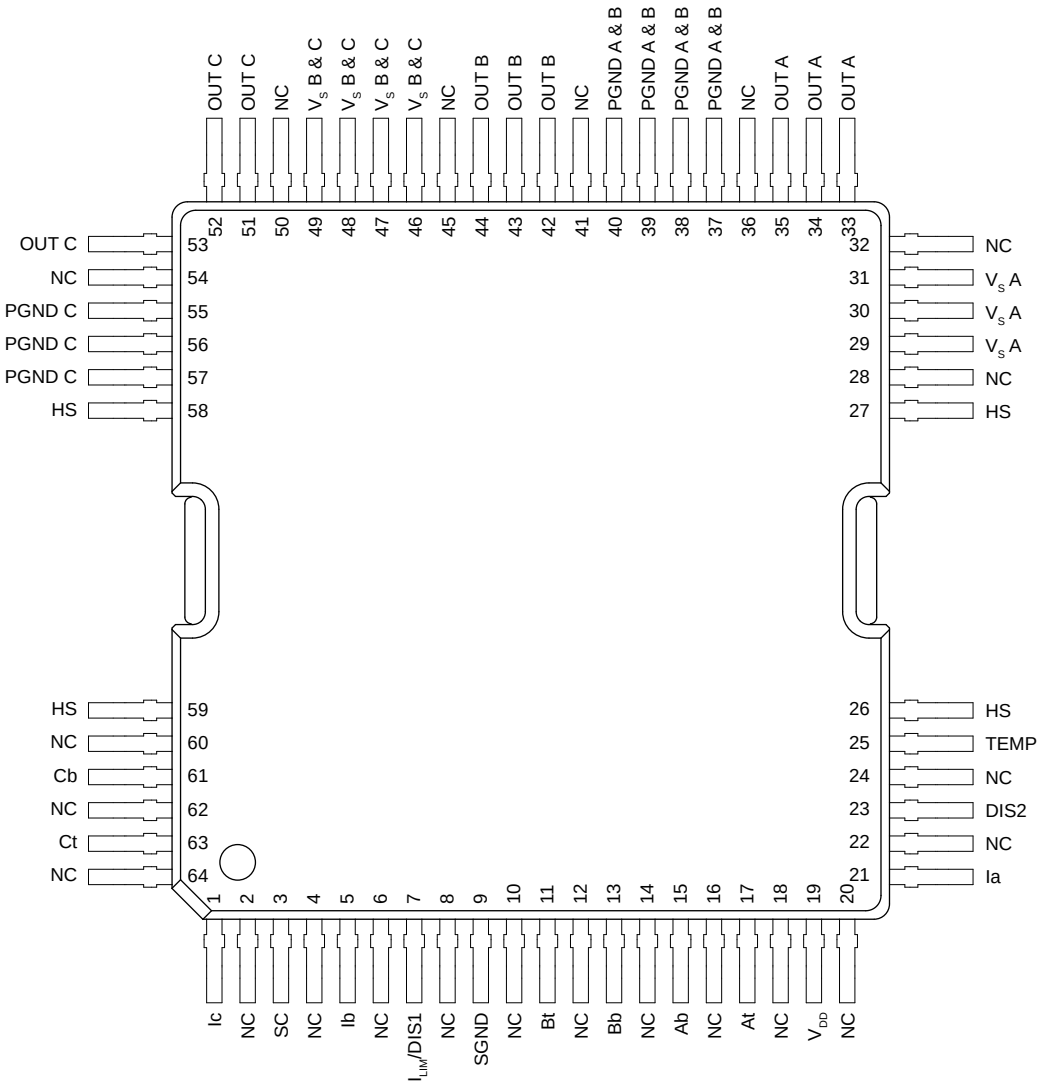


Table 1. Pin Descriptions

Pin #	Pin Name	Signal Type	Simplified Pin Description
29,30,31	V_S (phase A)	Power	High Voltage Supply (8.5-60V) supplies phase A only
51,52,53	OUT C	Power Output	Half Bridge C Power Output
55,56,57	PGND (phase C)	Power	High Current GND Return Path for Power Output C
3	SC	Logic Output	Indication of a short of an output to supply, GND or another phase
61	Cb	Logic Input	Logic high commands C phase lower FET to turn on
63	Ct	Logic Input	Logic high commands C phase upper FET to turn on
1	Ic	Analog Output	Phase C current sense output
5	Ib	Analog Output	Phase B current sense output
7	I_{LIM}/DIS1	Logic Input/Output	As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function.

TABLE 1. PIN DESCRIPTIONS - Cont.

Pin #	Pin Name	Signal Type	Simplified Pin Description
9	SGND	Power	Analog and digital GND – internally connected to PGND
11	Bt	Logic Input	Logic high commands B phase upper FET to turn on
13	Bb	Logic Input	Logic high commands B phase lower FET to turn on
15	Ab	Logic Input	Logic high commands A phase lower FET to turn on
17	At	Logic Input	Logic high commands A phase upper FET to turn on
19	V_{DD}	Power	Logic Supply (5V)
21	Ia	Analog Output	Phase A current sense output
23	DIS2	Logic Input	Logic high places all outputs in a high impedance state
25	TEMP	Logic Output	Thermal indication of die temperature above 135ºC
42,43,44	OUT B	Power Output	Half Bridge B Power Output
46,47,48,49	V_S (phase B&C)	Power	High Voltage Supply phase B&C
33,34,35	OUT A	Power Output	Half Bridge A Power Output
37,38,39,40	PGND (phase A&B)	Power	High Current GND Return Path for Power Outputs A&B
26,27,58,59	HS	Mechanical	Pins connected to the package heat slug
2,4,6,8,10, 12,14,16,18, 20,22,24,28, 32,36,41,45, 50,54,60,62, 64	NC	---	Do Not Connect

1.2 Pin Descriptions

V_S: Supply voltage for the output transistors. These pins require decoupling (1µF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V_S and PGND pins as possible. Additional capacitance will be required at the V_S pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that V_S pins 29-31 carry only the phase A supply current. Pins 46-49 carry supply current for phases B & C. Phase A may be operated at a different supply voltage from phases B & C. Both V_S voltages are monitored for undervoltage conditions.

OUT A, OUT B, OUT C: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t_{RR} specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs. (See Section 2.6)

PGND: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

SC: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor.

Ab, Bb, Cb: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If Ab, Bb, or Cb is high at the same time that a corresponding At, Bt, or Ct input is high, protection circuitry will turn off both FETs in order to prevent shoot-through on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

At, Bt, Ct: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

Ia, Ib, Ic: Current sense pins. The SA303 supplies a positive current to these pins which is proportional to the current flowing through the top side P-channel FET for that phase. Commutating currents flowing through the backbody diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.
The current sense pins are also internally compared with the current limit threshold voltage reference, Vth. If the voltage on any current sense pin exceeds Vth, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

I_{LIM}/DIS1: This pin is directly connected to the disable circuitry of the SA303. Pulling this pin to logic high places OUT A, OUT B, and OUT C in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

SGND: This is the ground return connection for the V_{DD} logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms,. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

VDD: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA303. This pin requires decoupling (at least 0.1µF capacitor with good high frequency characteristics is recommended) to the SGND pin.

DIS2: The DIS2 pin is a Schmitt triggered logic level input that places OUT A, OUT B, and OUT C in a high impedance state when pulled high. DIS2 has an internal 12kΩ pull-down resistor and may therefore be left unconnected.

TEMP: This logic level output goes high when the die temperature of the SA303 reaches approximately 135ºC. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor.

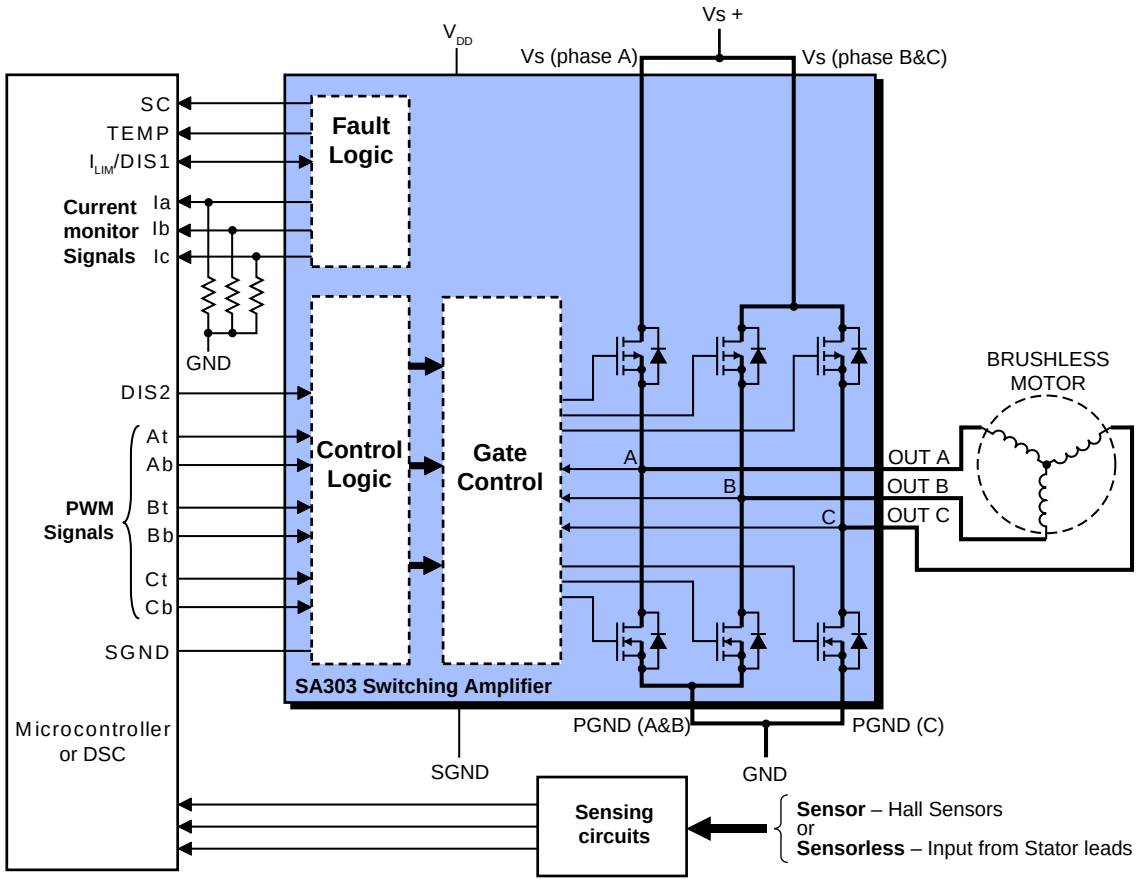
HS: These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

NC: These “no-connect” pins should be left unconnected.

2. SA303 OPERATION

The SA303 is designed primarily to drive three phase motors. However, it can be used for any application requiring three high current outputs. The signal set of the SA303 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for all three phases provide performance information which can be used to regulate or limit torque.

Figure 4. System Diagram



The block diagram in Figure 5 illustrates the features of the input and output structures of the SA303. For simplicity, a single phase is shown.

Figure 5. Input and output structures for a single phase

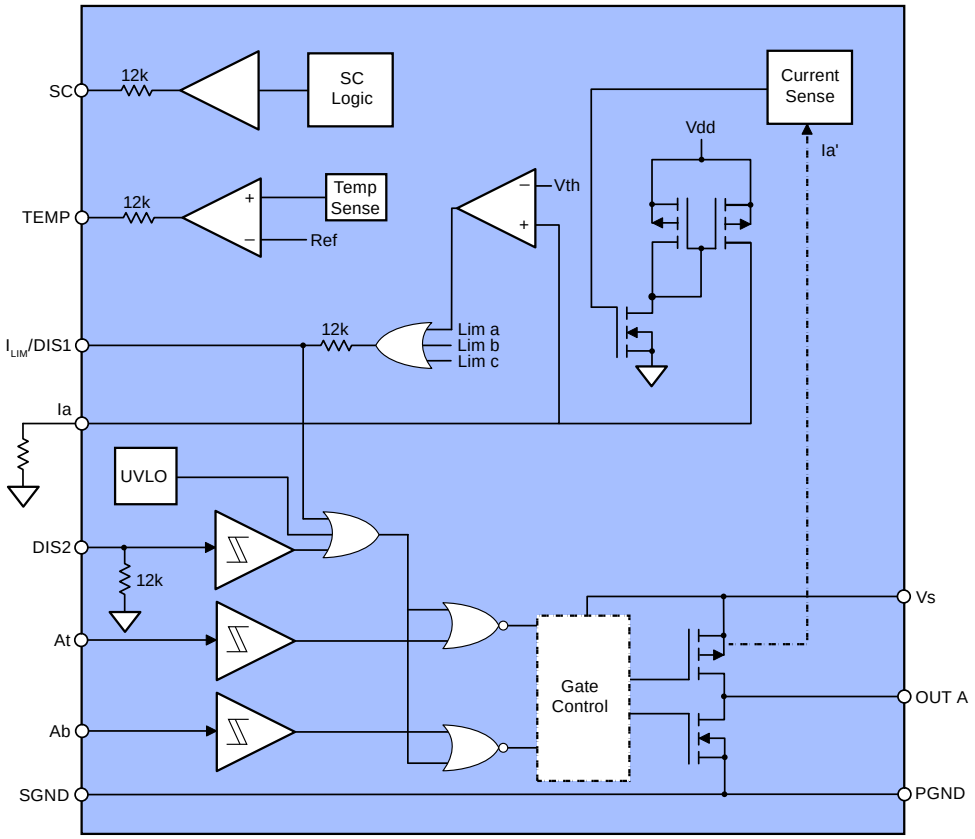


TABLE 2. Truth Table

At, Bt, Ct	Ab, Bb, Cb	Ia, Ib, Ic	I_{LIM}/DIS1	DIS2	OUT A, OUT B, OUT C	Comments
0	0	X	X	X	High-Z	Top and Bottom output FETs for that phase are turned off.
0	1	$<V_{th}$	0	0	PGND	Bottom output FET for that phase is turned on.
1	0	$<V_{th}$	0	0	VS	Top output FET for that phase is turned on.
1	1	X	X	X	High-Z	Both output FETs for that phase are turned off.
X	X	$>V_{th}$	1	X	High-Z	Voltage on Ia, Ib, or Ic has exceeded Vth, which causes I_{LIM}/DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases.
X	X	X	X	1	High-Z	DIS2 pin pulled high, which disables all outputs.
X	X	X	Pulled High	X	High-Z	Pulling the I_{LIM}/DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.
X	X	X	Pulled Low	0	Determined by PWM inputs	Pulling the DIS2 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.
X	X	X	X	X	High-Z	If V_S is below the UVLO threshold all output FETs will be disabled.

2.1 LAYOUT CONSIDERATIONS

Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the VS pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25µF per ampere of output current should be placed near the SA303 as well. Capacitor types rated for switching applications are the only types that should be considered. Note that phases B & C share a V_S connection and the bypass recommendation should reflect the sum of B & C phase current.

The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1µF to 0.47µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

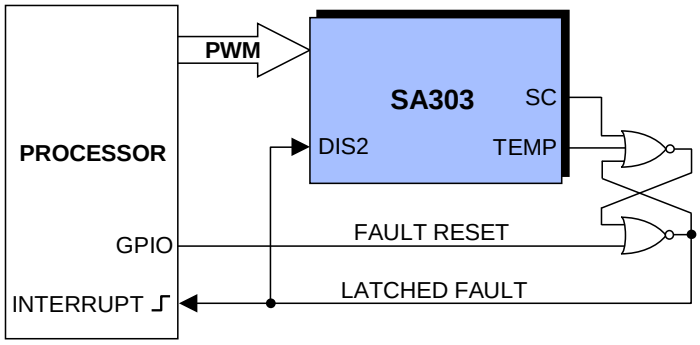
Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

2.2 FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA303 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA303.

Figure 6 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

Figure 6. External Fault Latch Circuit



In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA303 will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

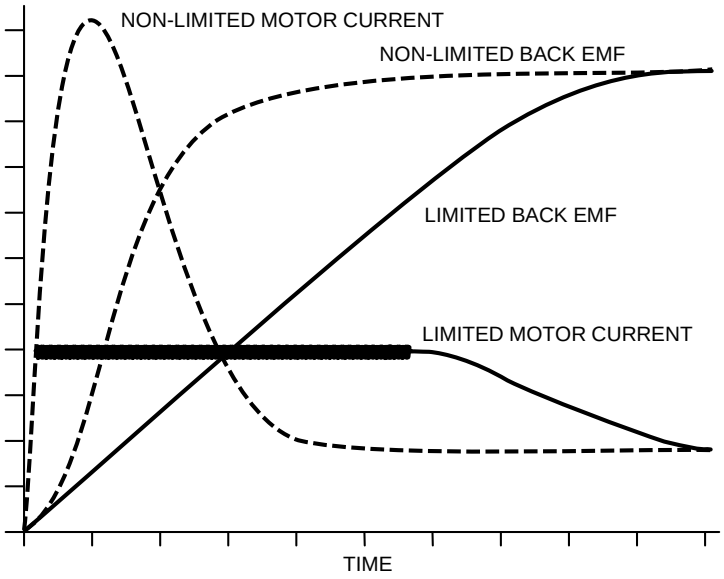
2.3 UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA303 unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lock out condition is in progress. The SA303 has two VS connections: one for phase A, and another for phases B & C. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

2.4 CURRENT SENSE

External power shunt resistors are not required with the SA303. Forward current in each top, Pchannel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the VDD supply. Headroom required for the current sense circuit is approximately .5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 4 of this datasheet.

Figure 7. Start-up Voltage and Current



2.5 CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at startup.

Because the output current of each upper output FET is measured, the SA303 is able to provide a very robust current limit scheme. This enables the SA303 to safely and easily drive virtually any brushless motor through a startup inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 7 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the three current sense pins exceeds the current limit threshold voltage (Vth), all outputs are disabled. After all current sense pins fall below the Vth threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (At, Bt, or Ct). With most commutation schemes, the current limit will reset each pwm cycle. This scheme regulates the peak current in each phase during each pwm cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

Figure 8 illustrates the current limit trigger and reset sequence. Current limit engages and I_{LIM}/DIS1 goes high when any current sense pin exceeds Vth. Notice that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a sub-cycle oscillation.

This oscillation can be seen on the I_{LIM}/DIS1 pin waveform in Figure 8. Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of At, Bt, and Ct except when commutating phases. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

The current limit feature may be disabled by tying the I_{LIM}/DIS1 pin to GND. The current sense pins will continue to provide top FET output current information.

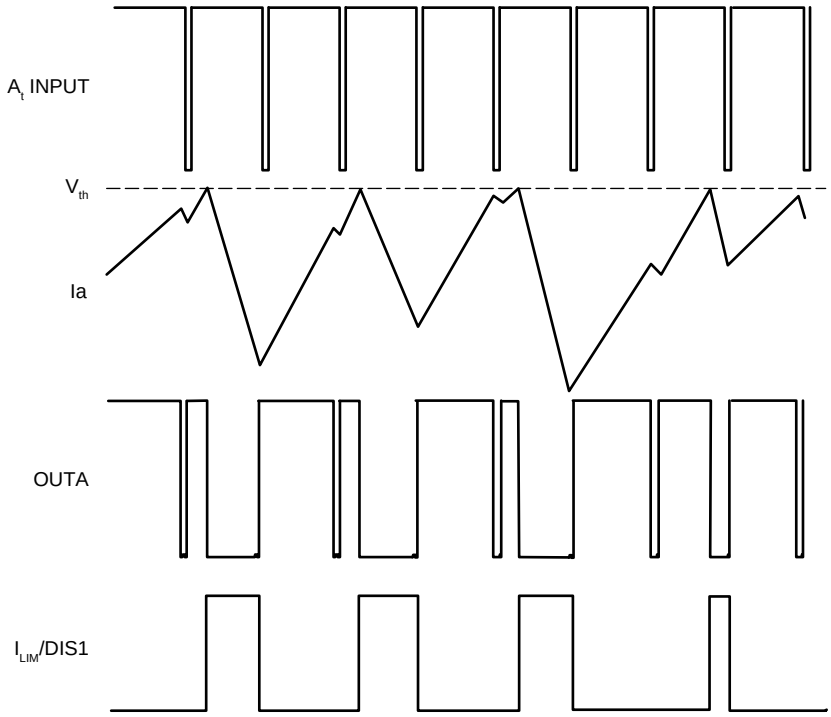
Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC

can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

2.6 EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

Figure 8. Current Limit Waveforms



3. POWER DISSIPATION

The thermally enhanced package of the SA303 allows several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents.

Figure 9. Schottky Diodes

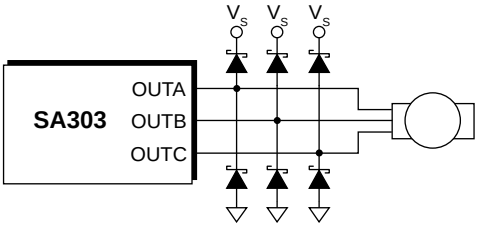
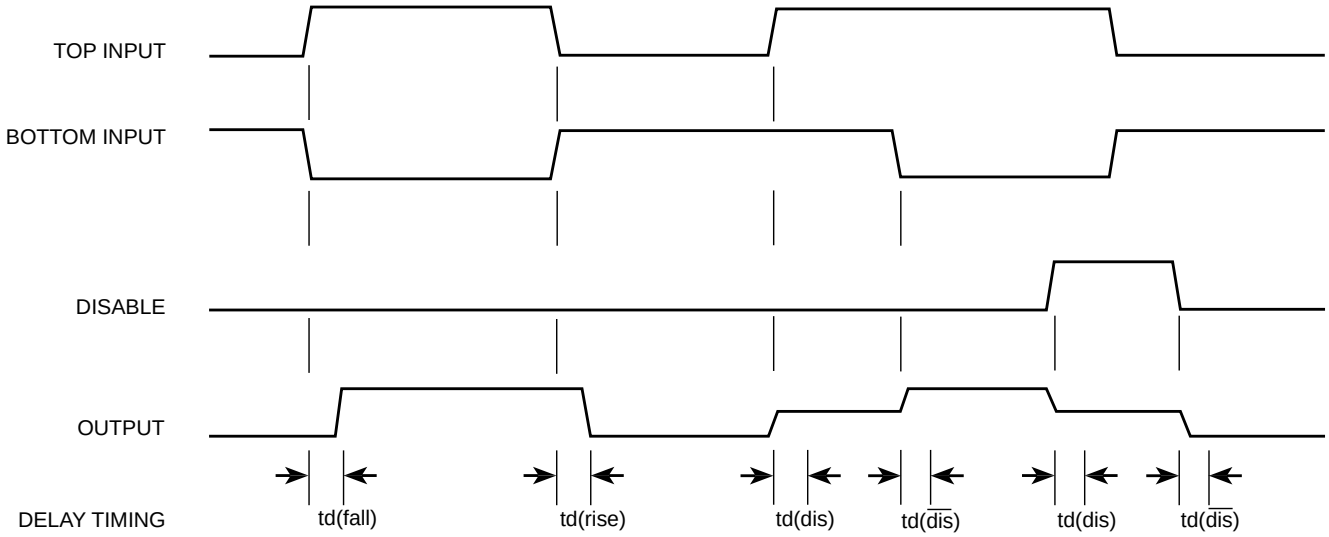


Figure 10. Timing Diagrams



Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA303. Applications vary widely and various thermal techniques are available to match the required performance. The patent pending mounting technique shown in Figure 12, with the SA303 inverted and suspended through a cutout in the PCB is adequate for power dissipation up to 17W with the HS33, a 1.5 inch long aluminum extrusion with four fins. In free air, mounting the PCB perpendicular to the ground, such that the heated air flows upward along the channels of the fins can provide a total Θ_{JA} of less than 14 ºC/W (9W max average P_D). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a Θ_{JA} of 16.66 ºC/W (7.5W max average P_D). In applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance.

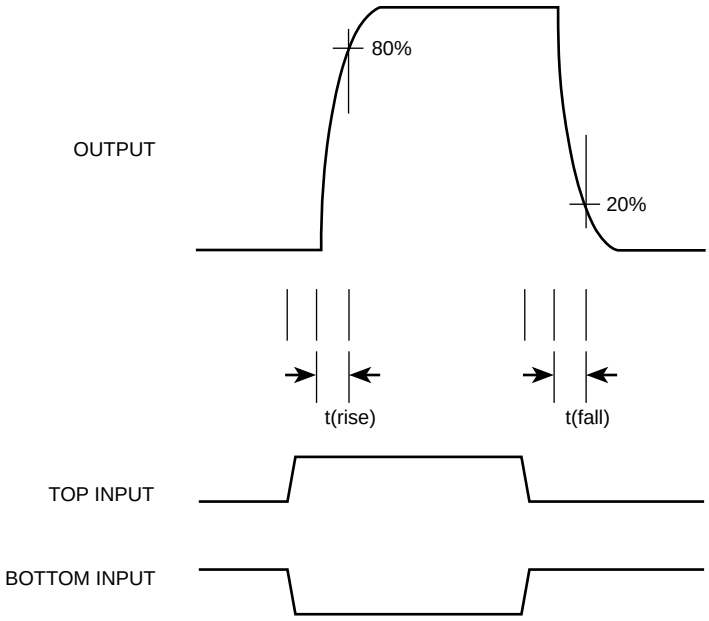


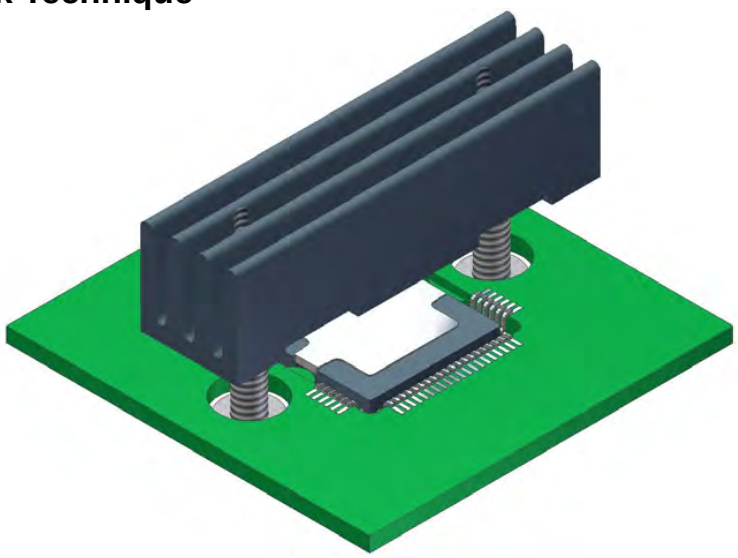
Figure 11. Output Response

4. ORDERING AND PRODUCT STATUS INFORMATION

MODEL	TEMPERATURE	PACKAGE	PRODUCTION STATUS
SA303-IHZ	-25 to 85ºC	64 pin Power QFP (HQ package drawing)	Samples Available 1Q09

Figure 12. Heatsink Technique

PATENT PENDING



3 Phase Switching Amplifier

RoHS COMPLIANT

FEATURES

- Low cost 3 phase intelligent switching amplifier
- Directly connects to most embedded Micro-controllers and Digital Signal Controllers
- Integrated gate driver logic with dead-time generation and shoot-through prevention
- Wide power supply range (8.5V to 60V)
- Over 15A peak output current per phase
- 5A continuous output current per phase
  8A continuous for A-Grade (SA306A)
- Independent current sensing for each output
- User programmable cycle-by-cycle current limit protection
- Over-current and over-temperature warning signals

APPLICATIONS

- 3 phase brushless DC motors
- Multiple DC brush motors
- 3 independent solenoid actuators

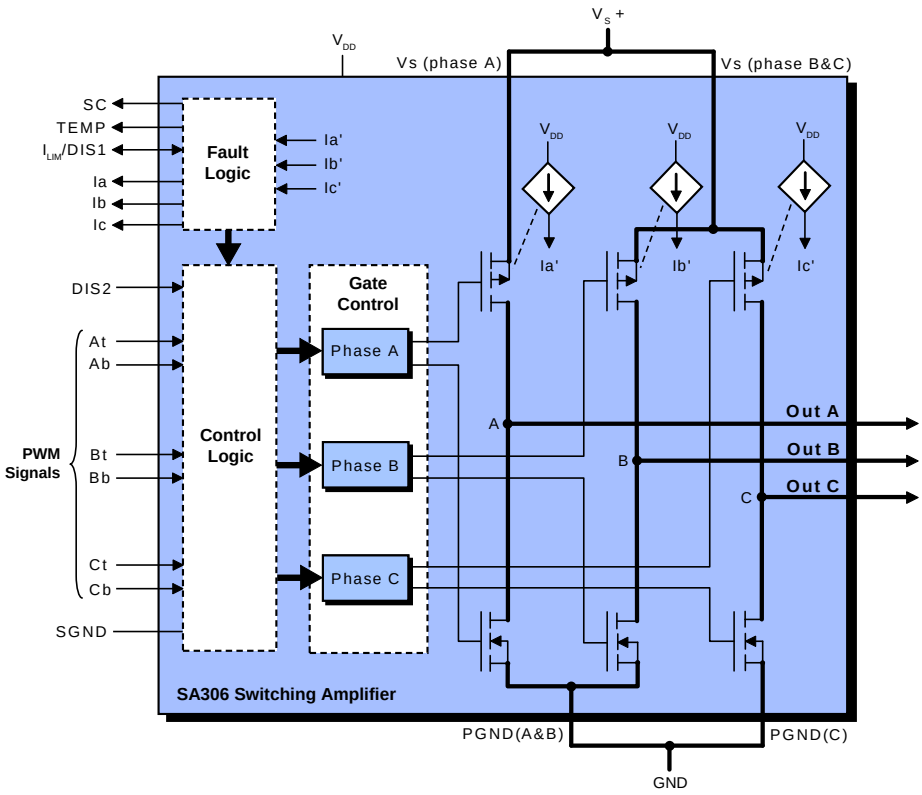
DESCRIPTION

The SA306 is a fully integrated switching amplifier designed primarily to drive three-phase Brushless DC (BLDC) motors. Three independent half bridges provide over 15 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram is provided in Figure 1.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA306 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

The Power Quad surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

Figure 1. Block Diagram



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_S		60	V
SUPPLY VOLTAGE	V_{DD}		5.5	V
LOGIC INPUT VOLTAGE		(-0.5)	(V_{DD}+0.5)	V
OUTPUT CURRENT, peak, 10ms[2]	I_{OUT}		17	A
POWER DISSIPATION, avg, 25ºC[2]	P_D		100	W
TEMPERATURE, junction[3]	T_J		150	°C
TEMPERATURE RANGE, storage	T_{STG}	−55	125	°C
OPERATING TEMPERATURE, case	T_A	−40	125	°C

SPECIFICATIONS

Parameter	Test Conditions[2]	SA306			SA306A			Units
		Min	Typ	Max	Min	Typ	Max	
LOGIC								
INPUT LOW				1			*	V
INPUT HIGH		1.8			*			V
OUTPUT LOW				0.3			*	V
OUTPUT HIGH		3.7			*			V
OUTPUT CURRENT (SC, Temp, I_{LIM}/DIS1)			50			*		mA
POWER SUPPLY								
V_S		UVLO	50	60			55	V
V_S UNDERVOLTAGE LOCKOUT, (UVLO)			9			*	*	V
V_{DD}		4.5		5.5	*		*	V
SUPPLY CURRENT, V_S	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		25	30		*	*	mA
SUPPLY CURRENT, V_{DD}	20 kHz (One phase switching at 50% duty cycle) , V_S=50V, V_{DD}=5V		5	6		*	*	mA
CURRENT LIMIT								
CURRENT LIMIT THRESHOLD (Vth)			3.95			*		V
Vth HYSTERESIS			100			*		mV
OUTPUT								
CURRENT, CONTINUOUS	25ºC Case Temperature	5			8			A
RISING DELAY, TD(RISE)	See Figure 10		270			*		ns
FALLING DELAY, TD(FALL)	See Figure 10		270			*		ns
DISABLE DELAY, TD(DIS)	See Figure 10		200			*		ns
ENABLE DELAY, TD($\overline{DIS}$)	See Figure 10		200			*		ns
RISE TIME, T(RISE)	See Figure 11		50			*		ns
FALL TIME, T(FALL)	See Figure 11		50			*		ns

SPECIFICATIONS, continued

Parameter	Test Conditions[2]	SA306			SA306A			Units
		Min	Typ	Max	Min	Typ	Max	
ON RESISTANCE SOURCING (P-CHANNEL)	5A Load		300	750		300	600	mΩ
ON RESISTANCE SINKING (N-CHANNEL)	5A Load		250	750		250	600	mΩ
THERMAL								
THERMAL WARNING			135			*		ºC
THERMAL WARNING HYSTERESIS			40			*		ºC
RESISTANCE, junction to case	Full temperature range		1.25	1.5		*	*	ºC/W
TEMPERATURE RANGE, case	Meets Specifications	-25		85	-40		125	ºC

NOTES:

* The specification of SA306A is identical to the specification for SA306 in applicable column to the left.

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.
3. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

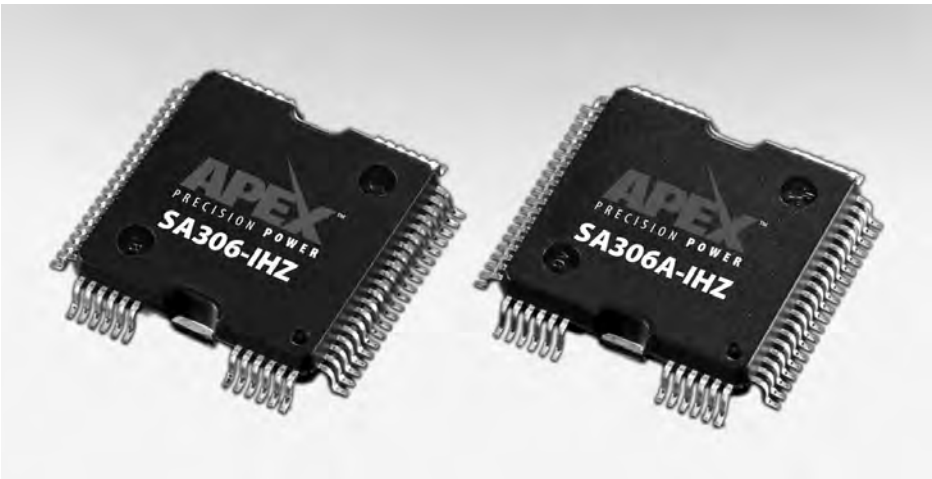
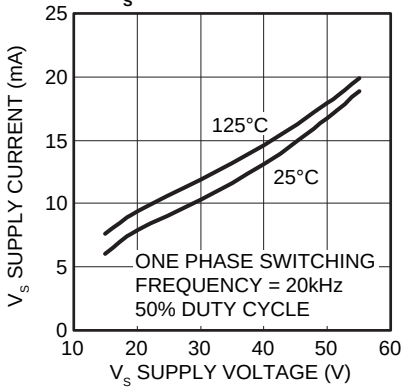
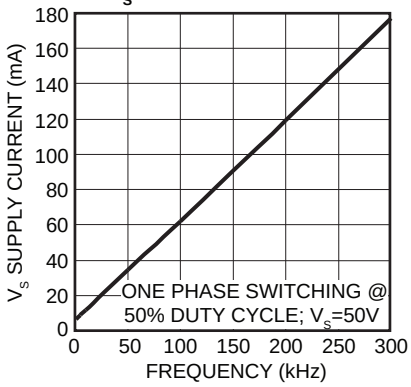


Figure 2. 64-Pin QFP, Package Style HQ

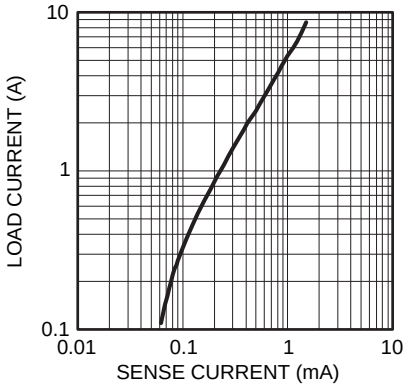
V_S SUPPLY CURRENT



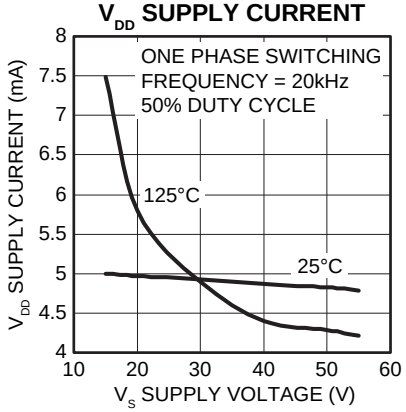
V_S SUPPLY CURRENT



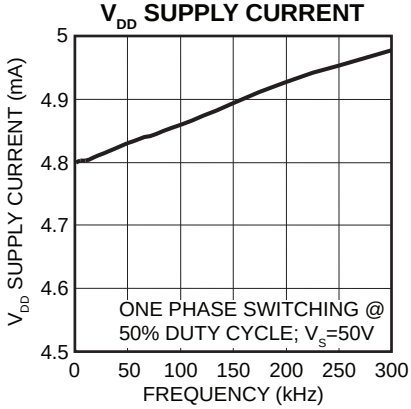
CURRENT SENSE



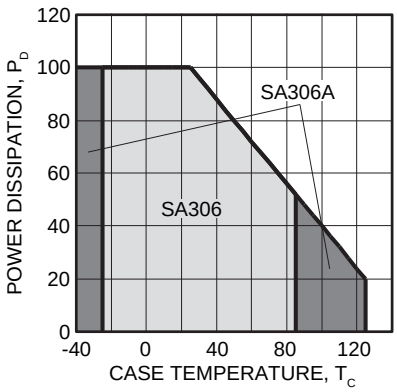
V_{DD} SUPPLY CURRENT



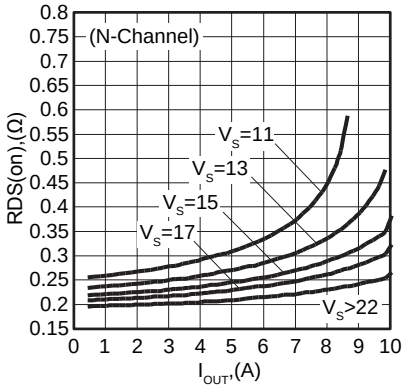
V_{DD} SUPPLY CURRENT



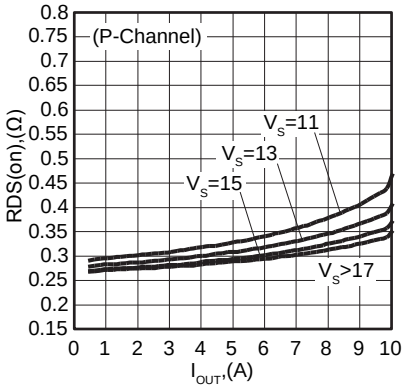
POWER DERATING



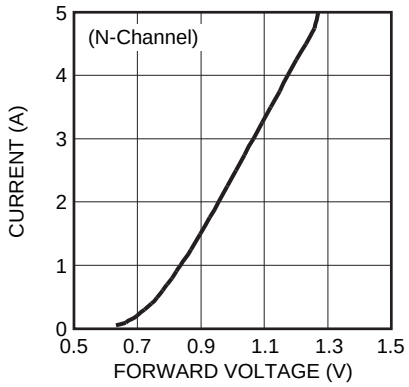
ON RESISTANCE - BOTTOM FET



ON RESISTANCE - TOP FET



DIODE FORWARD VOLTAGE - BOTTOM FET



DIODE FORWARD VOLTAGE - TOP FET

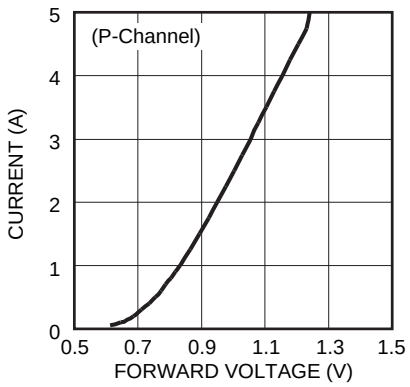


Figure 3. External Connections

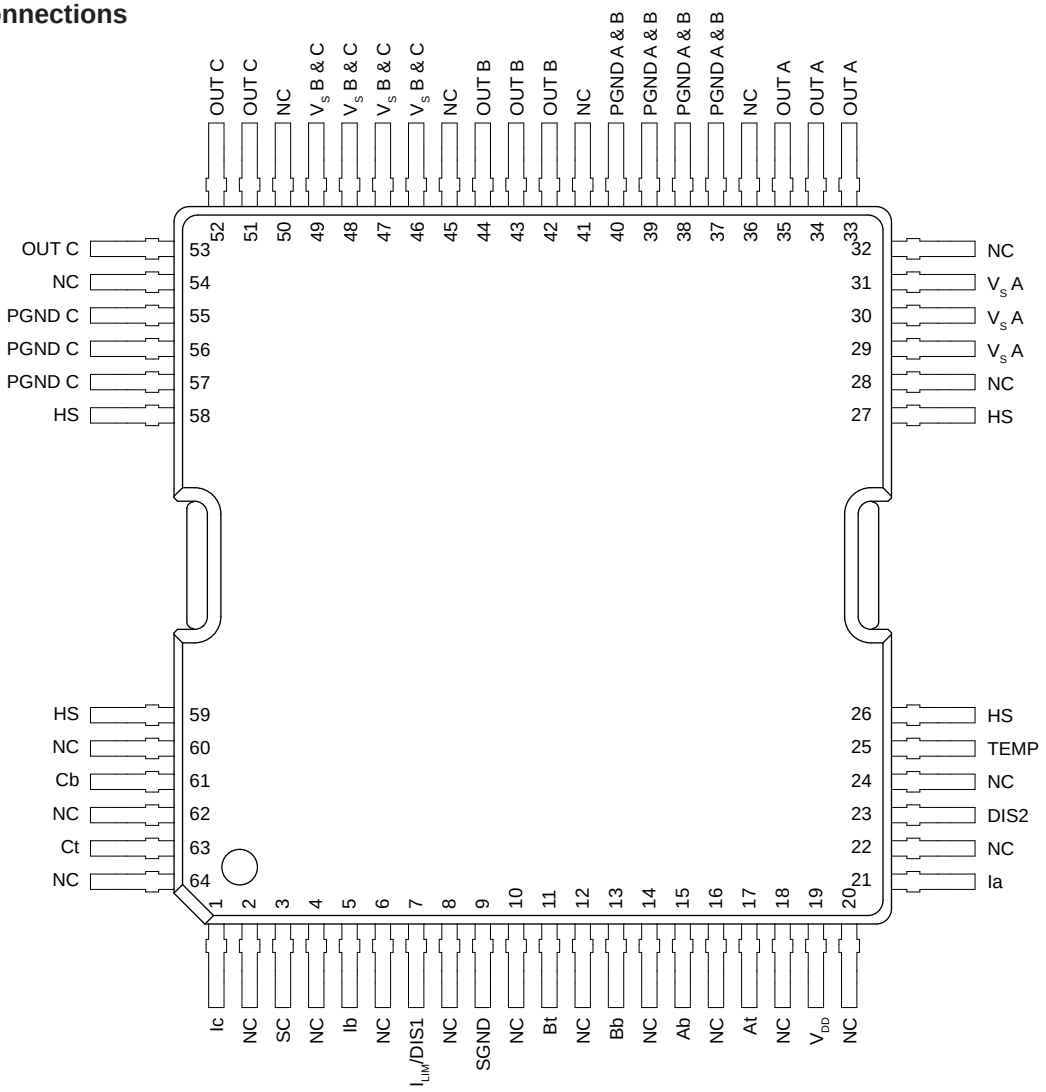


Table 1. Pin Descriptions			
Pin #	**Pin Name**	**Signal Type**	**Simplified Pin Description**
29,30,31	V_S (phase A)	Power	High Voltage Supply (8.5-60V) supplies phase A only
51,52,53	OUT C	Power Output	Half Bridge C Power Output
55,56,57	PGND (phase C)	Power	High Current GND Return Path for Power Output C
3	SC	Logic Output	Indication of a short of an output to supply, GND or another phase
61	Cb	Logic Input	Logic high commands C phase lower FET to turn on
63	Ct	Logic Input	Logic high commands C phase upper FET to turn on
1	Ic	Analog Output	Phase C current sense output
5	Ib	Analog Output	Phase B current sense output
7	I_{LIM}/DIS1	Logic Input/Output	As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function.
9	SGND	Power	Analog and digital GND – internally connected to PGND
11	Bt	Logic Input	Logic high commands B phase upper FET to turn on
13	Bb	Logic Input	Logic high commands B phase lower FET to turn on

Table 1. Pin Descriptions

Pin #	Pin Name	Signal Type	Simplified Pin Description
15	Ab	Logic Input	Logic high commands A phase lower FET to turn on
17	At	Logic Input	Logic high commands A phase upper FET to turn on
19	V_{DD}	Power	Logic Supply (5V)
21	Ia	Analog Output	Phase A current sense output
23	DIS2	Logic Input	Logic high places all outputs in a high impedance state
25	TEMP	Logic Output	Thermal indication of die temperature above 135ºC
42,43,44	OUT B	Power Output	Half Bridge B Power Output
46,47,48,49	V_S (phase B&C)	Power	High Voltage Supply phase B&C
33,34,35	OUT A	Power Output	Half Bridge A Power Output
37,38,39,40	PGND (phase A&B)	Power	High Current GND Return Path for Power Outputs A&B
26,27,58,59	HS	Mechanical	Pins connected to the package heat slug
2,4,6,8,10, 12,14,16,18, 20,22,24,28, 32,36,41,45, 50,54,60,62, 64	NC	---	Do Not Connect

1.2 Pin Descriptions

V_S: Supply voltage for the output transistors. These pins require decoupling (1µF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V_S and PGND pins as possible. Additional capacitance will be required at the V_S pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that Vs pins 29-31 carry only the phase A supply current. Pins 46-49 carry supply current for phases B & C. Phase A may be operated at a different supply voltage from phases B & C. Only the B & C supply pins (46-49) are monitored for undervoltage conditions.

OUT A, OUT B, OUT C: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t_{RR} specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs. (See Section 2.6)

PGND: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

SC: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor.

Ab, Bb, Cb: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If Ab, Bb, or Cb is high at the same time that a corresponding At, Bt, or Ct input is high, protection circuitry will turn off both FETs in order to prevent shoot-through current on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

At, Bt, Ct: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

Ia, Ib, Ic: Current sense pins. The SA306 supplies a positive current to these pins which is proportional to the current flowing through the top side P-channel FET for that phase. Commutating currents flowing through the back-body diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.
The current sense pins are also internally compared with the current limit threshold voltage reference, Vth. If the voltage on any current sense pin exceeds Vth, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

I_{LIM}/DIS1: This pin is directly connected to the disable circuitry of the SA306. Pulling this pin to logic high places OUT A, OUT B, and OUT C in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

SGND: This is the ground return connection for the V_{DD} logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms,. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

V_{DD}: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA306. This pin requires decoupling (at least 0.1µF capacitor with good high frequency characteristics is recommended) to the SGND pin.

DIS2: The DIS2 pin is a Schmitt triggered logic level input that places OUT A, OUT B, and OUT C in a high impedance state when pulled high. DIS2 has an internal 12kΩ pull-down resistor and may therefore be left unconnected.

TEMP: This logic level output goes high when the die temperature of the SA306 reaches approximately 135ºC. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor.

HS: These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

NC: These “no-connect” pins should be left unconnected.

2. SA306 OPERATION

The SA306 is designed primarily to drive three phase motors. However, it can be used for any application requiring three high current outputs. The signal set of the SA306 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for all three phases provide performance information which can be used to regulate or limit torque.

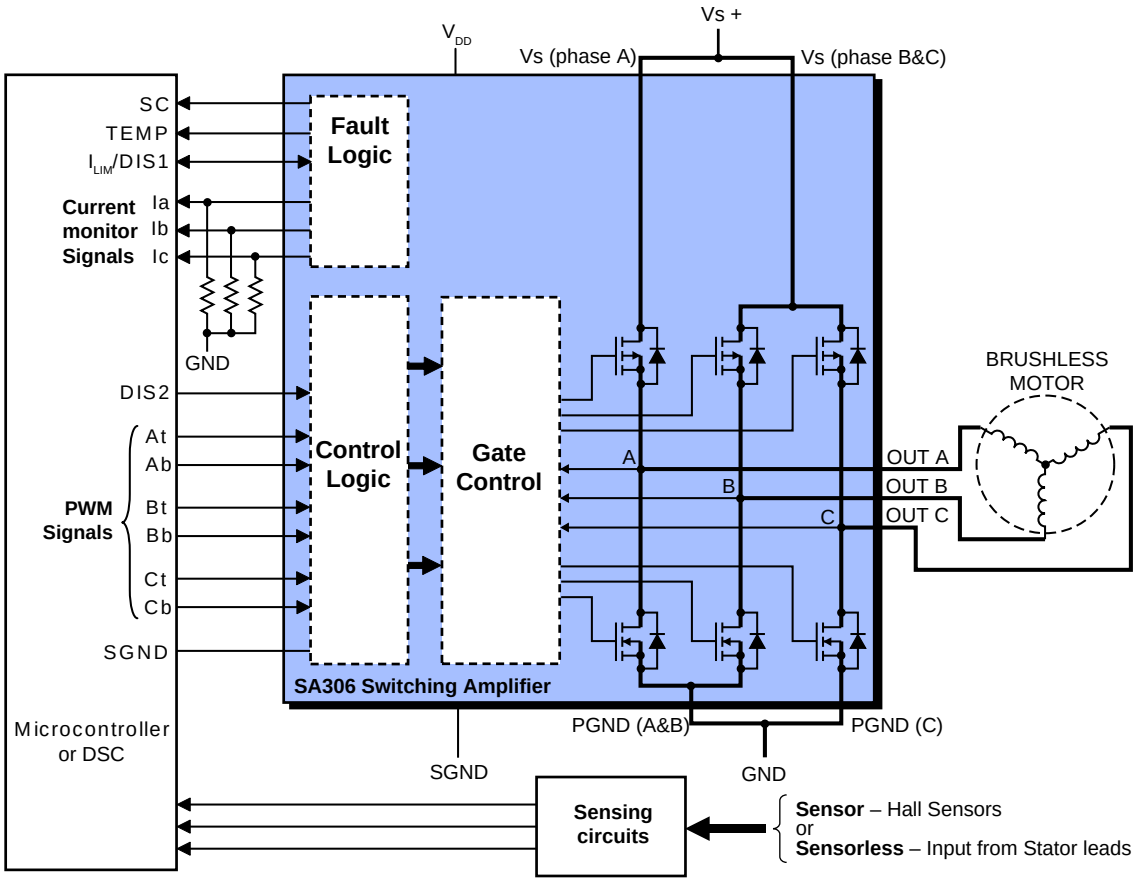


Figure 4. System Diagram

TABLE 2. TRUTH TABLE

At, Bt, Ct	Ab, Bb, Cb	Ia, Ib, Ic	I_{LIM}/DIS1	DIS2	OUT A, OUT B, OUT C	Comments
0	0	X	X	X	High-Z	Top and Bottom output FETs for that phase are turned off.
0	1	$<V_{th}$	0	0	PGND	Bottom output FET for that phase is turned on.
1	0	$<V_{th}$	0	0	VS	Top output FET for that phase is turned on.
1	1	X	X	X	High-Z	Both output FETs for that phase are turned off.
X	X	$>V_{th}$	1	X	High-Z	Voltage on Ia, Ib, or Ic has exceeded Vth, which causes I_{LIM}/DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases.
X	X	X	X	1	High-Z	DIS2 pin pulled high, which disables all outputs.
X	X	X	Pulled High	X	High-Z	Pulling the I_{LIM}/DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.
X	X	X	Pulled Low	0	Determined by PWM inputs	Pulling the DIS2 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.
X	X	X	X	X	High-Z	If V_S is below the UVLO threshold all output FETs will be disabled.

The block diagram in Figure 5 illustrates the features of the input and output structures of the SA306. For simplicity, a single phase is shown.

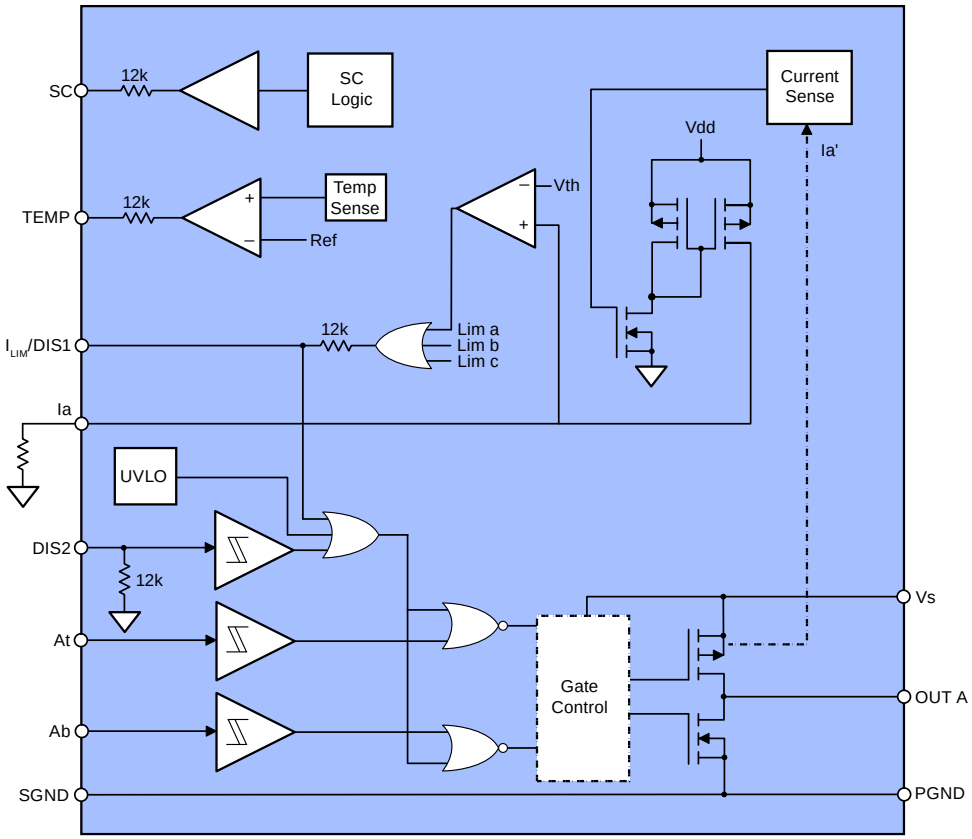


Figure 5. Input and output structures for a single phase

2.1 LAYOUT CONSIDERATIONS

Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25µF per ampere of output current should be placed near the SA306 as well. Capacitor types rated for switching applications are the only types that should be considered. Note that phases B & C share a V_S connection and the bypass recommendation should reflect the sum of B & C phase current.

The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1µF to 0.47µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

2.2 FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA306 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA306.

Figure 6 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

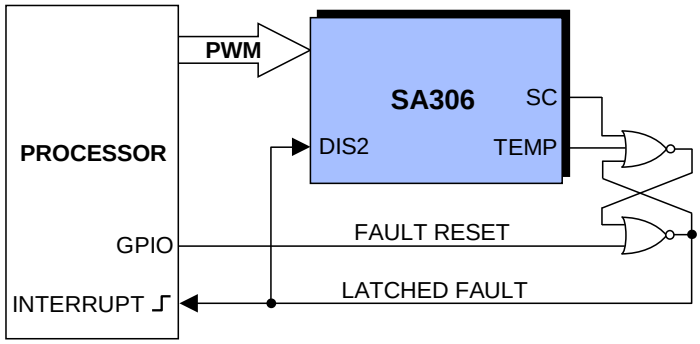


Figure 6. External Fault Latch Circuit

In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA306 will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

2.3 UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA306 unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lockout condition is in progress. The SA306 has two V_S connections: one for phase A, and another for phases B & C. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

2.4 CURRENT SENSE

External power shunt resistors are not required with the SA306. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the V_{DD} supply. Headroom required for the current sense circuit is approximately 0.5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 4 of this datasheet.

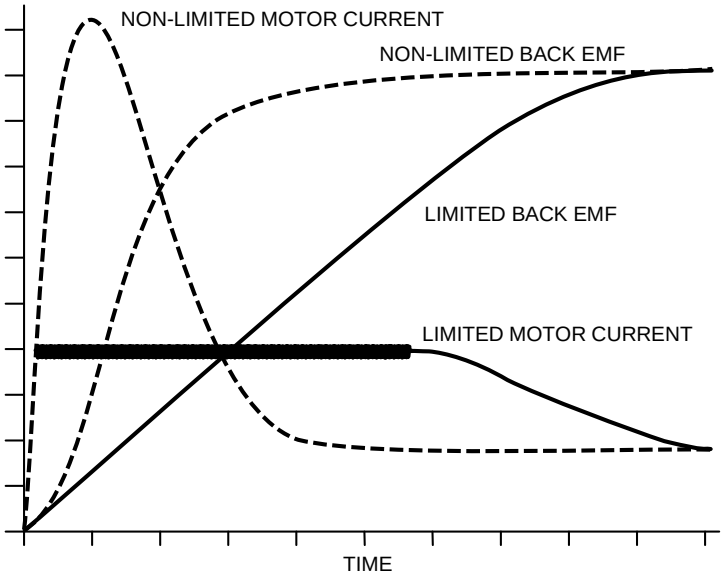


Figure 7. Start-up Voltage and Current

2.5 CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at start-up. Because the output current of each upper output FET is measured, the SA306 is able to provide a very robust current limit scheme. This enables the SA306 to safely and easily drive virtually any brushless motor through a start-up inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 7 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the three current sense pins exceeds the current limit threshold voltage (Vth), all outputs are disabled. After all current sense pins fall below the Vth threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (At, Bt, or Ct). With most commutation schemes, the current limit will reset each PWM cycle. This scheme regulates the peak current in each phase during each PWM cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

Figure 8 illustrates the current limit trigger and reset sequence. Current limit engages and I_{LIM}/DIS1 goes high when any current sense pin exceeds Vth. Notice that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a sub-cycle oscillation. This oscillation can be seen on the I_{LIM}/DIS1 pin waveform in Figure 8.

Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of At, Bt, and Ct except when commutating phases. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

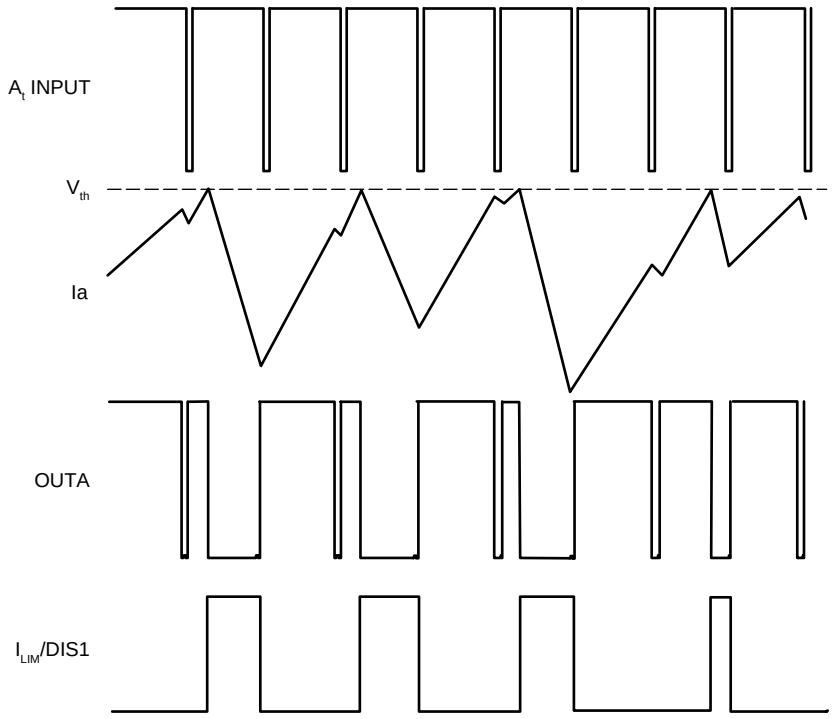


Figure 8. Current Limit Waveforms

The current limit feature may be disabled by tying the I_{LIM}/DIS1 pin to GND. The current sense pins will continue to provide top FET output current information. Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

2.6 EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce

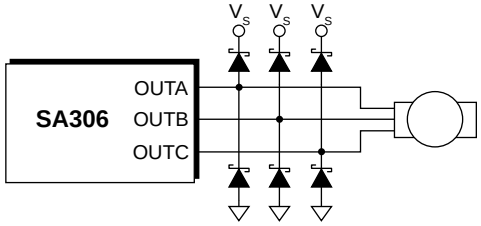


Figure 9. Schottky Diodes

power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

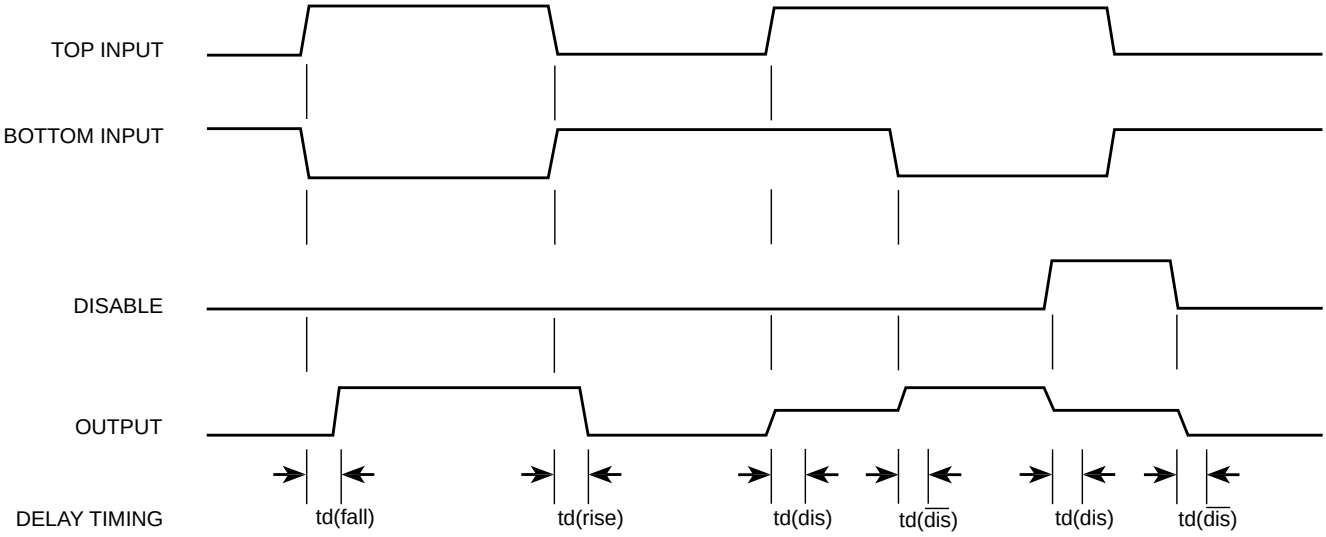


Figure 10. Timing Diagrams

3. POWER DISSIPATION

The thermally enhanced package of the SA306 allows several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents. Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA306. Applications vary widely and various thermal techniques are available to match the required performance. The patent pending mounting technique shown in Figure 12, with the SA306 inverted and suspended through a cutout in the PCB is adequate for power dissipation up to 17W with the HS33, a 1.5 inch long aluminum extrusion with four fins. In free air, mounting the PCB perpendicular to the ground, such that the heated air flows upward along the channels of the fins can provide a total Θ_{JA} of less than 14 ºC/W (9W max average P_D). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a Θ_{JA} of 16.66 ºC/W (7.5W max average P_D). In applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance.

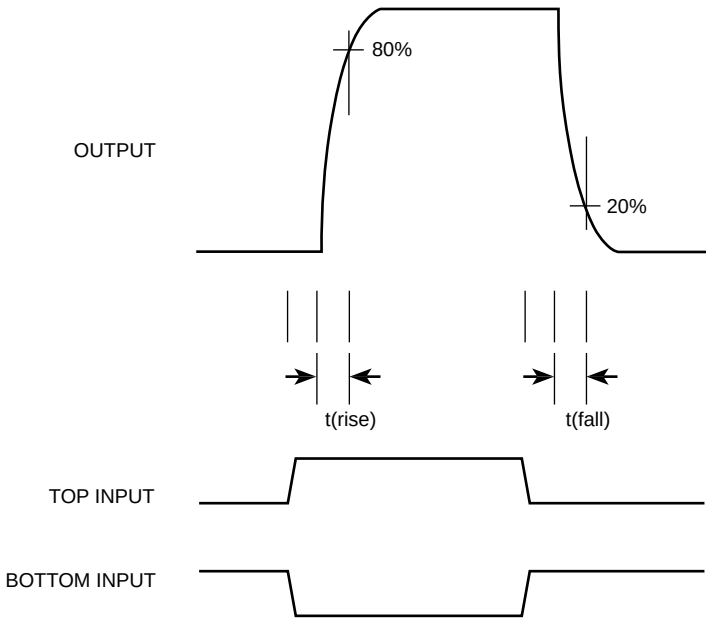


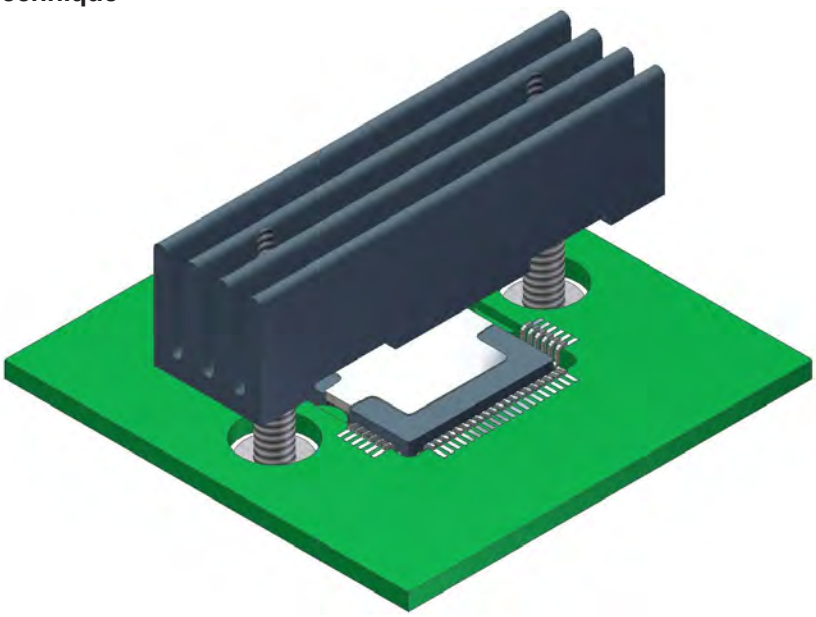
Figure 11. Output Response

4. ORDERING AND PRODUCT STATUS INFORMATION

MODEL	TEMPERATURE	PACKAGE	PRODUCTION STATUS
SA306-IHZ	-25 to 85ºC	64 pin Power QFP (HQ package drawing)	Samples Available
SA306A-FHZ	-40 to +125ºC	64 pin Power QFP (HQ package drawing)	Samples Available

Figure 12. Heatsink Technique

PATENT PENDING



CONTACTING CIRRUS LOGIC SUPPORT

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For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

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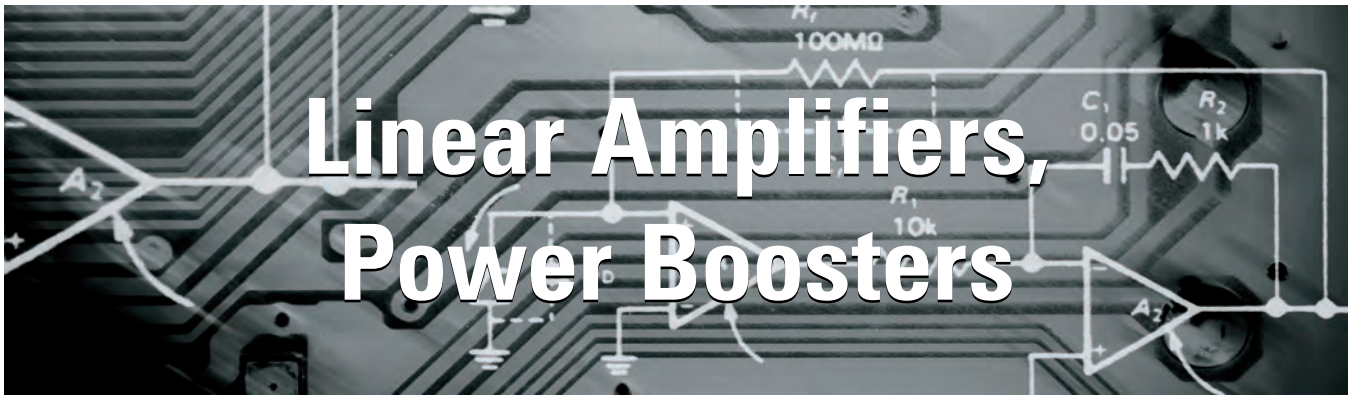

Linear Amplifiers, Power Boosters

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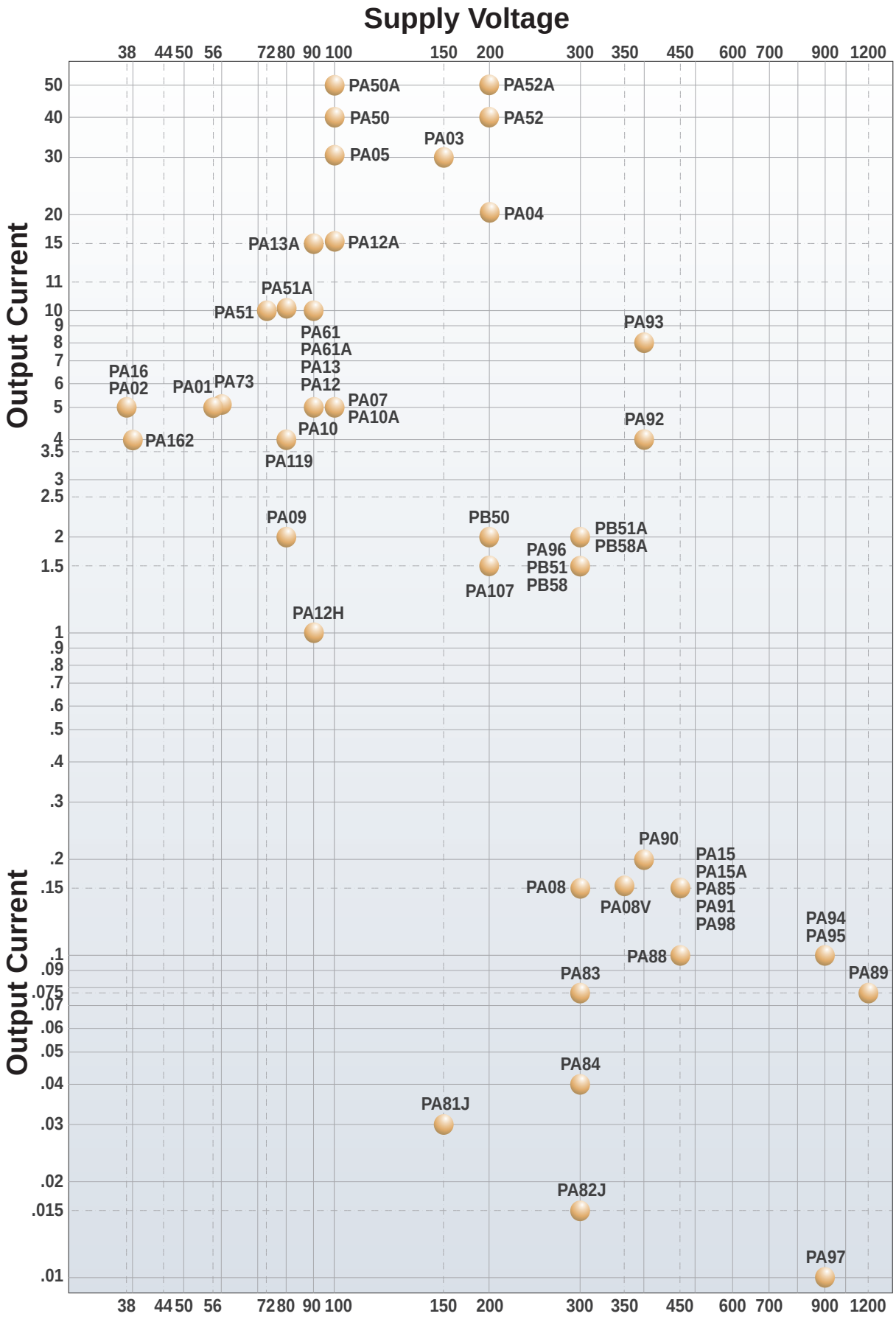
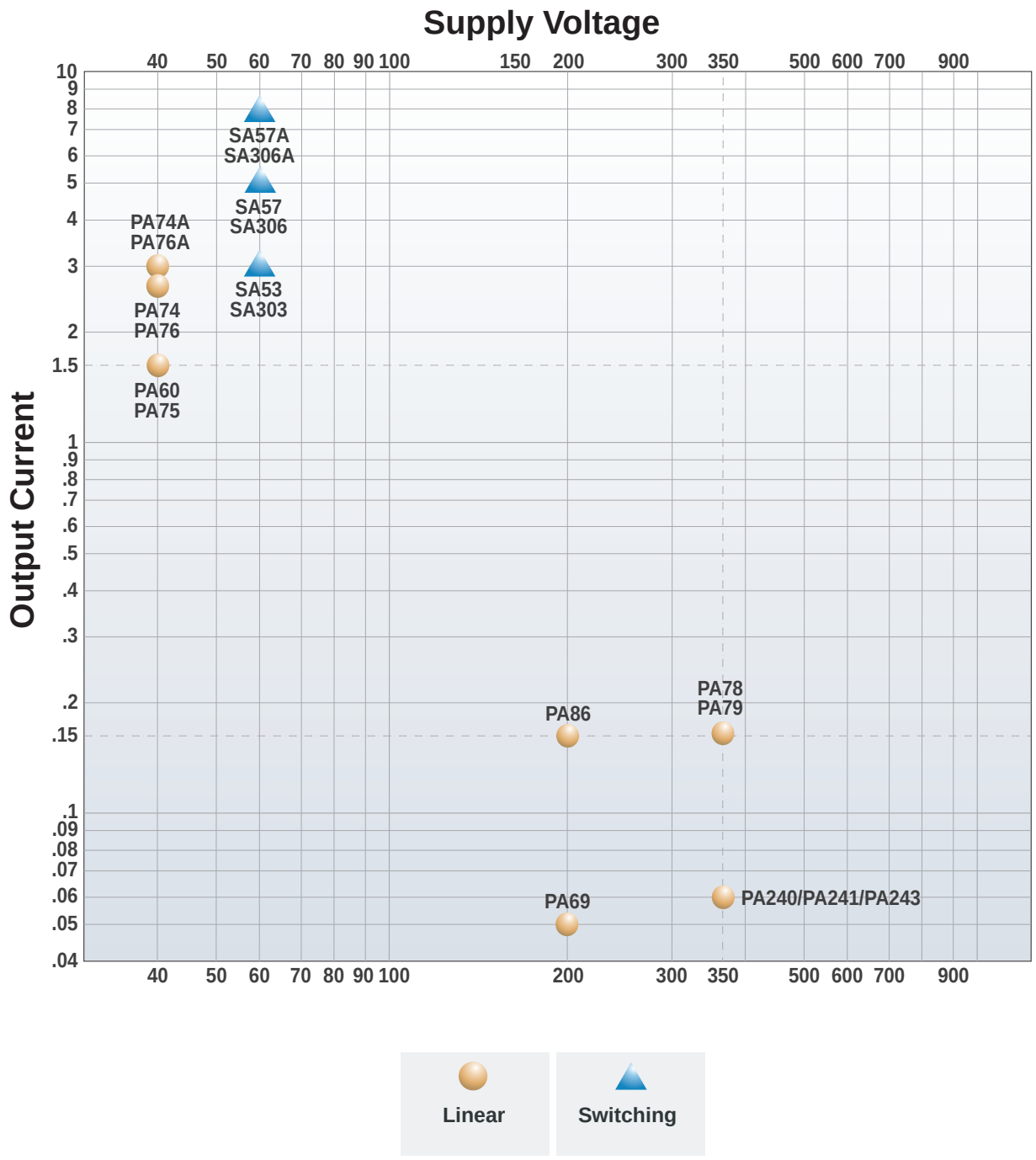
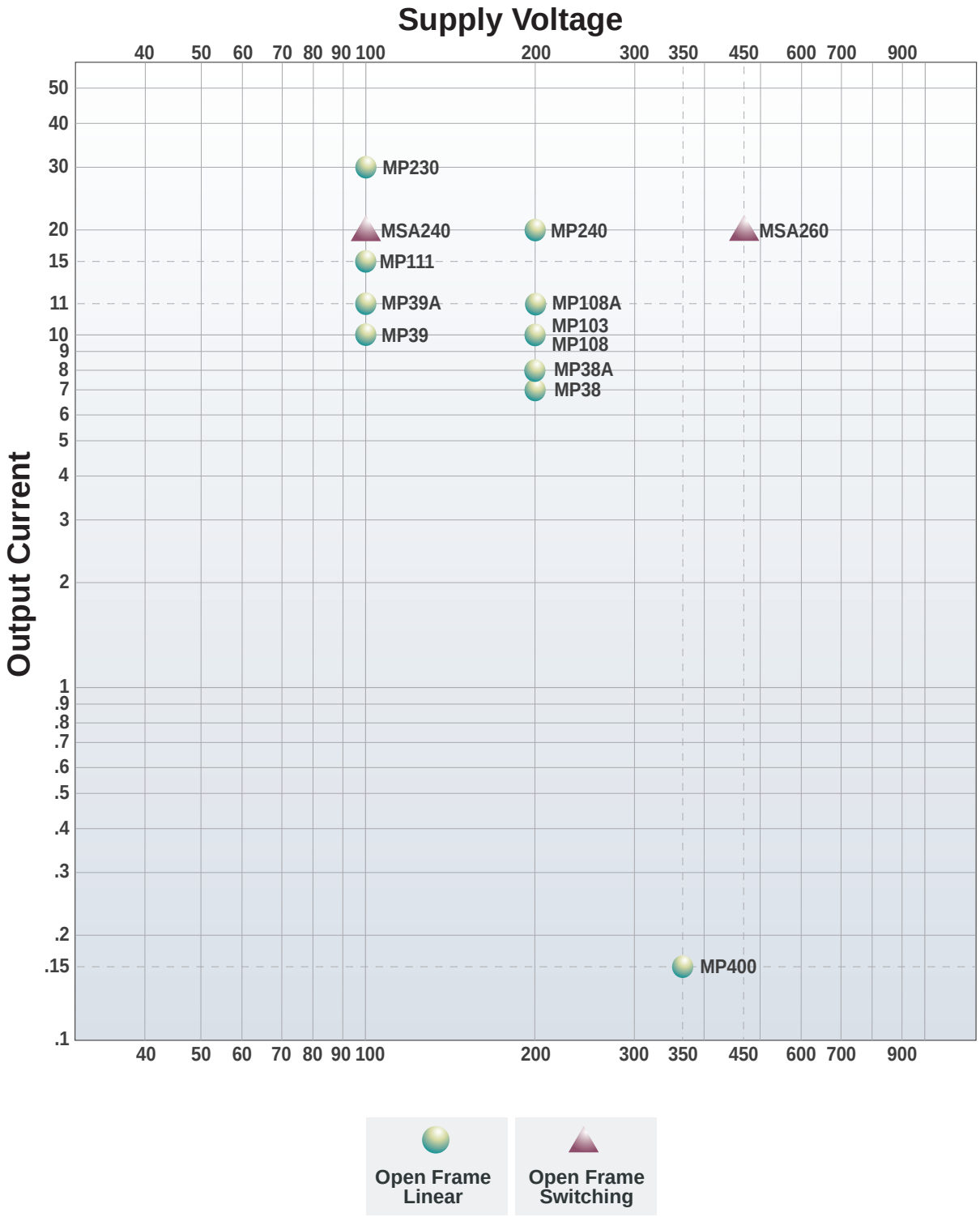
PRODUCT SELECTOR MATRIX - HYBRIDS



PRODUCT SELECTOR MATRIX - ICs



PRODUCT SELECTOR MATRIX - OPEN FRAME MODULES



Open Frame Product Design Technology

Driving Down the Cost of Power

Apex is driving down the cost of high power analog. For those applications with slightly more relaxed operating environments, the new Apex "Open Frame" product design delivers the power and thermal performance of a hybrid, but at a cost that is significantly less.

DELIVER THE POWER AT COST SAVINGS OF UP TO 75%

The open frame concept uses low-cost SMT (surface mount technology) construction to deliver the power analog performance you seek at a cost that makes selecting an off-the-shelf power solution an easy choice over a "do-it-yourself" discrete. Apex's open frame design is being integrated into both our linear power operational amplifier and PWM amplifier product lines to achieve per unit cost reductions of up to 75%.

THERMAL MANAGEMENT SOLVED

Working with high power in ranges above 5 amps or voltage supplies greater than 60 volts, comes with a difficult set of thermal management issues. A watt is a watt no matter how the amplifier is designed. The one constant is heat dissipation. For example, a 5 amp, 60 volt amplifier may have to dissipate hundreds of watts while driving the load. The primary challenge is to get the heat out of the amplifier's package.

For more than 30 years, traditional hybrid designs have achieved exceptional thermal management by soldering unpackaged power transistors (die) to a thick film metalized BeO (beryllium oxide) substrate. The power transistors take the brunt of the heat generated while driving the load. The use of BeO provides the hybrid design with superior heat conductance, while keeping the temperature of the power transistors under control.

With the open frame approach, thermal management actually begins with the individually packaged components. The surface mount power transistors are packaged in an industry-standard D2Pak with a copper slug on the back (the D2Pak is the surface mount version of the TO-220 package). The power transistor inside the D2Pak is soldered to the copper slug to provide a very low thermal resistance and an exceptionally wide heat spread angle (see below). When the D2Pak is soldered to the copper circuit layer of the open frame's isolated metal substrate (IMS), the thermal resistance is actually superior to that of the hybrid design.

CREATE MORE BOARD SPACE

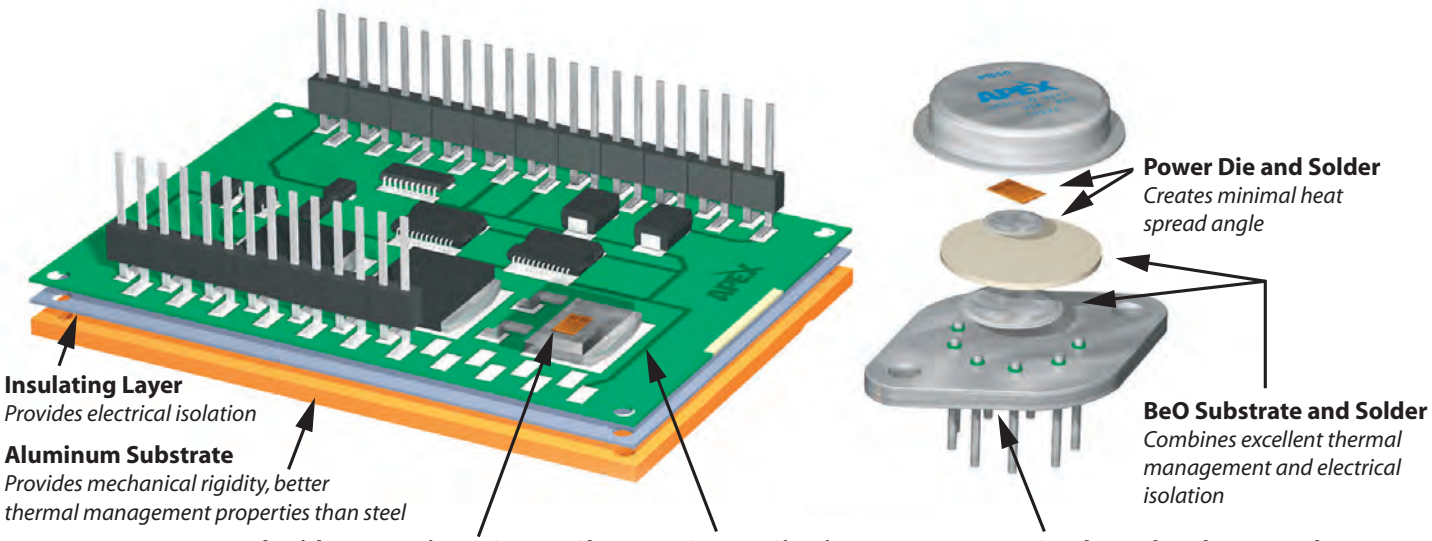
Although its footprint can be slightly larger than a hybrid design, an open frame amplifier actually allows you to create a smaller and less costly system. The open frame design incorporates the pins and circuitry on the same side of the substrate. When the open frame is mounted on a PCB, a 1/4" inch of space is created between the amplifier and the board.

With this mounting arrangement, power supply bypass capacitors can be placed very close to the amplifier's power supply pins while freeing-up valuable board space. This configuration also makes room for other required system components. Open frame products save additional board space by allowing the heatsink to be mounted on top of the device. This is in sharp contrast to a hybrid design that requires through-hole mounting of the hybrid and the heatsink, thus occupying valuable board space.

WHY ROLL YOUR OWN?

As designers continue to seek new technology that will decrease overall system costs and trim time-to-market, Apex's new open frame product design deserves serious consideration. An open frame design achieves the performance of a traditional power hybrid, but at a significantly lower cost. If you have considered an off-the-shelf power amplifier solution in the past, but you ended up "rolling your own" because you couldn't justify the price tag, a lower-cost option is finally here.

Open Frame vs. Hybrid Construction



Equivalent/Second Sources

Reliable Choices in Power Amplifiers

Through a combination of exceptional product performance, manufacturing integrity and long product life cycles, Apex Precision Power™ Products from Cirrus Logic have helped customers manage component obsolescence. Below is a cross reference listing for those industry models for which APEX can be used as a replacement or a second source. The list indicates the specific form and function each model can match: pin for pin replacement (P/F), pin for pin but with major performance differences (P/D) and a functional equivalent (F/E).

Alternative	Apex Part	Fit Notes
Texas Instruments, Burr-Brown		
3571/3572	PA01	P/D
	PA07	P/D
	PA10	P/D
	PA12	P/D
	PA61	P/D
3573	PA73	P/F
3573AM	PA83	P/F
3573AMQ	PA73	P/F
3581/3582/3583	PA83	P/F
3581J	PA81J	P/F
3582J	PA82J	P/F
3583J	PA83	P/F
3584/3584J	PA84	P/D
OPA2541	PA76	P/F
OPA2544	PA60	P/D
OPA501	PA51	P/F
	PA61	P/D
OPA502BM	PA12	P/D
OPA502SM	PA12A	P/D
OPA511AM	PA01	P/D
	PA10	P/D
OPA512	PA12	P/F
	PA10	P/D
OPA512SM	PA12A	P/F
OPA541	PA02	F/E
	PA10	P/D
	PA07	P/D
	PA12	P/D
	PA51	P/D
	PA61	P/D
OPA548	PA01	F/E
	PA73	F/E

(P/F) = Pin for pin compatible - form, fit and functional replacement
(P/D) = Pin for pin compatible - major performance differences noted
(F/E) = Functional equivalent - not pin for pin compatible - major differences noted

MP38 • MP38A

Power Operational Amplifier

FEATURES

- HIGH INTERNAL DISSIPATION — 125 Watts
- HIGH VOLTAGE, HIGH CURRENT — 200V, 10A
- HIGH SLEW RATE — 10V/µs
- 4 WIRE CURRENT LIMIT SENSING
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±95V
- INDUSTRIAL AUDIO
- PACKAGE OPTION - DIP10 - DUAL-IN-LINE

30-PIN DIP
PACKAGE STYLE CL

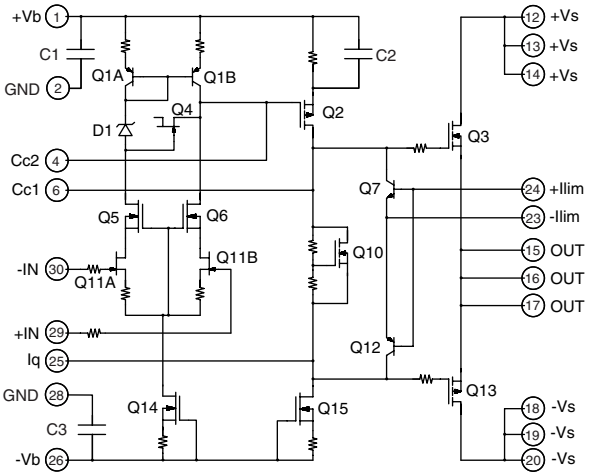
DESCRIPTION

The MP38 is a cost-effective high voltage MOSFET power operational amplifier constructed with surface mount components on a thermally conductive but electrically isolated substrate.

While the cost is low the MP38 offers many of the same features and performance specifications found in much more expensive hybrid power amplifiers.

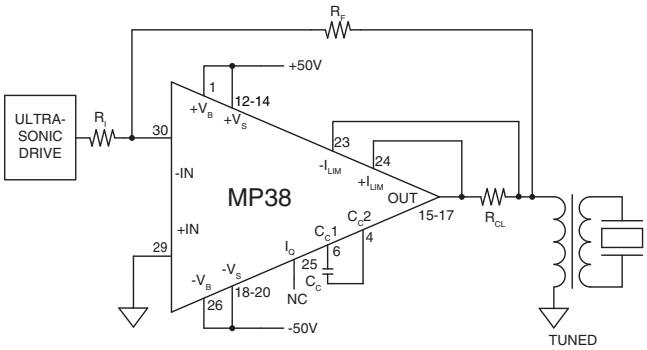
The metal substrate allows the MP38 to dissipate power up to 125 watts and its power supply voltages can range up to +/- 100 Volts (200V total). Optional boost voltage inputs allow the small signal portion of the amplifier to operate at higher supply voltages than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high current for extra efficient operation. External compensation tailors performance to the user needs. A four-wire sense technique allows current limiting without the need to consider internal or external mili-ohm parasitic resistance in the output line. An Iq pin is available which can be used to shut off the quiescent current in the output stage. The output stage then operates class C and lowers quiescent power dissipation. This is useful in applications where output crossover distortion is not important.

EQUIVALENT SCHEMATIC



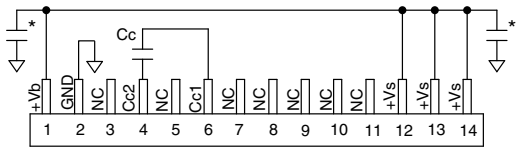
TYPICAL APPLICATION REF: APPLICATION NOTE 25

The high power bandwidth and high voltage output of the MP38 allows driving ultra-sonic transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the MP38.

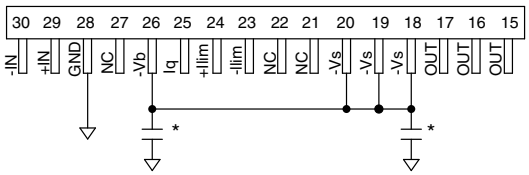


ULTRA-SONIC AMPLIFIER

EXTERNAL CONNECTIONS



COMPONENT SIDE VIEW



* SEE "BYPASSING" PARAGRAPH

Phase Compensation

Gain	Cc	Rc
1	470pF	100Ω
≥ 3	220pF	Short
≥ 10	100pF	Short

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	$\pm V_S$ ±20V
OUTPUT CURRENT, within SOA	25A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	200°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–40 to +105°C
OPERATING TEMPERATURE RANGE, case	–40 to +85°C

SPECIFICATIONS

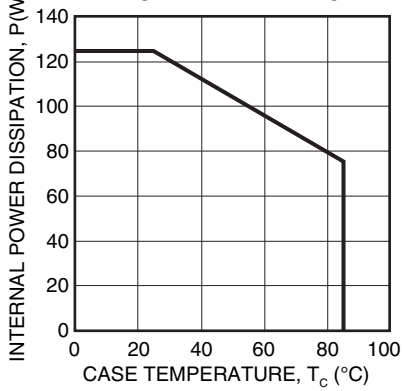
PARAMETER	TEST CONDITIONS[1]	MP38 MIN	MP38 TYP	MP38 MAX	MP38A MIN	MP38A TYP	MP38A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10			3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		*	*	µV/°C
OFFSET VOLTAGE, vs. supply			15			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			*		µV/W
BIAS CURRENT, initial			10	200		*	100	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		*	30	pA
INPUT IMPEDANCE, DC			10^{10}			*		Ω
INPUT CAPACITANCE			20			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B \mp 15$	$\pm V_B \mp 12$		*	*		V
COMMON MODE REJECTION, DC	Full temp, range, V_{CM}= ±20V	86	98		*	*		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @15Hz	Full temperature range, C_C = 100pF	94	113		*	*		db
GAIN BANDWIDTH PRODUCT	I_O=10A		2			*		MHz
POWER BANDWIDTH	R_L=20Ω, V_O = 180V p-p C_C = 100pF		20			*		kHz
PHASE MARGIN	Full temperature range		60			*		◦
OUTPUT								
VOLTAGE SWING	I_O=10A	$\pm V_S \mp 8.8$	$\pm V_S \mp 6.6$		*	*		V
VOLTAGE SWING	$\pm V_B = \pm V_S$ ±10V, I_O=10A	$\pm V_S \mp 6.8$	$\pm V_S \mp 4$		*	*		V
SETTLING TIME to .1%	A_V=+1,10V step, R_L =4Ω		2.5			*		µs
SLEW RATE	A_V= –10, C_C= 100pF	10			*			V/µs
CAPACITIVE LOAD	Full temperature range, A_V=+1	10			*			nF
RESISTANCE			4			*		Ω
CURRENT, CONTINUOUS				10			11	A
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±75	±100	*	*	*	V
CURRENT, quiescent, boost supply				22			*	mA
CURRENT, quiescent, total				26			*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz			.9			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz			1.2			*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-40		85	*		*	°C

NOTES: * The specification of MP38A is identical to the specification for MP38 in applicable column to the left.

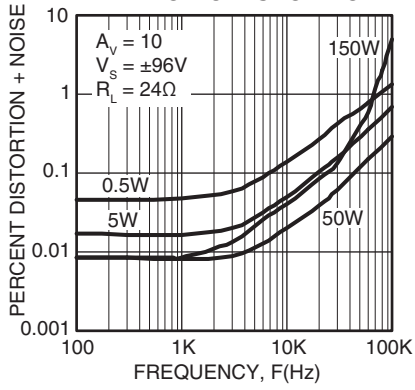
1. Unless otherwise noted: T_C = 25°C, R_C = 100Ω, C_C = 470pF. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The MP38 must be used with a heat sink or the quiescent power may drive the unit to junction temperatures higher than 175°C.

CAUTION The MP38 is constructed from MOSFET transistors. ESD handling procedures must be observed.

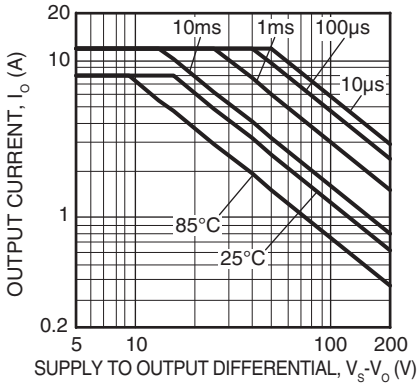
POWER DERATING



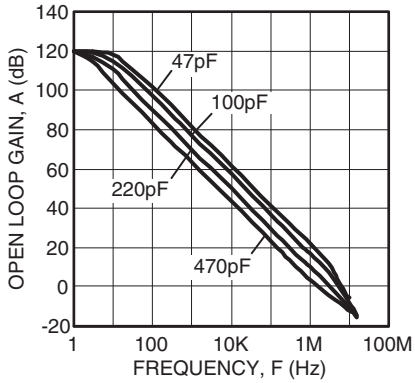
HARMONIC DISTORTION



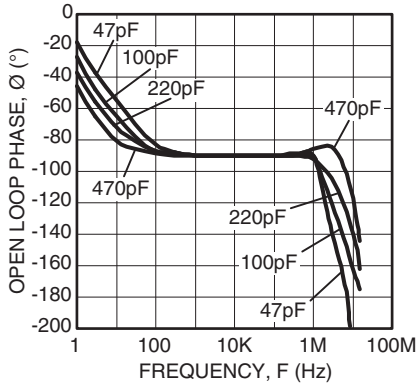
SOA



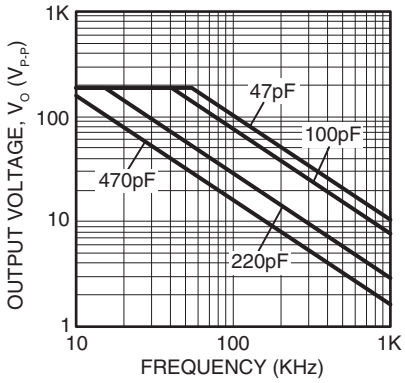
SMALL SIGNAL RESPONSE



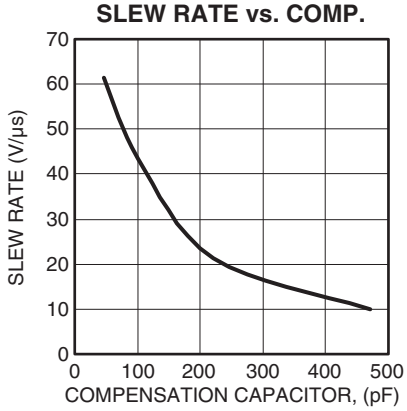
SMALL SIGNAL PHASE



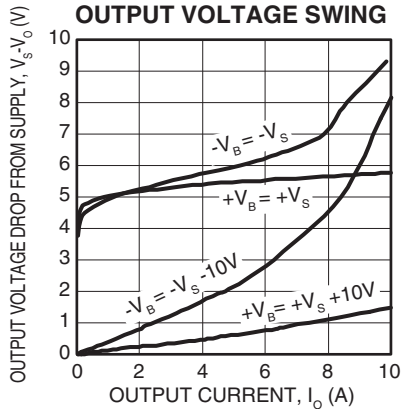
POWER RESPONSE



SLEW RATE vs. COMP.



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. **For the current limit to work correctly pin 24 must be connected to the amplifier output side and pin 23 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.** This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.7}{I_{LIMIT}}$$

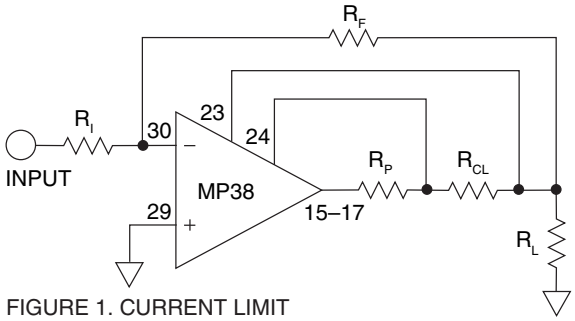


FIGURE 1. CURRENT LIMIT

BOOST OPERATION

With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_S$ (pins 12-14) and $-V_S$ (pins 18-20) are connected to the high current output stage. An additional 10V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swing to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

BYPASSING

Proper bypassing of the power supply pins is crucial for proper operation. Bypass the ±Vs pins with a aluminum electrolytic capacitor with a value of at least 10µF per amp of expected output current. In addition a .47µF to 1µF ceramic capacitor should be placed in parallel with each aluminum electrolytic capacitor. Both of these capacitors have to be placed as close to the power supply pins as physically possible. If not connected to the Vs pins (See BOOST OPERATION) the V_B pins should also be bypassed with a .47µF to 1µF ceramic capacitor.

USING THE IQ PIN FUNCTION

Pin 25 (Iq) can be tied to pin 6 (Cc1) to eliminate the class AB biasing current from the output stage. Typically this would remove 1-4 mA of quiescent current. The resulting decrease in quiescent power dissipation may be important in some applications. Note that implementing this option will raise the output impedance of the amplifier and increase crossover distortion as well.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 4 and 6. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate.

APPLICATION REFERENCES

For additional technical information please refer to the following application notes.

AN 1	General Operating Considerations
AN 11	Thermal Techniques
AN 38	Loop Stability with Reactive Loads

Power Operational Amplifier

FEATURES

- HIGH INTERNAL DISSIPATION — 125 Watts
- HIGH VOLTAGE, HIGH CURRENT — 100V, 10A
- HIGH SLEW RATE — 10V/µs
- 4 WIRE CURRENT LIMIT SENSING
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±45V
- INDUSTRIAL AUDIO
- PACKAGE OPTION - DIP10 - DUAL-IN-LINE

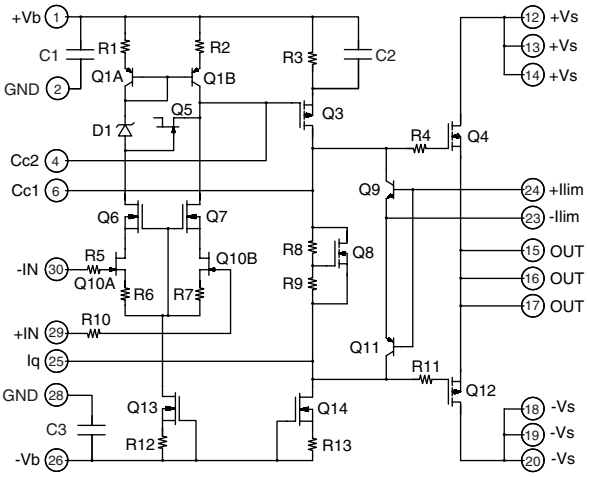
DESCRIPTION

The MP39 is a cost-effective high voltage MOSFET power operational amplifier constructed with surface mount components on a thermally conductive but electrically isolated substrate.

While the cost is low the MP39 offers many of the same features and performance specifications found in much more expensive hybrid power amplifiers.

The metal substrate allows the MP39 to dissipate power up to 125 watts and its power supply voltages can range up to +/- 50 Volts (100V total). Optional boost voltage inputs allow the small signal portion of the amplifier to operate at higher supply voltages than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high current for extra efficient operation. External compensation tailors performance to the user needs. A four-wire sense technique allows current limiting without the need to consider internal or external mili-ohm parasitic resistance in the output line. An Iq pin is available which can be used to shut off the quiescent current in the output stage. The output stage then operates class C and lowers quiescent power dissipation. This is useful in applications where output crossover distortion is not important.

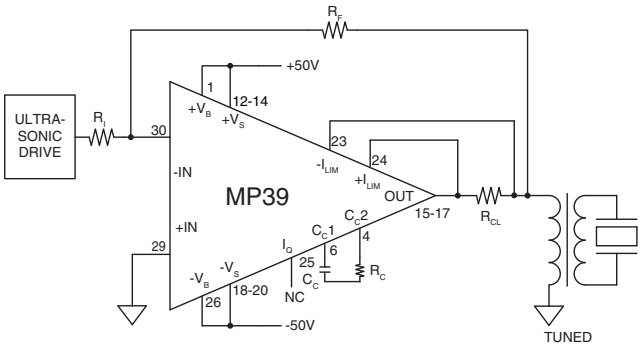
EQUIVALENT SCHEMATIC



30-pin DIP
PACKAGE STYLE CL

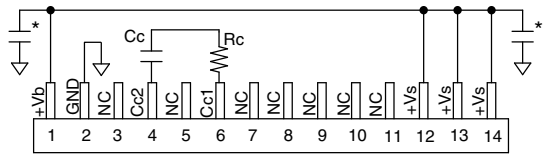
TYPICAL APPLICATION REF: APPLICATION NOTE 25

The high power bandwidth and high voltage output of the MP39 allows driving ultra-sonic transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the MP39.

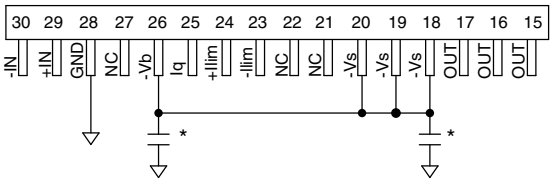


ULTRA-SONIC AMPLIFIER

EXTERNAL CONNECTIONS



COMPONENT SIDE VIEW



* SEE "BYPASSING" PARAGRAPH

Phase Compensation

Gain	Cc	Rc
1	470pF	100Ω
≥ 3	220pF	Short
≥ 10	100pF	Short

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE	$\pm V_S$ ±20V
OUTPUT CURRENT, within SOA	25A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	200°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–40 to +105°C
OPERATING TEMPERATURE RANGE, case	–40 to +85°C

SPECIFICATIONS

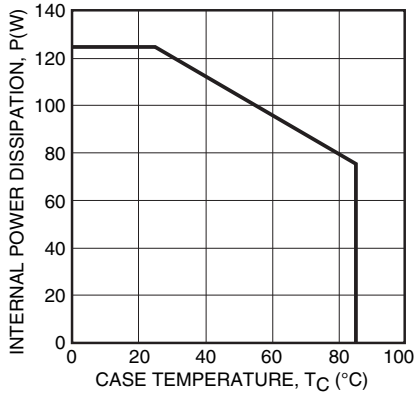
PARAMETER	TEST CONDITIONS[1]	MP39 MIN	MP39 TYP	MP39 MAX	MP39A MIN	MP39A TYP	MP39A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		*	3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		*	*	µV/°C
OFFSET VOLTAGE, vs. supply			15			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			*		µV/W
BIAS CURRENT, initial			10	200		*	100	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		*	30	pA
INPUT IMPEDANCE, DC			10^{10}			*		Ω
INPUT CAPACITANCE			20			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$ ∓15	$\pm V_B$ ∓12		*	*		V
COMMON MODE REJECTION, DC	Full temp, range, V_{CM}= ±20V	86	98		*	*		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @15Hz	Full temperature range, C_C = 100pF	94	113		*	*		db
GAIN BANDWIDTH PRODUCT	I_O=10A		2			*		MHz
POWER BANDWIDTH	R_L=10Ω, V_O = 90V p-p C_C = 100pF		40			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	I_O=10A	$\pm V_S$ ∓8.8	$\pm V_S$ ∓6.0		*	*		V
VOLTAGE SWING	$\pm V_B$ = $\pm V_S$ ±10V, I_O=10A	$\pm V_S$ ∓6.8	$\pm V_S$ ∓1.1		*	*		V
SETTLING TIME to .1%	A_V=+1,10V step, R_L =4Ω		2.5			*		µs
SLEW RATE	A_V= –10, C_C= 100pF	10			*			V/µs
CAPACITIVE LOAD	Full temperature range, A_V=+1	10			*			nF
RESISTANCE			4			*		Ω
CURRENT, CONTINUOUS				10			11	A
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±40	±50	*	*	*	V
CURRENT, quiescent, boost supply				22			*	mA
CURRENT, quiescent, total				26			*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz			.9			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz			1.2			*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-40		85	*		*	°C

NOTES: * The specification of MP39A is identical to the specification for MP39 in applicable column to the left.

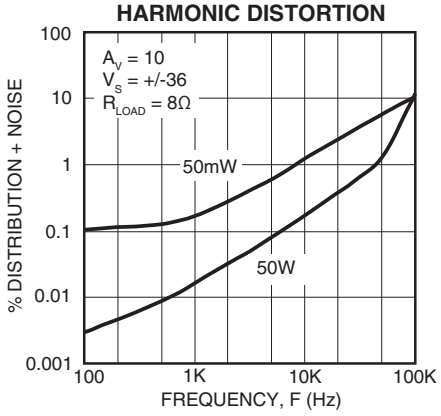
1. Unless otherwise noted: T_C = 25°C, R_C = 100Ω, C_C = 470pF. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B$ = $\pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The MP39 must be used with a heat sink or the quiescent power may drive the unit to junction temperatures higher than 175°C.

CAUTION The MP39 is constructed from MOSFET transistors. ESD handling procedures must be observed.

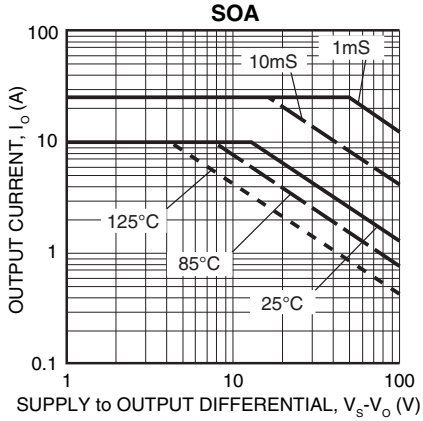
POWER DERATING



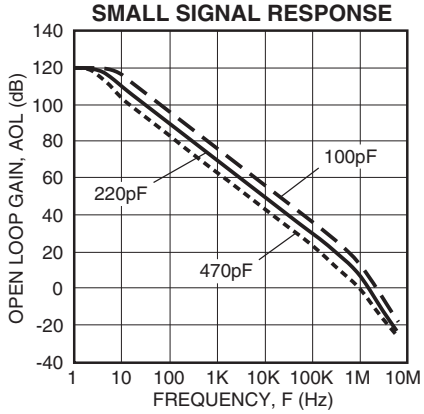
HARMONIC DISTORTION



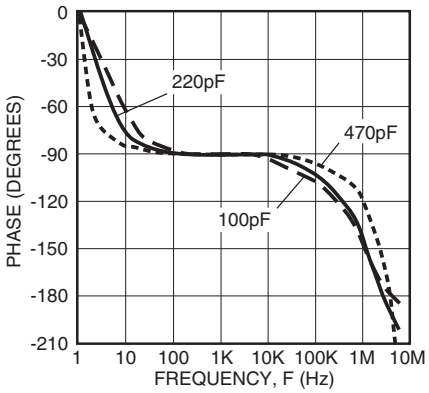
SOA



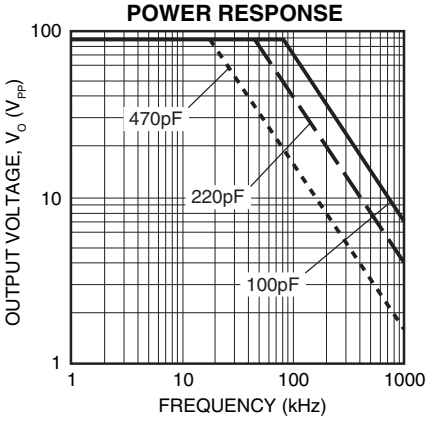
SMALL SIGNAL RESPONSE



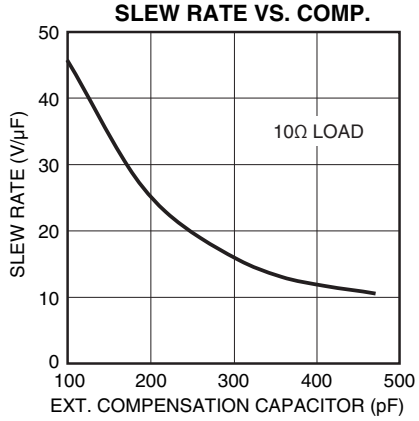
PHASE RESPONSE



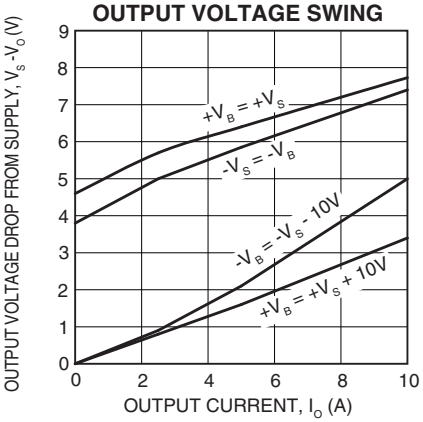
POWER RESPONSE



SLEW RATE VS. COMP.



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 24 must be connected to the amplifier output side and pin 23 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1. This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.7}{I_{LIMIT}}$$

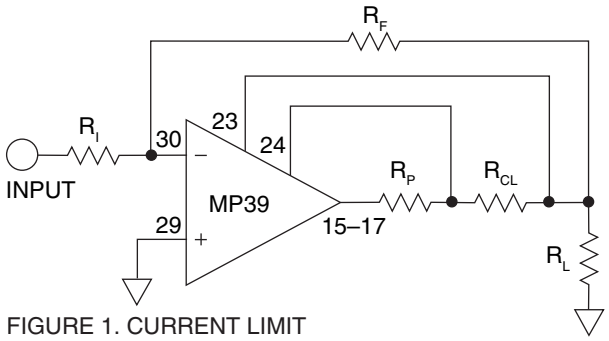


FIGURE 1. CURRENT LIMIT

BOOST OPERATION

With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_S$ (pins 12-14) and $-V_S$ (pins 18-20) are connected to the high current output stage. An additional 10V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swing to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

BYPASSING

Proper bypassing of the power supply pins is crucial for proper operation. Bypass the ±Vs pins with a aluminum electrolytic capacitor with a value of at least 10µF per amp of expected output current. In addition a .47µF to 1µF ceramic capacitor should be placed in parallel with each aluminum electrolytic capacitor. Both of these capacitors have to be placed as close to the power supply pins as physically possible. If not connected to the Vs pins (See BOOST OPERATION) the V_B pins should also be bypassed with a .47µF to 1µF ceramic capacitor.

USING THE IQ PIN FUNCTION

Pin 25 (Iq) can be tied to pin 6 (Cc1) to eliminate the class AB biasing current from the output stage. Typically this would remove 1-4 mA of quiescent current. The resulting decrease in quiescent power dissipation may be important in some applications. Note that implementing this option will raise the output impedance of the amplifier and increase crossover distortion as well.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 4 and 6. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate.

APPLICATION REFERENCES

For additional technical information please refer to the following application notes.

AN01	General Operating Considerations
AN11	Thermal Techniques
AN38	Loop Stability with Reactive Loads

Power Operational Amplifiers

FEATURES

- Low Cost Integrated Solution
- Output Current >10A Within SOA
- Internal Power Dissipation 35 W Per Channel
- 167V/µS Slew Rate

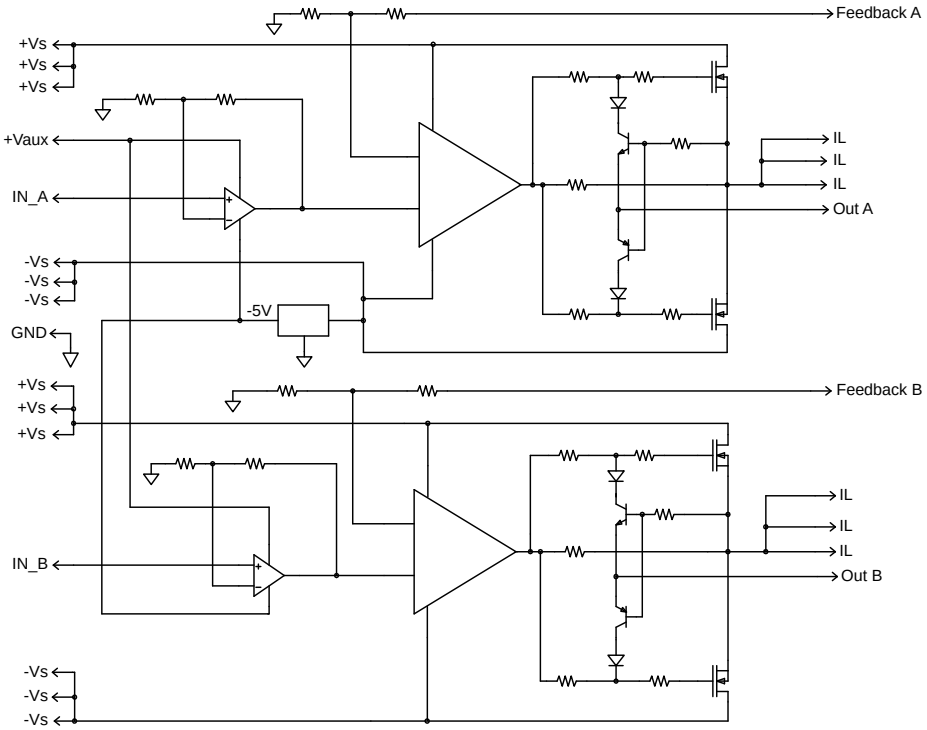
APPLICATIONS

- Piezoelectric Actuation For Ink Jet Printer Nozzles

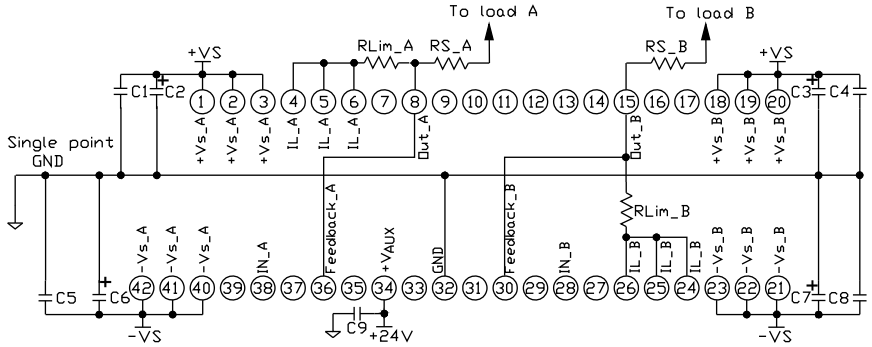
GENERAL DESCRIPTION

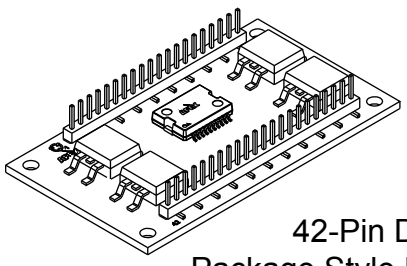
The MP103 is a high voltage, high output current dual channel operational amplifier for driving capacitive loads such as piezo devices use in ink jet printing applications. The MP103 utilizes proprietary IC's combined with discrete semiconductor and passive elements on a thermally conductive insulated metal substrate, delivering very high power from a compact module. The amplifier gain is fixed at 65 V/V when the feedback pin is connected to the V_{OUT} pin. Internal compensation provides optimum slew rate and insures stability. The only external components required are the current limit resistors R_{LIM}, a series isolation resistor R_S and the power supply bypass capacitors.

EQUIVALENT CIRCUIT DIAGRAM



EXTERNAL CONNECTIONS





42-Pin DIP
Package Style FC

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	$+V_S$ to $-V_S$		200	V
SUPPLY VOLTAGE, $-V_S$	$-V_S$	-30		V
SUPPLY VOLTAGE, $+V_{AUX}$	$+V_{AUX}$		30	V
OUTPUT CURRENT, pk, per Channel (Within SOA)	$I_{O(PK)}$		15	A
POWER DISSIPATION, internal, Each Channel	P_D		35	W
INPUT VOLTAGE	V_{IN}	-5	V_{AUX}	V
TEMPERATURE, pin solder, 10s			225	°C
TEMPERATURE, junction (Note 2)	T_J		150	°C
TEMPERATURE RANGE, storage	T_S	−40	105	°C

SPECIFICATIONS

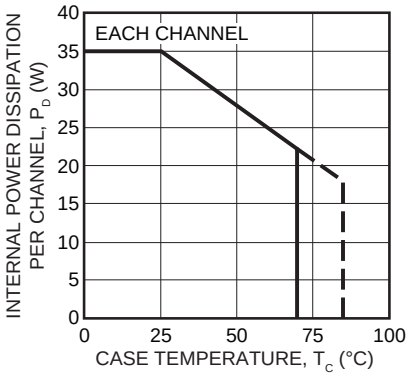
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT (Each Channel)					
OFFSET VOLTAGE		-6.7	±2	6.7	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		±2		µV/°C
BIAS CURRENT, initial (Note 3)		-6.6	±3.3	6.6	µA
INPUT RESISTANCE, DC			300		KΩ
INPUT CAPACITANCE			1.5		pF
INPUT VOLTAGE RANGE		-3.4		$+V_{AUX}$ - 2	V
NOISE	f = 10KHz		600		nV/√Hz
GAIN (Each Channel)					
FIXED GAIN	Feedback connected to V_{OUT}	63.5	65	66.5	V/V
GAIN BANDWIDTH, -3db	C_L = 47nF		230		KHz
POWER BANDWIDTH, $130V_{P-P}$	$+V_S$ = 145V, $-V_S$ = -15V		230		KHz
OUTPUT (Each Channel)					
VOLTAGE SWING	I_O = 10A	$+V_S$ - 15	$+V_S$ - 9		V
VOLTAGE SWING	I_O = -5A	$-V_S$ + 15	$-V_S$ + 14		V
CURRENT, Peak, Source			12		A
SLEW RATE	R_S=1.0Ω, C_L=47nF, $V_{IN} \geq 8V_{P-P}$	167			V/µS
POWER SUPPLY (Note 4)					
VOLTAGE, $-V_S$		-7	-15	-20	V
VOLTAGE, $+V_{AUX}$			24	25	V
VOLTAGE, $+V_S$		$-V_S$ + 20	145	$-V_S$ + 200	V
CURRENT, quiescent, $-V_S$			19	26	mA
CURRENT, quiescent, $+V_{AUX}$			13.5	15	mA
CURRENT, quiescent, $+V_S$			1	5	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 5)	Full temperature range, f ≥ 60Hz		1.5	1.75	°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz		3.1	3.6	°C/W
RESISTANCE, junction to air	Full temperature range		12.5	14	°C/W
TEMPERATURE RANGE, case		0		70	°C

NOTES:

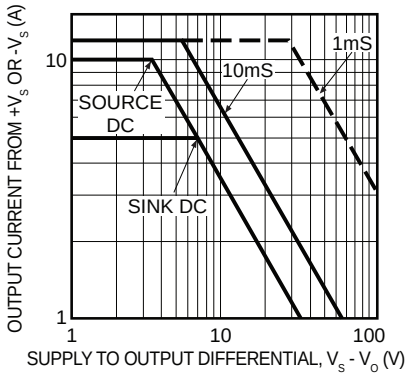
1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stages. $+V_{AUX}$ denotes the positive supply voltage to the input stages.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

TYPICAL PERFORMANCE GRAPHS

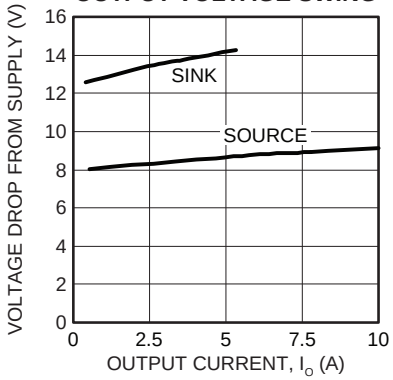
POWER DERATING



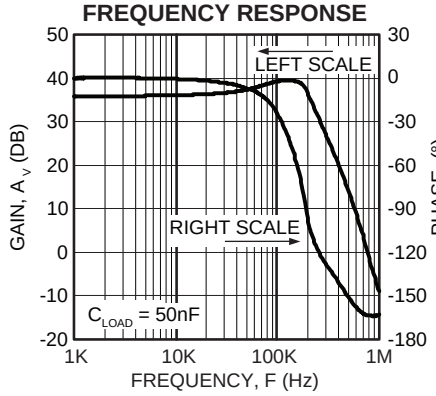
SOA



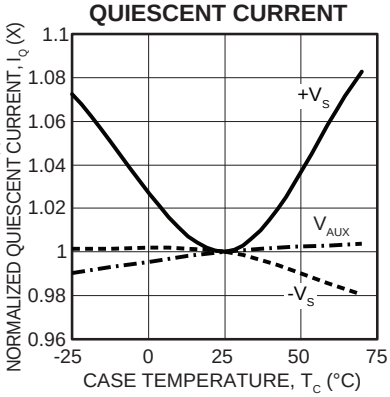
OUTPUT VOLTAGE SWING



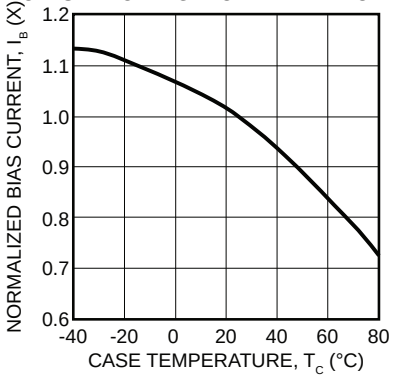
FREQUENCY RESPONSE



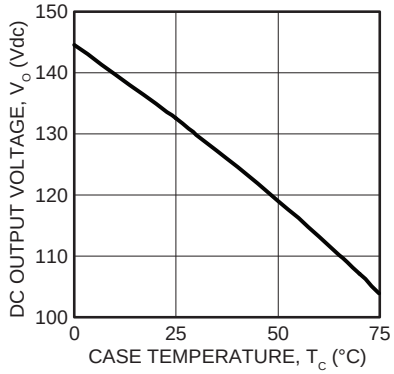
QUIESCENT CURRENT



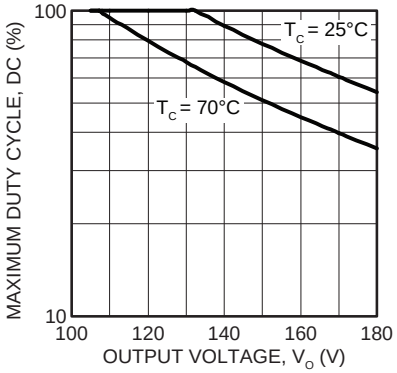
OFFSET VOLTAGE vs. TEMPERATURE



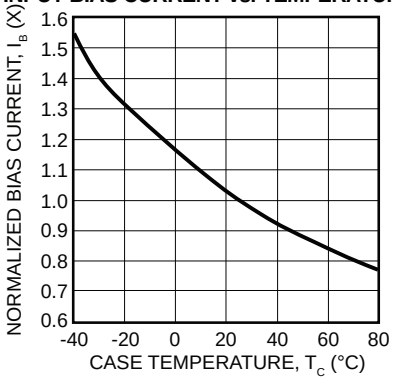
MAX. DC OUTPUT VOLTAGE

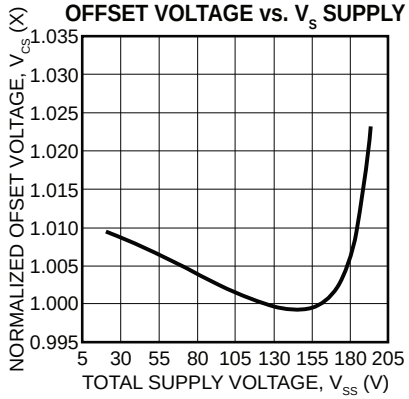


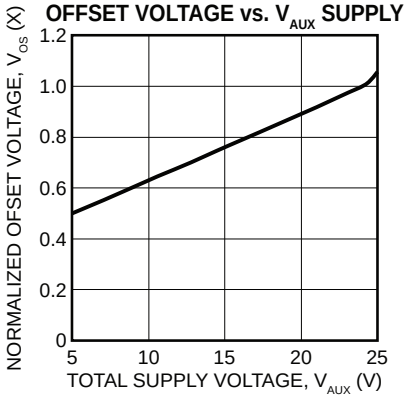
MAX. OUTPUT PULSE DUTY CYCLE

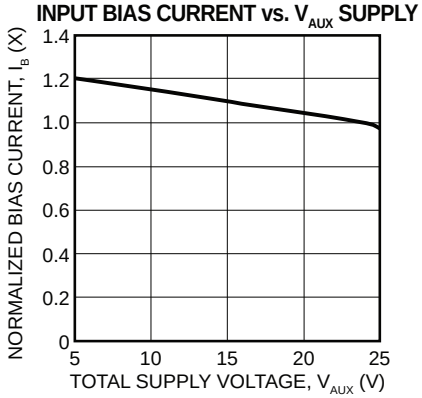


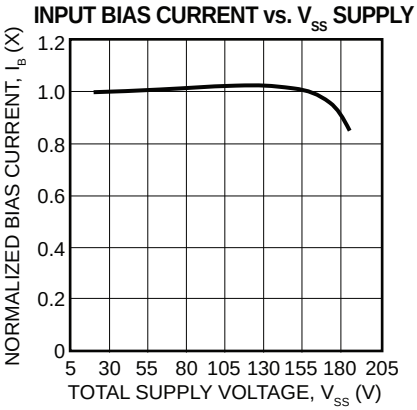
INPUT BIAS CURRENT vs. TEMPERATURE

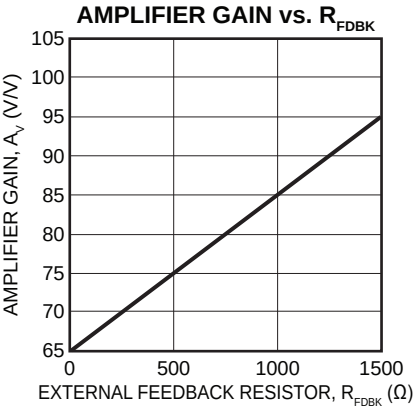


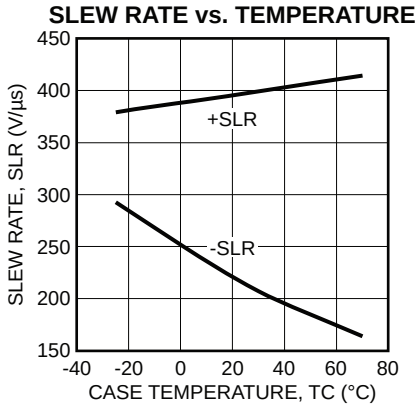












PIN DESCRIPTIONS

Pin #	Pin name	Description
1,2,3	$+V_S$_A	Positive high voltage power supply pins for channel A.
4,5,6	I_L_A	High current output pins for channel A. A current limit resistor must be placed between these pins and the output pin 8.
8	Out_A	Output pin for channel A.
15	Out_B	Output pin for channel B.
18,19,20	$+V_S$_B	Positive high voltage power supply pins for channel B.
21,22,23	$-V_S$_B	Negative power supply pins for channel B.
24,25,26	I_L_B	High current output pins for channel B. A current limit resistor must be placed between these pins and the output pin 15.
28	IN_B	Input pin for channel B.
30	Feedback_B	Feed back pin for channel B. This pin must be connected to output B pin 15 to close the feedback loop. When connected directly to pin 15 the closed loop voltage gain of channel B is 65 V/V. The gain can be increased by inserting a 1/4 W resistor between pins 30 and 15.
32	GND	Ground
34	$+V_{AUX}$	+24V voltage power supply pin. A 24 V power supply is required for operation of front end small signal circuitry of each channel.
36	Feedback_A	Feed back pin for channel A. This pin must be connected to output A pin 8 to close the feedback loop. When connected directly to pin 8 the closed loop voltage gain of channel A is 65 V/V. The gain can be increased by inserting a 1/4 W resistor between pins 36 and 8.
38	IN_A	Input pin for channel A.
40,41,42	$-V_S$_A	Negative power supply pins for channel A.

GENERAL

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AMPLIFIER GAIN

When the feedback pin for each channel is connected to the corresponding OUT pin, the gain of the amplifier is internally set to 65 V/V. The amplifier gain can be increased by connecting a resistor between the feedback and Out pin. The amplifier gain will be increased approximately 1 V/V for each additional 49.9Ω added between the feedback and OUT pin.

SAFE OPERATING AREA

The MOSFET output stage of the MP103 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP103. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. Duplicate the supply bypass for the supply terminals of each amplifier channel. A bypass capacitor of 0.1µF or greater is recommended for the $+V_{AUX}$ terminal.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30Ω. The current limit function can be disabled by shorting the I_L pin to the OUT pin.

$$R_{LIM} = 0.7/I_{LIM}$$

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

SERIES ISOLATION RESISTOR, R_S

To insure stability with all capacitive loads a series isolation resistor should be included between the output and the load as shown in the external connections drawing. A 1Ω resistor works well for capacitive loads between 135pF and 44nF. The resistor will affect the rise and fall time of the output pulse at the capacitive load. This can be compensated for on the input signal.

BACKPLATE GROUNDING

The substrate of the MP103 is an insulated metal substrate. It is required that it be connected to signal ground. This is accomplished when the ground pin (Pin 32) is properly connected signal ground.

MP108 • MP108A

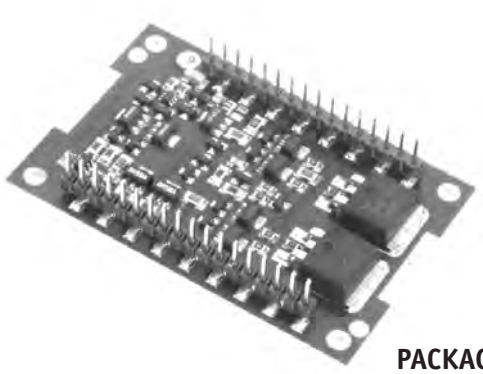
Power Operational Amplifier

FEATURES

- LOW COST
- HIGH VOLTAGE - 200 VOLTS
- HIGH OUTPUT CURRENT - 10 AMPS
- 100 WATT DISSIPATION CAPABILITY
- 300kHz POWER BANDWIDTH

APPLICATIONS

- INKJET PRINTER HEAD DRIVE
- PIEZO TRANSDUCER DRIVE
- INDUSTRIAL INSTRUMENTATION
- REFLECTOMETERS
- ULTRA-SOUND TRANSDUCER DRIVE

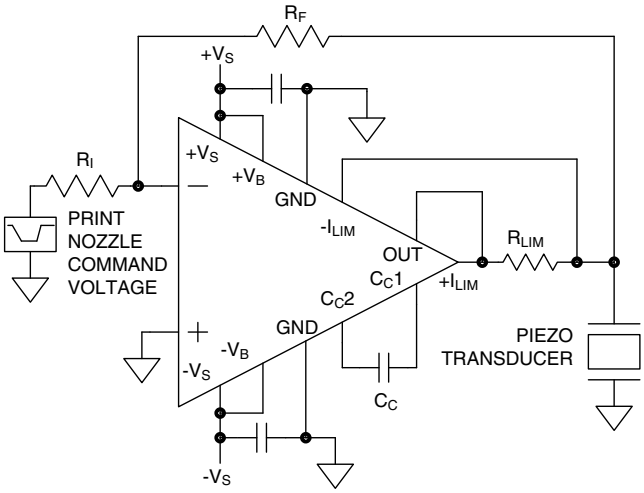


34-PIN DIP
PACKAGE STYLE FD

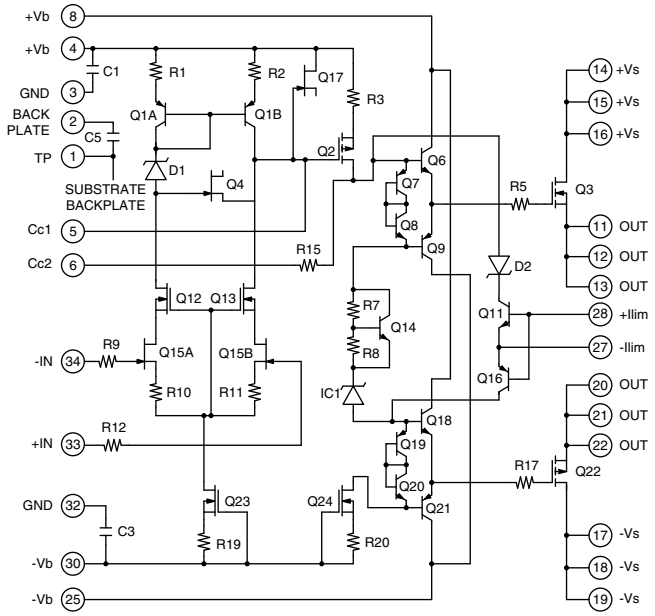
DESCRIPTION

The MP108 operational amplifier is a surface mount constructed component that provides a cost effective solution in many industrial applications. The MP108 offers outstanding performance that rivals much more expensive hybrid components yet has a footprint of only 4 sq in. The MP108 has many optional features such as four-wire current limit sensing and external compensation. The 300 kHz power bandwidth and 10 amp output of the MP108 makes it a good choice for piezo transducer drive applications. The MP108 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

TYPICAL APPLICATION



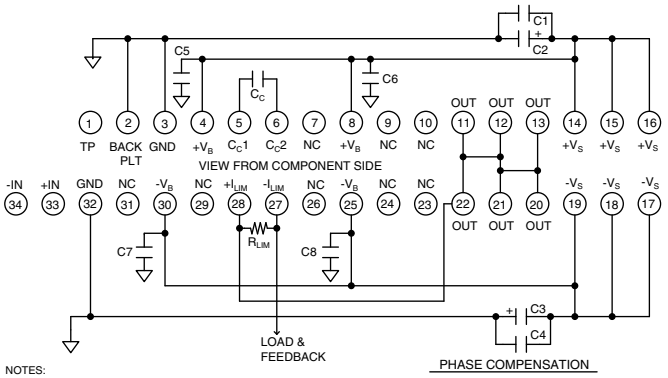
EQUIVALENT CIRCUIT DIAGRAM



INKJET NOZZLE DRIVE

The MP108's fast slew rate and wide power bandwith make it an ideal nozzle driver for industrial inkjet printers. The 10 amp output capability can drive hundreds of nozzles simultaneously.

EXTERNAL CONNECTIONS



NOTES:
C_C IS NPO (COG) RATED FOR FULL SUPPLY VOLTAGE $+V_S$ TO $-V_S$
BOTH PINS 3 AND 32 REQUIRED CONNECTED TO SIGNAL GROUND
C2 AND C3 ELECTROLYTIC 10µF PER AMP OUTPUT CURRENT
C1,C4,C5-8 HIGH QUALITY CERAMIC 0.1µF
ALL OUTPUT PINS MUST BE TIED TOGETHER

PHASE COMPENSATION

C_C	GAIN W/O BOOST	TYP. SLEW RATE
100pF	1	55 V/µS
33pF	4	135 V/µS
10pF	10	170 V/µS
C_C	GAIN W BOOST	TYP. SLEW RATE
470pF	1	12 V/µS
220pF	3	35 V/µS
33pF	10	135 V/µS

ABSOLUTE MAXIMUM RATINGS

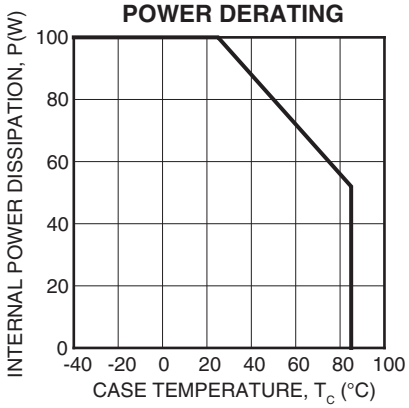
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
SUPPLY VOLTAGE, $+V_B$	$+V_S$ + 15V[6]
SUPPLY VOLTAGE, $-V_B$	$-V_S$ – 15V[6]
OUTPUT CURRENT, peak	12A, within SOA
POWER DISSIPATION, internal, DC	100W
INPUT VOLTAGE	$+V_B$ to $-V_B$
TEMPERATURE, pin solder, 10s	225°C.
TEMPERATURE, junction[2]	150°C.
TEMPERATURE RANGE, storage	-40 to 105°C.
OPERATING TEMPERATURE, case	-40 to 85°C.

SPECIFICATIONS

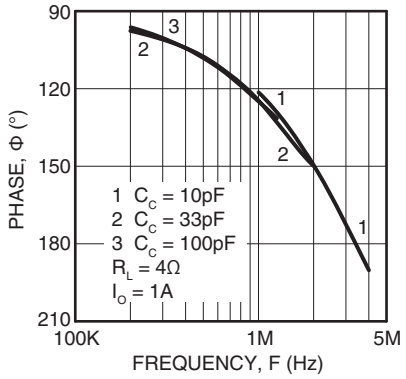
PARAMETER	TEST CONDITIONS[1]	MP108 MIN	MP108 TYP	MP108 MAX	MP108A MIN	MP108A TYP	MP108A MAX	UNITS
INPUT								
OFFSET VOLTAGE			1	5		*	3	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50		*	*	µV/°C
OFFSET VOLTAGE vs. supply				20			*	µV/V
BIAS CURRENT, initial[3]				100			70	pA
BIAS CURRENT vs. supply				0.1			*	pA/V
OFFSET CURRENT, initial				50			30	pA
INPUT RESISTANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE				$+V_B$ - 15			*	V
COMMON MODE VOLTAGE RANGE				$-V_B$ + 15			*	V
COMMON MODE REJECTION, DC		92			*			dB
NOISE	1MHz bandwidth, 1kΩ R_S		10			*		µV RMS
GAIN								
OPEN LOOP @ 15Hz	R_L = 10KΩ, C_C = 10pF	96			*			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C = 10pF		10			*		MHz
PHASE MARGIN	Full temperature range	45			*			degrees
OUTPUT								
VOLTAGE SWING	I_O = 10A	$+V_S$ - 10	$+V_S$ - 8.6		*	*		V
VOLTAGE SWING	I_O = -10A	$-V_S$ + 10	$-V_S$ + 7		*	*		V
VOLTAGE SWING	I_O = 10A, $+V_B$ = $+V_S$ +10V	$+V_S$ - 1.6			*			V
VOLTAGE SWING	I_O = -10A, $-V_B$ = $-V_S$ -10V	$-V_S$ + 5.1			*			V
CURRENT, continuous, DC		10			11			A
SLEW RATE, A_V = -20	C_C = 10pF	150	170		*	*		V/µS
SETTLING TIME, to 0.1%	2V Step		1			*		µS
RESISTANCE	No load, DC		5			*		Ω
POWER BANDWIDTH 180V_{P-P}	C_C = 10pF, $+V_S$ = 100V, $-V_S$ = -100V		300			*		kHz
POWER SUPPLY								
VOLTAGE		±15	±75	±100	*	*	*	V
CURRENT, quiescent			50	65		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, f ≤ 60Hz			1			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz			1.25			*	°C/W
RESISTANCE, junction to air	Full temperature range			13			*	°C/W
TEMPERATURE RANGE, case		-40		85	*		*	°C

NOTES:
1. Unless otherwise noted: T_C=25°C, compensation C_C=100pF, DC input specifications are value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stage. $+V_B$ and $-V_B$ denote the positive and negative supply voltages to the input stages.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Power supply voltages $+V_B$ and $-V_B$ must not be less than $+V_S$ and $-V_S$ respectively.

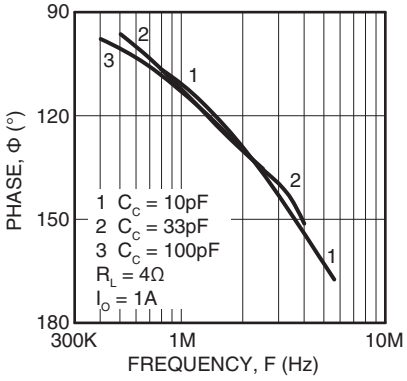
POWER DERATING



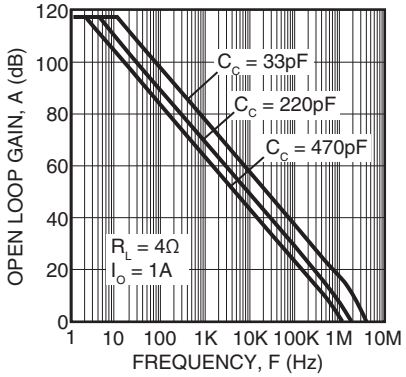
PHASE RESPONSE W/ BOOST



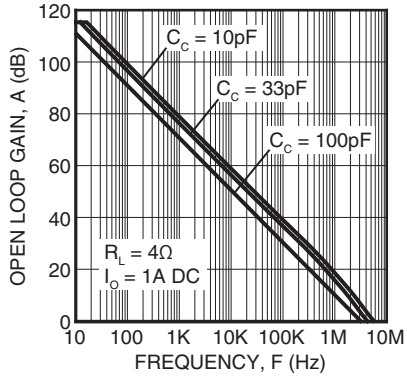
PHASE RESPONSE W/O BOOST



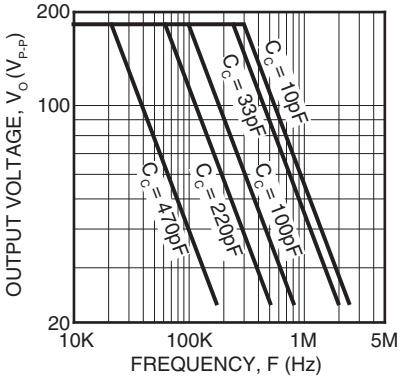
SMALL SIGNAL RESPONSE W/ BOOST



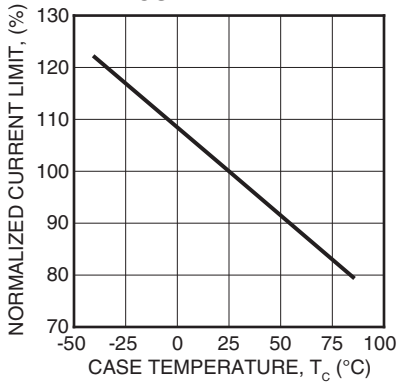
SMALL SIGNAL RESPONSE W/O BOOST



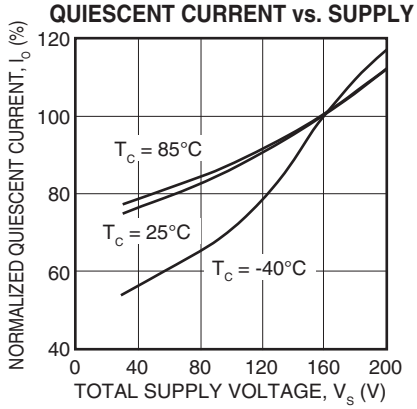
POWER RESPONSE



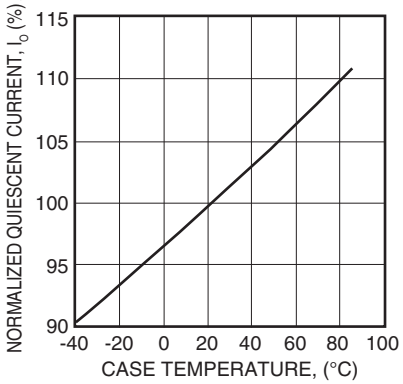
CURRENT LIMIT



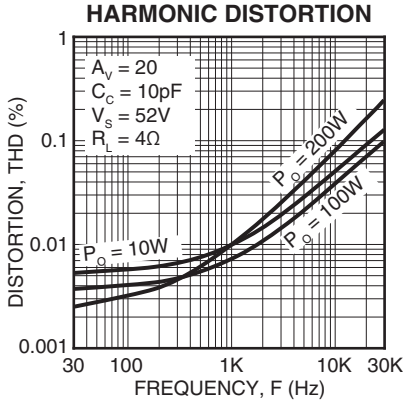
QUIESCENT CURRENT vs. SUPPLY



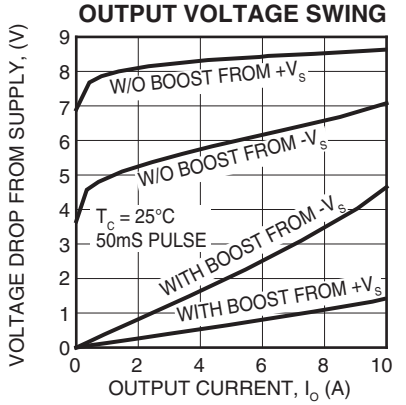
QUIESCENT CURRENT vs. TEMPERATURE



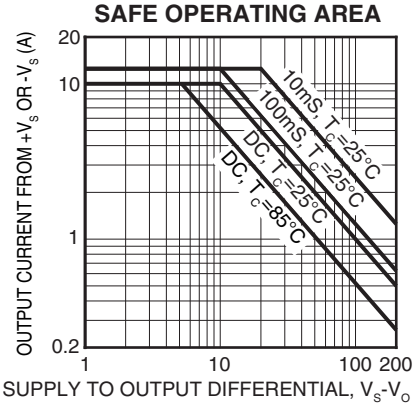
HARMONIC DISTORTION



OUTPUT VOLTAGE SWING



SAFE OPERATING AREA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

The MP108 has two ground pins (pins 3, 32). These pins provide a return for the internal capacitive bypassing of the small signal portions of the MP108. The two ground pins are **not** connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

SAFE OPERATING AREA

The MOSFET output stage of the MP108 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph on previous page). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

COMPENSATION

The external compensation capacitor C_C is connected between pins 5 and 6. Unity gain stability can be achieved with any capacitor value larger than 100pF for a minimum phase margin of 45 degrees. At higher gains more phase shift can usually be tolerated in most designs and the compensation capacitor value can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C for the application. An NPO (COG) type capacitor is required rated for the full supply voltage (200V).

OVERVOLTAGE PROTECTION

Although the MP108 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP108. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. In most applications power supply terminals $+V_B$ and $-V_B$ will be connected to $+V_S$ and $-V_S$ respectively. Supply voltages $+V_B$ and $-V_B$ are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP108 at pins 8 and 25 must be connected to $+V_B$ and $-V_B$ at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See the external connections diagram on page 1.

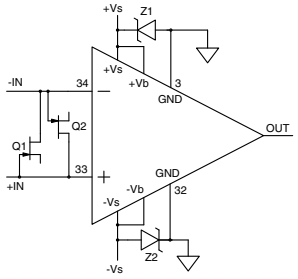


FIGURE 1
OVERVOLTAGE PROTECTION

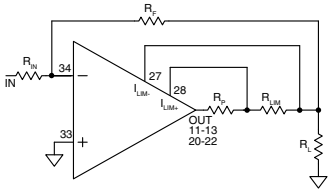


FIGURE 2
4 WIRE CURRENT LIMIT

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances RP, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifierís high current output stage. $+V_B$ (pins 4,8) and $-V_B$ (pins 25,30) are connected to the small signal stages and $+V_S$ (pins 14-16) and $-V_S$ (pins 17-19) are connected to the high current output stage. An additional 10V on the $+V_B$ and $-V_B$ pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to the $+V_B$ and $-V_B$ pins respectively. The $+V_B$ and $-V_B$ pins must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

BACKPLATE GROUNDING

The substrate of the MP108 is an insulated metal substrate. It is required that it be connected to signal ground. Connect pin 2 (back plate) to signal ground. The back plate will then be AC grounded to signal ground through a 1µF capacitor.

MP111 • MP111A

Power Operational Amplifier

FEATURES

- LOW COST
- HIGH VOLTAGE - 100 VOLTS
- HIGH OUTPUT CURRENT- 50 AMP PULSE OUTPUT, 15 AMP CONTINUOUS
- 170 WATT DISSIPATION CAPABILITY
- 130 V/uS SLEW RATE
- 500kHz POWER BANDWIDTH

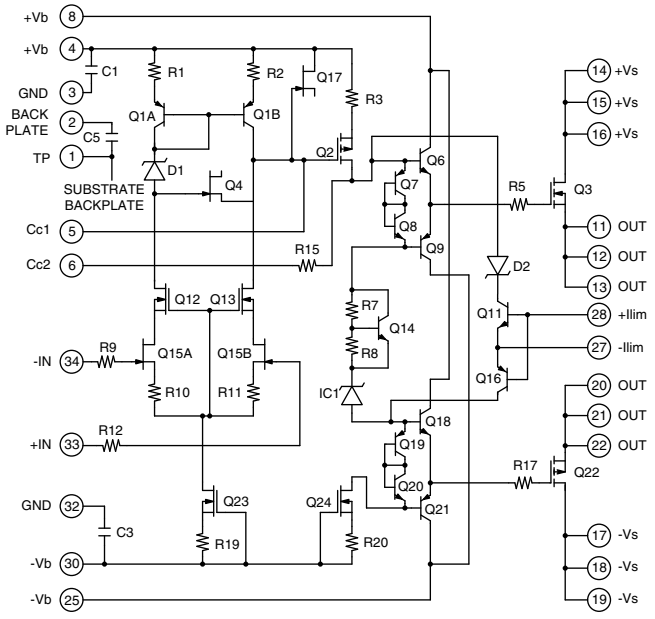
APPLICATIONS

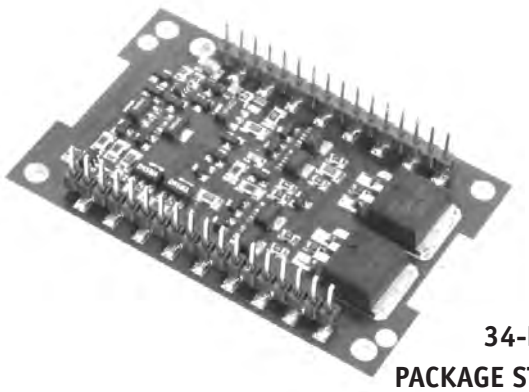
- INKJET PRINTER HEAD DRIVE
- PIEZO TRANSDUCER DRIVE
- INDUSTRIAL INSTRUMENTATION
- REFLECTOMETERS
- ULTRA-SOUND TRANSDUCER DRIVE

DESCRIPTION

The MP111 operational amplifier is a surface mount constructed component that provides a cost-effective solution in many industrial applications. The MP111 offers outstanding performance that rivals much more expensive hybrid components yet has a footprint of only 4 sq in. The MP111 has many optional features such as four-wire current limit sensing and external compensation. The 500 kHz power bandwidth and 15 amp continuous and 50A pulse output of the MP111 makes it a good choice for piezo transducer drive applications. The MP111 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

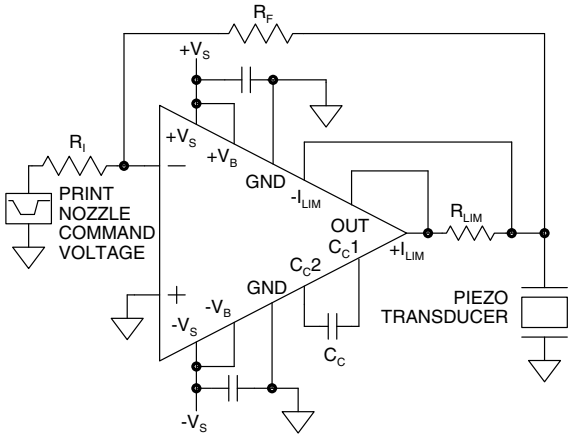
EQUIVALENT CIRCUIT DIAGRAM





34-PIN DIP
PACKAGE STYLE FD

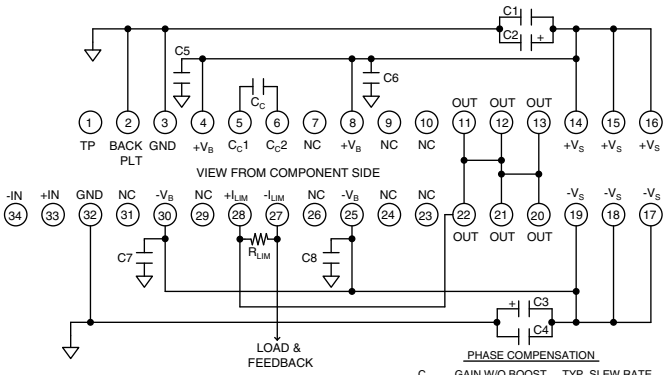
TYPICAL APPLICATION



INKJET NOZZLE DRIVE

The MP111's fast slew rate and wide power bandwith make it an ideal nozzle driver for industrial inkjet printers. The 50 amp pulse output capability can drive hundreds of inkjet nozzles simultaneously.

EXTERNAL CONNECTIONS



NOTES:
C_C IS NPO (COG) RATED FOR FULL SUPPLY VOLTAGE $+V_S$ TO $-V_S$.
BOTH PINS 3 AND 32 REQUIRED CONNECTED TO SIGNAL GROUND.
C2 AND C3 ELECTROLYTIC ≥ 10µF PER AMP OUTPUT CURRENT.
C1, C4, C5-8 HIGH QUALITY CERAMIC ≥ 0.1µF.
ALL OUTPUT PINS MUST BE TIED TOGETHER.
SEE PACKAGE OUTLINE FD IN THE OUTLINE DIMENSIONS DATASHEET.

PHASE COMPENSATION

C_C	GAIN W/O BOOST	TYP. SLEW RATE
100pF	≥1	55 V/µS
68pF	≥4	60 V/µS
33pF	≥10	130 V/µS

C_C	GAIN W BOOST	TYP. SLEW RATE
470pF	≥3	12 V/µS
220pF	≥6	27 V/µS
100pF	≥10	55 V/µS

ABSOLUTE MAXIMUM RATINGS

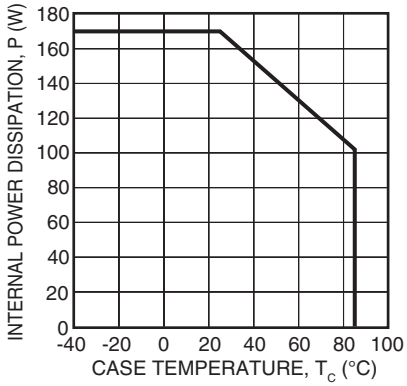
EXTERNAL CONNECTIONS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
SUPPLY VOLTAGE, $+V_B$	$+V_S$ + 15V[6]
SUPPLY VOLTAGE, $-V_B$	$-V_S$ – 15V[6]
OUTPUT CURRENT, peak	50A, within SOA
POWER DISSIPATION, internal, DC	170W
INPUT VOLTAGE	$+V_B$ to $-V_B$
DIFFERENTIAL INPUT VOLTAGE	±25V
TEMPERATURE, pin solder, 10s	225°C.
TEMPERATURE, junction[2]	175°C.
TEMPERATURE RANGE, storage	-40 to 105°C.
OPERATING TEMPERATURE, case	-40 to 85°C.

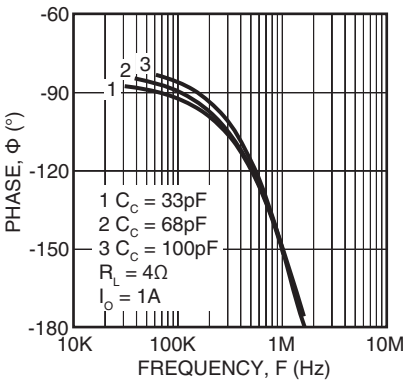
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE			1	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial[3]				100	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT RESISTANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE				$+V_B$ - 15	V
COMMON MODE VOLTAGE RANGE				$-V_B$ + 15	V
COMMON MODE REJECTION, DC		92			dB
NOISE	1MHz bandwidth, 1kΩ R_S		10		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 10KΩ, C_C = 33pF	96			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C = 33pF		6		MHz
PHASE MARGIN	Full temperature range	45			degrees
OUTPUT					
VOLTAGE SWING	I_O = 15A	$+V_S$ - 10	$+V_S$ - 8.4		V
VOLTAGE SWING	I_O = -15A	$-V_S$ + 10	$-V_S$ + 5.8		V
VOLTAGE SWING	I_O = 15A, $+V_B$ = $+V_S$ +10V	$+V_S$ - 0.8			V
VOLTAGE SWING	I_O = -15A, $-V_B$ = $-V_S$ -10V	$-V_S$ + 1.0			V
CURRENT, continuous, DC		15			A
SLEW RATE, A_V = -20	C_C = 33pF	100	130		V/µS
SETTLING TIME, to 0.1%	2V Step		1		µS
RESISTANCE	No load, DC		3		Ω
POWER BANDWIDTH 80V_{P-P}	C_C = 33pF, $+V_S$ = 50V, $-V_S$ = -50V		500		kHz
POWER SUPPLY					
VOLTAGE		±15	±45	±50	V
CURRENT, quiescent			142	157	mA
THERMAL					
RESISTANCE, AC, junction to case[5]	Full temperature range, f ≥ 60Hz			.65	°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz			.88	°C/W
RESISTANCE, junction to air	Full temperature range			13	°C/W
TEMPERATURE RANGE, case		-40		85	°C

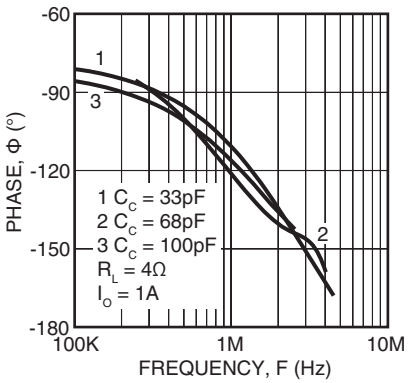
POWER DERATING



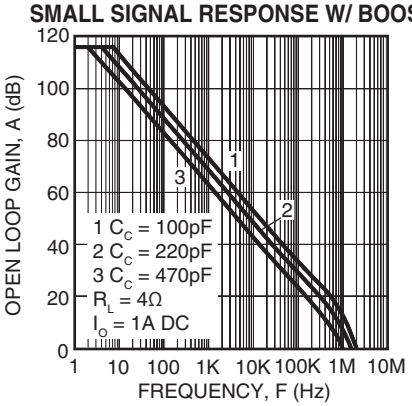
PHASE RESPONSE W/ BOOST



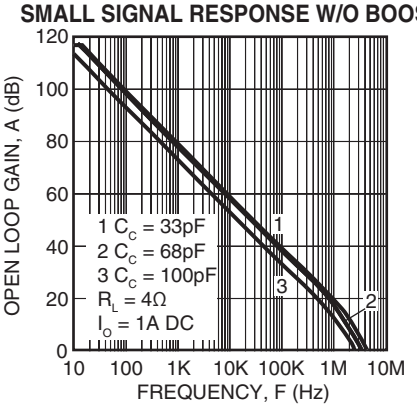
PHASE RESPONSE W/O BOOST



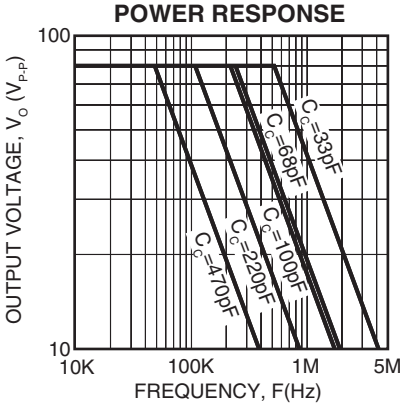
SMALL SIGNAL RESPONSE W/ BOOST



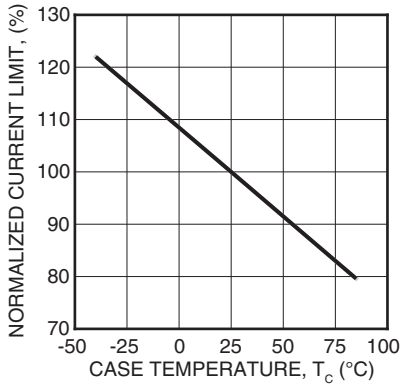
SMALL SIGNAL RESPONSE W/O BOOST



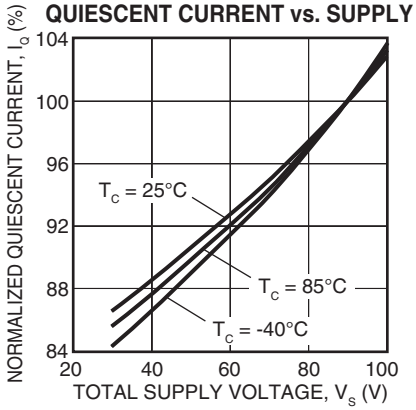
POWER RESPONSE



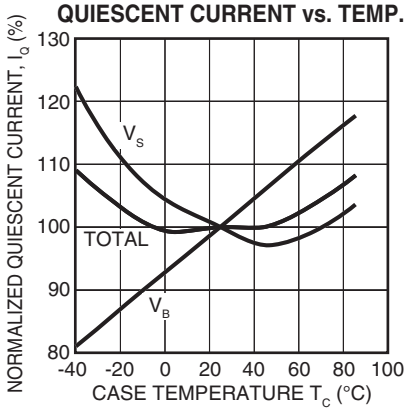
CURRENT LIMIT



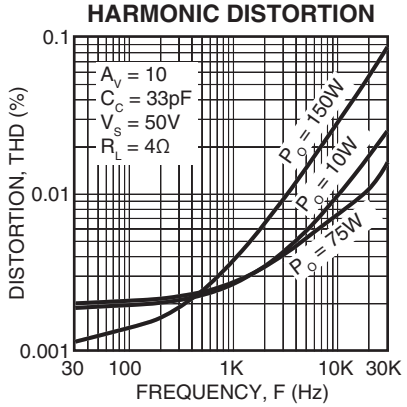
QUIESCENT CURRENT vs. SUPPLY



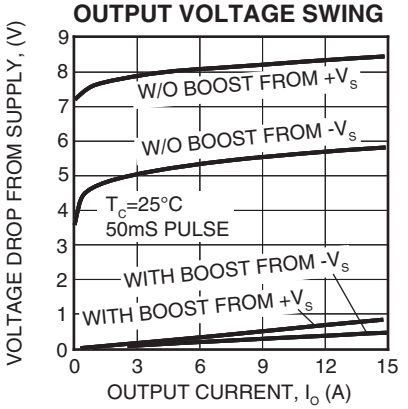
QUIESCENT CURRENT vs. TEMP.



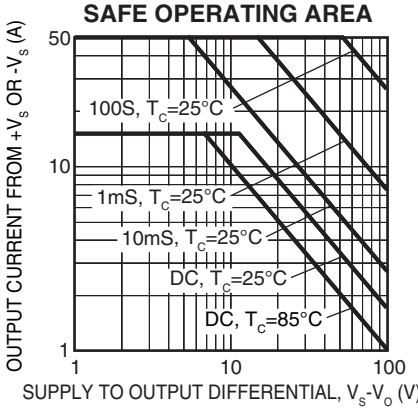
HARMONIC DISTORTION



OUTPUT VOLTAGE SWING



SAFE OPERATING AREA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

The MP111 has two ground pins (pins 3, 32). These pins provide a return for the internal capacitive bypassing of the small signal portions of the MP111. The two ground pins are not connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

SAFE OPERATING AREA

The MOSFET output stage of the MP111 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph on previous page). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

COMPENSATION

The external compensation capacitor C_C is connected between pins 5 and 6. Unity gain stability can be achieved with any capacitor value larger than 100pF for a minimum phase margin of 45 degrees. At higher gains more phase shift can usually be tolerated in most designs and the compensation capacitor value can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C for the application. An NPO (COG) type capacitor is required rated for the full supply voltage (100V).

OVERVOLTAGE PROTECTION

Although the MP111 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP111. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. In most applications power supply terminals +Vb and -Vb will be connected to $+V_S$ and $-V_S$ respectively. Supply voltages +Vb and -Vb are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP111 at pins 8 and 25 must be connected to +Vb and

-Vb at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See the external connections diagram on page 1.

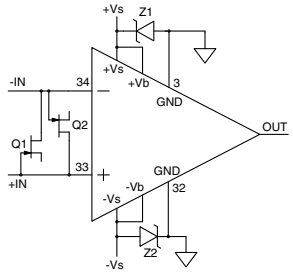


FIGURE 1
OVERVOLTAGE PROTECTION

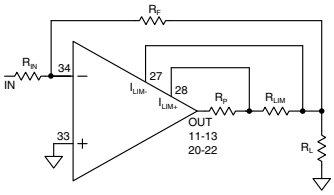


FIGURE 2
4 WIRE CURRENT LIMIT

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances R_P, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifier's high current output stage. +Vb (pins 4,8) and -Vb (pins 25,30) are connected to the small signal stages and $+V_S$ (pins 14-16) and $-V_S$ (pins 17-19) are connected to the high current output stage. An additional 10V on the +Vb and -Vb pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to the +Vb and -Vb pins respectively. The +Vb and -Vb pins must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

BACKPLATE GROUNDING

The substrate of the MP111 is an insulated metal substrate. It is required that it be connected to signal ground. Connect pin 2 (back plate) to signal ground. The back plate will then be AC grounded to signal ground through a 1µF capacitor.

Power Operational Amplifier

FEATURES

- LOW COST
- HIGH VOLTAGE - 100 VOLTS
- HIGH OUTPUT CURRENT - 30 AMPS
- 210 WATT DISSIPATION CAPABILITY

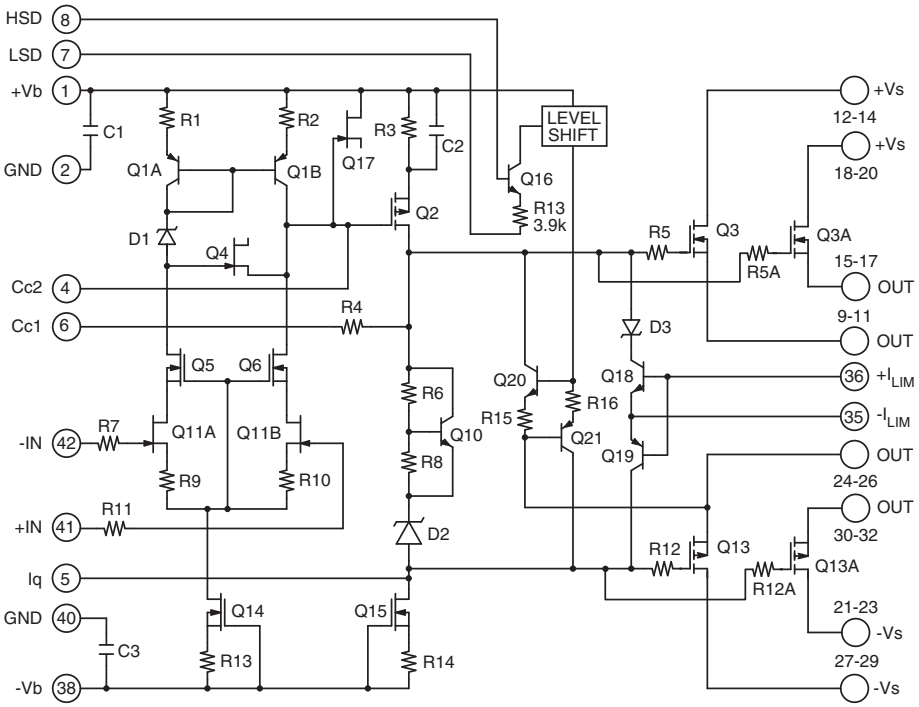
APPLICATIONS

- MOTOR DRIVE
- MAGNETIC DEFLECTION
- PROGRAMMABLE POWER SUPPLIES
- INDUSTRIAL AUDIO AMPLIFIER

GENERAL DESCRIPTION

The MP230 operational amplifier is a surface mount constructed component that provides a cost effective solution in many industrial applications. The MP230 offers outstanding performance that rivals many much more expensive hybrid components yet has a footprint of only 4.7 sq in. The MP230 has many optional features such as four-wire current limit sensing, a shutdown control and external compensation. In addition, the class A/B output stage biasing can be turned off for lower quiescent current with class C operation in applications where crossover distortion is less important such as when driving motors, for example. A boost voltage feature biases the output stage for close linear swings to the supply rail for extra efficient operation. The MP230 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

EQUIVALENT CIRCUIT DIAGRAM



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$				100	V
SUPPLY VOLTAGE, $+V_B$ (BOOST)	(Note 6)			$+V_S$ + 15	V
SUPPLY VOLTAGE, $-V_B$ (BOOST)	(Note 6)			$-V_S$ – 15V	V
OUTPUT CURRENT, peak, within SOA				40	A
POWER DISSIPATION, internal, DC				210	W
INPUT VOLTAGE				$+V_B$ to $-V_B$	V
TEMPERATURE, pin solder, 10s				225	°C
TEMPERATURE, junction	(Note 2)			175	°C
TEMPERATURE RANGE, storage			−40	105	°C
OPERATING TEMPERATURE, case			−40	85	°C

SPECIFICATIONS

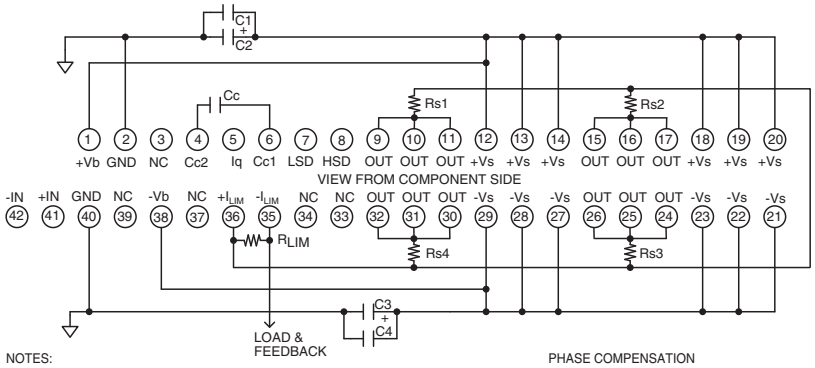
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE			1	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial (Note 3)				100	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT IMPEDANCE, DC			100		GΩ
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE				$+V_S$ - 13	V
COMMON MODE VOLTAGE RANGE				$-V_S$ + 13	V
COMMON MODE REJECTION, DC		92			dB
NOISE	100kHz bandwidth, 1kΩ R_S		5		µV RMS
SHUTDOWN, active	HSD - LSD	4.5	5	5.5	V
SHUTDOWN, inactive	HSD - LSD	-0.5	0	0.25	V
GAIN					
OPEN LOOP @ 15Hz	R_L = 1KΩ, C_C = 100pF	96			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C = 100pF		2		MHz
PHASE MARGIN	Full temperature range	60			°
OUTPUT					
VOLTAGE SWING	I_O = 30A	$+V_S$ - 10	$+V_S$ - 7		V
VOLTAGE SWING	I_O = -30A	$-V_S$ + 10	$-V_S$ + 8		V
VOLTAGE SWING	I_O = 30A, $+V_B$ = $+V_S$ +10V	$+V_S$ - 1.5			V
VOLTAGE SWING	I_O = -30A, $-V_B$ = $-V_S$ -10V	$-V_S$ + 3.0			V
CURRENT, continuous, DC		30			A
SLEW RATE, A_V = -10	C_C = 100pF	12	15		V/µS

Parameter	Test Conditions	Min	Typ	Max	Units
SETTLING TIME, to 0.1%	A_V = -1, 10V Step, C_C = 470pF		2.5		µS
RESISTANCE, open loop	DC, 10A Load		0.1		Ω
POWER SUPPLY					
VOLTAGE		±15	±45	±50	V
CURRENT, quiescent, total			27	35	mA
CURRENT, boost supply			17		mA
CURRENT, shutdown or class C quiescent			17		mA
THERMAL					
RESISTANCE, AC, junction to case (Note 5)	Full temp range, f ≥ 60Hz			0.6	°C/W
RESISTANCE, DC, junction to case	Full temp range, f < 60Hz			0.7	°C/W
RESISTANCE, junction to air	Full temp range			14	°C/W
TEMPERATURE RANGE, case		-40		85	°C

NOTES:

1. Unless otherwise noted: T_C = 25°C, compensation C_C = 470pF, DC input specifications are ± value given, power supply voltage is typical rating. Amplifier operated without boost feature.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the + and - output stage supply voltages. $+V_B$ and $-V_B$ denote the + and - input stage supply voltages (boost voltages).
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Power supply voltages $+V_B$ and $-V_B$ must not be less than $+V_S$ and $-V_S$ respectively.

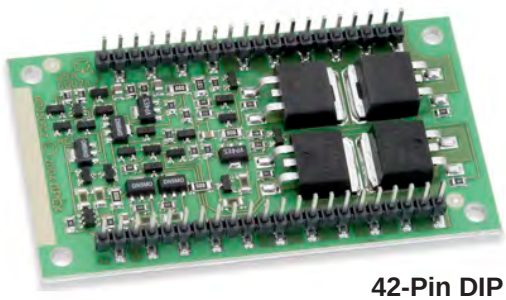
EXTERNAL CONNECTIONS



NOTES:
C_C IS NPO (COG) RATED FOR FULL SUPPLY VOLTAGE $+V_S$ TO $-V_S$.
BOTH PINS 2 AND 40 REQUIRED CONNECTED TO SIGNAL GROUND.
C2 AND C3 ELECTROLYTIC ≤10µF PER AMP OUTPUT CURRENT.
C1 AND C4 HIGH QUALITY CERAMIC ≤0.1µF.
SEE TEXT FOR SELECTION OF VALUES FOR Rs1 - Rs4.

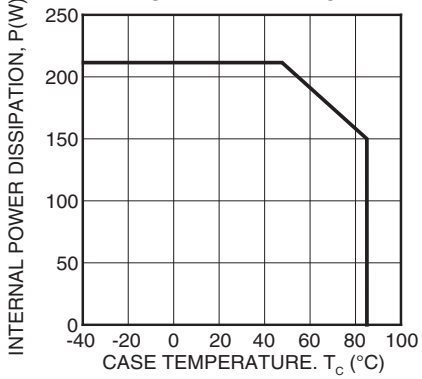
PHASE COMPENSATION

C_C	GAIN W/O BOOST	GAIN W/BOOST	TYP. SLEW RATE
470pF	≤1	≤8	8V/µS
220pF	≤4	≤15	12V/µS
100pF	≤10	≤30	15V/µS

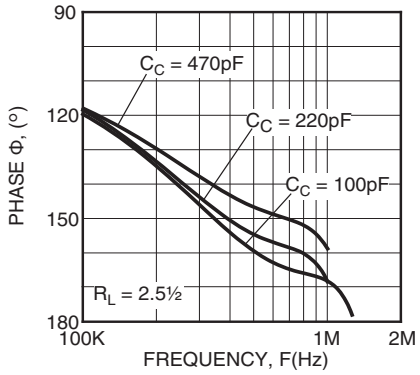


42-Pin DIP
Package Style FC

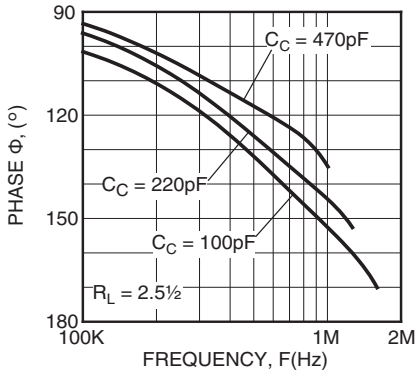
POWER DERATING



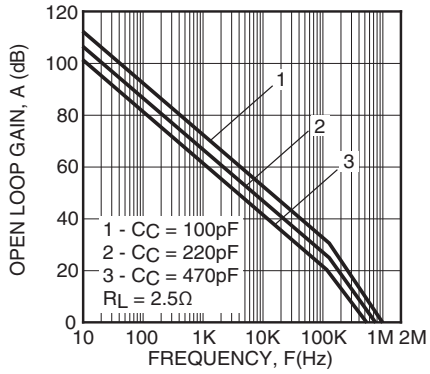
PHASE RESPONSE W/BOOST



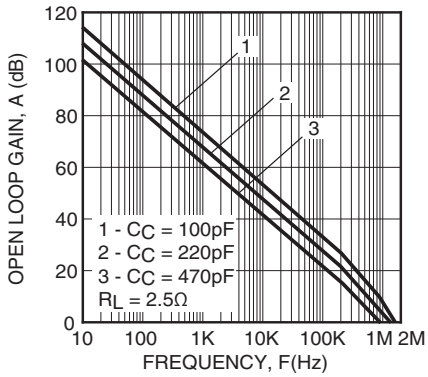
PHASE RESPONSE W/O BOOST



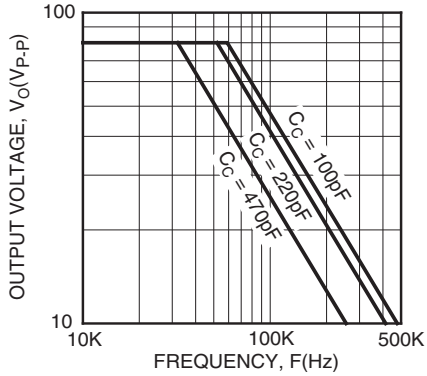
SMALL SIGNAL RESPONSE W/ BOOST



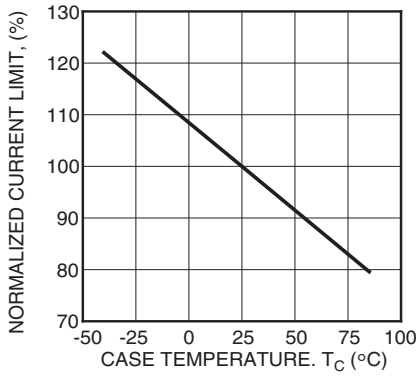
SMALL SIGNAL RESPONSE W/O BOOST



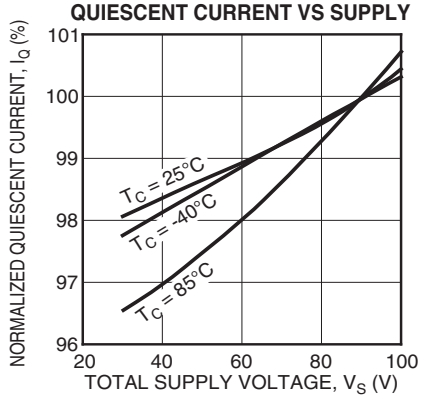
POWER RESPONSE



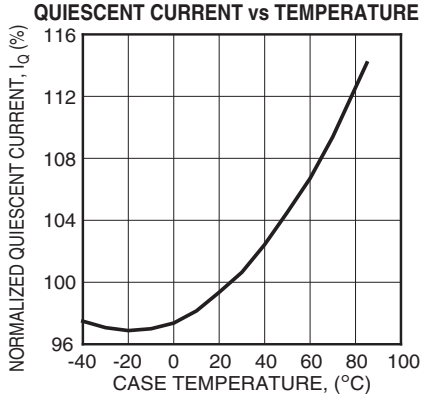
CURRENT LIMIT



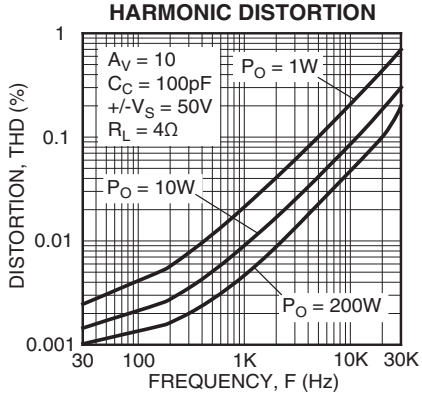
QUIESCENT CURRENT VS SUPPLY



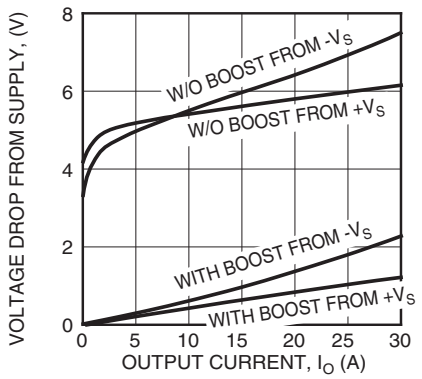
QUIESCENT CURRENT vs TEMPERATURE



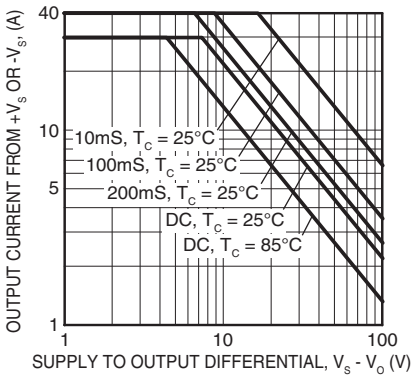
HARMONIC DISTORTION



OUTPUT VOLTAGE SWING



SAFE OPERATING AREA

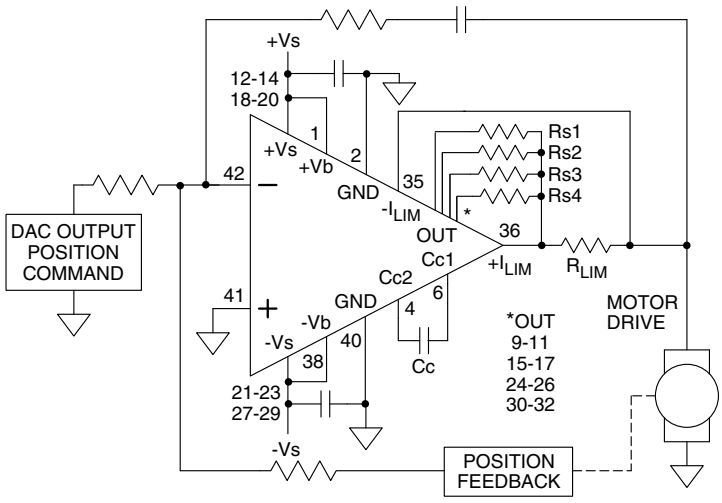


E

TYPICAL APPLICATION

MOTOR POSITION CONTROL

The MOSFET output stage of the MP230 provides superior SOA performance compared to bipolar output stages where secondary breakdown is a concern. The extended SOA is ideal in motor drive applications where the back EMF of the motor may impose simultaneously both high voltage and high current across the output stage transistors. In the figure above a mechanical to electrical feedback position converter allows the MP230 to drive the motor in either direction to a set point determined by the DAC voltage.



GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power’s complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

The MP230 has two ground pins (pins 2, 40). These pins provide a return for the internal capacitive bypassing of the small signal stages of the MP230. The two ground pins are not connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

BALANCING RESISTOR SELECTION (R_{S1}-R_{S4})

The MP230 uses parallel sets of output transistors. To ensure that the load current is evenly shared among the transistors external balancing resistors R_{S1}-R_{S4} are required. To calculate the required value for each of the resistors use: $R = 4.5 / I^2$,where I is the maximum expected output current. For example, with a maximum output current of 10A each balancing resistor should be 0.045 ohms. Each resistor dissipates 1.125W at the maximum current. Use a **non-inductive** 2W rated resistor. A ready source for such resistors is the IRC resistor series LR available from Mouser Electronics.

SAFE OPERATING AREA

The MOSFET output stage of the MP230 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph on previous page). The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

COMPENSATION

The external compensation capacitor C_C is connected to pins 4 and 6. Unity gain stability can be achieved with C_C = 470pF for a minimum phase margin of 60 degrees. At higher gains more phase shift can usually be tolerated and C_C can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C. A 100V NPO (COG) type capacitor is required. Boost operation requires more compensation or higher gains than with normal operation due to the increased capacitance of the output transistors when the output signal swings close to the supply rails.

OVERVOLTAGE PROTECTION

Although the MP230 can withstand differential input voltages up to ±25V, in some applications additional external protection may be needed. 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be

required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

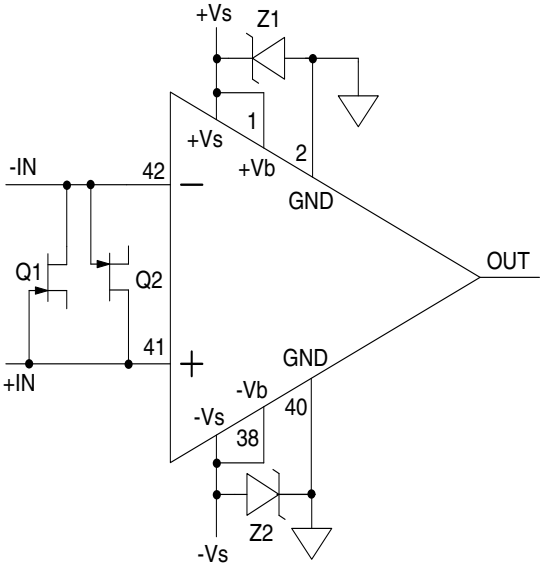


FIGURE 1: OVERVOLTAGE PROTECTION

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP230. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors 0.1µF or greater. In most applications power supply terminals $+V_B$ and $-V_B$ will be connected to $+V_S$ and $-V_S$ respectively. Although $+V_B$ and $-V_B$ are bypassed internally it is recommended to bypass $+V_B$ and $-V_B$ with 0.1µF externally. Additionally, ground pins 2 and 40 must be connected to the system signal ground.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 36 must be connected to the amplifier output side and pin 35 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances RP, formed by socket and solder joints as well as internal amplifi er losses.The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

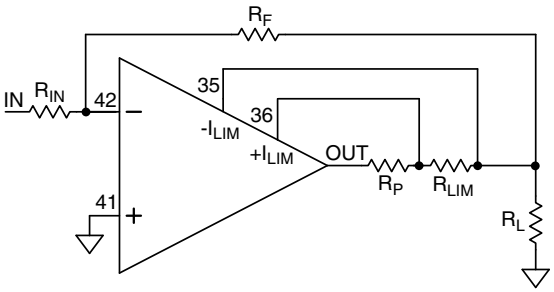


FIGURE 2: 4 WIRE CURRENT LIMIT

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifier's high current output stage. $+V_B$ (pin 1) and $-V_B$ (pin 38) are connected to the small signal stages. An additional 10V on the $+V_B$ and $-V_B$ pin is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to $+V_B$ and $-V_B$ respectively. $+V_B$ and $-V_B$ must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

SHUTDOWN

The output stage is turned off by applying a 5V level to HSD (pin 8) relative to LSD (pin 7). This is a non-latching circuit. As long as HSD remains high relative to LSD the output stage will be turned off. LSD will normally be tied to signal ground but LSD may float from $-V_B$ to $+V_B$ - 15V. Shutdown can be used to lower quiescent current for standby operation or as part of a load protection circuit.

BIAS CLASS OPTION

Normally pin 5 (Iq) is left open. But when pin 5 is connected to pin 6 (Cc1) the quiescent current in the output stage is disabled. This results in lower quiescent power, but also class C operation of the output stage and the resulting crossover distortion. In many applications, such as driving motors, the distortion may be unimportant and lower standby power dissipation is an advantage.

Power Operational Amplifier

FEATURES

- LOW COST
- HIGH VOLTAGE - 200 VOLTS
- HIGH OUTPUT CURRENT - 20 AMPS
- 170 WATT DISSIPATION CAPABILITY

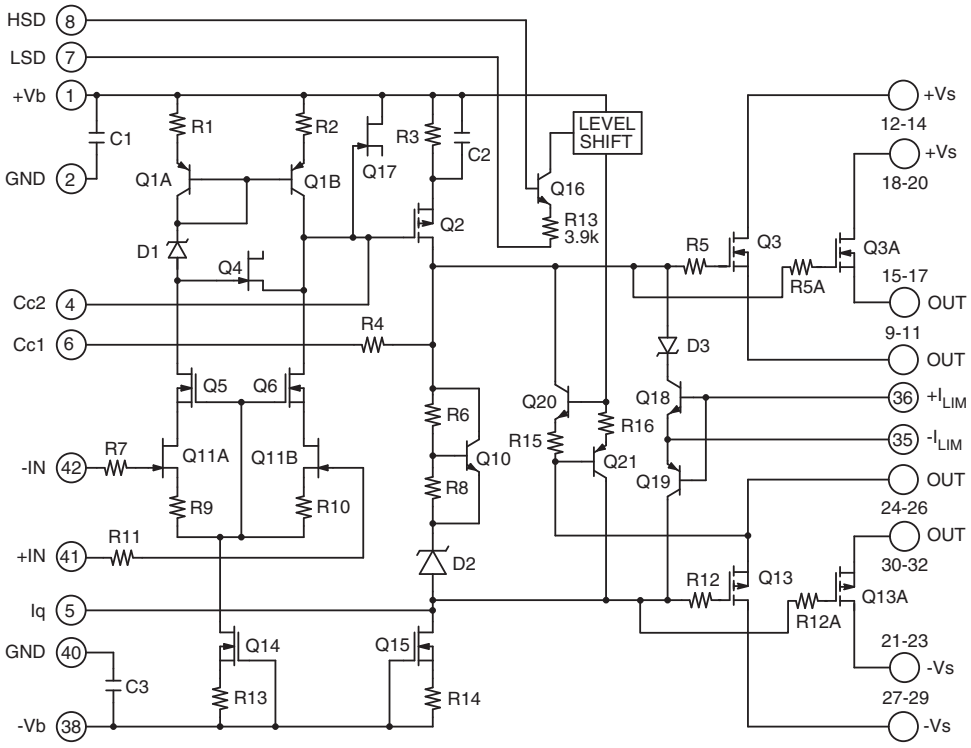
APPLICATIONS

- MOTOR DRIVE
- MAGNETIC DEFLECTION
- PROGRAMMABLE POWER SUPPLIES
- INDUSTRIAL AUDIO AMPLIFIER

GENERAL DESCRIPTION

The MP240 operational amplifier is a surface mount constructed component that provides a cost effective solution in many industrial applications. The MP240 offers outstanding performance that rivals much more expensive hybrid components yet has a footprint of only 4.7 sq in. The MP240 has many optional features such as four-wire current limit sensing, a shutdown control and external compensation. In addition, the class A/B output stage biasing can be turned off for lower quiescent current with class C operation in applications where crossover distortion is less important such as when driving motors, for example. A boost voltage feature biases the output stage for close linear swings to the supply rail for extra efficient operation. The MP240 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

EQUIVALENT CIRCUIT DIAGRAM



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$				200	V
OUTPUT CURRENT, $+V_B$	(Note 6)			$+V_S$ + 15V	V
POWER DISSIPATION, $-V_B$	(Note 6)			$-V_S$ - 15V	V
OUTPUT CURRENT, peak, within SOA				25	A
POWER DISSIPATION, internal, DC				170	W
INPUT VOLTAGE				$+V_B$ to $-V_B$	V
TEMPERATURE, pin solder, 10s				225	°C
TEMPERATURE, junction	(Note 2)			150	°C
TEMPERATURE RANGE, storage			−40	105	°C
OPERATING TEMPERATURE, case			−40	85	°C

SPECIFICATIONS

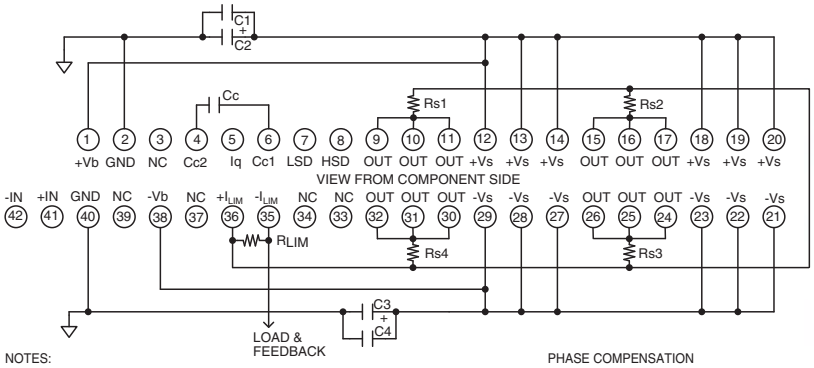
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE			1	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial (Note 3)				100	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT IMPEDANCE, DC			100		GΩ
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE				$+V_B$ - 15	V
COMMON MODE VOLTAGE RANGE				$-V_B$ + 15	V
COMMON MODE REJECTION, DC		92			dB
DIFFERENTIAL INPUT VOLTAGE				±25	V
NOISE	1MHz bandwidth, 1kΩ R_S		5		µV RMS
SHUTDOWN, active	HSD - LSD	4.5	5	5.5	V
SHUTDOWN, inactive	HSD - LSD	-0.5	0	0.25	V
GAIN					
OPEN LOOP @ 15Hz	R_L = 1KΩ, C_C = 100pF	96			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C = 100pF		1.8		MHz
PHASE MARGIN	Full temperature range	60			°
OUTPUT					
VOLTAGE SWING	I_O = 20A	$+V_S$ - 10	$+V_S$ - 7		V
VOLTAGE SWING	I_O = -20A	$-V_S$ + 10	$-V_S$ + 8		V
VOLTAGE SWING	I_O = 20A, $+V_B$ = $+V_S$ +10V	$+V_S$ - 3.0	$+V_S$ - 2.0		V
VOLTAGE SWING	I_O = -20A, $-V_B$ = $-V_S$ -10V	$-V_S$ + 6.0	$-V_S$ + 5.0		V
CURRENT, continuous, DC		20			A
SLEW RATE, A_V = -10	C_C = 100pF	12	14		V/µS

Parameter	Test Conditions	Min	Typ	Max	Units
SETTLING TIME, to 0.1%	A_V = -1, 10V Step, C_C = 680pF		5		µS
RESISTANCE, open loop	DC, 10A Load		0.2		Ω
POWER SUPPLY					
VOLTAGE		±15	±75	±100	V
CURRENT, quiescent, total			16.5	25	mA
CURRENT, shutdown or class C quiescent			8.5		mA
CURRENT, boost supply			8.5		mA
THERMAL					
RESISTANCE, AC, junction to case (Note 5)	Full temp range, f ≥ 60Hz			0.58	°C/W
RESISTANCE, DC, junction to case	Full temp range, f < 60Hz			0.73	°C/W
RESISTANCE, junction to air	Full temp range			14	°C/W
TEMPERATURE RANGE, case		-40		85	°C

NOTES:

1. Unless otherwise noted: T_C = 25°C, compensation C_C = 680pF, DC input specifications are ± value given, power supply voltage is typical rating. Amplifier operated without boost feature.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the + and - output stage supply voltages. $+V_B$ and $-V_B$ denote the + and - input stage supply voltages (boost voltages).
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Power supply voltages $+V_B$ and $-V_B$ must not be less than $+V_S$ and $-V_S$ respectively.

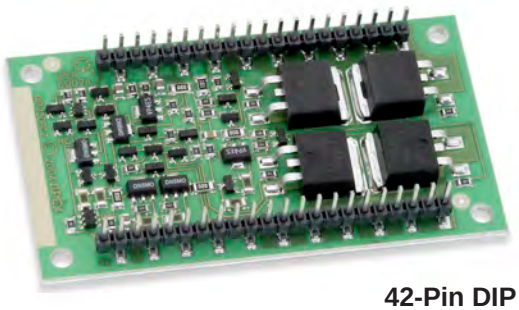
EXTERNAL CONNECTIONS



NOTES:
C_C IS NPO (COG) RATED FOR FULL SUPPLY VOLTAGE $+V_S$ TO $-V_S$.
BOTH PINS 2 AND 40 REQUIRED CONNECTED TO SIGNAL GROUND.
C2 AND C3 ELECTROLYTIC ≤10µF PER AMP OUTPUT CURRENT.
C1 AND C4 HIGH QUALITY CERAMIC ≤0.1µF.
SEE TEXT FOR SELECTION OF VALUES FOR Rs1 - Rs4.

PHASE COMPENSATION

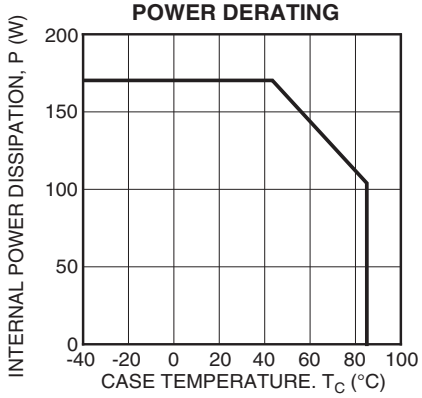
C_C	GAIN W/O BOOST	GAIN W/BOOST	TYP. SLEW RATE
680pF	≤1	≤3	3V/µS
330pF	≤3	≤6	6V/µS
100pF	≤10	≤13	14V/µS



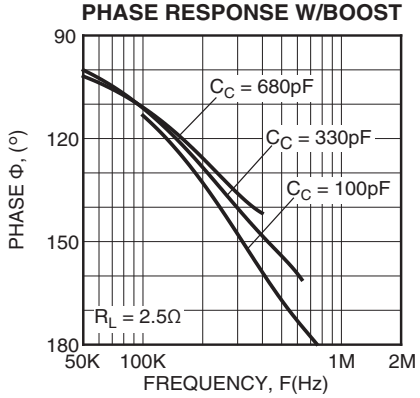
42-Pin DIP
Package Style FC

TYPICAL PERFORMANCE GRAPHS

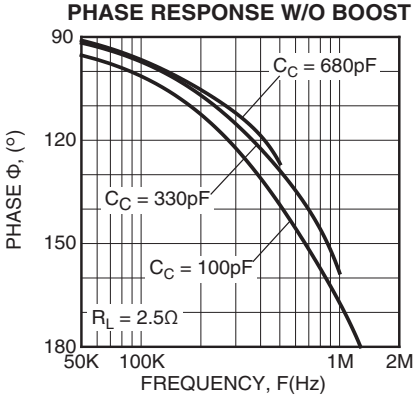
POWER DERATING



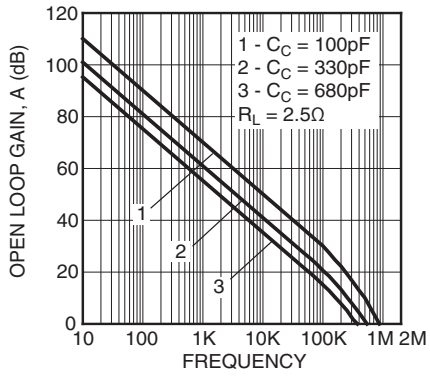
PHASE RESPONSE W/BOOST



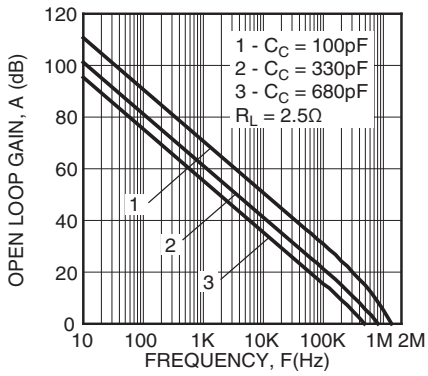
PHASE RESPONSE W/O BOOST



SMALL SIGNAL RESPONSE W/ BOOST



SMALL SIGNAL RESPONSE W/O BOOST



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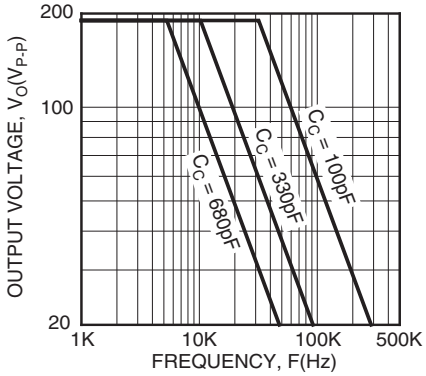
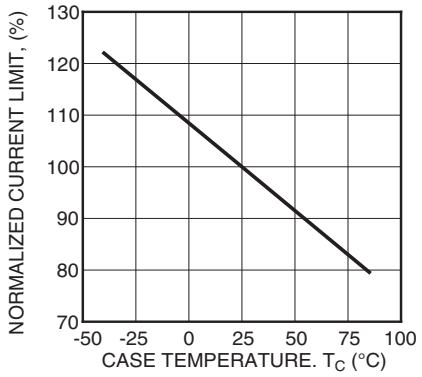
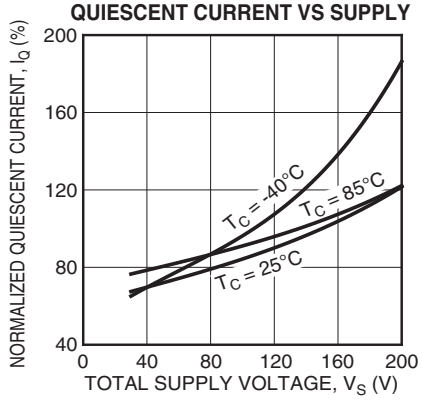


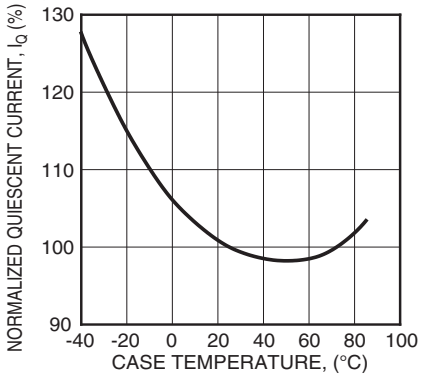
CURRENT LIMIT



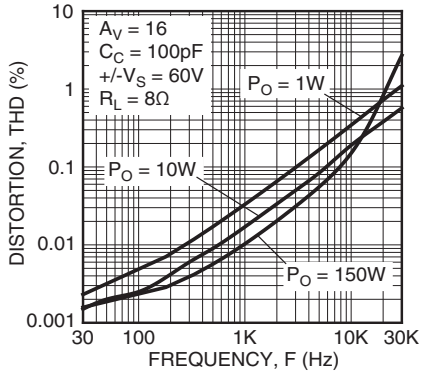
QUIESCENT CURRENT VS SUPPLY



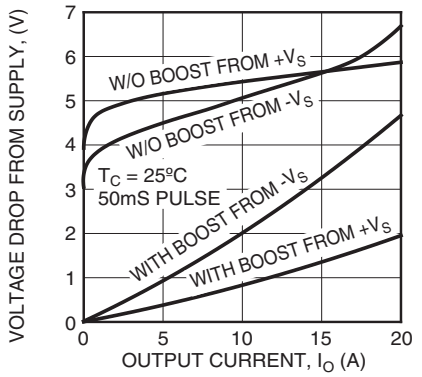
QUIESCENT CURRENT vs TEMPERATURE



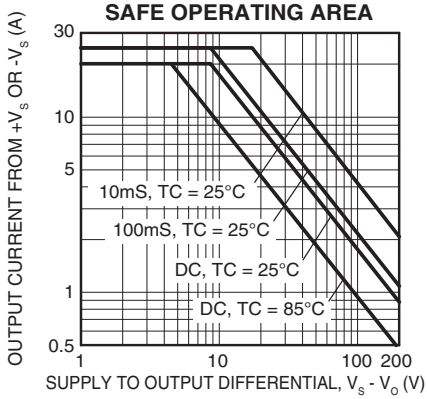
HARMONIC DISTORTION



OUTPUT VOLTAGE SWING



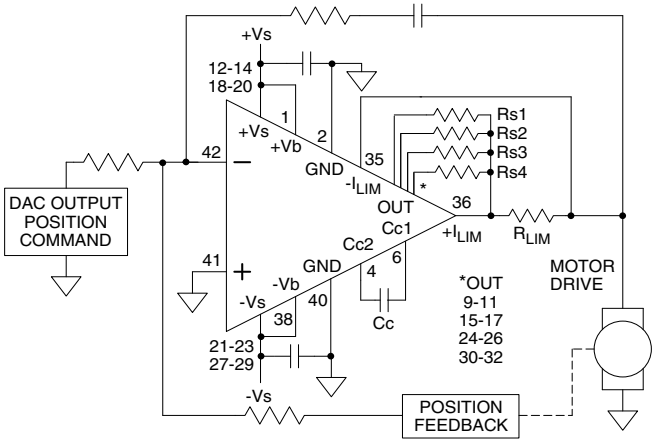
SAFE OPERATING AREA



TYPICAL APPLICATION

MOTOR POSITION CONTROL

The MOSFET output stage of the MP240 provides superior SOA performance compared to bipolar output stages where secondary breakdown is a concern. The extended SOA is ideal in motor drive applications where the back EMF of the motor may impose simultaneously both high voltage and high current across the output stage transistors. In the figure above a mechanical to electrical feedback position converter allows the MP240 to drive the motor in either direction to a set point determined by the DAC voltage.



The MP400 is ideally suited to driving both piezo actuation and deflection applications off of a single low voltage supply. The circuit above boosts a system 24V buss to 350V to drive an ink jet print head. The MP400s high speed deflection amplifier is biased for single supply operation by external resistors R2 – R6, so that a 0 to 5V DAC can be used as the input to the amplifier to drive the print head from 0 to >300V.

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Although the MP240 can withstand differential input voltages up to ±25V, in some applications additional external protection may be needed. 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

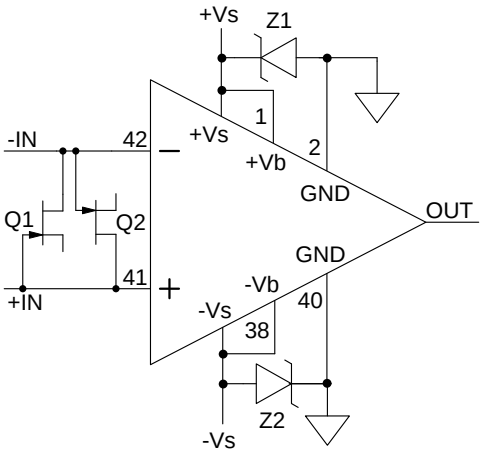


FIGURE 1: OVERVOLTAGE PROTECTION

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP240. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors 0.1µF or greater. In most applications power supply terminals $+V_B$ and $-V_B$ will be connected to $+V_S$ and $-V_S$ respectively. Although $+V_B$ and $-V_B$ are bypassed internally it is recommended to bypass $+V_B$ and $-V_B$ with 0.1µF externally. Additionally ground pins 2 and 40 must be connected to the system signal ground.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 36 must be connected to the amplifier output side and pin 35 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances R_P, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

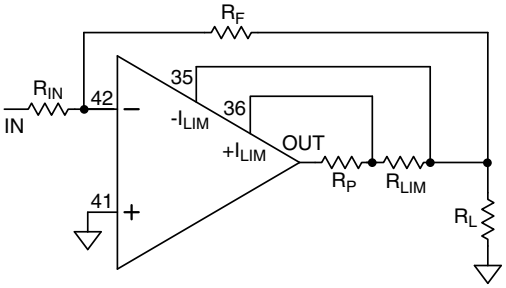


FIGURE 2: 4 WIRE CURRENT LIMIT

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifier's high current output stage. $+V_B$ (pin 1) and $-V_B$ (pin 38) are connected to the small signal stages. An additional 10V on the $+V_B$ and $-V_B$ pin is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to $+V_B$ and $-V_B$ respectively. $+V_B$ and $-V_B$ must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

SHUTDOWN

The output stage is turned off by applying a 5V level to HSD (pin 8) relative to LSD (pin 7). This is a non-latching circuit. As long as HSD remains high relative to LSD the output stage will be turned off. LSD will normally be tied to signal ground but LSD may float from $-V_B$ to $+V_B$ - 15V. Shutdown can be used to lower quiescent current for standby operation or as part of a load protection circuit.

BIAS CLASS OPTION

Normally pin 5 (Iq) is left open. But when pin 5 is connected to pin 6 (Cc1) the quiescent current in the output stage is disabled. This results in lower quiescent power, but also class C operation of the output stage and the resulting crossover distortion. In many applications, such as driving motors, the distortion may be unimportant and lower standby power dissipation is an advantage.

Power Operational Amplifiers

FEATURES

- Low Cost
- Wide Common Mode Range
- Standard Supply Voltage
  - Single Supply: 10 V to 50 V
- Output Current - 150 mA Continuous
- Output Voltage 50-350 V
- 350 V/µS Slew Rate
- 200 kHz Power Bandwidth

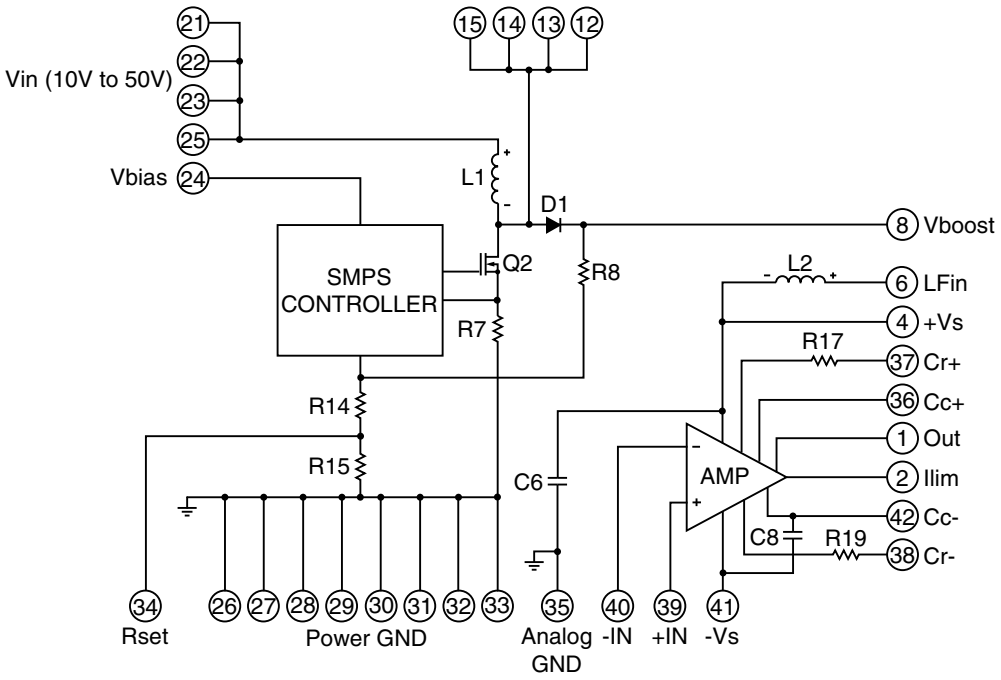
Applications

- Piezoelectric positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

GENERAL DESCRIPTION

The MP400FC combines a high voltage, high speed precision power op amp with a supply voltage boost function in an integrated thermally conductive module. The voltage boost function uses a switch mode power supply (SMPS) to boost the input power supply voltage. This allows the user the benefits of using his standard 12 V or 24 V buss without the need to design a high voltage supply to power the op amp. The SMPS voltage is adjustable from 50-350 V, allowing for op amp output voltages up to 340 V. External phase compensation provides the user with the flexibility to tailor gain, slew rate and bandwidth for a specific application. The unique design of this amplifier provides extremely high slew rates in pulse applications while maintaining low quiescent current. The output stage is well protected with a user defined current limit. Safe Operating Area (SOA) must be observed for reliable operation.

EQUIVALENT CIRCUIT DIAGRAM



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_{CC}$ to GND			50	V
OUTPUT CURRENT, peak within SOA			200	mA
POWER DISSIPATION, internal, DC, Amplifier			14.2	W
OUTPUT POWER, SMPS			67	W
INPUT VOLTAGE, Differential		-16	16	V
INPUT VOLTAGE, Common Mode		-16	16	V
TEMPERATURE, pin solder, 10s			225	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	105	°C
OPERATING TEMPERATURE, case		−40	85	°C

SPECIFICATIONS

Parameter	Test Conditions	Min	Typ	Max	Units
AMPLIFIER INPUT					
OFFSET VOLTAGE			8	40	mV
OFFSET VOLTAGE vs. temperature	0 to 85°C (Case)		-63		µV/°C
OFFSET VOLTAGE vs. supply				32	µV/V
BIAS CURRENT, initial (Note 3)			8.5	200	pA
OFFSET CURRENT, initial			12	400	pA
INPUT RESISTANCE, DC			10^6		Ω
COMMON MODE VOLTAGE RANGE, pos.			$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC		90	118		dB
NOISE	700KHz bandwidth		418		µV RMS
AMPLIFIER GAIN					
OPEN LOOP @ 15 Hz		89	120		dB
GAIN BANDWIDTH PRODUCT @ 1 MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
AMPLIFIER OUTPUT					
VOLTAGE SWING	I_O = 10 mA		$\|V_S\|$ - 2		V
VOLTAGE SWING	I_O = 100 mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
VOLTAGE SWING	I_O = 150 mA		$\|V_S\|$ - 10		V
CURRENT, continuous, DC		150			mA
SLEW RATE		100	350		V/µS
SETTLING TIME, to 0.1%	2 V Step		1		µS
RESISTANCE, No load	R_{LIM} = 6.2 Ω		44		Ω
POWER BANDWIDTH, 300 V_{P-P}	$+V_S$ = 160 V, $-V_S$ = -160 V		200		kHz
CURRENT, quiescent, amplifier only		0.2	0.7	2.5	mA

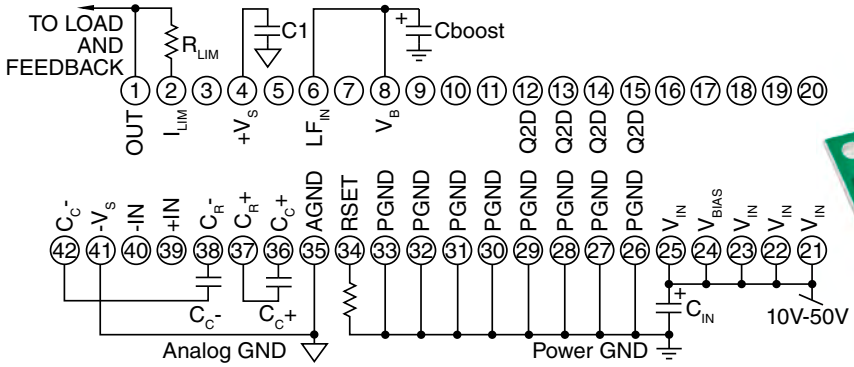
SPECIFICATIONS, (cont).

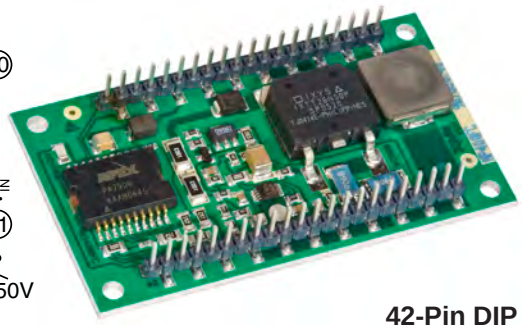
Parameter	Test Conditions	Min	Typ	Max	Units
SMPS					
INPUT VOLTAGE, V_{IN}		10		50	V
SMPS OUTPUT VOLTAGE, V_B		46.75		365	V
SMPS OUTPUT CURRENT, I_S	V_B = 10x V_{IN}	150			mA
OUTPUT VOLTAGE TOLERANCE	$V_B \leq$ 10x V_{IN}, $I_S \leq$ 150 mA, R_{SET} = 1%		+/-2	6.5	%
VOLTAGE BOOST			10		x input V
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range, f<60Hz		7.7	8.8	°C/W
RESISTANCE, junction to air	Full temperature range		46		°C/W
TEMPERATURE RANGE, case		0		70	°C

NOTES:

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stage.

EXTERNAL CONNECTIONS





42-Pin DIP
Package Style FC

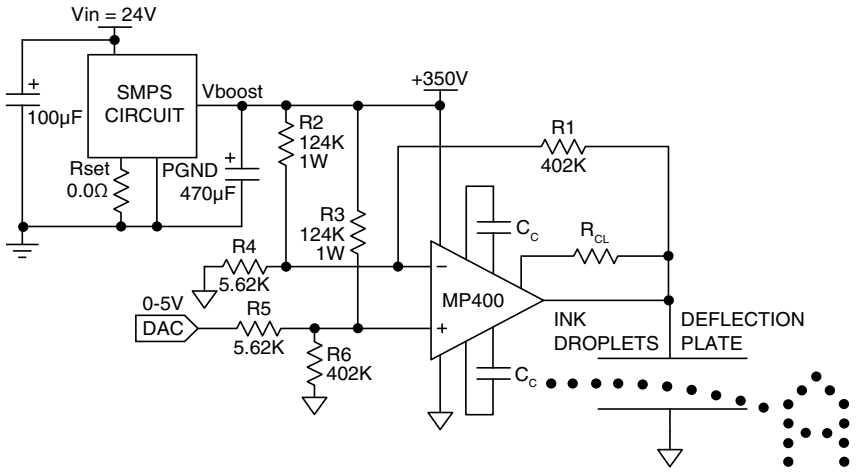
PIN DESCRIPTIONS

Pin #	Pin name	Description
21 - 23, 25	V_{IN}	Input voltage pins for the on board high voltage switch mode power supply.
24	V_{BIAS}	Input voltage pin for the boost controller circuitry. This pin is typically tied to V_{IN}
12 – 15	Q2D	Drain node of the SMPS MOSFET switch. An external RC snubber may be connect from this node to power ground to reduce or eliminate overshoot and ringing at switch turn off, reducing switching noise on the SMPS.
8	V_B	This is the output of the high voltage SMPS and typically is tied to pin 6, L_{FIN}. Other loads can be added to this pin as long as the maximum output power of the SMPS is not exceeded. For proper operation, an external high voltage, low ESR capacitor must be connected to this pin. Refer to the paragraph titled “SMPS Output Capacitor”.
6	L_{FIN}	The high voltage SMPS, V_B , is connected to this pin to power the MP400FC amplifier through a 47 µH filter inductor. The supply current in to this pin can not exceed 200 mA.
4	$+V_S$	MP400FC amplifier high voltage supply pin. This pin is used for external supply bypass. A high quality ceramic capacitor of at least 1uF should be used. The high voltage SMPS, V_B, can be connected directly to this pin, bypassing the 47 µH filter inductor.
34	R_{SET}	SMPS voltage set resistor. A resistor is connected from this pin to power ground to set the SMPS voltage.
26 – 33	PGND	Power ground. SMPS switching circuits are referenced to ground through these pins.
35	AGND	Analog ground for MP400FC amplifier circuits. AGND and PGND are connected at one point on the MP400FC. Avoid external connections between AGND and PGND.
41	$-V_S$	This pin is typically connected to AGND. However, an external negative supply voltage can be connected to this pin.
39	+IN	Amplifier non-inverting input
40	-IN	Amplifier inverting input
1	V_{OUT}	Amplifier output
2	I_{LIM}	Amplifier current limit. A current limit resistor must be connected between I_{LIM} and V_{OUT}. R_{LIM} = $0.7/I_{LIM}$.
36	C_R+	+ side compensation capacitor connection one.
37	C_C+	+ side compensation capacitor connection two.
38	C_R-	- side compensation capacitor connection one.
42	C_C-	- side compensation capacitor connection two.

Unused pins should be left open. This is mandatory for pins 3, 5, 7, 9, 11 and 16.

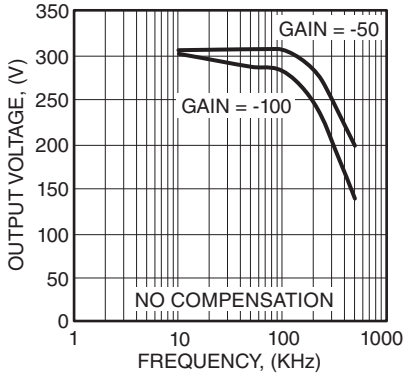
TYPICAL APPLICATION

The MP400FC is ideally suited to driving both piezo actuation and deflection applications off of a single low voltage supply. The circuit above boosts a system 24 V buss to 350 V to drive an ink jet print head. The MP400FCs high speed deflection amplifier is biased for single supply operation by external resistors R2 – R6, so that a 0 to 5 V DAC can be used as the input to the amplifier to drive the print head from 0 to >300 V.

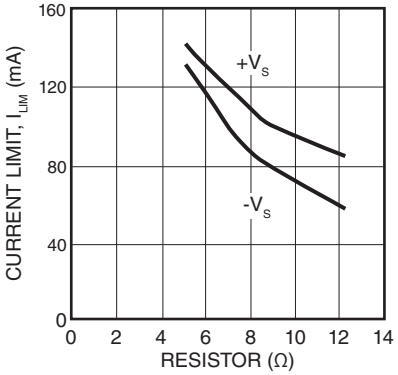


TYPICAL PERFORMANCE GRAPHS

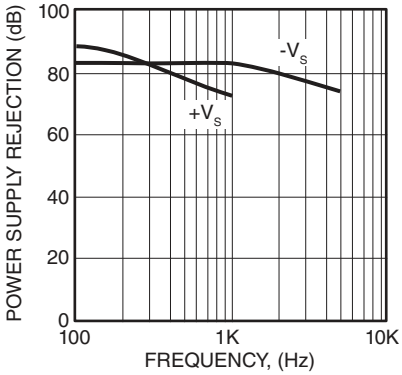
POWER RESPONSE



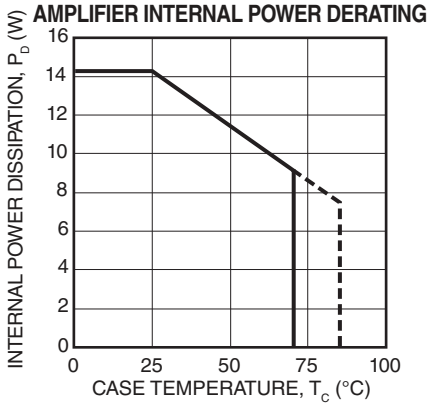
CURRENT LIMIT



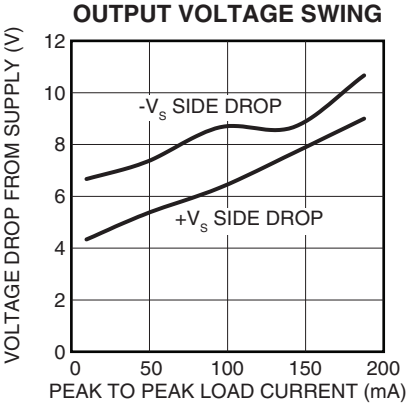
POWER SUPPLY REJECTION



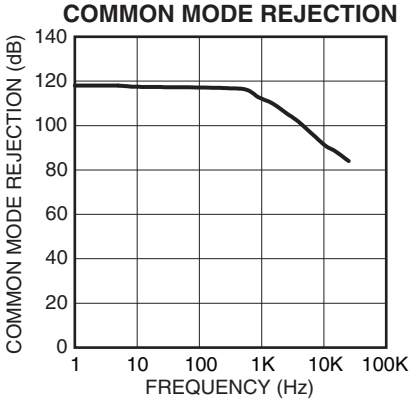
AMPLIFIER INTERNAL POWER DERATING



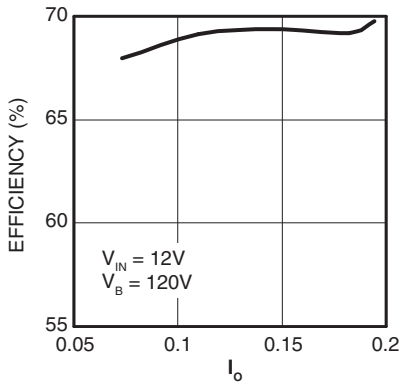
OUTPUT VOLTAGE SWING



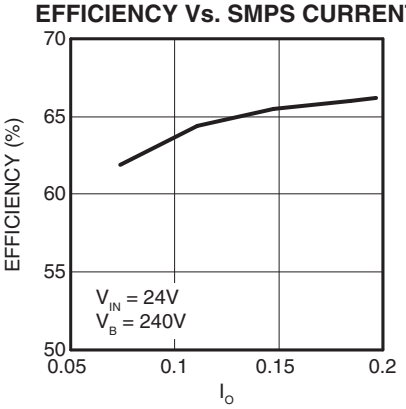
COMMON MODE REJECTION



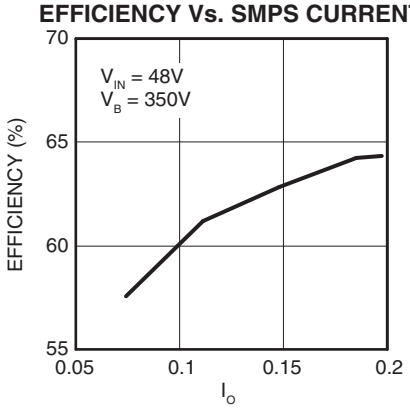
EFFICIENCY Vs. SMPS CURRENT



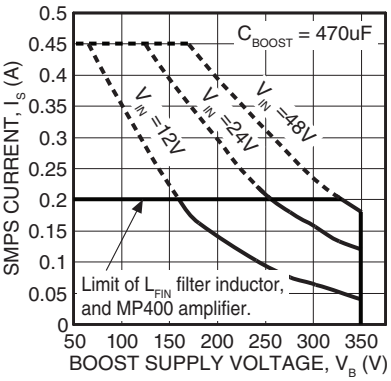
EFFICIENCY Vs. SMPS CURRENT



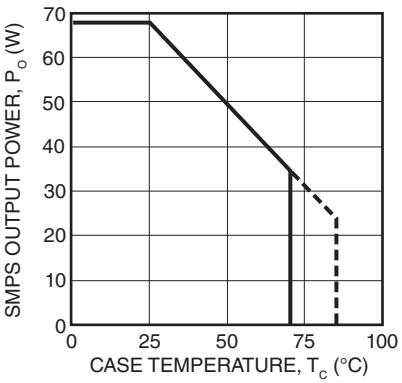
EFFICIENCY Vs. SMPS CURRENT



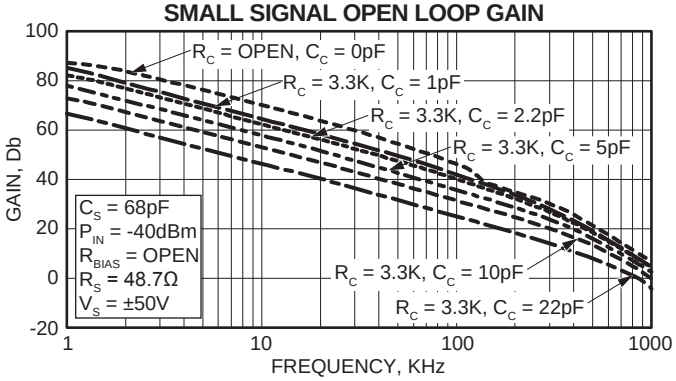
SMPS CURRENT VS. SMPS VOLTAGE



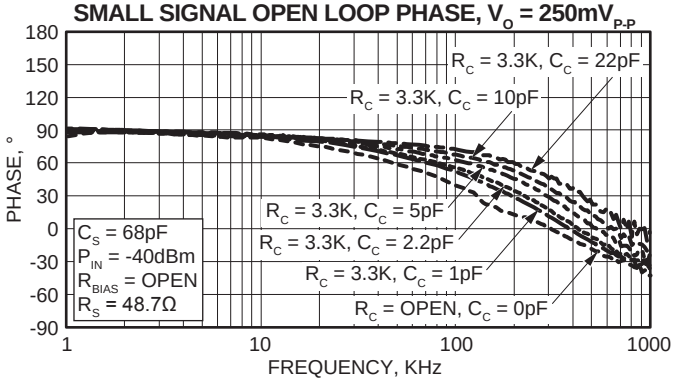
SMPS POWER DERATING



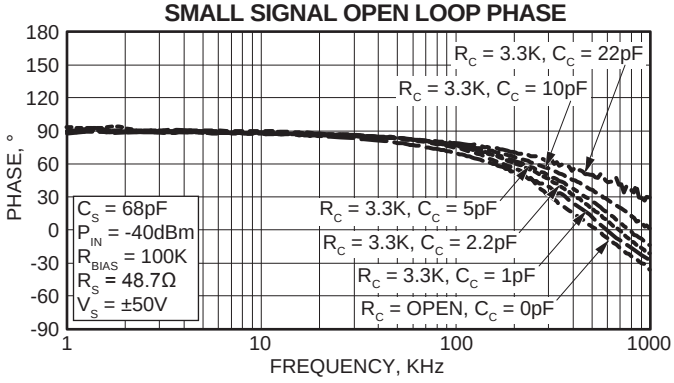
SMALL SIGNAL OPEN LOOP GAIN



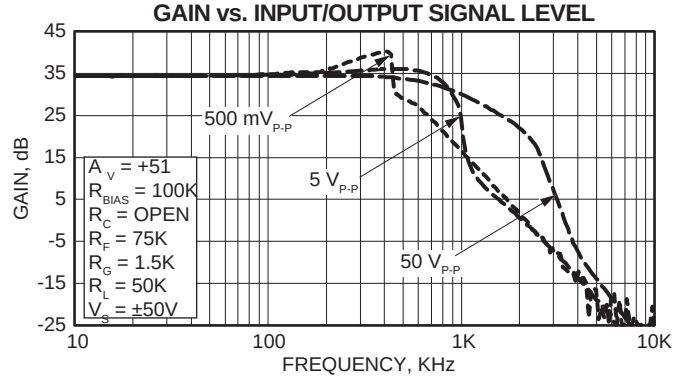
SMALL SIGNAL OPEN LOOP PHASE, V_O = 250mV$_{P-P}$



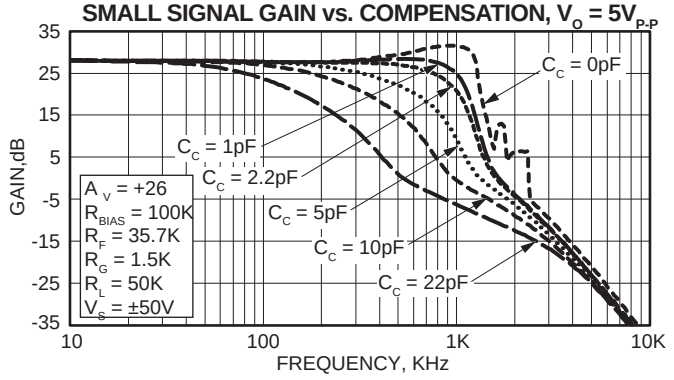
SMALL SIGNAL OPEN LOOP PHASE



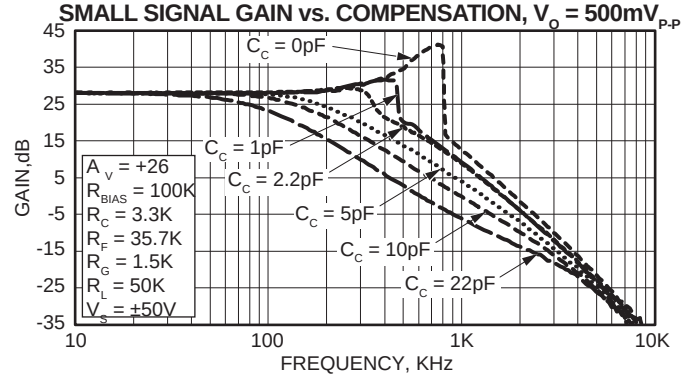
GAIN vs. INPUT/OUTPUT SIGNAL LEVEL



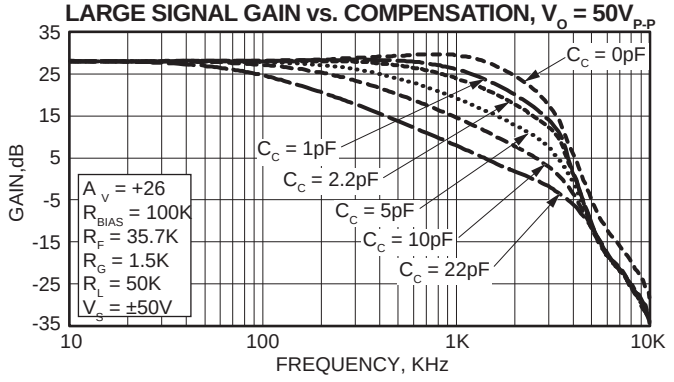
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 5V$_{P-P}$

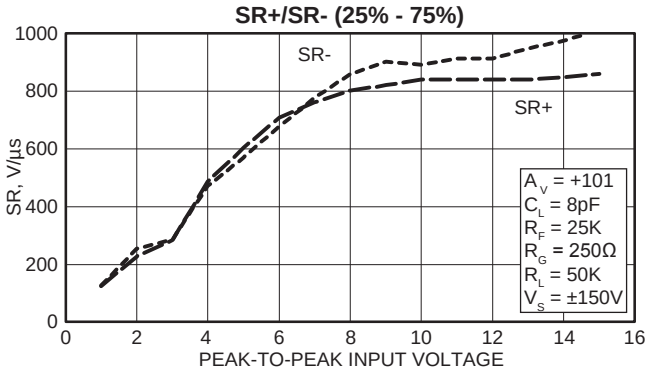


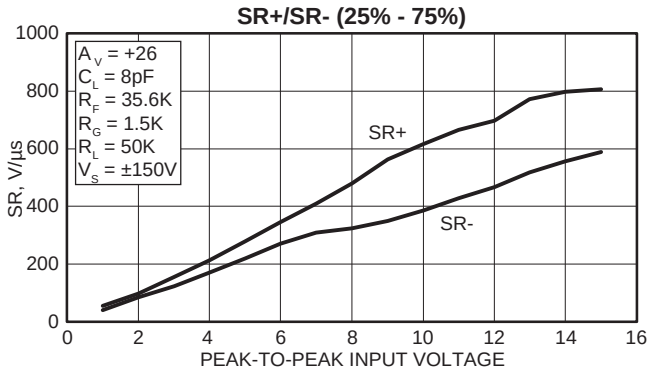
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 500mV$_{P-P}$

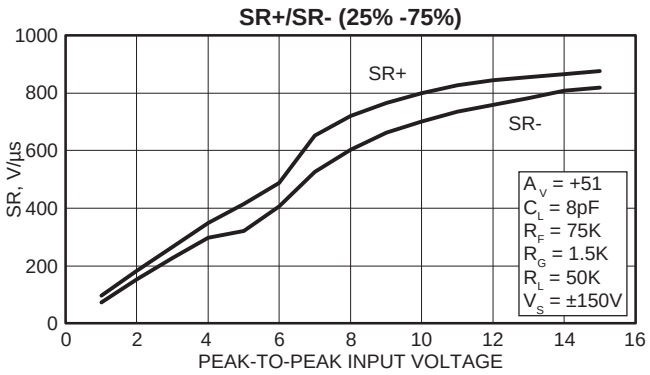


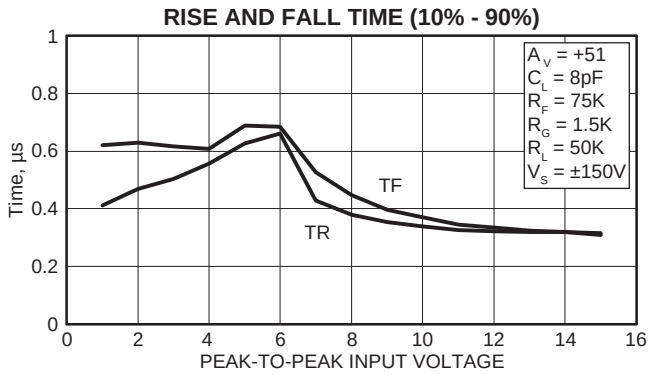
LARGE SIGNAL GAIN vs. COMPENSATION, V_O = 50V$_{P-P}$

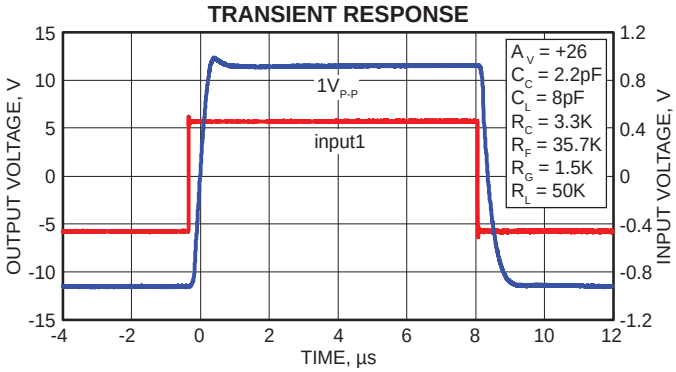


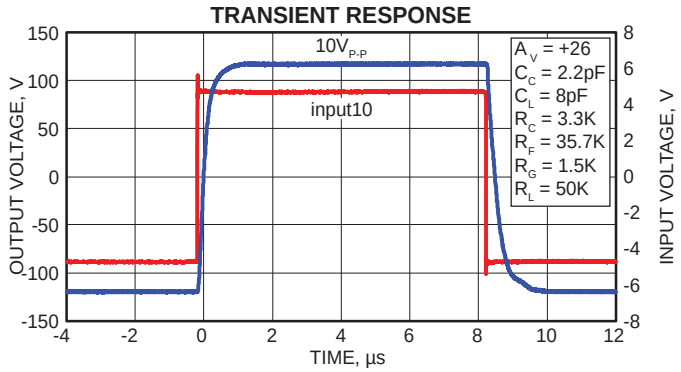

SR+/SR- (25% - 75%)
SR-
SR+
A V = +101
C L = 8pF
R F = 25K
R G = 250Ω
R L = 50K
V S = ±150V
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE

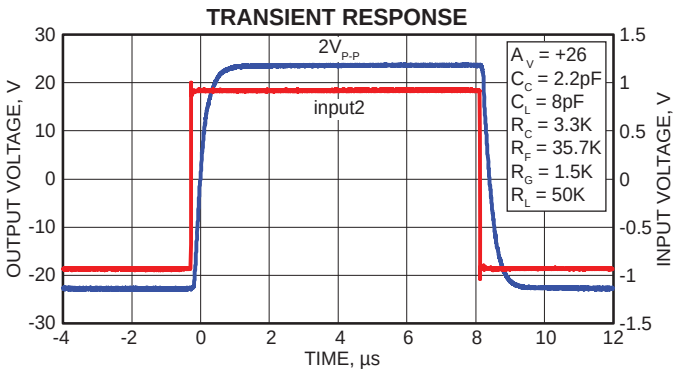

SR+/SR- (25% - 75%)
A V = +26
C L = 8pF
R F = 35.6K
R G = 1.5K
R L = 50K
V S = ±150V
SR+
SR-
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE

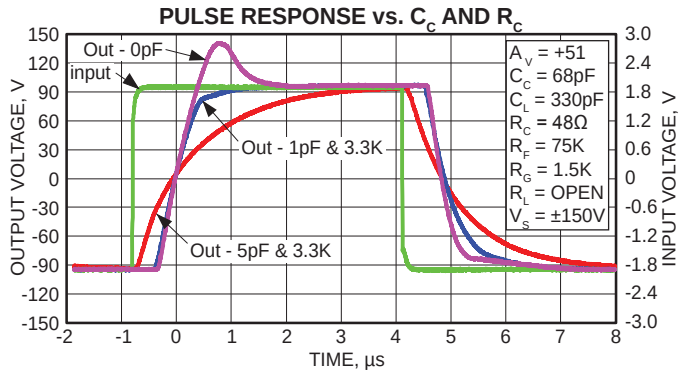

SR+/SR- (25% -75%)
SR+
SR-
A V = +51
C L = 8pF
R F = 75K
R G = 1.5K
R L = 50K
V S = ±150V
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE


RISE AND FALL TIME (10% - 90%)
A V = +51
C L = 8pF
R F = 75K
R G = 1.5K
R L = 50K
V S = ±150V
TF
TR
Time, µs
PEAK-TO-PEAK INPUT VOLTAGE

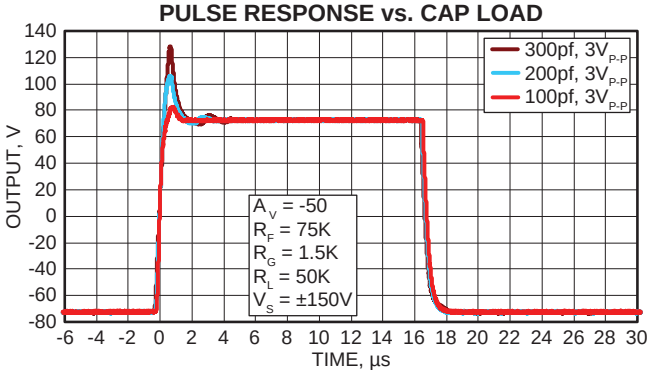

TRANSIENT RESPONSE
A V = +26
C C = 2.2pF
C L = 8pF
R C = 3.3K
R F = 35.7K
R G = 1.5K
R L = 50K
1V P-P
input1
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs


TRANSIENT RESPONSE
A V = +26
C C = 2.2pF
C L = 8pF
R C = 3.3K
R F = 35.7K
R G = 1.5K
R L = 50K
10V P-P
input10
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs

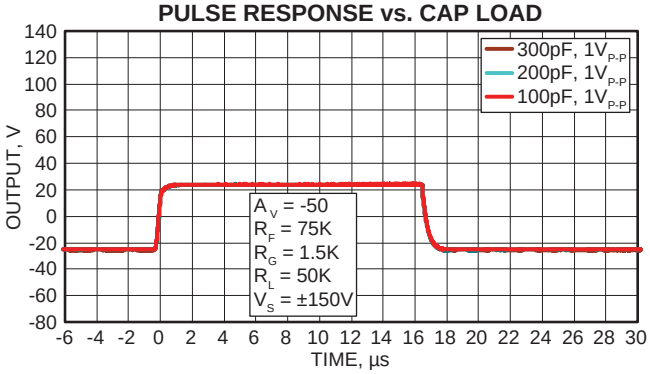

TRANSIENT RESPONSE
A V = +26
C C = 2.2pF
C L = 8pF
R C = 3.3K
R F = 35.7K
R G = 1.5K
R L = 50K
2V P-P
input2
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs


PULSE RESPONSE vs. C C AND R C
A V = +51
C C = 68pF
C L = 330pF
R C = 48Ω
R F = 75K
R G = 1.5K
R L = OPEN
V S = ±150V
Out - 0pF
input
Out - 1pF & 3.3K
Out - 5pF & 3.3K
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs

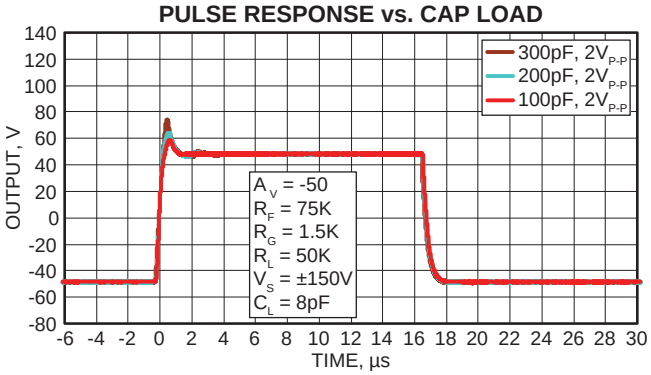
PULSE RESPONSE vs. CAP LOAD



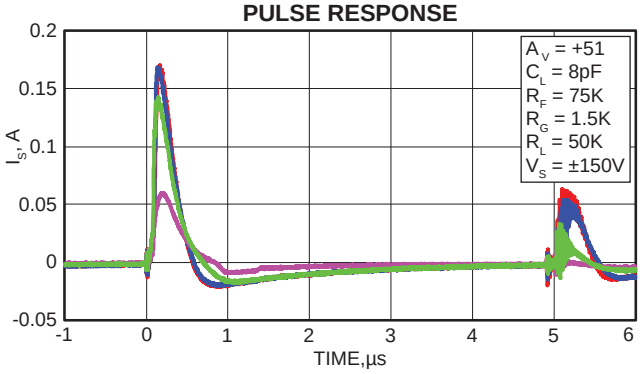
PULSE RESPONSE vs. CAP LOAD



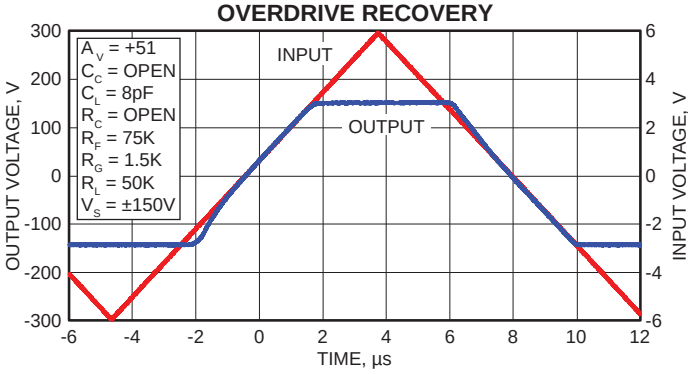
PULSE RESPONSE vs. CAP LOAD



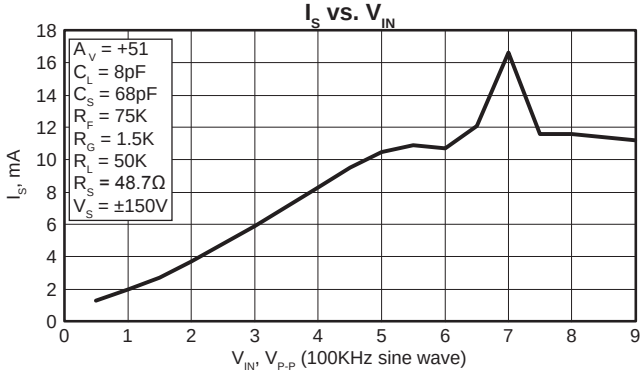
PULSE RESPONSE



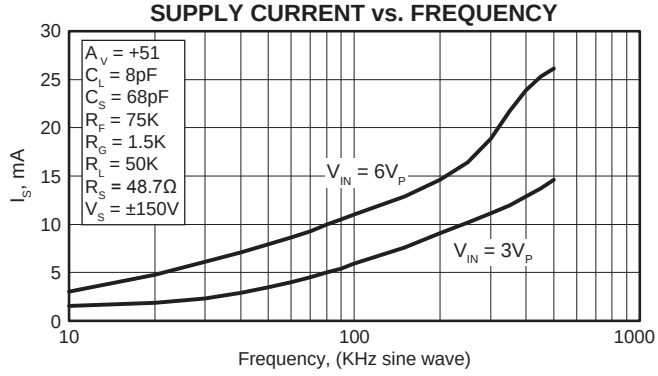
OVERDRIVE RECOVERY

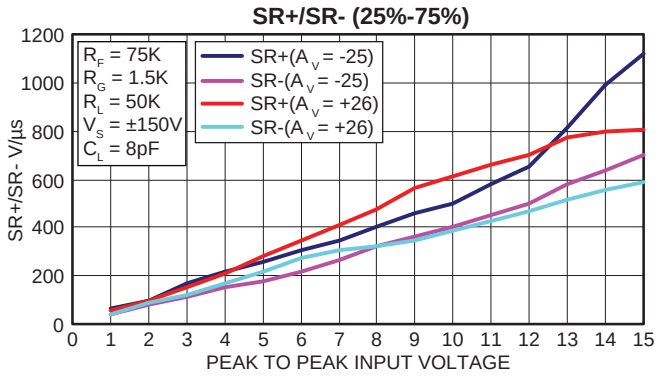


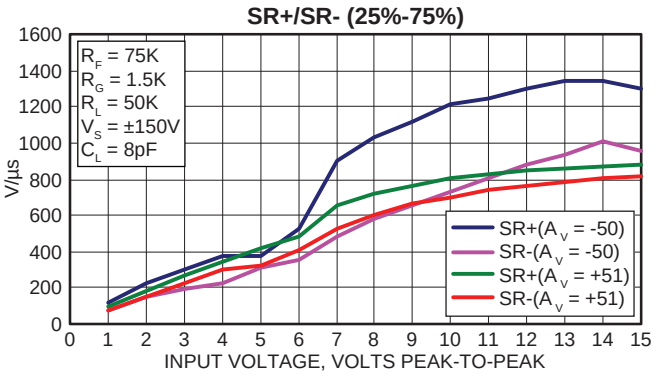
I_S vs. V_{IN}



SUPPLY CURRENT vs. FREQUENCY







GENERAL

Please read Application note 1 “General operating considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, and current limit. There you will also find a complete application notes library, technical seminar workbook, and evaluation kits.

THEORY OF OPERATION

The PA78 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.

SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA78 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA78 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1 µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA78. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, R_{BIAS}, between C_C- and V_S+. The size of R_{BIAS} will depend upon the application but 500 µA (50 V V+ supply/100K) of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA78 is externally compensated and performance can be optimized to the application. Unlike the R_{BIAS} technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the tradeoffs between bandwidth and stability. Due to the unique design of the PA78, two symmetric compensation networks are required. The compensation capacitor C_C must be rated for a working voltage of the full operating supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature.

The PA78 requires an external 33 pF capacitor between C_C- and $-V_S$ to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

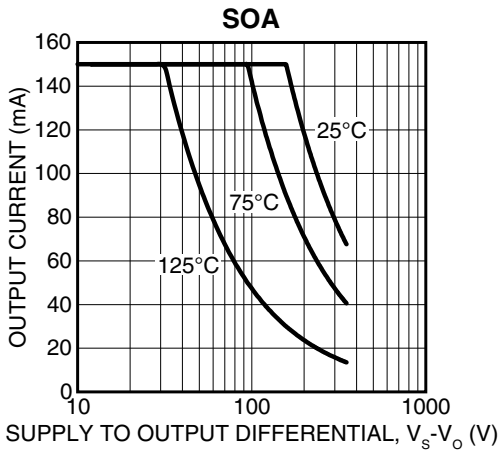
As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from 1 V_{P-P} to 15 V_{P-P}, the slew rate increases from 50 V/µs to well over 350 V/µs.

Notice the knee in the Rise and Fall times plot, at approximately 6 V_{P-P} input voltage. Beyond this point the output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA78 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current vs. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.

The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.



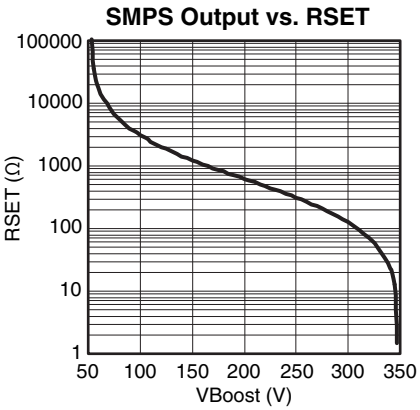
CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The maximum practical value for R_{LIM} is about 12 Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for Rlim in the intended application. Current limit may not protect against short circuit conditions with supply voltages over 200 V.

LAYOUT CONSIDERATIONS

The PA78 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1µF capacitor to GND is also sufficient if a DC connection is undesirable

Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of LC interactions and oscillations.



SMPS OPERATION

The MP400FC is designed to operate off of a standard voltage rail. Typical values include 12 V, 24 V, or 48 V. The addition of the on-board SMPS eliminates the need to design or purchase a high voltage power supply. The only inputs required by the SMPS are the V_{IN} source. Input and output filter capacitor, and boost voltage set resistor (R_{SET}).

The SMPS output can be adjusted between a minimum of 50 V to a maximum of 350 V. The voltage boost adjustment is independent of V_{IN}. Adjustment to the boost level is made through a resistor from the R_{SET} pin to ground. The resistor value is:

$$R_{SET} = \frac{1.85 \cdot 10^5}{V_{BOOST} - 49.95} - 615$$

Where V_{BOOST} = desired SMPS voltage.

Example: 1) Desired V_{BOOST} = 160 V

2) R_{SET} = 1K (1066 by equation)

If R_{SET} is open, V_{BOOST} will be 50 V. If R_{SET} is shorted to ground V_{BOOST} will be limited to 350 V.

Note that while the MP400 SMPS generates a positive voltage from 50 V to 350 V, the amplifier may operate from a variety of supply voltages. Symmetric, asymmetrical and single supply configurations can be used so long as the total supply voltage from $+V_S$ to $-V_S$ does not exceed 350 V. The amplifier performance graphs in this datasheet include some plots taken with symmetrical supplies, but those plots generally apply to all supply configurations.

SMPS OUTPUT CAPACITOR

An external SMPS output filter capacitor is required for proper operation. ESR considerations prevail in the choice of the output filter capacitor. Select the highest value capacitor that meets the following ESR requirement. The minimum value for C_{BOOST} is 100 µF.

$ESR = dVo/I_{LPK}$

Where,

dVo = The maximum acceptable output ripple voltage

I_{LPK} = Peak inductor current = $(1/L) \cdot V_{IN} \cdot ton$

L = 10^{-6} if the internal inductor is used.

V_{IN} = Input voltage of the application.

ton = $\sqrt{(2 \cdot Io \cdot L \cdot ((Vo + 0.6 - V_{IN})/(F_{SW} \cdot V_{IN}^2)))}$

V_{BOOST} = The boost supply voltage of the application.

I_O = The maximum continuous output current for the application.

F_{SW} = 100 KHz switching frequency of the MP400FC boost supply.

SMPS INPUT CAPACITOR

An external input capacitor is required. This capacitor should be at least 100 µF.

THERMAL CONSIDERATIONS

For reliable operation the MP400FC will require a heatsink for most applications. When choosing the heatsink the power dissipation in the op amp and the SMPS MOSFET switch (Q2) are both considered. The power dissipation of the op amp is determined in the same manner as any power op amp. The power dissipation of the MOSFET switch (Q2) is the sum of the power dissipation due to conduction and the switching power.

$$P_{D(Q2)} = (I_{IN(pk)}^{2} \bullet R_{DS(ON)} \bullet D) + (I_{IN(pk)} \bullet V_{IN} \bullet t_r \bullet F_{SW})$$

Where:

V_{IN} = SMPS input voltage
V_B = SMPS output voltage
I_O = Total SMPS output current
F_{SW} = 100 KHz
$R_{DS(ON)}$ = 0.621 Ω
t_r = 82 x 10^{-9}s
D = $t_1 \bullet F_{SW}$

$$t_1 = \sqrt{2 \bullet I_O \bullet 10 \times 10^{-6} \bullet \left(\frac{V_B - V_{IN}}{F_{SW} \bullet V_{IN}^{2}} \right)}$$

$$I_{IN(pk)} = \frac{V_B \bullet t_d}{10 \times 10^{-6}}$$

$$t_d = t_1 \bullet \left(\frac{V_B}{V_B - V_{IN}} \right) - t_1$$

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

PA01 • PA73

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- LOW COST, ECONOMY MODEL — PA01
- HIGH OUTPUT CURRENT — Up to ±5A PEAK
- EXCELLENT LINEARITY — PA01
- HIGH SUPPLY VOLTAGE — Up to ±30V
- ISOLATED CASE — 300V

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

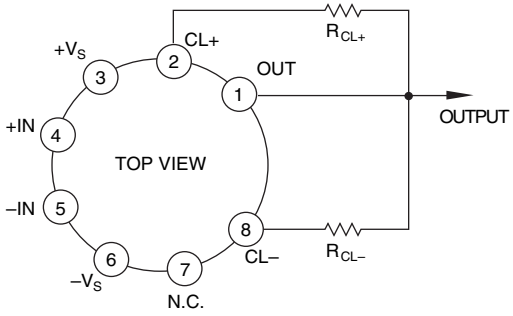
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 20kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 48V
- AUDIO AMPLIFIERS UP TO 50W RMS

DESCRIPTION

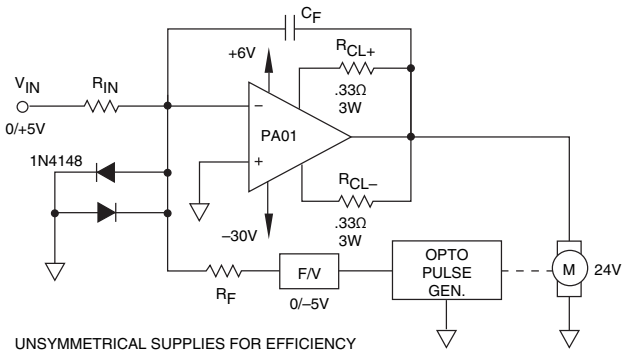
The PA01 and PA73 are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the PA01 has a class A/B output stage. The PA73 has a simple class C output stage (see Note 1) to reduce cost for motor control and other applications where crossover distortion is not critical and to provide interchangeability with type 3573 amplifiers. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit resistors. These amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EXTERNAL CONNECTIONS



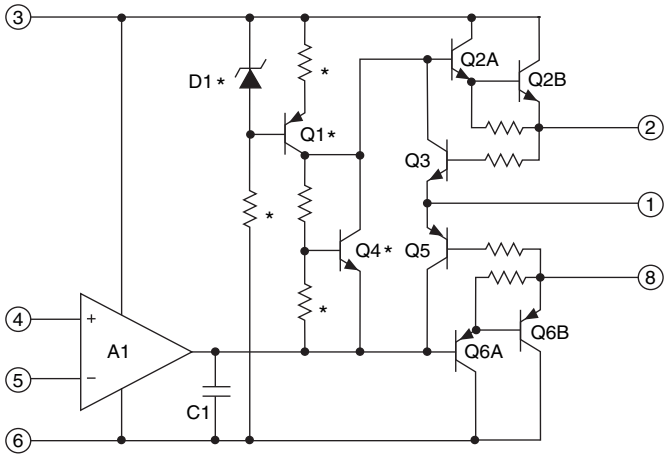
TYPICAL APPLICATION



Unidirectional Optical Speed Control

The pulse output of a non-contact optical sensor drives a voltage-to-frequency converter which generates feedback for the op amp. With the loop closed in this manner, the op amp corrects for any variations in the speed due to changing load. Because of operation in only one direction, an unsymmetrical supply is used to maximize efficiency of both power op amp and power supply. High speed diodes at the input protect the op amp from commutator noise which may be generated by the motor.

EQUIVALENT SCHEMATIC



NOTE 1: * Indicates not used in PA73. Open base of Q2A connected to output of A1.

ABSOLUTE MAXIMUM RATINGS

	PA01	PA73
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	60V	68V
OUTPUT CURRENT, within SOA	5A	5A
POWER DISSIPATION, internal	67W	67W
INPUT VOLTAGE, differential	±37V	±37V
INPUT VOLTAGE, common-mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, junction[1]	200°C	200°C
TEMPERATURE, pin solder -10s	300°C	300°C
TEMPERATURE RANGE, storage	–65 to +150°C	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C	–25 to +85°C

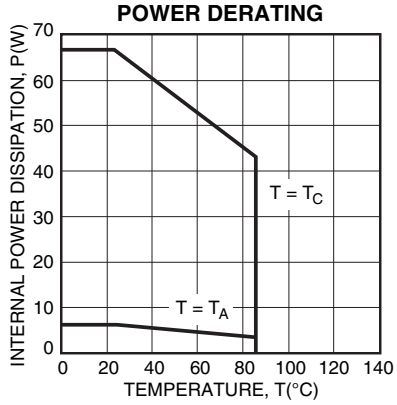
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA01 MIN	PA01 TYP	PA01 MAX	PA73 MIN	PA73 TYP	PA73 MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±12		*	±10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±35			*	±200	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±15	±50		*	±40	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05	±.4		*	*	nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.02			*		nA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		*	*	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.05			*		nA/°C
INPUT IMPEDANCE, common-mode	T_C = 25°C		200			*		MΩ
INPUT IMPEDANCE, differential	T_C = 25°C		10			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–6	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	T_C = 25°C, $V_{CM} = V_S$ –6V	70	110		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	91	113		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 4A, $V_O = 40V_{PP}$	15	23		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–10	$\pm V_S$–5		$\pm V_S$–8	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6	$\pm V_S$–5		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 46mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	±5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 2.5Ω	1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			1			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±28	*	*	±30	V
CURRENT, quiescent	T_C = 25°C		20	50		2.6	5	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

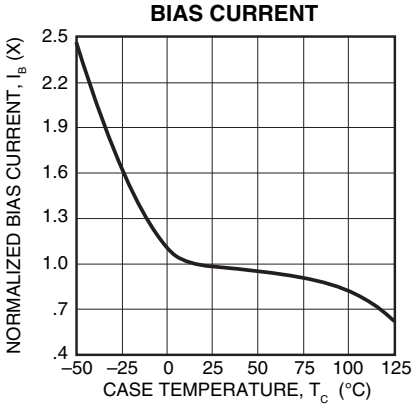
NOTES: * The specification of PA73 is identical to the specification for PA01 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

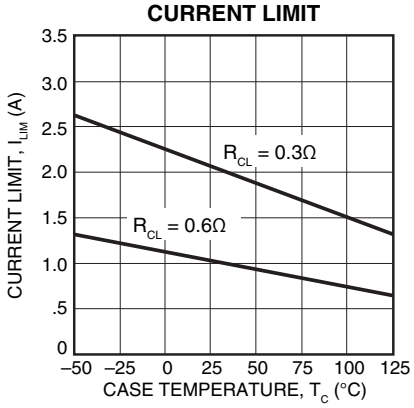
POWER DERATING



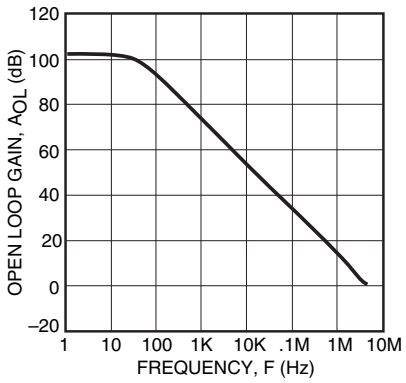
BIAS CURRENT



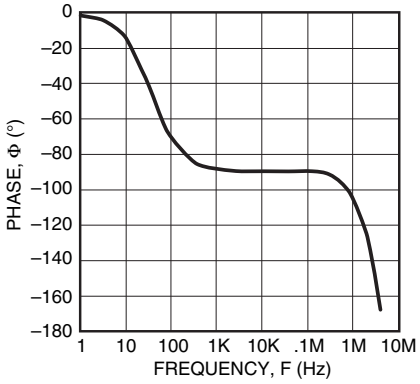
CURRENT LIMIT



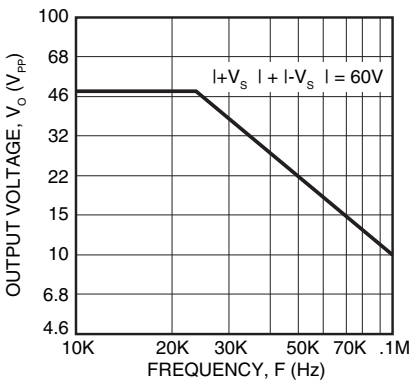
SMALL SIGNAL RESPONSE



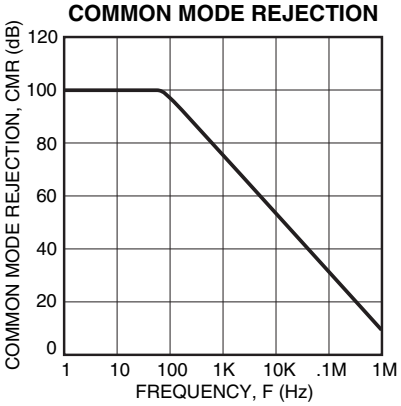
PHASE RESPONSE



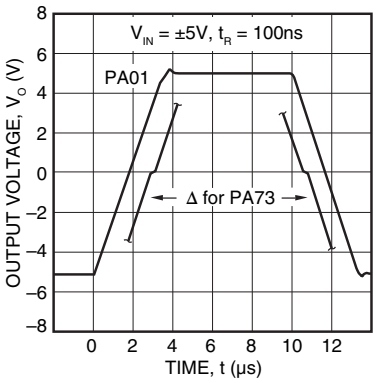
POWER RESPONSE



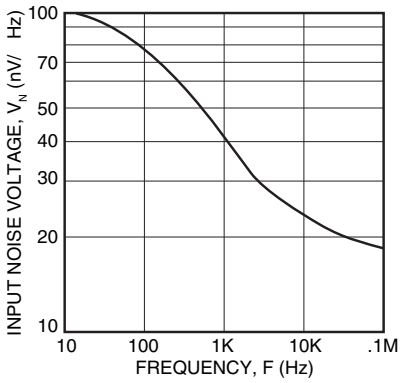
COMMON MODE REJECTION



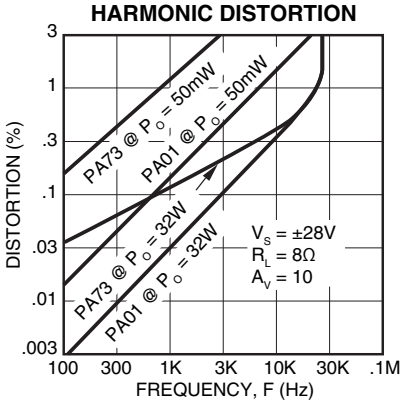
PULSE RESPONSE



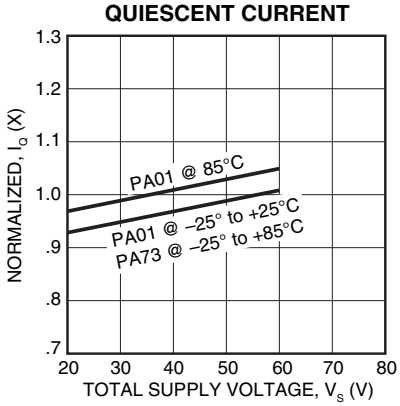
INPUT NOISE



HARMONIC DISTORTION



QUIESCENT CURRENT



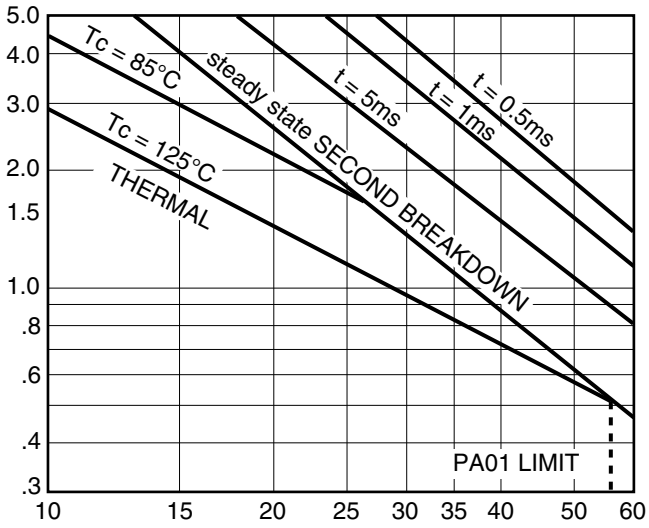
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.cirrus.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

1. For sine wave outputs, use Power Design[1] to plot a load line. Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.

   For other waveform outputs, manual load line plotting is recommended. Applications Note 22, SOA AND LOAD LINES, will be helpful. A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges.

2. EMF generating or reactive load and short circuits to the supply rail or shorts to common are safe if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
34V	.58A	1.1A
30V	.46A	1.4A
25V	.61A	1.7A
20V	.86A	2.1A
15V	1.3A	2.9A

3. The output stage is protected against occaisional transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

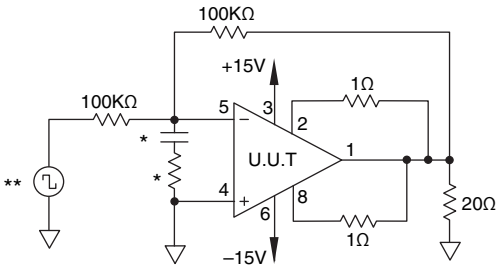
Proper operation requires the use of two current limit resistors, connected as shown, in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm; however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

[1] Note 1. Power Design is a self-extracting Excel spreadsheet available free from www.cirrus.com

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±28V	V_{IN} = 0, A_V = 100		5	mA
1	Input Offset Voltage	V_{OS}	25°C	±28V	V_{IN} = 0, A_V = 100		±10	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
1	Input Offset Voltage	V_{OS}	25°C	±30V	V_{IN} = 0, A_V = 100		±10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±28V	V_{IN} = 0		±40	nA
1	Input Bias Current, –IN	$–I_B$	25°C	±28V	V_{IN} = 0		±40	nA
1	Input Offset Current	I_{OS}	25°C	±28V	V_{IN} = 0		±25	nA
3	Quiescent Current	I_Q	–55°C	±28V	V_{IN} = 0, A_V = 100		5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±28V	V_{IN} = 0, A_V = 100		±15.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±22.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±30V	V_{IN} = 0, A_V = 100		±16	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±28V	V_{IN} = 0		±72	nA
3	Input BiasCurrent, –IN	$–I_B$	–55°C	±28V	V_{IN} = 0		±72	nA
3	Input Offset Current	I_{OS}	–55°C	±28V	V_{IN} = 0		±60	nA
2	Quiescent Current	I_Q	125°C	±28V	V_{IN} = 0, A_V = 100		7	mA
2	Input Offset Voltage	V_{OS}	125°C	±28V	V_{IN} = 0, A_V = 100		±16.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±23.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±30V	V_{IN} = 0, A_V = 100		±17.3	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±28V	V_{IN} = 0		±80	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±28V	V_{IN} = 0		±80	nA
2	Input Offset Current	I_{OS}	125°C	±28V	V_{IN} = 0		±80	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±18.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 50mA	V_O	25°C	±30V	R_L = 500Ω	25		V
4	Output Voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±18V	R_L = 12Ω, R_{CL} = 1Ω	.54	.86	A
4	Stability/Noise	E_N	25°C	±28V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±28V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
6	Output Voltage, I_O = 5A	V_O	–55°C	±18.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 50mA	V_O	–55°C	±30V	R_L = 500Ω	25		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±30V	R_L = 12Ω	24		V
6	Stability/Noise	E_N	–55°C	±30V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±28V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
6	Common Mode Rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 50mA	V_O	125°C	±30V	R_L = 500Ω	25		V
5	Output Voltage, I_O = 2A	V_O	125°C	±30V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	125°C	±28V	R_L = 500Ω, A_V= 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±28V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA02 • PA02A

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH POWER BANDWIDTH — 350kHz
- HIGH SLEW RATE — 20V/µs
- FAST SETTLING TIME — 600ns
- LOW CROSSOVER DISTORTION — Class A/B
- LOW INTERNAL LOSSES — 1.2V at 2A
- HIGH OUTPUT CURRENT — ±5A PEAK
- LOW INPUT BIAS CURRENT — FET Input
- ISOLATED CASE — 300 VDC

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

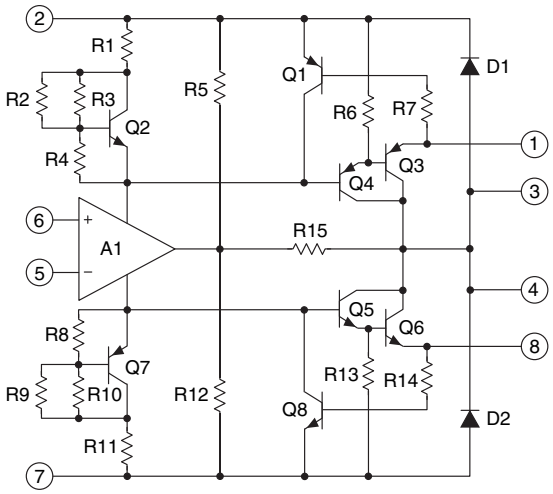
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 kHz
- AUDIO AMPLIFIERS UP TO 30W RMS

DESCRIPTION

The PA02 and PA02A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting resistors (down to 10mA). Both amplifiers are internally compensated but are not recommended for use as unity gain followers. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

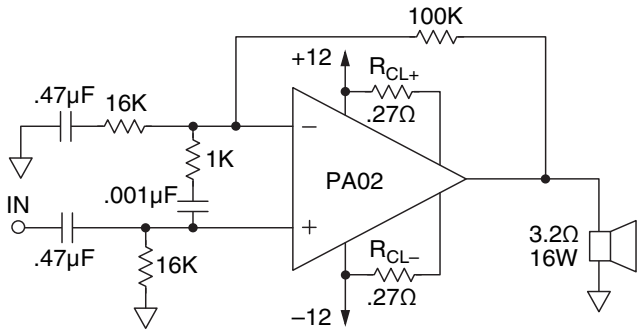
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. Isolation washers are not recommended. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

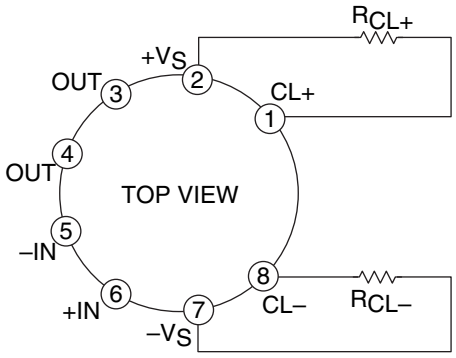
Vehicular Sound System Power Stage



LOW INTERNAL LOSS MAXIMIZES EFFICIENCY

When system voltages are low and power is at a premium, the PA02 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA02, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network. The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	38V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	48W
INPUT VOLTAGE, differential	±30V
INPUT VOLTAGE, common mode	$-V_S$+2V to $+V_S$–2V
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

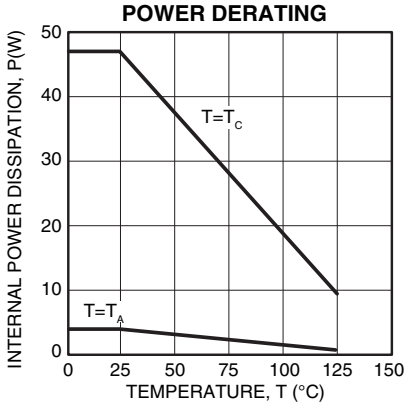
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 6]	PA02 MIN	PA02 TYP	PA02 MAX	PA02A MIN	PA02A TYP	PA02A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±50		*	±25	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±6			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		50	200		25	100	pA
BIAS CURRENT, vs. temperature	T_C = 85°C			200			*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		25	100		15	50	pA
OFFSET CURRENT, vs. temperature	T_C = 85°C			100			*	pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		1000			*		GΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLT. RANGE[5], Pos.	Full temperature range	$+V_S$ –6	$+V_S$ –3		*	*		V
COMMON MODE VOLT. RANGE[5], Neg.	Full temperature range	$-V_S$ +6	$-V_S$ +5		*	*		V
COMMON MODE REJECTION, DC	Full temperature range	70	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1kΩ load		103			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 10kΩ load	86	100		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, 10Ω load		4.5			*		MHz
POWER BANDWIDTH	T_C = 25°C, 10Ω load		350			*		kHz
PHASE MARGIN	Full temp. range, 10Ω load		30			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A, R_{CL} = .08Ω	±V_S –4	±V_S –3		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	±V_S –2	±V_S –1.2		*	*		V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.6			*		µs
SLEW RATE	T_C = 25°C	13	20		*	*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V > 10		SOA			*		
HARMONIC DISTORTION	P_O = .5W, F = 1kHz, R_L = 10Ω		.004			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, A_V = 1		100			*		ns
SMALL SIGNAL overshoot	R_L = 10Ω, A_V = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temperature range	±7	±15	±19	*	*	*	V
CURRENT, quiescent	T_C = 25°C		27	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

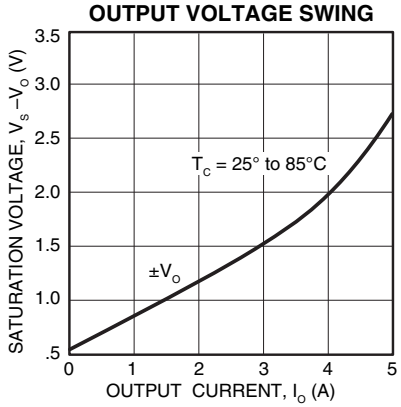
NOTES: * The specification of PA02A is identical to the specification for PA02 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Exceeding CMV range can cause the output to latch.
6. Full temperature specifications are guaranteed but not 100% tested.
7. The absolute maximum negative input voltage is equal to the negative power supply voltage plus 1V (-Vs + 1V).

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

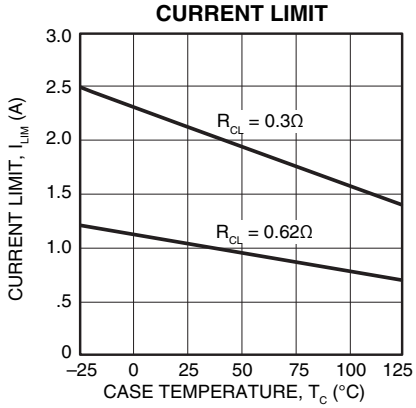
POWER DERATING



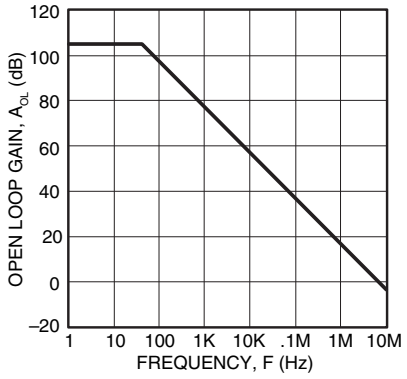
OUTPUT VOLTAGE SWING



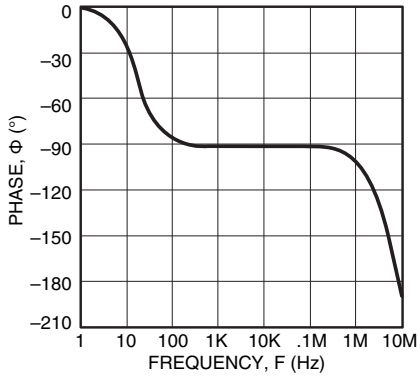
CURRENT LIMIT



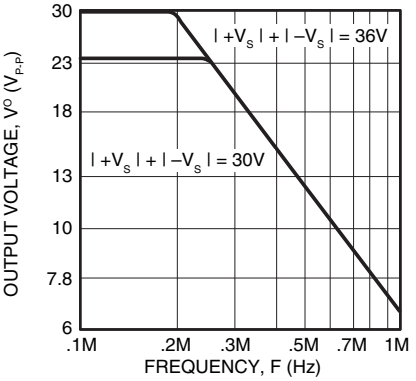
SMALL SIGNAL RESPONSE



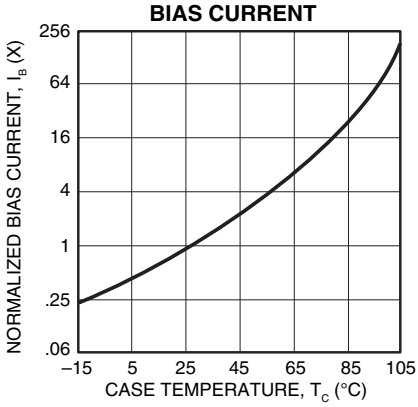
PHASE RESPONSE



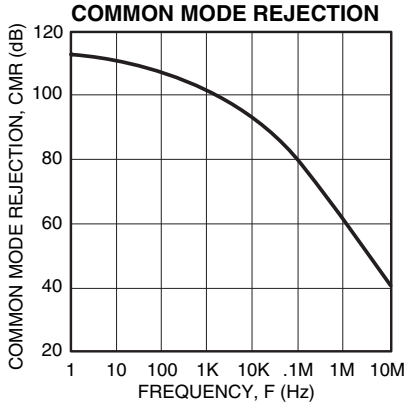
POWER RESPONSE



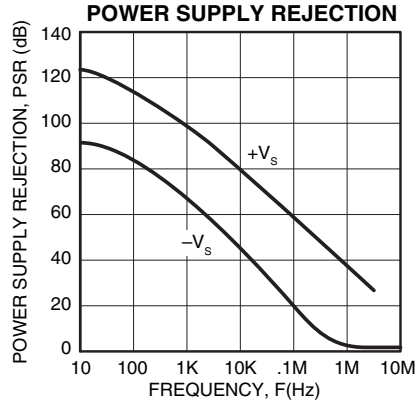
BIAS CURRENT



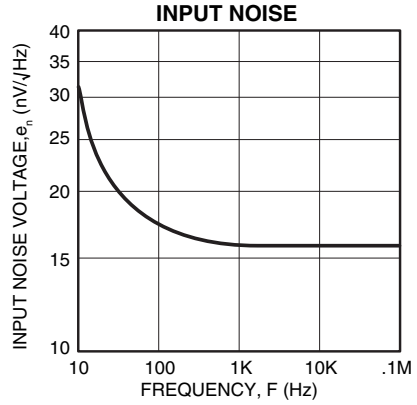
COMMON MODE REJECTION



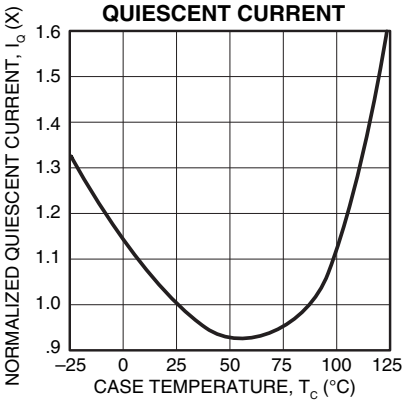
POWER SUPPLY REJECTION



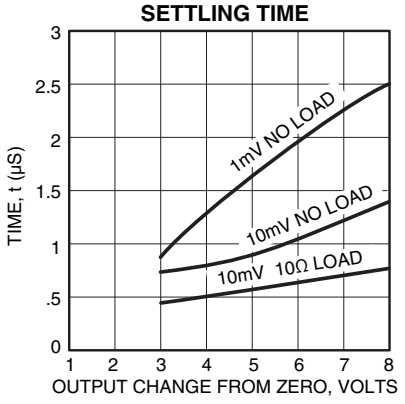
INPUT NOISE



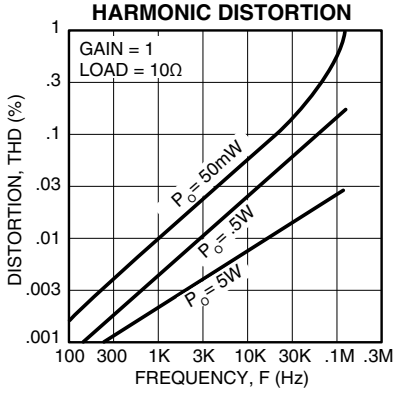
QUIESCENT CURRENT



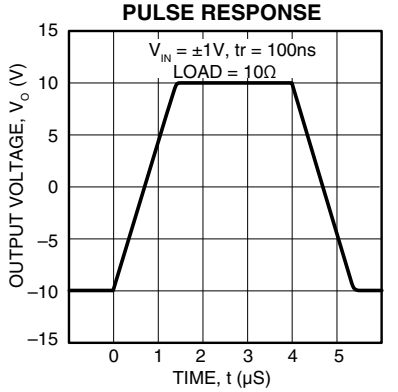
SETTLING TIME



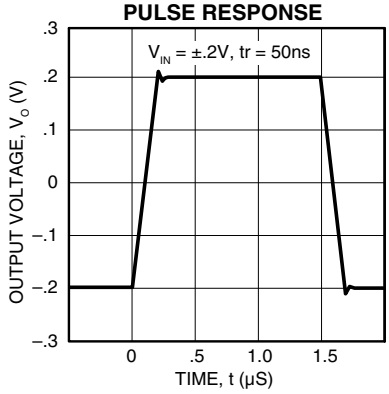
HARMONIC DISTORTION



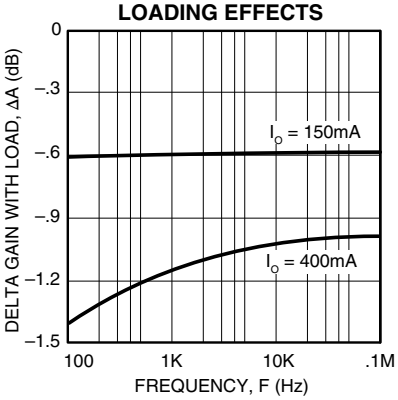
PULSE RESPONSE



PULSE RESPONSE



LOADING EFFECTS

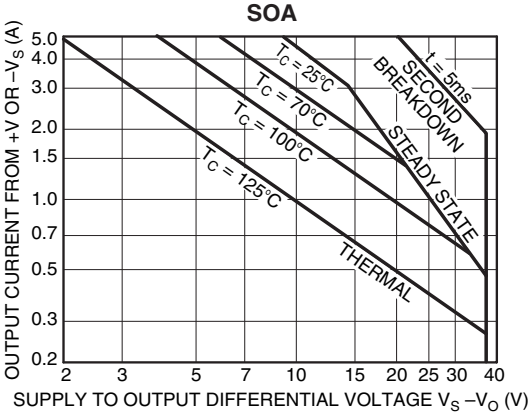


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA

SOA



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Under transient conditions, capacitive and dynamic* loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
18V	2mF	0.7mF	.2H	10mH
15V	10mF	2.2mF	.7H	25mH
10V	25mF	10mF	5H	50mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A, or 17V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L OR EMF LOAD	SHORT TO COMMON
18V	.5A	1.7A
15V	.7A	2.8A
10V	1.6A	4.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

DEVICE MOUNTING

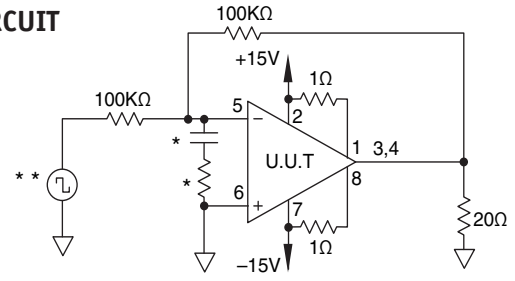
The case (mounting flange) is electrically isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω		40	mA
1	Input offset voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		10	mV
1	Input offset voltage	V_{OS}	25°C	±7V	V_{IN} = 0, A_V = 100		11.6	mV
1	Input offset voltage	V_{OS}	25°C	±19V	V_{IN} = 0, A_V = 100		10.8	mV
1	Input bias current, +IN	$+I_B$	25°C	±15V	V_{IN} = 0		200	pA
1	Input bias current, –IN	$–I_B$	25°C	±15V	V_{IN} = 0		200	pA
1	Input offset current	I_{OS}	25°C	±15V	V_{IN} = 0		100	pA
3	Quiescent current	I_Q	–55°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω		60	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		14	mV
3	Input offset voltage	V_{OS}	–55°C	±7V	V_{IN} = 0, A_V = 100		15.6	mV
3	Input offset voltage	V_{OS}	–55°C	±19V	V_{IN} = 0, A_V = 100		14.8	mV
3	Input bias current, +IN	$+I_B$	–55°C	±15V	V_{IN} = 0		200	pA
3	Input bias current, –IN	$–I_B$	–55°C	±15V	V_{IN} = 0		200	pA
3	Input offset current	I_{OS}	–55°C	±15V	V_{IN} = 0		100	pA
2	Quiescent current	I_Q	125°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω		60	mA
2	Input offset voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		15	mV
2	Input offset voltage	V_{OS}	125°C	±7V	V_{IN} = 0, A_V = 100		16.6	mV
2	Input offset voltage	V_{OS}	125°C	±19V	V_{IN} = 0, A_V = 100		15.8	mV
2	Input bias current, +IN	$+I_B$	125°C	±15V	V_{IN} = 0		30	nA
2	Input bias current, –IN	$–I_B$	125°C	±15V	V_{IN} = 0		30	nA
2	Input offset current	I_{OS}	125°C	±15V	V_{IN} = 0		10	nA
4	Output voltage, I_O = 5A	V_O	25°C	±9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
4	Output voltage, I_O = 36mA	V_O	25°C	±19V	R_L = 500Ω	18		V
4	Output voltage, I_O = 2A	V_O	25°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
4	Current limits	I_{CL}	25°C	±9V	R_L = 5Ω, R_{CL} = 1Ω	.54	.86	A
4	Stability/noise	E_N	25°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew rate	SR	25°C	±18V	R_L = 500Ω	13	100	V/µs
4	Open loop gain	A_{OL}	25°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
4	Common mode rejection	CMR	25°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB
6	Output voltage, I_O = 5A	V_O	–55°C	±9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
6	Output voltage, I_O = 36mA	V_O	–55°C	±19V	R_L = 500Ω	18		V
6	Output voltage, I_O = 2A	V_O	–55°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
6	Stability/noise	E_N	–55°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew rate	SR	–55°C	±18V	R_L = 500Ω	13	100	V/µs
6	Open loop gain	A_{OL}	–55°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
6	Common mode rejection	CMR	–55°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB
5	Output voltage, I_O = 3A	V_O	125°C	±7V	R_L = 1Ω, R_{CL} = 0Ω	3		V
5	Output voltage, I_O = 36mA	V_O	125°C	±19V	R_L = 500Ω	18		V
5	Output voltage, I_O = 2A	V_O	125°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
5	Stability/noise	E_N	125°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew rate	SR	125°C	±18V	R_L = 500Ω	8.5	100	V/µs
5	Open loop gain	A_{OL}	125°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
5	Common mode rejection	CMR	125°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

Replacing the LH0101 with the APEX PA02

BACKGROUND

In 1985, Apex Precision Power first addressed inquiries on how the PA02 could be used to second source the LH0101. Now, because of Apex Precision Power's commitment to continue production of the PA02, it is the part of choice for most new designs. For retrofit situations, the PA02 can be substituted for the LH0101 without requiring a PC layout change.

COMPARING THE LH0101 AND THE PA02

The PA02 can satisfy the majority of applications now using the 0101, and can often do it with improved frequency response, linearity and distortion. The table below and the notes that follow compare the two devices.

KEY SPECIFICATION COMPARISON

	LH0101 K	LH0101 AK	LH0101 CK	LH0101 ACK	**PA02**	**PA02A**	**PA02M**	Units
V_{OS}, Initial	10	3	10	3	10	3	10	mV
V_{OS}, vs. Temp	15	7	15	7	13	5.5	15	mV
Bias Current, Initial	1000	300	1000	300	200	100	200	pA
Offset Current, Initial	250	75	250	75	100	50	100	pA
Temp Range	–55/+125	–55/+125	–25/+85	–25/+85	–25/+85	–55/+125	–55/+125	°C
Power Bandwidth	300	300	300	300	350	350	350	kHz
Slew Rate (minimum)	N/A	7.5	N/A	7.5	13	13	13	V/µs
Distortion @ 0.5w, 1 kHz, 10 ohms (typical)	0.008	0.008	0.008	0.008	0.004	0.004	0.004	%

Note: The LH0101 is rated from ±5V to ±22V. The PA02 is rated from ±7V to ±19V. Do not use the PA02 below ±7V (14V total) or above ±19V (38V total).

PIN-OUT COMPARISON

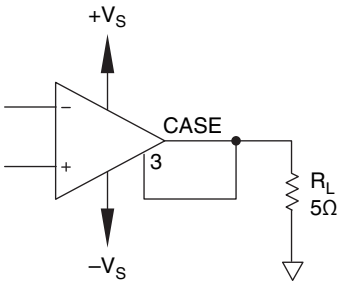
LH0101 Function	Pin No.	PA02 Function
SC+	1	RCL+
V+	2	$+V_S$
Feedback	3	Out
(Note 1)	4	Out
–IN	5	–IN
+IN	6	+IN
V–	7	$–V_S$
SC–	8	RCL–
Out	Case	Isolated

NOTE 1: MAY BE "OUT" OR "N/C", DEPENDING ON DATA SHEET REVISION

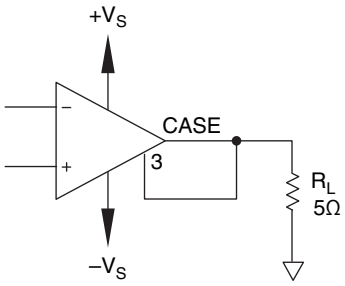
The PA02 can often drop into the LH0101 socket and improve performance in the areas noted above. This "drop in" status applies when the LH0101 does not employ the swing enhancement network. More simply stated, where Pin No. 3 is tied directly to the output (i.e., the case), the 0101 and PA02 are often interchangeable. For circuits which do employ the swing enhancement, one resistor should be removed and another replaced with a jumper. This retrofit saves parts and assembly cost and improves circuit efficiency by eliminating the drop across each of the two resistors. In both cases, the case of the PA02 is tied to the output. This is acceptable.

"DROP IN" EXAMPLE

LH0101

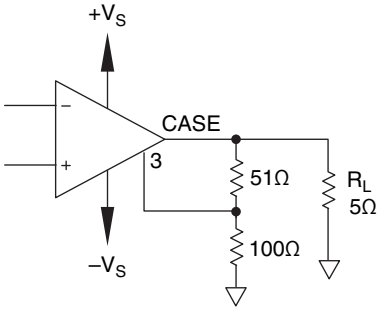


PA02

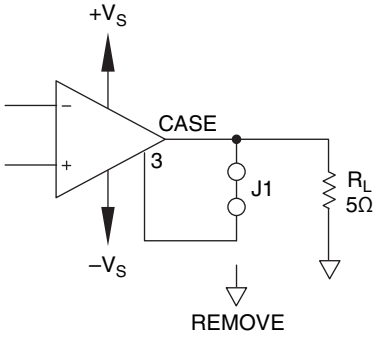


MODIFICATION EXAMPLE

LH0101



PA02



QUESTIONS?

If you have questions, or would like further assistance converting your design to the PA02, please call the Apex Precision Power Applications Design Support Request at (800) 625-4084.

Power Operational Amplifiers

FEATURES

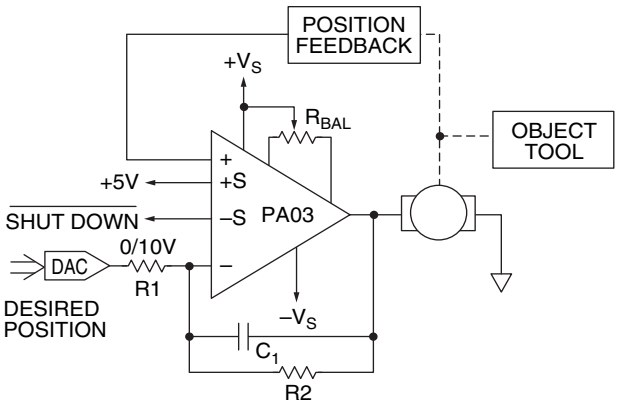
- MO-127 COPPER POWER DIP™ PACKAGE
- HIGH INTERNAL POWER DISSIPATION
  — 500 watts
- HIGH VOLTAGE OPERATION — ±75V
- VERY HIGH CURRENT — ±30 amps
- INTERNAL SOA PROTECTION
- OUTPUT SWINGS CLOSE TO SUPPLY RAILS
- EXTERNAL SHUTDOWN CONTROL

APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD DEFLECTION
- PROGRAMMABLE POWER SUPPLIES to ±68V
- TRANSDUCER/AUDIO TO 1000W

12-PIN DIP
PACKAGE STYLE CU

TYPICAL APPLICATION



DESCRIPTION

The super power PA03 advances the state of the art in both brute force power and self protection against abnormal operating conditions. Its features start with a copper dip package developed by Apex Precision Power to extend power capabilities well beyond those attainable with the familiar TO-3 package. The increased pin count of the new package provides additional control features, while the superior thermal conductivity of copper allows substantially higher power ratings.

The PA03 incorporates innovative current limiting circuits limiting internal power dissipation to a curve approximating the safe operating area of the power transistors. The internal current limit of 35A is supplemented with thermal sensing which reduces the current limit as the substrate temperature rises. Furthermore, a subcircuit monitors actual junction temperatures and with a response time of less than ten milliseconds reduces the current limit further to keep the junction temperature at 175°C.

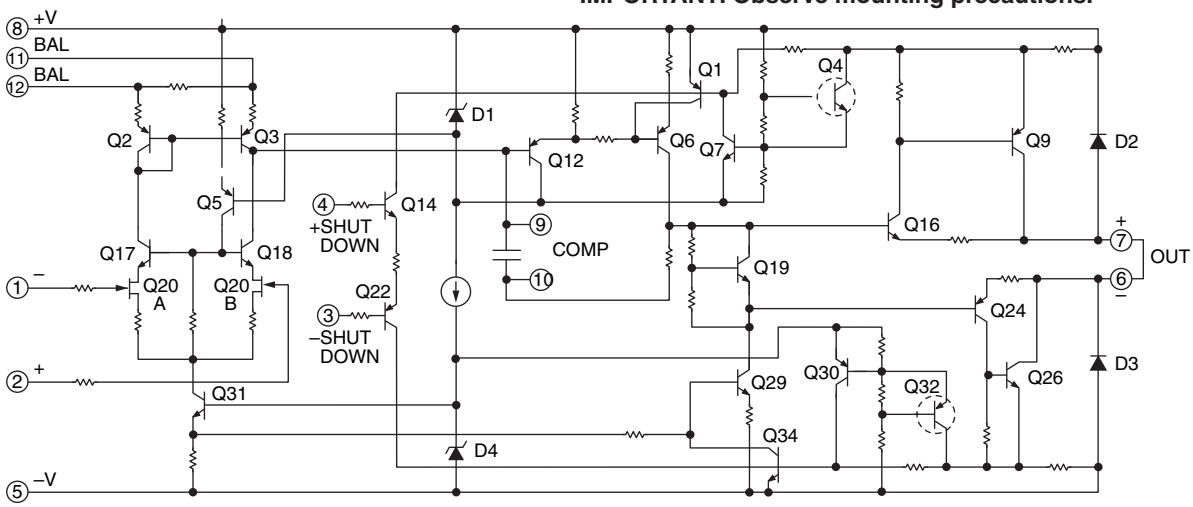
The PA03 also features a laser trimmed high performance FET input stage providing superior DC accuracies both initially and over the full temperature range.

The PA03 output power stages contain fast reverse recovery diodes for sustained high energy flyback protection.

This hybrid integrated circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 Copper, 12-pin Power Dip™ package (see Package Outlines), is hermetically sealed and isolated from the internal circuits. Insulating washers are not recommended.

IMPORTANT: Observe mounting precautions.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, within SOA	Internally limited
POWER DISSIPATION, internal	500W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMP. RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE, differential	±5V
SHUTDOWN VOLTAGE, common mode	$\pm V_S$

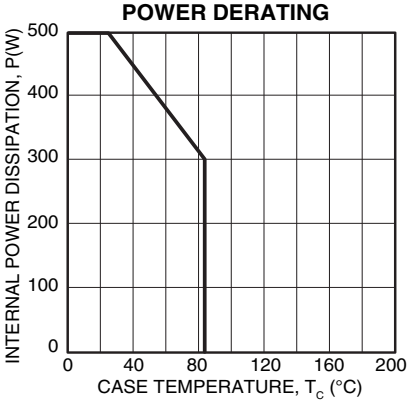
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA03 MIN	PA03 TYP	PA03 MAX	PA03A MIN	PA03A TYP	PA03A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		± .5	± 2		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$ –10V			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	108		*	*		dB
SHUTDOWN CURRENT[4]	Full temperature range		100			*		µA
SHUTDOWN VOLTAGE	Full temp. range, amp enabled			.85			*	V
SHUTDOWN VOLTAGE	Full temp. range, amp disabled	3.5			*			V
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	92	102		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 15A, V_O = $88V_{PP}$		30			*		kHz
PHASE MARGIN	Full temp. range, C_C = 1.8nF		65			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 30A	$\pm V_S$ –7	6.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 12A	$\pm V_S$ –5	4.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 146mA	$\pm V_S$ –4	3.5		*	*		V
CURRENT, peak	T_C = 25°C	30			*			A
SETTLING TIME to .1%	T_C = 25°C, 10V step		8			*		µs
SLEW RATE	T_C = 25°C, C_C - open		8			*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V = 1	2			*			nF
SHUTDOWN DELAY	T_C = –25°C, disable		10			*		µs
	T_C = –25°C, operate		20			*		µs
POWER SUPPLY								
VOLTAGE	Full temperature range	± 15	± 50	± 75	*	*	*	V
CURRENT, quiescent[6]	T_C = 25°C		125	300		*	*	mA
CURRENT, disable mode	Full temperature range		25	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, F>60Hz		.22	.28		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, F<60Hz		.25	.3		*	*	°C/W
RESISTANCE, junction to ambient	Full temperature range		14			*		°C/W
TEMPERATURE, junction	Sustained operation			150			*	°C
TEMPERATURE RANGE, case	Meets full range specification	– 25		85	*		*	°C

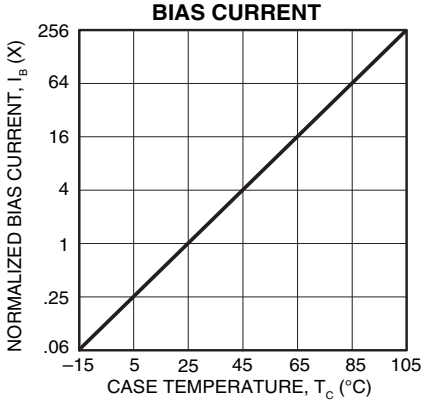
NOTES: * The specification of PA03A is identical to the specification for PA03 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if both shutdown inputs are least 1V inside supply rails. If one of the shutdown inputs is tied to a supply rail, the current in that pin may increase to 2.4mA.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The PA03 must be used with a heatsink or the quiescent power may drive the unit into thermal shutdown.

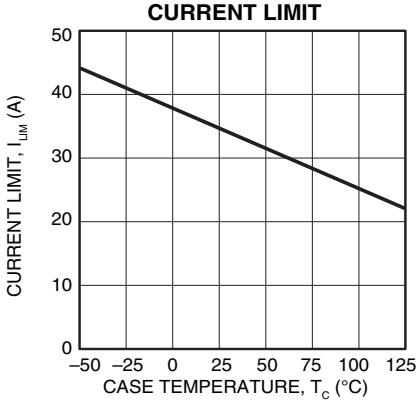
POWER DERATING



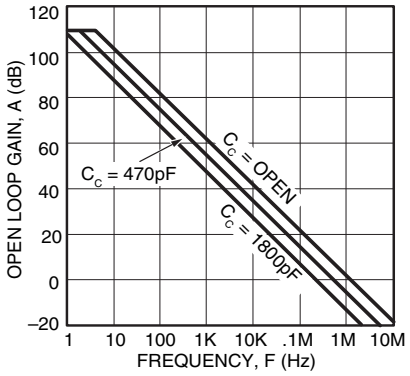
BIAS CURRENT



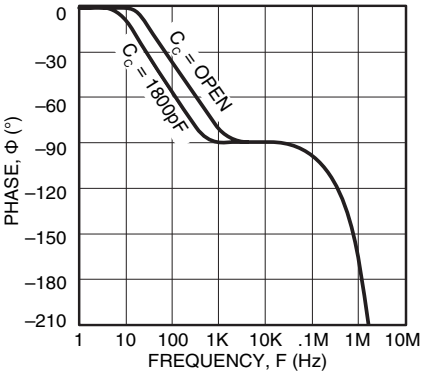
CURRENT LIMIT



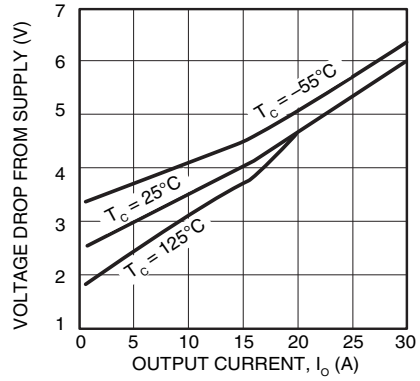
SMALL SIGNAL RESPONSE



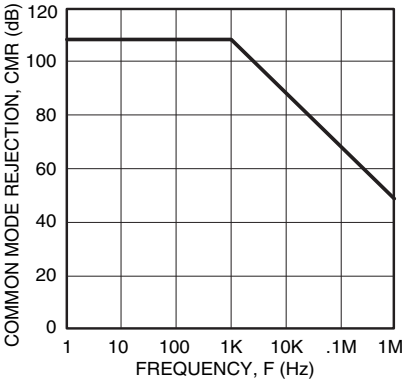
PHASE RESPONSE



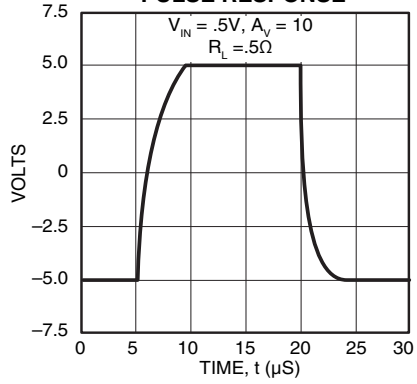
OUTPUT VOLTAGE SWING



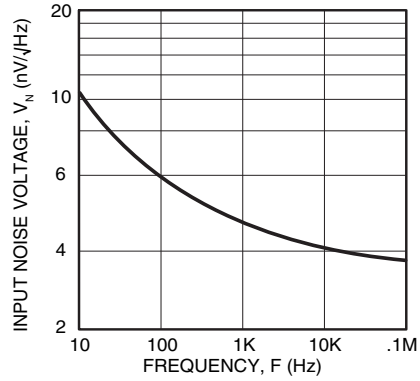
COMMON MODE REJECTION



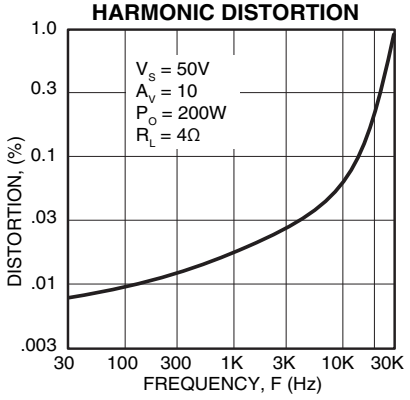
PULSE RESPONSE



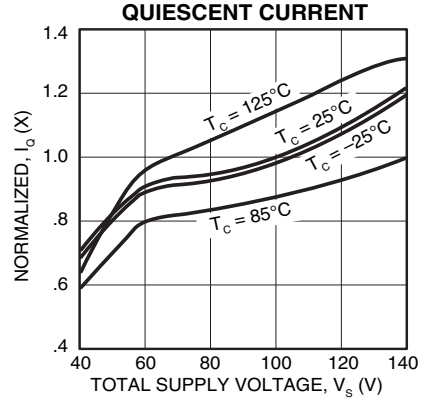
INPUT NOISE



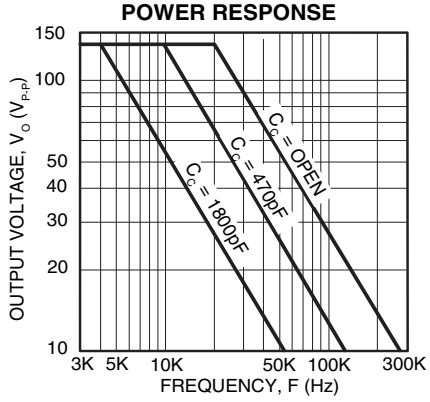
HARMONIC DISTORTION



QUIESCENT CURRENT

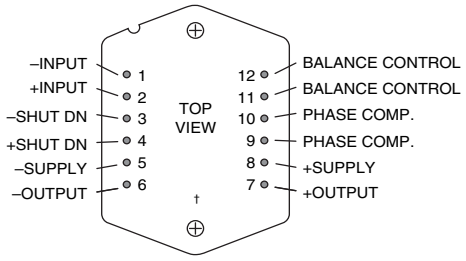


POWER RESPONSE



CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

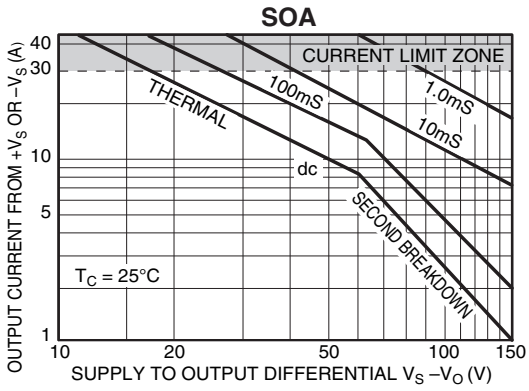
EXTERNAL CONNECTIONS



Pins 6 & 7 must be connected together.

If unused, tie Pins 11 & 12 to +SUPPLY.

† IMPORTANT: OBSERVE MOUNTING PRECAUTIONS. REVERSE INSERTION WILL DESTROY UNIT.



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

MOUNTING PRECAUTIONS

The PA03 copper base is very soft and easily bent. Do not put any stress on the mounting ears of this package. This calls for caution when pushing the amplifier into certain types of packaging foam and particularly when inserting the device into a socket. Insert the amplifier into the socket only by pushing on the perimeter of the package lid. Pushing the unit into the socket by applying pressure to the mounting tabs will bend the base due to the high insertion force required. The base will then not contact the heatsink evenly resulting in very poor heat transfer. To remove a unit from a socket, pry the socket away from the heatsink so that the heatsink will support the amplifier base evenly. Recommended mounting torque is 8–10 in.-lbs. (.9–1.13 N•m).

SAFE OPERATING AREA (SOA)

Due to the internal (non-adjustable) current limit of the PA03, worst case power dissipation calculations must assume current capability of 46 amps. Application specific circuits should be checked against the SOA curve when relying upon current limit for fault protection.

SAFE OPERATING AREA CURVES

Second breakdown limitations do apply to the PA03 but are less severe, since junction temperature limiting responds within 10ms. Stress levels shown as being safe for more than 10ms duration will merely cause thermal shutdown.

Under normal operating conditions, activation of the thermal shutdown is a sign that the internal junction temperatures have reached approximately 175°C. Thermal shutdown is a short term safety feature. If the conditions remain that cause thermal shutdown, the amplifier will oscillate in and out of shutdown, creating peak high power stresses, destroying useful signals, and reducing the reliability of the device.

BALANCE CONTROL

The voltage offset of the PA03 may be externally adjusted to zero. To implement this adjustment install a 100 to 200 ohm potentiometer between pins 11 and 12 and connect the wiper arm to the positive supply. Bypass pins 11 and 12 each with at least a .01µF ceramic capacitor.

If the optional adjust provision is not used, connect both pins 11 and 12 to the positive supply.

OUTPUT STAGE SHUTDOWN

The entire power stage of the PA03 may be disabled using one of the circuits shown in Figure 1. There are many applications for this function. One is a load protection based on power delivered to the load or thermal rise. Another one is conservation of power when using batteries. The control voltage requirements accommodate a wide variety logic drivers.

1. CMOS operating at +5V can drive the control pins directly.
2. CMOS operating at greater than 5V supplies need a voltage divider.
3. TTL logic needs a pull up resistor to +5V to provide a swing to the fully disabled voltage (3.5V). When not using the shutdown feature, connect both pins 3 and 4 to common.

PHASE COMPENSATION

At low gain settings an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered. A frequency of 1 MHz is most appropriate to calculate gain. Operation at gains below 10, without the external compensation capacitor opens the possibility of oscillations near output saturation regions when under load, the improper operation of the thermal shutdown circuit. This can result in amplifier destruction.

At gains of 10 or more:

1. No external components are required.
2. Typical slew rate will be 8V/µs.
3. Typical phase margin will be 70°.

At a gain of 3:
1. Connect a 470pF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 5V/µs.
3. Typical phase margin will be 45°.

At unity gain:
1. Connect a 1.8nF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 1.8V/µs.
3. Typical phase margin will be 65°.

FIGURE 1a. DIRECT DRIVE OF SHUTDOWN

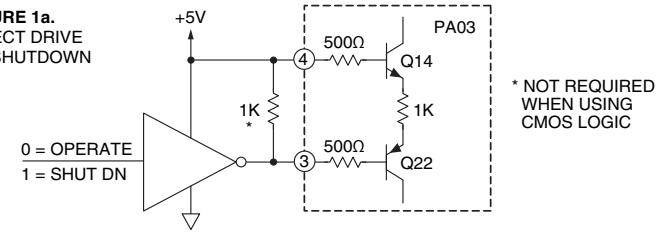


FIGURE 1b. HIGH VOLTAGE LOGIC INTERFACE

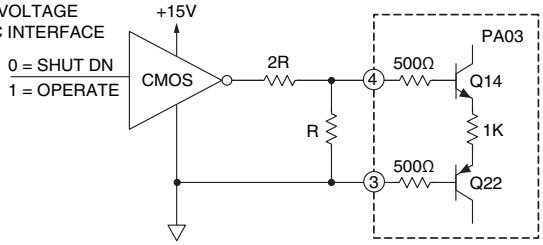
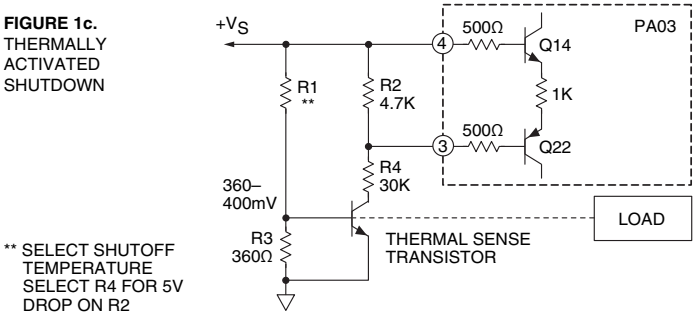


FIGURE 1c. THERMALLY ACTIVATED SHUTDOWN



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

PA04 • PA04A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- HIGH INTERNAL DISSIPATION — 200 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 200V, 20A
- HIGH SLEW RATE — 50V/µS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SLEEP MODE CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK09

APPLICATIONS

- SONAR TRANSDUCER DRIVER
- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±95V
- AUDIO UP TO 400W

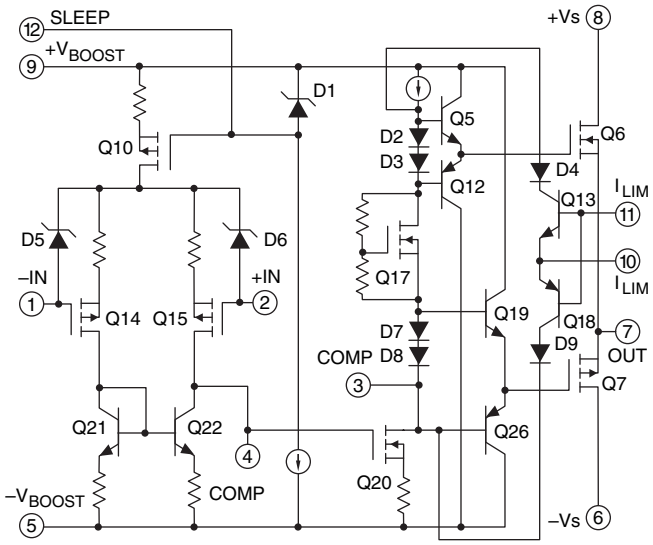
DESCRIPTION

The PA04 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA04 is a highly flexible amplifier. The sleep mode feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line.

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers will void product warranty.

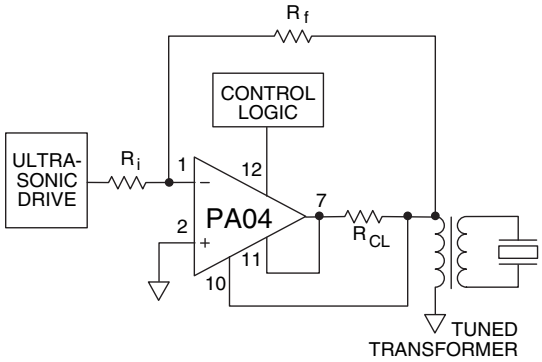
EQUIVALENT SCHEMATIC



12-PIN DIP
PACKAGE STYLE CR

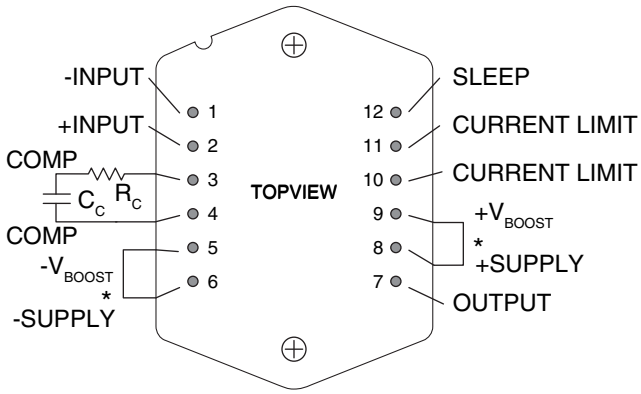
TYPICAL APPLICATION

The high power bandwidth and high voltage output of the PA04 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA04. Control logic turns off the amplifier in sleep mode.



Sonar Transducer Driver

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	100pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE
*See "BOOST OPERATION" paragraph.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, within SOA	20A
POWER DISSIPATION, internal	200W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA04 MIN	PA04 TYP	PA04 MAX	PA04A MIN	PA04A TYP	PA04A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			15			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$-8			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	98		*	*		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 100pF	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	I_O = 10A		2			*		MHz
POWER BANDWIDTH	R_L = 4.5Ω, V_O = 180V p-p C_C = 100pF, R_C = 120Ω		90			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 15A	$\pm V_S$-8.8	$\pm V_S$-7.5		*	*		V
VOLTAGE SWING	V_{BOOST} = Vs + 5V, I_O = 20A	$\pm V_S$-6.8	$\pm V_S$-5.5		*	*		V
CURRENT, peak		20			*			A
SETTLING TIME to .1%	A_V = 1, 10V step, R_L = 4Ω		2.5			*		µs
SLEW RATE	A_V = 10, C_C = 100pF, R_C = 120Ω	40	50			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = +1	10			*			nF
RESISTANCE			2			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±75	±100	*	*	*	V
CURRENT, quiescent, boost supply			30	40		*	*	mA
CURRENT, quiescent, total			70	90		*	*	mA
CURRENT, quiescent, total, sleep mode	Full temperature range		3	5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.5	.6		*	*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

NOTES: * The specification of PA04A is identical to the specification for PA04 in applicable column to the left.

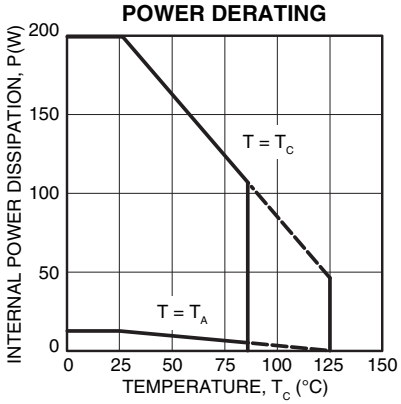
1. Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA04 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

CAUTION

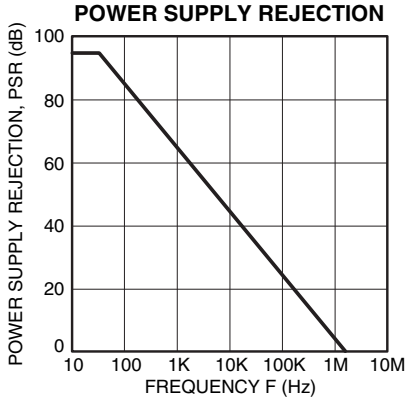
The PA04 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

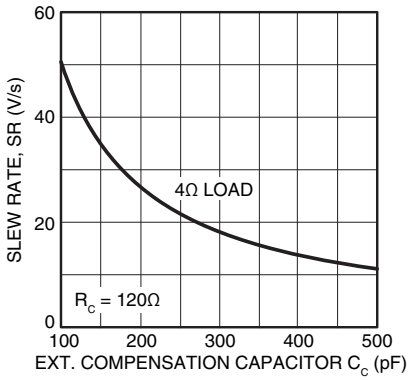
POWER DERATING



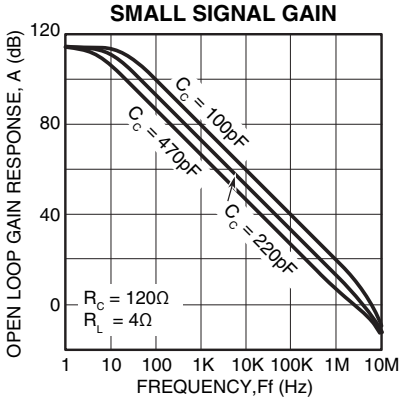
POWER SUPPLY REJECTION



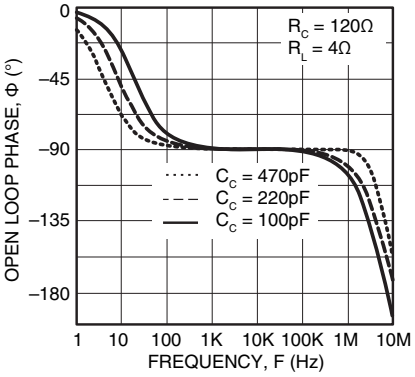
SLEW RATE



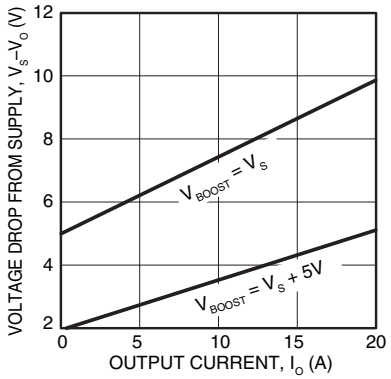
SMALL SIGNAL GAIN



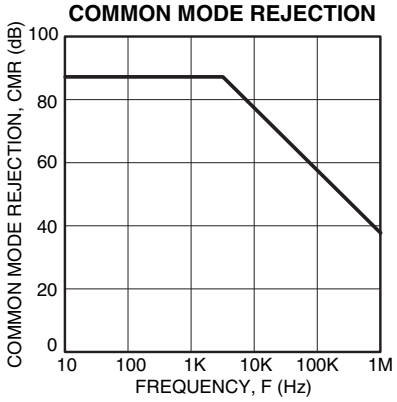
SMALL SIGNAL PHASE



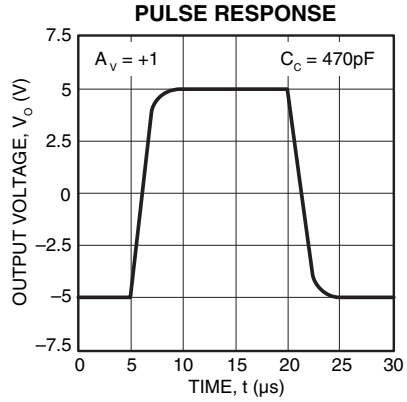
OUTPUT VOLTAGE SWING



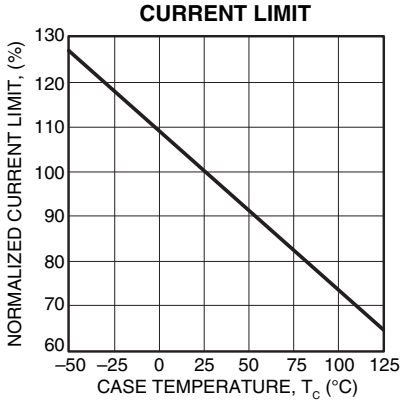
COMMON MODE REJECTION



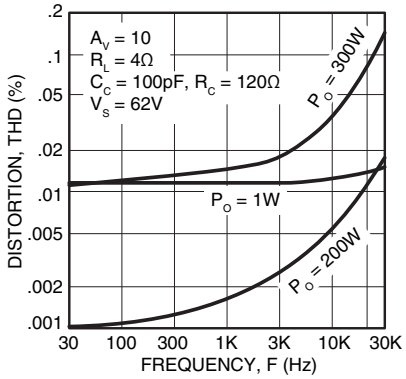
PULSE RESPONSE



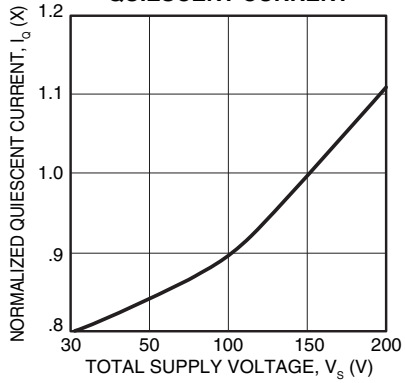
CURRENT LIMIT



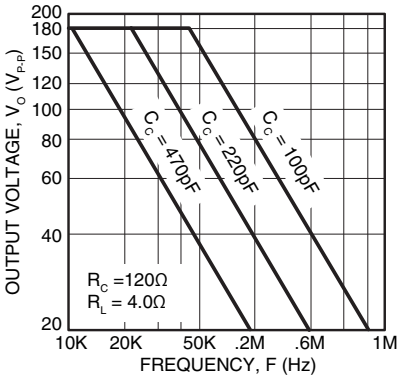
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



E

GENERAL

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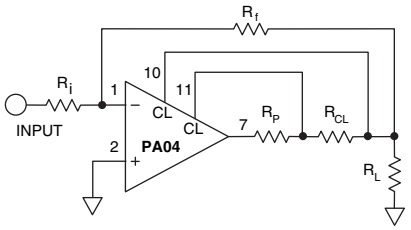
CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1. This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.76}{I_{LIMIT}}$$

Figure 1.
Current Limit.

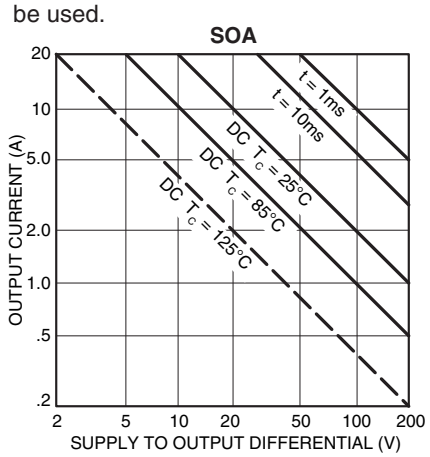


SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SLEEP MODE OPERATION

In the sleep mode, pin 12 (sleep) is tied to pin 9 ($+V_{BOOST}$). This disables the amplifier's internal reference and the amplifier shuts down except for a trickle current of 3 mA which flows into pin 12. Pin 12 should be left open if the sleep mode is not required.

Several possible circuits can be built to take advantage of this mode. In Figure 2A a small signal relay is driven by a logic gate. This removes the requirement to deal with the common mode voltage that exists on the shutoff circuitry since the sleep mode is referenced to the $+V_{BOOST}$ voltage.

In Figure 2B, circuitry is used to level translate the sleep mode input signal. The differential input activates sleep mode with a differential logic level signal and allows common mode voltages to $\pm V_{BOOST}$.

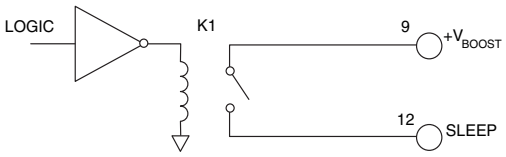


FIGURE 2A. SLEEP MODE CIRCUIT.

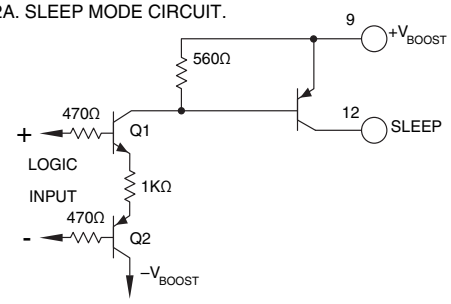


FIGURE 2B. SLEEP MODE CIRCUIT.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9) and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- HIGH INTERNAL DISSIPATION — 250 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 100V, 30A
- HIGH SLEW RATE — 100V/µS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SHUTDOWN CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK09

APPLICATIONS

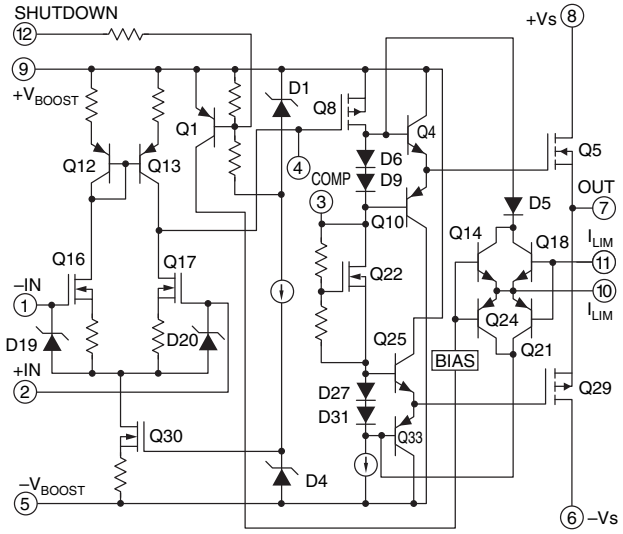
- LINEAR AND ROTARY MOTOR DRIVES
- sonar transducer driver
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±45V
- AUDIO UP TO 500W

DESCRIPTION

The PA05 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA05 is a highly flexible amplifier. The shutdown control feature allows the output stage to be turned off for standby operation or load protection during fault conditions. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors slew rate and bandwidth performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line. The output stage is protected by thermal limiting circuits above junction temperatures of 175°C.

EQUIVALENT SCHEMATIC

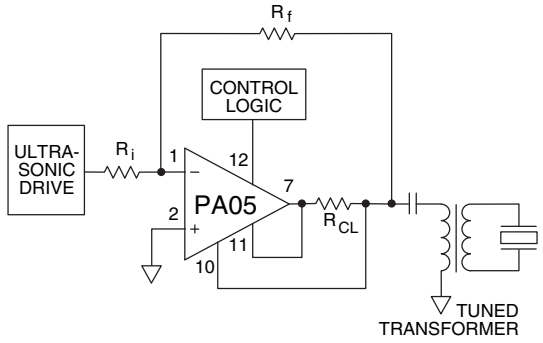


12-PIN POWER DIP PACKAGE STYLE CR

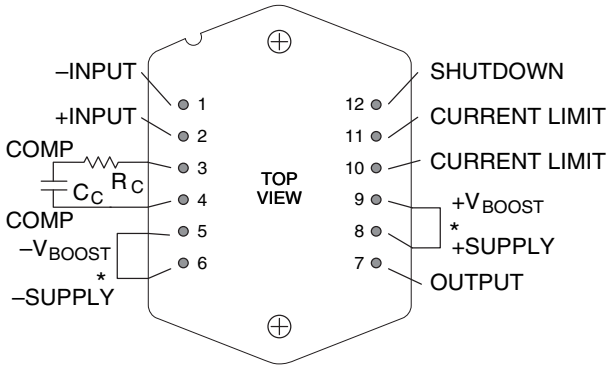
The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

TYPICAL APPLICATION

The high power bandwidth of the PA05 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA05. Control logic turns off the amplifier's output during shutdown.



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	82pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

*See BOOST OPERATION paragraph.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, continuous within SOA	30A
POWER DISSIPATION, internal	250W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA05 MIN	PA05 TYP	PA05 MAX	PA05A MIN	PA05A TYP	PA05A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			10	30		*	*	µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$–8			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	90	100		*	*		dB
INPUT NOISE	100KHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 82pF	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L = 10Ω		3			*		MHz
POWER BANDWIDTH	R_L = 4Ω, V_O = $80V_{P-P}$, A_V = –10 C_C = 82pF, R_C = 120Ω		400			*		kHz
PHASE MARGIN	Full temperature range, C_C = 470pF		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 20A	$\pm V_S$–9.5	$\pm V_S$–8.7		*	*		V
VOLTAGE SWING	V_{BOOST} = Vs + 5V, I_O = 30A	$\pm V_S$–5.8	$\pm V_S$–5.0		*	*		V
CURRENT, peak		30			*			A
SETTLING TIME to .1%	A_V = +1, 10V step, R_L = 4Ω		2.5			*		µs
SLEW RATE	A_V = –10, C_C = 82pF, R_C = 120Ω	80	100			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = +1	2.2			*			nF
RESISTANCE	I_O = 0, No load, 2MHz		5			*		Ω
	I_O = 1A, 2MHz		2			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±45	±50	*	*	*	V
CURRENT, quiescent, boost supply			46	56		*	*	mA
CURRENT, quiescent, total			90	120		*	*	mA
CURRENT, quiescent, total, shutdown			46	56		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.4	.5		*	*	°C/W
RESISTANCE, junction to air[4]	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

NOTES: * The specification of PA05A is identical to the specification for PA05 in applicable column to the left.

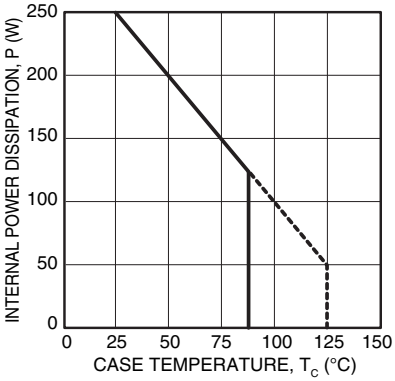
1. Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA05 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

CAUTION

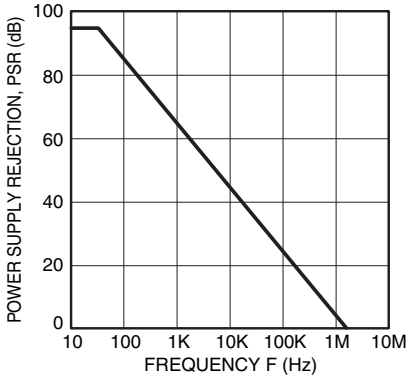
The PA05 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

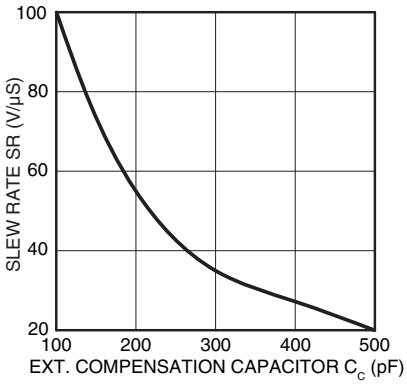
POWER DERATING



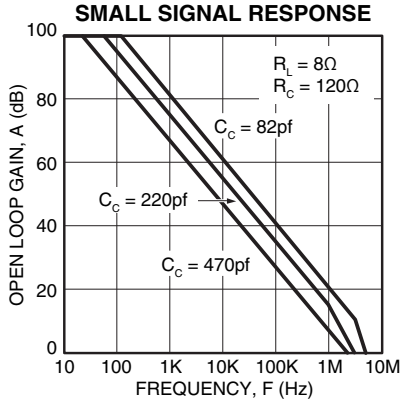
POWER SUPPLY REJECTION



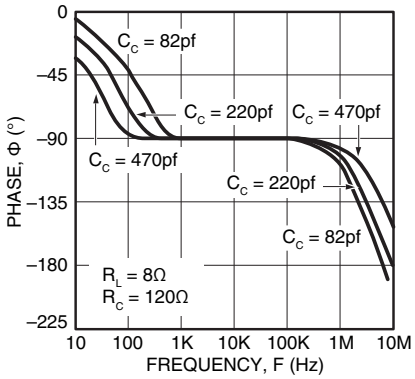
SLEW RATE vs. COMP



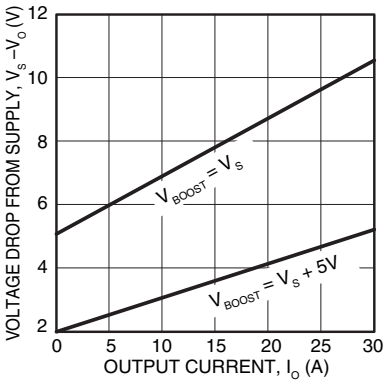
SMALL SIGNAL RESPONSE



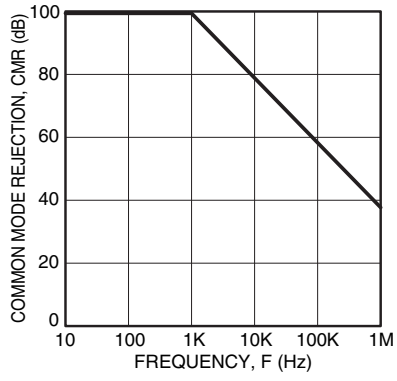
PHASE RESPONSE



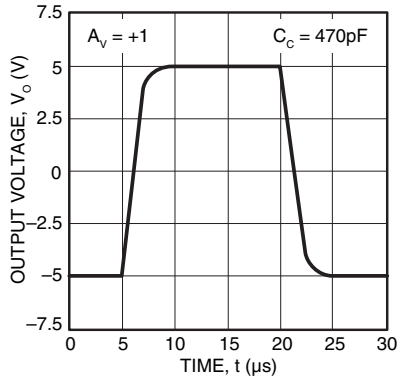
OUTPUT VOLTAGE SWING



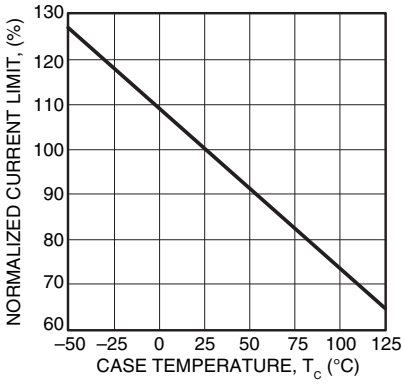
COMMON MODE REJECTION



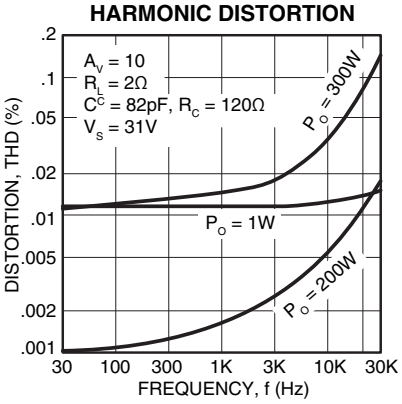
PULSE RESPONSE



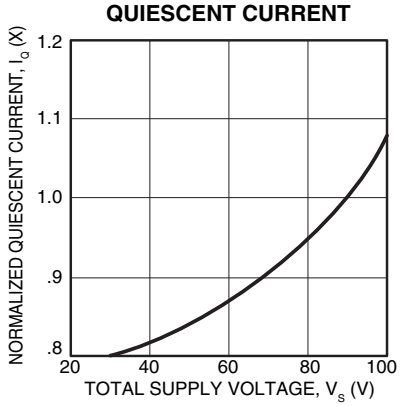
CURRENT LIMIT



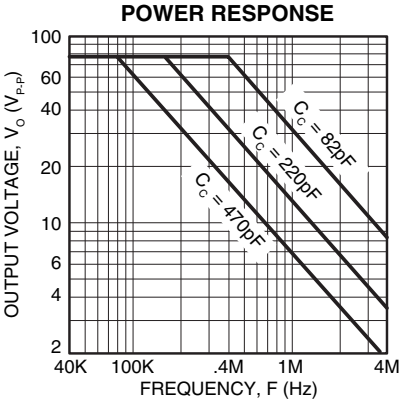
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

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CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. *For the current limit to work correctly, pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.* This connection will bypass any parasitic resistances, R_P formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1. If current limiting is not used, pins 10 and 11 must be tied to pin 7.

The value of the current limit resistor can be calculated as follows:

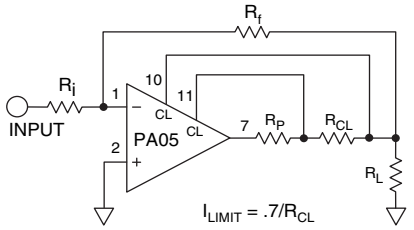


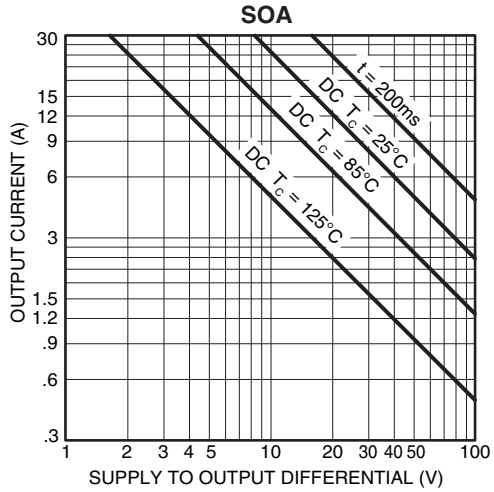
FIGURE 1. CURRENT LIMIT

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



The output stage thermal protection circuit engages when junction temperatures reach approximately 175C. If the condition remains that caused the shutdown, the amplifier may oscillate in and out of shutdown, creating high peak power stresses reducing the reliability of the device.

SHUTDOWN OPERATION

To disable the output stage, pin 12 is connected to ground via relay contacts or via an electronic switch. The switching device must be capable of sinking 2mA to complete shutdown and capable of standing off the supply voltage $+V_S$. See Figure 2 for suggested circuits.

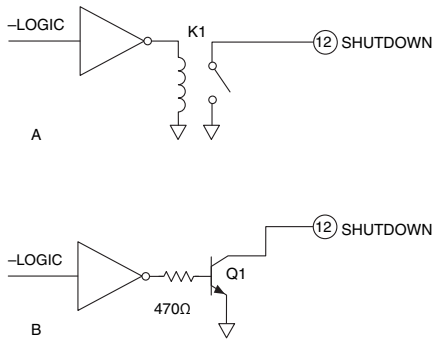


FIGURE 2. SHUTDOWN OPERATION

From an internal circuitry standpoint, shutdown is just a special case of current limit where the allowed output current is zero. As with current limit, however, a small current does flow in the output during shutdown. A load impedance of 100 ohms or less is required to insure the output transistors are turned off. Note that even though the output transistors are off the output pin is not open circuited because of the shutdown operating current.

BOOST OPERATION

With the V_{BOOST} feature, the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9), and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains, more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

PA07 • PA07A

FET Input Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- LOW BIAS CURRENT — FET Input
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±12V TO ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

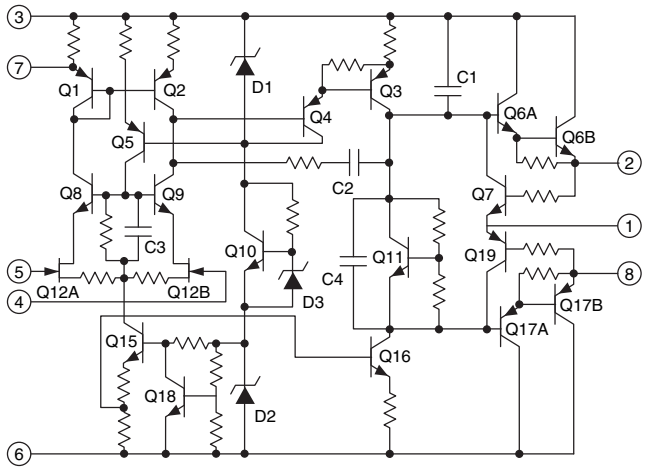
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

DESCRIPTION

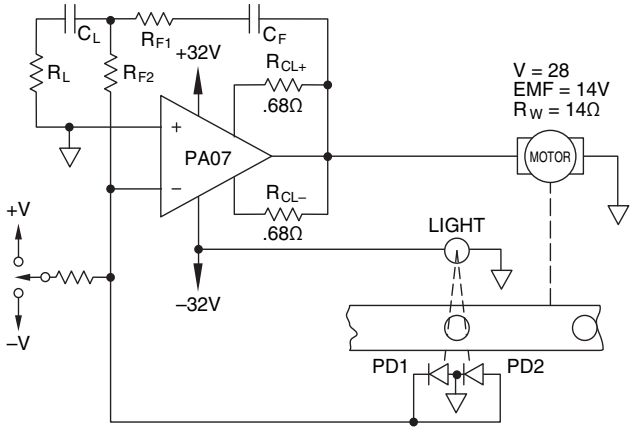
The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



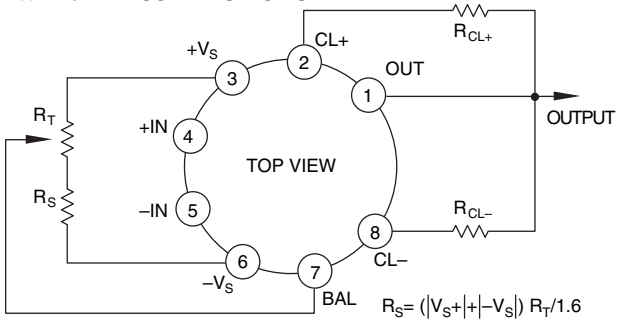
TYPICAL APPLICATION



Negates optoelectronic instabilities
Lead network minimizes overshoot
SEQUENTIAL POSITION CONTROL

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C1 and R1 optimize system response by reducing overshoot. The very low bias current of the PA07 augments performance of the integrator circuit.

EXTERNAL CONNECTIONS



NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	67W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

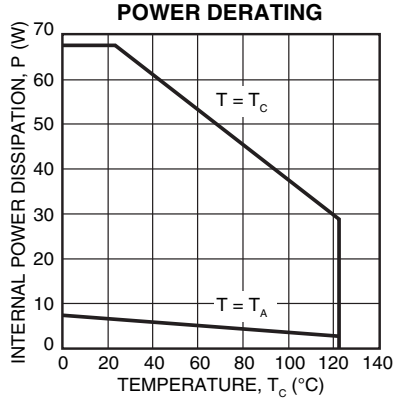
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA07 MIN	PA07 TYP	PA07 MAX	PA07A MIN	PA07A TYP	PA07A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT,vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	Full temperature range, V_{CM} = ±20V		120			*		dB
GAIN								
OPEN LOOP GAIN at 15Hz	T_C = 25°C, R_L = 15Ω	89	95		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, R_L = 15Ω		1.3			*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L = 15Ω		18			*		kHz
PHASE MARGIN	Full temperature range, R_L = 15Ω		70			*		°
OUTPUT								
VOLTAGE SWING[4]	Full temp. range, I_O = 5A	$\pm V_S$–5			*			V
VOLTAGE SWING[4]	Full temp. range, I_O = 2A	$\pm V_S$–5			*			V
VOLTAGE SWING[4]	Full temp. range, I_O = 90mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		1.5			*		µs
SLEW RATE	T_C = 25°C		5			*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			1			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±12	±35	±50	*	*	*	V
CURRENT, quiescent	T_C = 25°C		18	30		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

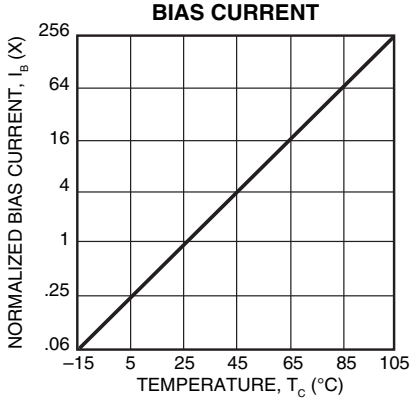
NOTES: * The specification of PA07A is identical to the specification for PA07 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

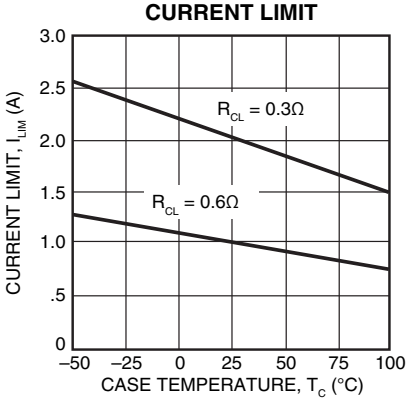
POWER DERATING



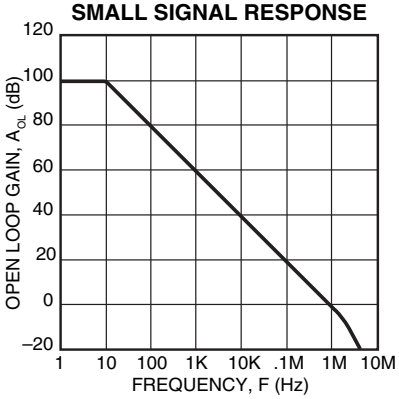
BIAS CURRENT



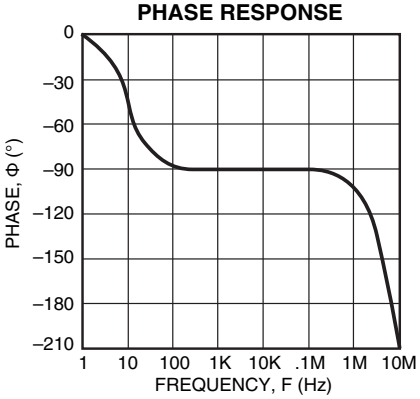
CURRENT LIMIT



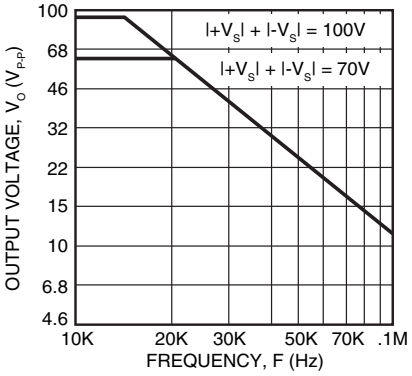
SMALL SIGNAL RESPONSE



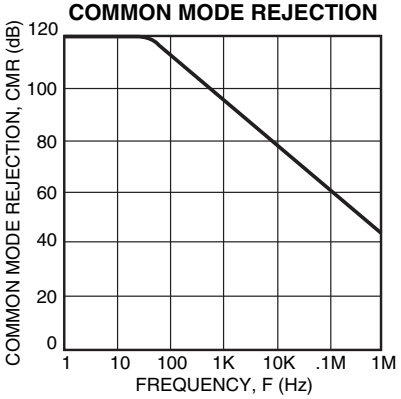
PHASE RESPONSE



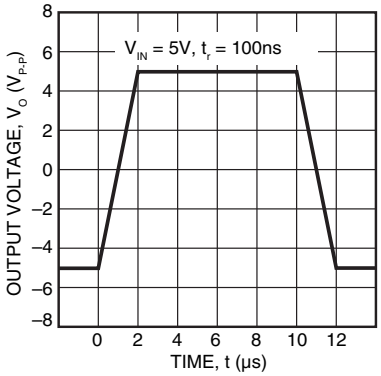
POWER RESPONSE



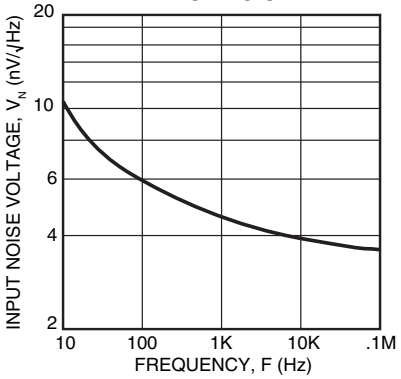
COMMON MODE REJECTION



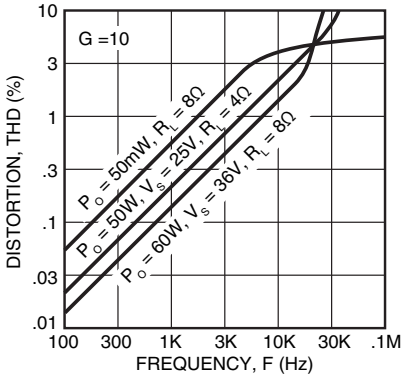
PULSE RESPONSE



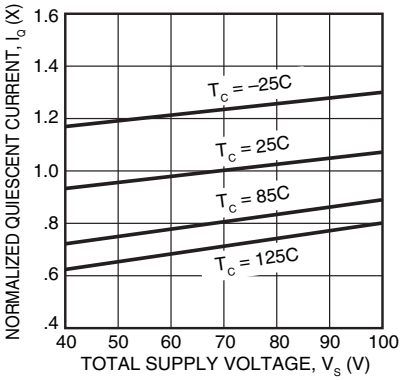
INPUT NOISE



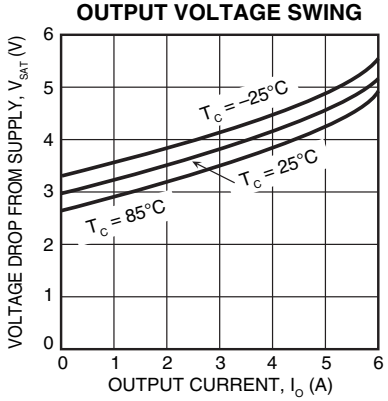
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



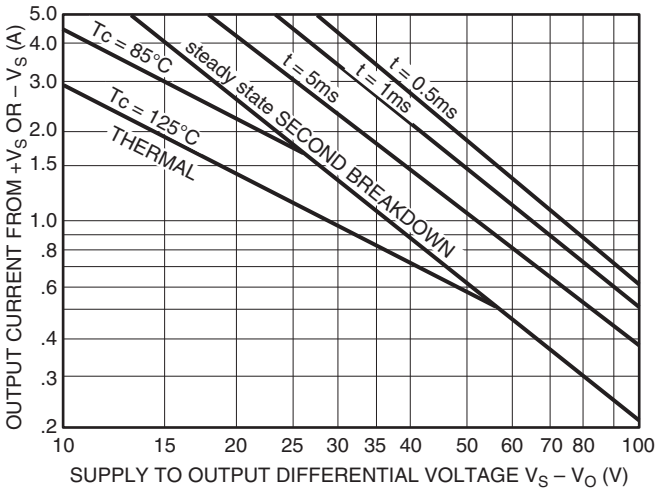
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.



SAFE OPERATING AREA CURVES

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the new SOA graph.
   For sine wave outputs, use Power Design[1] to plot a load line. Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.
   For other waveform outputs, manual load line plotting is recommended. Applications Note 22, SOA AND LOAD LINES, will be helpful. A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges.
2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.21A	.61A
40V	.3A	.87A
30V	.46A	1.4A
20V	.87A	2.5A
15V	1.4A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

CURRENT LIMIT

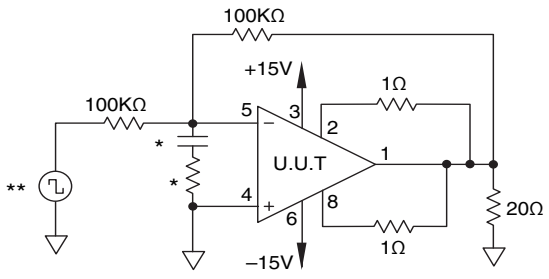
Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for R_{CL} is .12Ω, however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

[1] Note 1. Power Design is a self-extracting Excel spreadsheet available free from www.Cirrus.com

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		4.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		46	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		6.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±50V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		30	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		7.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±15.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 90mA	V_O	25°C	±50V	R_L = 500Ω	45		V
4	Output Voltage, I_O = 2A	V_O	25°C	±29V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±19V	R_L = 12Ω, R_{CL} = 1Ω	.54	.86	A
4	Stability/Noise	E_N	25°C	±35V	R_L = 100Ω, A_V = 1, C_L = 1nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500Ω	2.5	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500Ω, F = 15Hz	89		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB
6	Output Voltage, I_O = 5A	V_O	–55°C	±15.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 90mA	V_O	–55°C	±50V	R_L = 500Ω	45		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±29V	R_L = 12Ω	24		V
6	Stability/Noise	EN	–55°C	±35V	R_L = 100Ω, A_V = 1, C_L = 1nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500Ω	2.5	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500Ω, F = 15Hz	89		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 90mA	V_O	125°C	±50V	R_L = 500Ω	45		V
5	Output Voltage, I_O = 2A	V_O	125°C	±29V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	125°C	±35V	R_L = 100Ω, A_V = 1, C_L = 1nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500Ω	1.25	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500Ω, F = 15Hz	89		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA08 • PA08A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH OUTPUT CURRENT — Up to ±150mA
- LOW BIAS CURRENT — FET Input

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

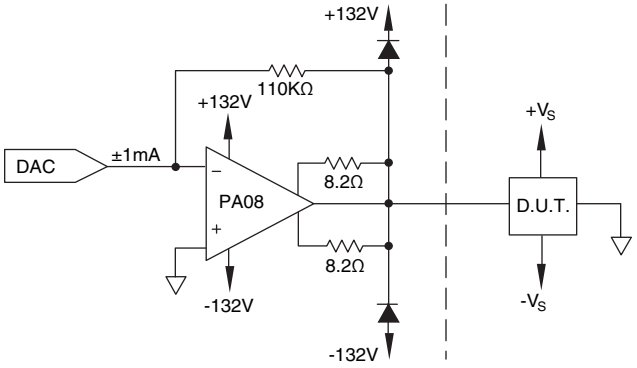
8-PIN TO-3
PACKAGE STYLE CE

DESCRIPTION

The PA08 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

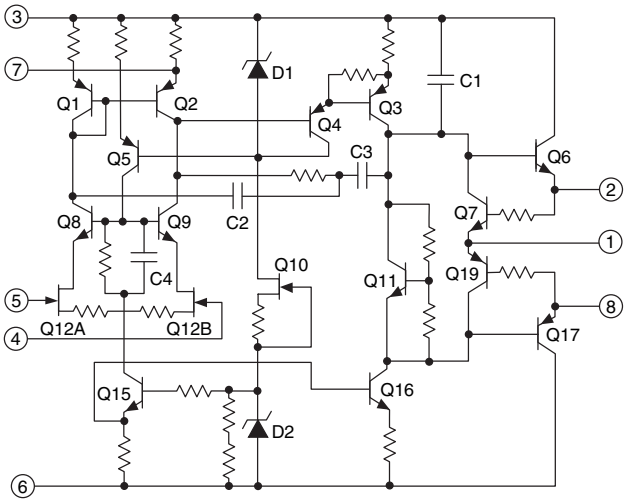
TYPICAL APPLICATION



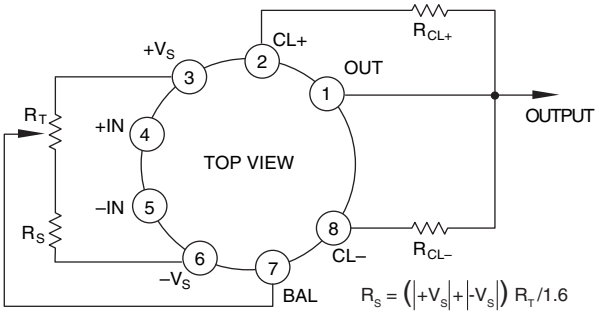
ATE PIN DRIVER

The PA08 as a pin driver is capable of supplying high test voltages to a device under test (DUT). Due to the possibility of short circuits to any terminal of the DUT, current limit must be set to be safe when limiting with a supply to output voltage differential equal to the amplifier supply plus the largest magnitude voltage applied to any other pin of the DUT. In addition, flyback diodes are recommended when the output of the amplifier exits any equipment enclosure to prevent damage due to electrostatic discharges. Refer to Application Note 7 for details on accuracy considerations of this circuit.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



$R_S = \left(|+V_S| + |-V_S|\right) R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	200mA
POWER DISSIPATION, internal at T_C = 25°C	17.5W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

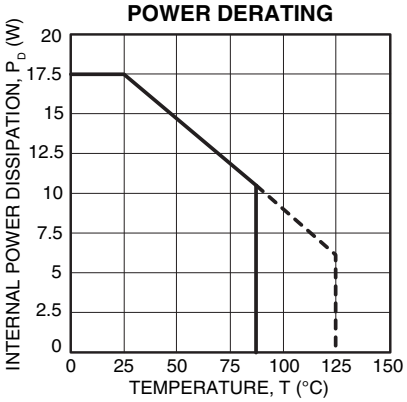
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA08 MIN	PA08 TYP	PA08 MAX	PA08A MIN	PA08A TYP	PA08A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25°C to +85°C		±15	±30		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			*	2	µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√kh
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^5			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	T_C = –25°C to +85°C	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	T_C = –25°C to +85°C, V_{CM} = ±90V		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = ∞		118			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1.2KΩ	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, R_L = 1.2KΩ		5			*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L = 1.2KΩ		90			*		kHz
PHASE MARGIN	T_C = –25 to +85°C		60			*		°
OUTPUT								
VOLTAGE SWING[4]	T_C = 25°C, I_O = 150mA	$\pm V_S$–15	$\pm V_S$–8		*	*		V
VOLTAGE SWING[4]	T_C = –25° C to +85°C, I_O = ±75mA	$\pm V_S$–10	$\pm V_S$–5		*	*		V
VOLTAGE SWING[4]	T_C = –25° C to +85°C, I_O = ±20mA	$\pm V_S$–5	$\pm V_S$–3		*	*		V
CURRENT, peak	T_C = 85°C	150			*			mA
SLEW RATE	T_C = 25°C		30		20	*		V/µs
CAPACITIVE LOAD, A_V = 1	T_C = –25 to +85°C			10			*	nF
CAPACITIVE LOAD, A_V > 4	T_C = –25 to +85°C			SOA			*	
SETTLING TIME to .1%	T_C = 25°C, R_L = 1.2KΩ, 2V step		1			*		µs
POWER SUPPLY								
VOLTAGE	T_C = –55 to +125°C	±15	±100	±150	*	*	*	V
CURRENT, quiescent	T_C = 25°C		6	8.5		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	T_C = –55 to +125°C, F > 60Hz		4.26			*		°C/W
RESISTANCE, DC junction to case	T_C = –55 to +125°C, F < 60Hz		6.22	8.57		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

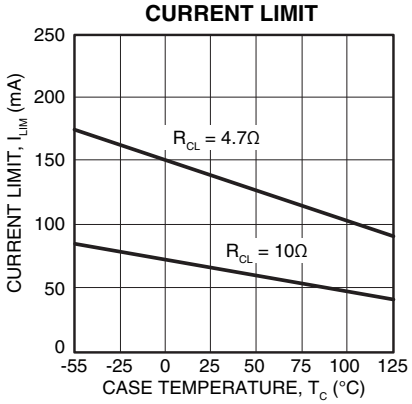
NOTES: * The specification of PA08A is identical to the specification for PA08 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage specified under typical (TYP) applies unless otherwise noted.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

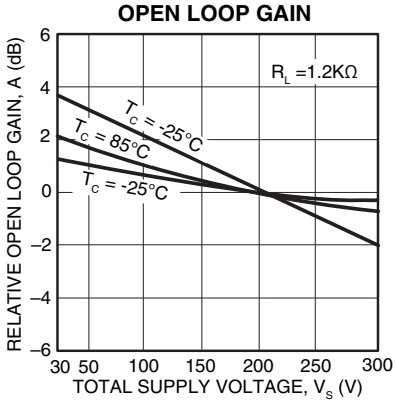
POWER DERATING



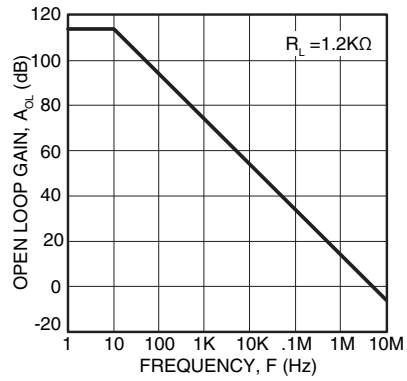
CURRENT LIMIT



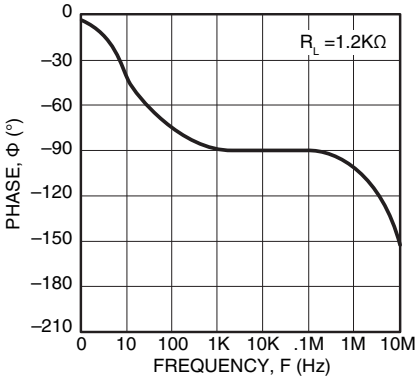
OPEN LOOP GAIN



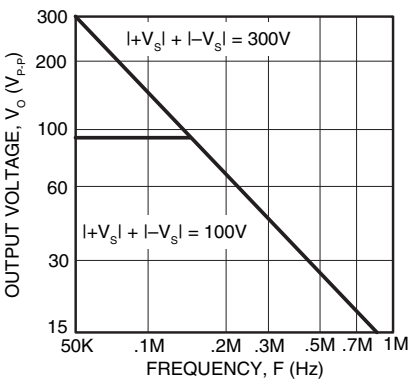
SMALL SIGNAL RESPONSE



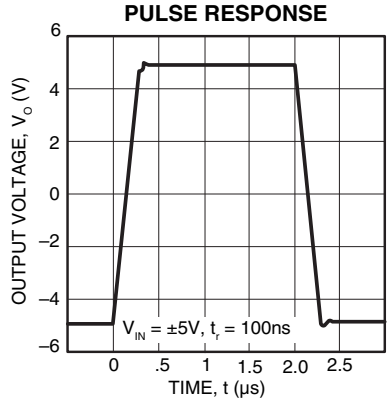
PHASE RESPONSE



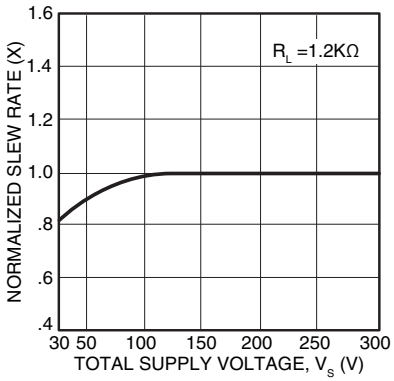
POWER RESPONSE



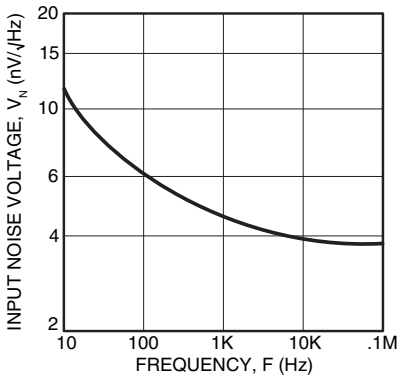
PULSE RESPONSE



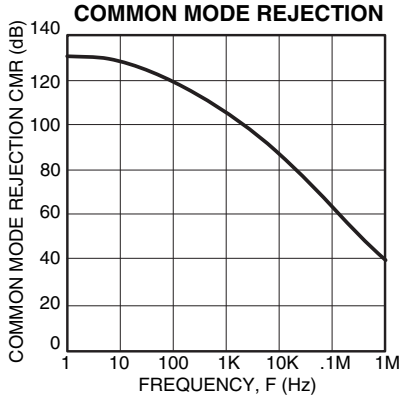
SLEW RATE



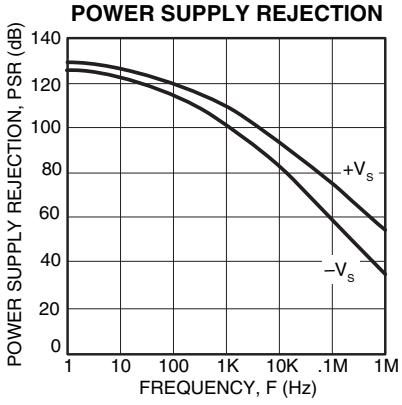
INPUT NOISE



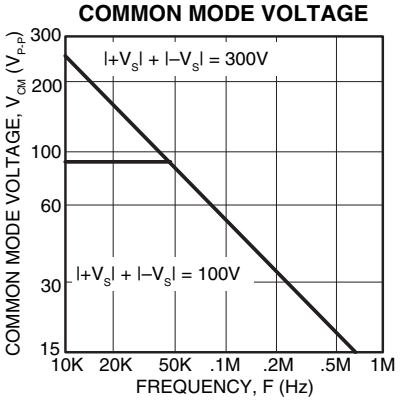
COMMON MODE REJECTION



POWER SUPPLY REJECTION



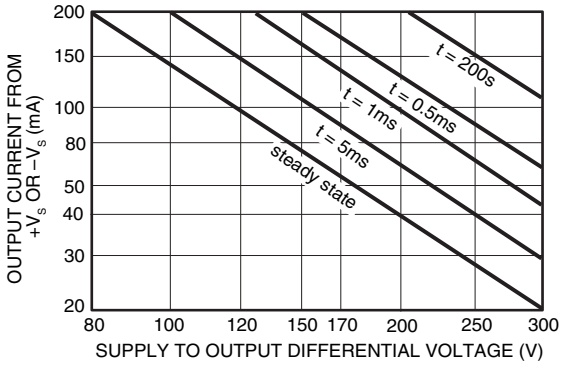
COMMON MODE VOLTAGE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)



The output stage of most power amplifiers has two distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, the following capacitive and inductive loads are safe with the current limits set to the maximum:

$\pm V_S$	C(MAX)	L(MAX)
150V	.4µF	280mH
125V	.9µF	380mH
100V	2µF	500mH
75V	10µF	1200mH
50V	100µF	13H

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or simple shorts to common if the current limits are set as follows:

$\pm V_S$	SHORT TO $\pm V_{SC}$, C, L, OR EMF LOAD	SHORT TO COMMON
150V	20mA	67mA
125V	27mA	90mA
100V	42mA	130mA
75V	67mA	200mA
50V	130mA	200mA

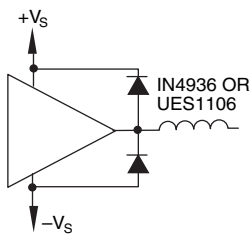
These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INDUCTIVE LOADS

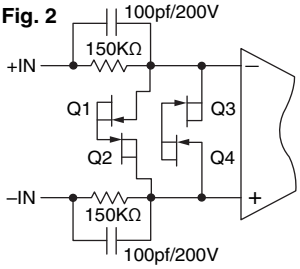
Two external diodes as shown in Figure 1, are required to protect these amplifiers from flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

Fig. 1



PROTECTION, INDUCTIVE LOAD

Fig. 2



PROTECTION, OVERVOLTAGE

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

INPUT PROTECTION

The input is protected against common mode voltages up to the supply rails and differential voltages up to ±50V. Increased protection against differential input voltages can be obtained by adding 2 resistors, 2 capacitors and 4 diode connected FETs as shown in Figure 2.

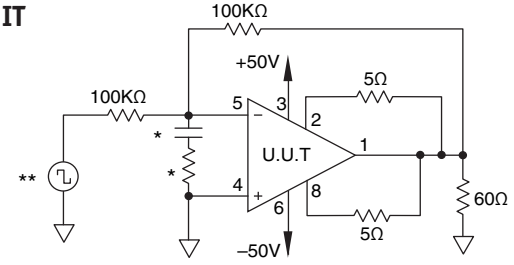
CURRENT LIMITING

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 3.24Ω. However, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±100V	V_{IN} = 0, A_V = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±100V	V_{IN} = 0, A_V = 100		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		3.7	mV
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±100V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±100V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±100V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±100V	V_{IN} = 0, A_V = 100		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±100V	V_{IN} = 0, A_V = 100		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		6.1	mV
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		5.4	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±100V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±100V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±100V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±100V	V_{IN} = 0, A_V = 100		12	mA
2	Input Offset Voltage	V_{OS}	125°C	±100V	V_{IN} = 0, A_V = 100		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		6.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		6	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±100V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±100V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±100V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 150mA	V_O	25°C	±31V	R_L = 100Ω	15		V
4	Output Voltage, I_O = 29mA	V_O	25°C	±150V	R_L = 5K	145		V
4	Output Voltage, I_O = 80mA	V_O	25°C	± 90V	R_L = 1K	80		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±100V	R_L = 5K, A_V = 1, C_L = 1nF		1	mV
4	Slew Rate	SR	25°C	±100V	R_L = 5K	20	100	V/µs
4	Open Loop Gain	A_{OL}	25°C	±100V	R_L = 5K, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 100mA	V_O	–55°C	±31V	R_L =100Ω	10		V
6	Output Voltage, I_O = 29mA	V_O	–55°C	±150V	R_L = 5K	145		V
6	Output Voltage, I_O = 70mA	V_O	–55°C	±90V	R_L = 1K	70		V
6	Stability/Noise	E_N	–55°C	±100V	R_L = 5K, A_V = 1, C_L = 1nF		1	mV
6	Slew Rate	SR	–55°C	±100V	R_L = 5K	20	100	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±100V	R_L = 5K, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 150mA	V_O	125°C	±31V	R_L = 100Ω	15		V
5	Output Voltage, I_O = 29mA	V_O	125°C	±150V	R_L = 5K	145		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±90V	R_L = 1K	80		V
5	Stability/Noise	E_N	125°C	±100V	R_L = 5K, A_V = 1, C_L = 1nF		1	mV
5	Slew Rate	SR	125°C	±100V	R_L = 5K	20	100	V/µs
5	Open Loop Gain	A_{OL}	125°C	±100V	R_L = 5K, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- EXTENDED SUPPLY RANGE
  - UP TO ±175V or
  - 350V TOTAL
- PROVIDES PA08 PERFORMANCE
  - UP TO ±150mA
  - PROGRAMMABLE CURRENT LIMIT
  - LOW DRIFT FET INPUT

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- PROGRAMMABLE POWER SUPPLIES UP TO 340V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PIEZO ELECTRIC TRANSDUCERS
- HIGH VOLTAGE INSTRUMENTATION

DESCRIPTION

The PA08V is an extended supply range operational amplifier capable of output voltage swings of ±170V with dual supplies or 340V total supply voltage on single or non-symmetric supplies.

High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased class A-B for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin to TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

SPECIFICATIONS

Specifications of the standard PA08 apply with the benefit of supply ratings being extended to ±175V. Design changes enabling the total supply rating of 350V have no effect on the shape of the typical performance graphs.

GENERAL CONSIDERATIONS

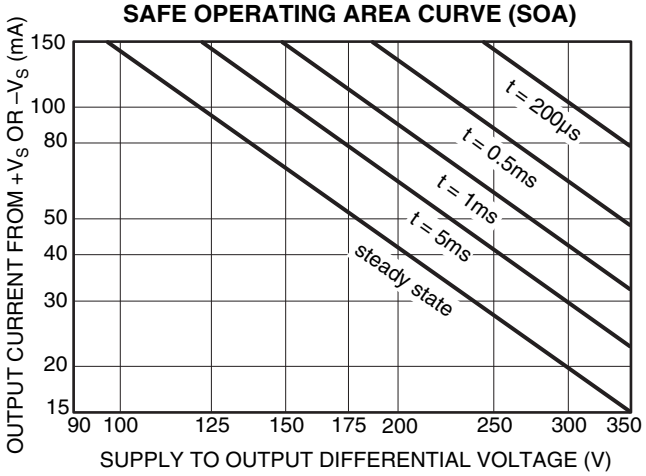
SAFE OPERATING AREA

The extended safe operating area is as follows:

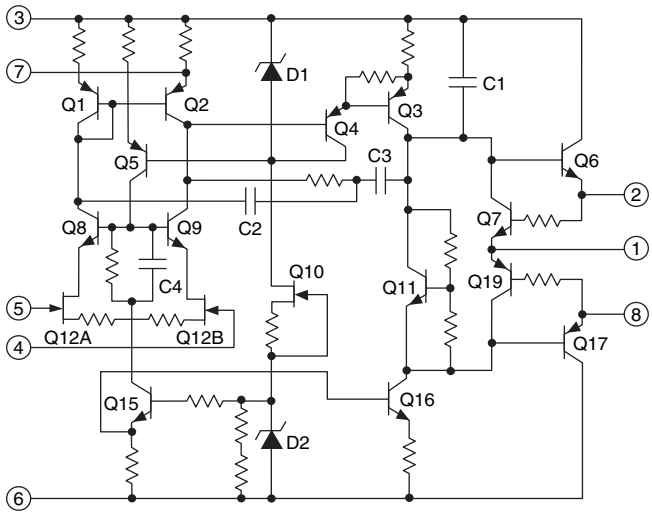
When operating on ±175V, maximum safe values of capacitive and inductive loading are .2µF and 200mH. Maximum safe current limit for a short to common is 50mA, and for a short to supply rails, the maximum is 15mA.

Please consult the PA08 data sheet for basic information on this amplifier, plus the application notes in this Apex Precision Power DATA BOOK, for recommendations on stability, current limiting, heatsinks, bypassing, and suggestions for circuit functions.

SAFE OPERATING AREA CURVE (SOA)



EQUIVALENT SCHEMATIC



PA09 • PA09A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- POWER MOS TECHNOLOGY — 2A peak rating
- HIGH GAIN BANDWIDTH PRODUCT — 150MHz
- VERY FAST SLEW RATE — 200V/µs
- PROTECTED OUTPUT STAGE — Thermal shutoff
- EXCELLENT LINEARITY — Class A/B output
- WIDE SUPPLY RANGE — ±12V to ±40V
- LOW BIAS CURRENT, LOW NOISE — FET input

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- VIDEO DISTRIBUTION AND AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS TO 2MHz
- COAXIAL LINE DRIVERS
- POWER LED OR LASER DIODE EXCITATION

DESCRIPTION

The PA09 is a high voltage, high output current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary Power MOS output stage. For optimum linearity, especially at low levels, the Power MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The CE, 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

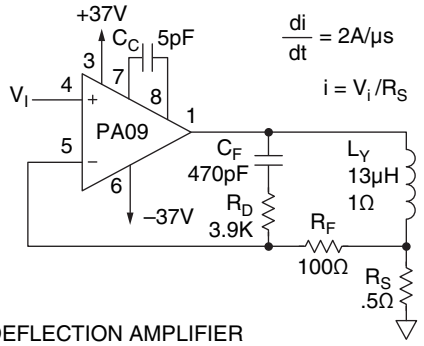
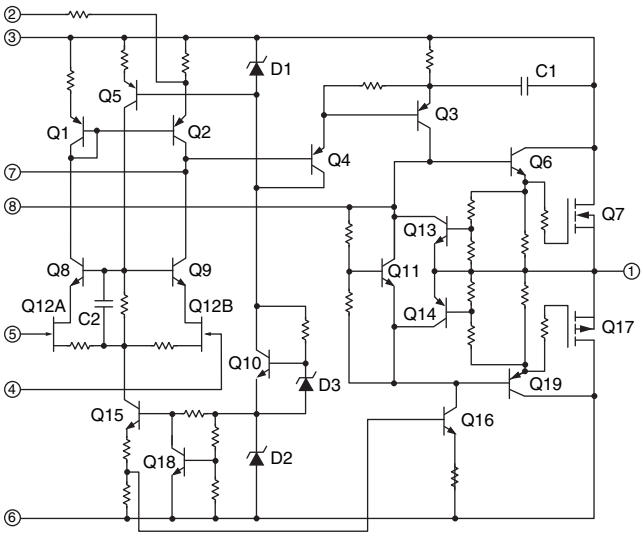


FIGURE 1. PA09 AS DEFLECTION AMPLIFIER

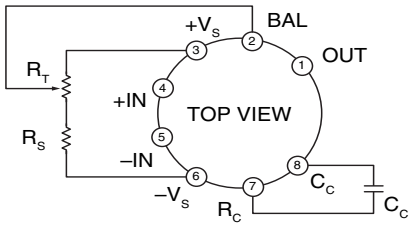
DEFLECTION AMPLIFIER (FIGURE 1)

The deflection amplifier circuit of Figure 1 achieves arbitrary beam positioning for a fast heads-up display. Maximum transition times are 4µs while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor (R_S) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of R_D, R_F and C_F serves to shift from a current feedback via R_S to a direct voltage feedback at high frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



$R_S = (|+V_S| + |-V_S|)\ R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

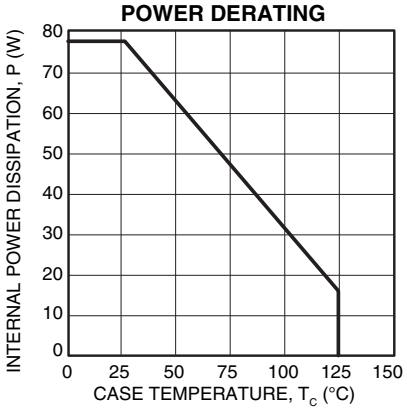
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA09 MIN	PA09 TYP	PA09 MAX	PA09A MIN	PA09A TYP	PA09A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	± 3		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			10			*		µV/V
BIAS CURRENT, initial			5	100		3	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			6			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–10	$\pm V_S$–8		*	*		V
COMMON MODE REJECTION, DC	Full temperature range, $V_{CM} = \pm 20V$		104			*		dB
GAIN								
OPEN LOOP GAIN at 15Hz	$R_L = 1k\Omega$	80	98			*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$C_C = 5pF$		150			*		MHz
POWER BANDWIDTH	$R_L = 15\Omega$, $C_C = 5pF$		750			*		KHz
POWER BANDWIDTH	$R_L = 15\Omega$, $C_C = 100pF$		150			*		KHz
OUTPUT								
VOLTAGE SWING[3]	Full temperature range, $I_O = 2A$	$\pm V_S$ –8	$\pm V_S$ –7		*	*		V
CURRENT, PEAK			4.5			*		A
SETTLING TIME to 1%	4V step, $C_C = 100pF$		.75			*		µs
SETTLING TIME to .1%	4V step, $C_C = 100pF$		1.3			*		µs
SLEW RATE	$C_C = 5pF$		220			*		V/µs
SLEW RATE	$C_C = 100pF$		25			*		V/µs
RESISTANCE			7.5			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	± 12	± 35	± 40	*	*	*	V
CURRENT, quiescent			70	85		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	Full temperature range, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temperature range, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+ 85	*	*	*	°C

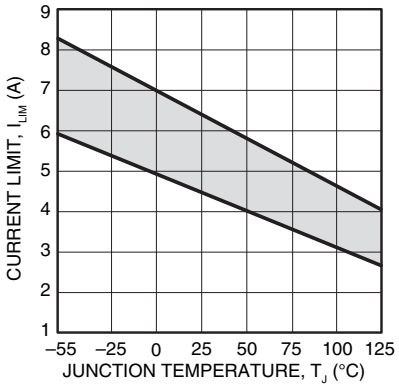
NOTES: * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. Unless otherwise noted: $T_C = 25°C$, supply voltage = ±35V.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

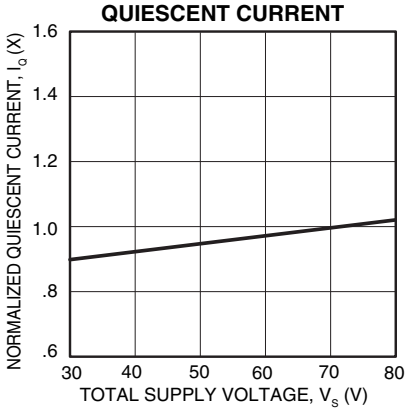
POWER DERATING



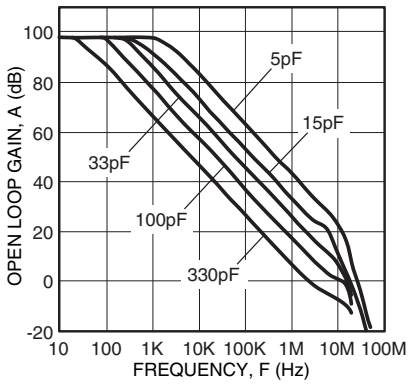
CURRENT LIMIT



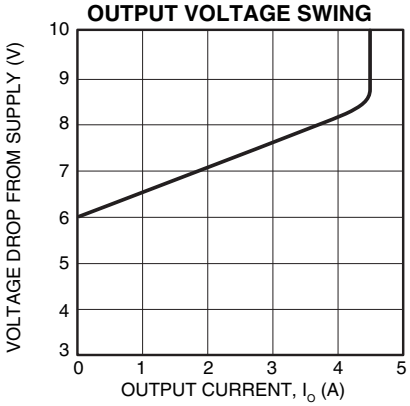
QUIESCENT CURRENT



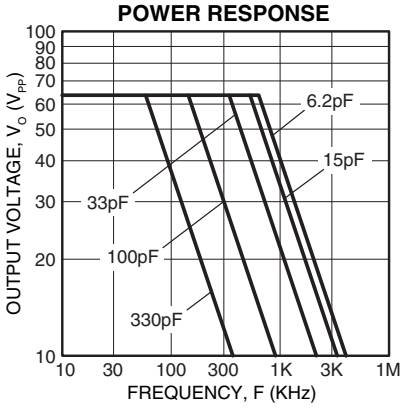
SMALL SIGNAL RESPONSE



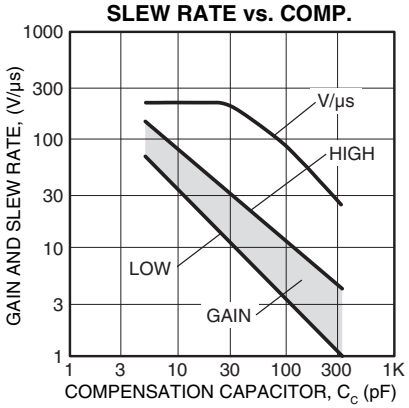
OUTPUT VOLTAGE SWING



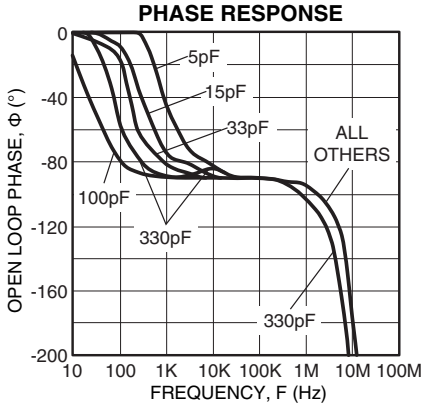
POWER RESPONSE



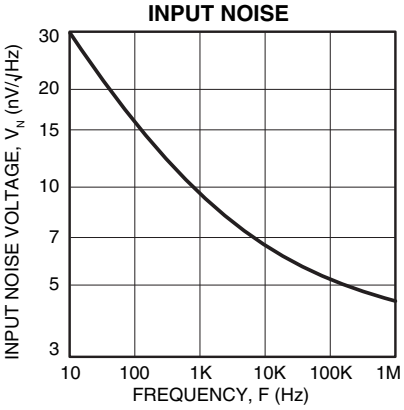
SLEW RATE vs. COMP.



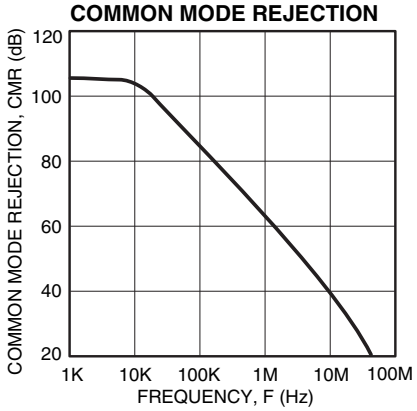
PHASE RESPONSE



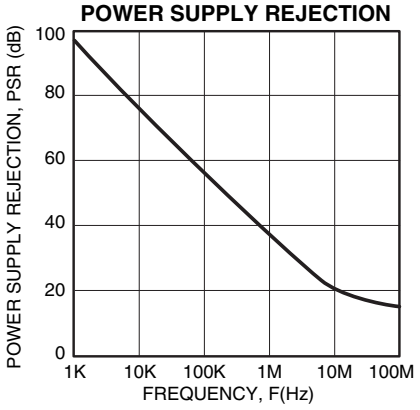
INPUT NOISE



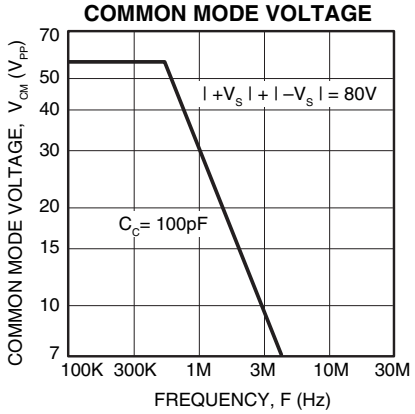
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

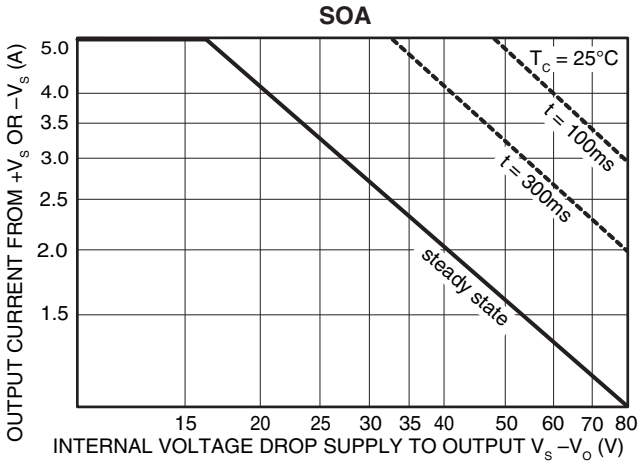
SUPPLY VOLTAGE

The specified voltage ($\pm V_S$) applies for a dual (±) supply having equal voltages. A nonsymmetrical (ie. +70/–10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



SAFE OPERATING AREA CURVES

The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

$\pm V_S$	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1µF	11mH
30V	500µF	24mH
20V	2500µF	75mH
15V	∞	100mH

2. Short circuits to ground are safe with dual supplies up to ±20V.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47µF in parallel with a .47µF ceramic capacitor directly connected from the power supply pins to the ground plane.

OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities. "Single point" is a key phrase here; a ground plane should be used as shielding rather than a current path. Leaving the case of the PA09 floating will cause oscillations in some applications.

COMPENSATION

The PA09 is extremely flexible in terms of choice of compensation capacitor for any given gain. The most common ranges are shown in the COMPENSATION typical performance graph. Swinging closer to the supply rails, heavier loads, faster input signal rise and fall times and higher supply voltages all tend to demand larger values of compensation capacitor. This capacitor must be rated at least as high as the total voltage applied to the amplifier. In making specific value choices, use the square wave stability test presented in APPLICATION NOTE 19, Figures 40 and 41.

In addition to small signal testing, if the application includes step functions in the input signal, use this circuit to measure large signal response. By increasing square wave amplitude to the maximum of the application, this test may show significant distortion of the output waveform following the square wave transitions. In this case the faster input stages of the PA09 are out-running the output stage and overload recovery time creates the distortion. This speed relationship is also why slew rate does not increase for compensation values below about 27pF.

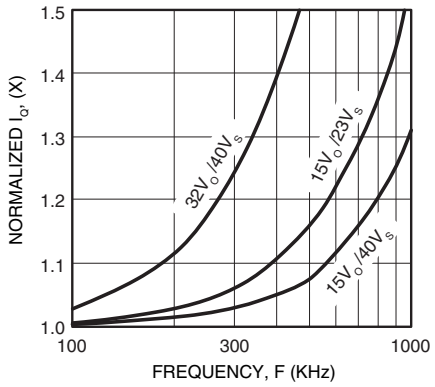
SUPPLY CURRENT

When swinging large signals, the output stage of the PA09 demands extra supply current. The following graphs illustrate this current for several conditions for both sine and square wave signals. Current is exclusive of any load current and will affect both supply rating and thermal ratings. When calculating internal power dissipation, multiply this current times total supply voltage.

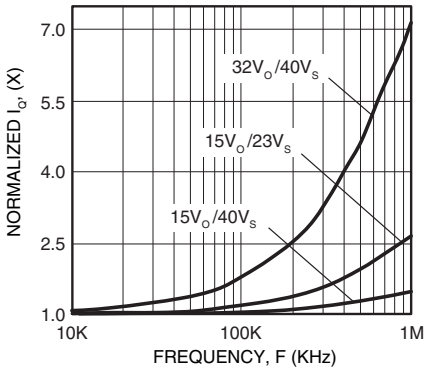
Note that swinging closer to the supply rail demands more

current. Output voltage is given as peak. Currents are average responding supply readings, but AC monitoring will reveal current pulses corresponding to periods of high slew rate. For

QUIESCENT vs. SINE DRIVE



QUIESCENT vs. SQUARE DRIVE



example, driving ±30V outputs at 500KHz on ±40V supplies produces a .8A pulse during negative slew and a 1.2A pulse during positive slew. If the input signal is over driven by several times the output swing capability, pulses up to 4A may be seen.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier, If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Pay very careful attention to supply bypassing and circuit grounding. This is very important when step functions are driven and the PA09 shares supplies with more active devices.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.

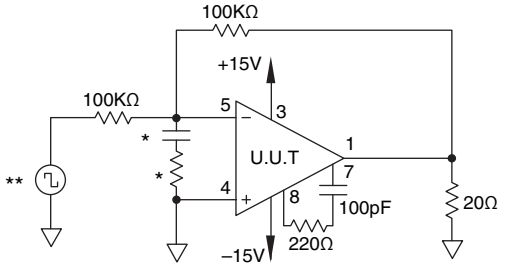
CURRENT LIMIT

Internal current limiting is provided in the PA09. Note the current limit curve given under typical performance graphs is based on junction temperature. If the amplifier is operated at cold junction temperatures, current limit could be as high as 8 amps. This is above the maximum allowed current on the SOA curve of 5 amps. Systems using this part must be designed to keep the maximum output current to less than 5 amps under all conditions. The internal current limit only provides this protection for junction temperatures of 80°C and above.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		85	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		5.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Inout Bias Current, –IN	$–I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		165	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		5.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input BiasCurrent, –IN	$–I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		140	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		6	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		8.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 3A	V_O	25°C	±21.3V	R_L = 3.75Ω	11.3		V
4	Output Voltage, I_O = 66mA	V_O	25°C	±40V	R_L = 500Ω	33		V
4	Output Voltage, I_O = 2A	V_O	25°C	± 38V	R_L = 15Ω	30		V
4	Current Limits	I_{CL}	25°C	±32.2V	R_L = 3.75Ω	3.4	6	A
4	Stability/Noise	E_N	25°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500Ω	25	500	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
6	Output Voltage, I_O = 3A	V_O	–55°C	±21.3V	R_L = 3.75Ω	11.3		V
6	Output Voltage, I_O = 66mA	V_O	–55°C	±40V	R_L = 500Ω	33		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±38V	R_L = 15Ω	30		V
6	Stability/Noise	E_N	–55°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500Ω	25	500	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
5	Output Voltage, I_O = 66mA	V_O	125°C	±40V	R_L = 500Ω	33		V
5	Output Voltage, I_O = 1A	V_O	125°C	±23.5V	R_L = 15Ω	15		V
5	Stability/Noise	E_N	125°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500Ω,	20	500	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA10 • PA10A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- GAIN BANDWIDTH PRODUCT — 4MHz
- TEMPERATURE RANGE — –55 to +125°C (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

APPLICATIONS

- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

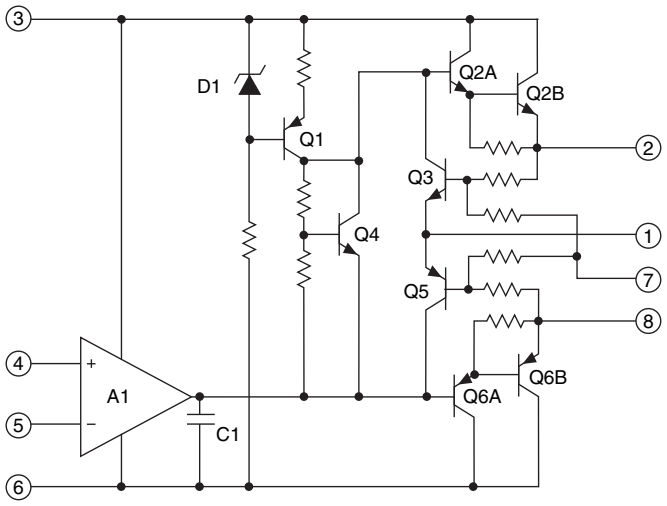
8-PIN TO-3
PACKAGE STYLE CE

DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

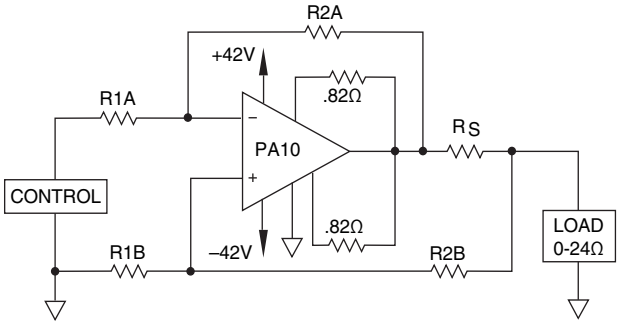
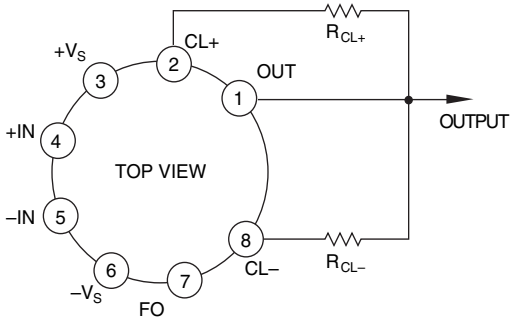


FIGURE 1. VOLTAGE-TO-CURRENT CONVERSION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

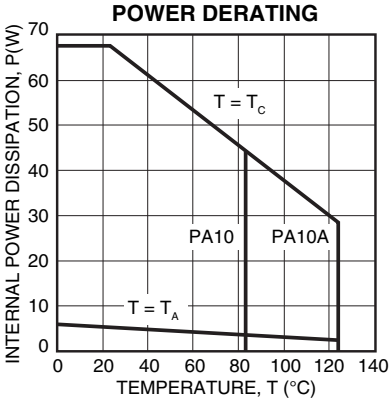
PARAMETER	TEST CONDITIONS[2,5]	PA10 MIN	PA10 TYP	PA10 MAX	PA10A MIN	PA10A TYP	PA10A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µVW
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 15Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		35			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–8	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2	3		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1			.68			*	nF
CAPACITIVE LOAD	Full temperature range, A_V = 2.5			10			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

NOTES: * The specification of PA10A is identical to the specification for PA10 in applicable column to the left.

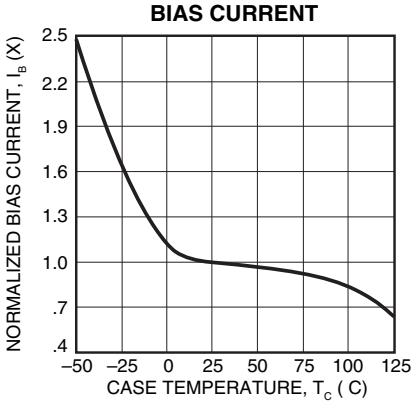
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

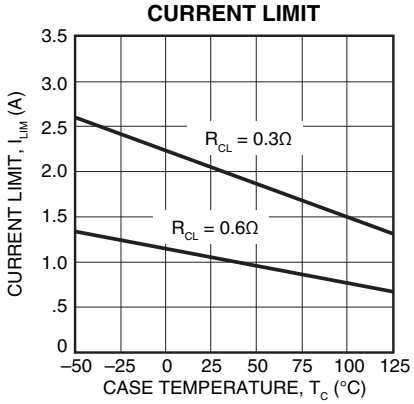
POWER DERATING



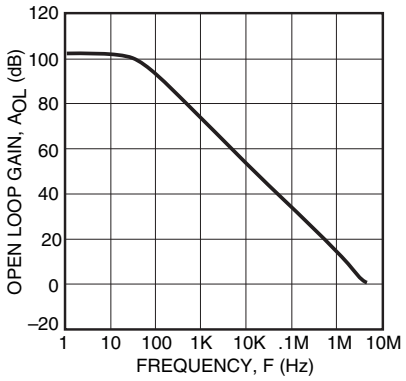
BIAS CURRENT



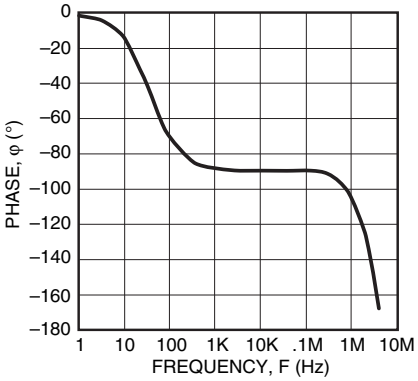
CURRENT LIMIT



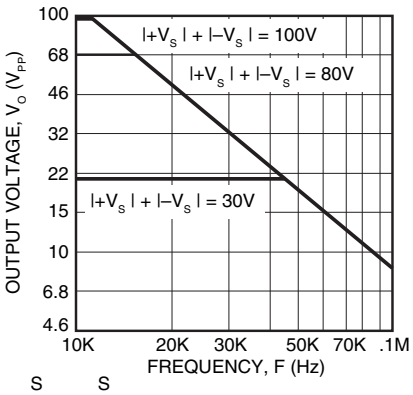
SMALL SIGNAL RESPONSE



PHASE RESPONSE

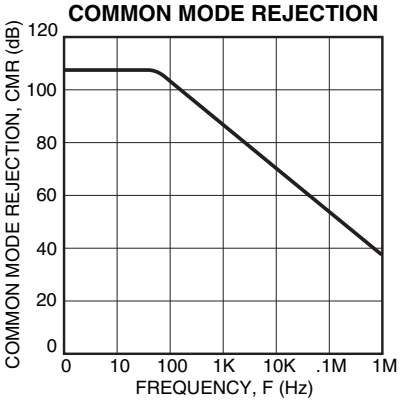


POWER RESPONSE

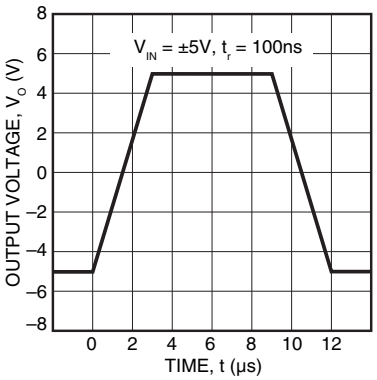


S S

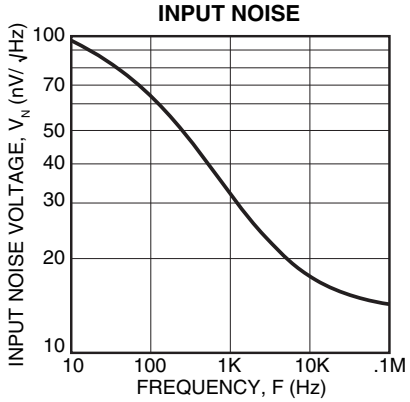
COMMON MODE REJECTION



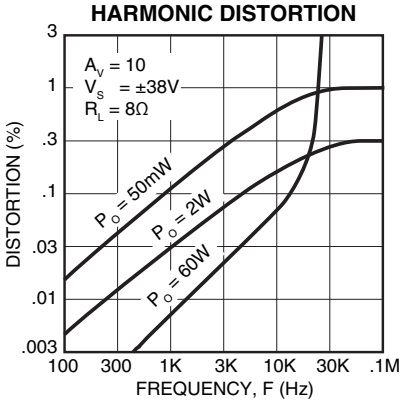
PULSE RESPONSE



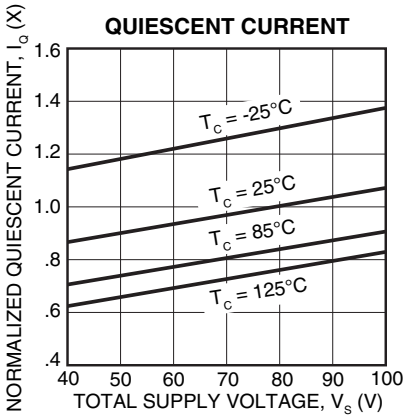
INPUT NOISE



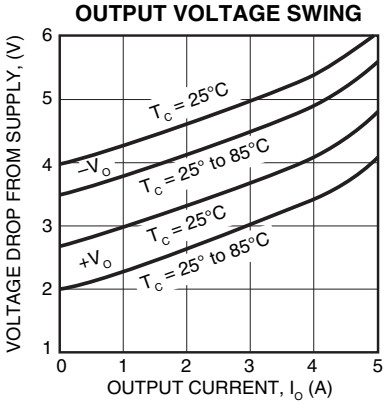
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



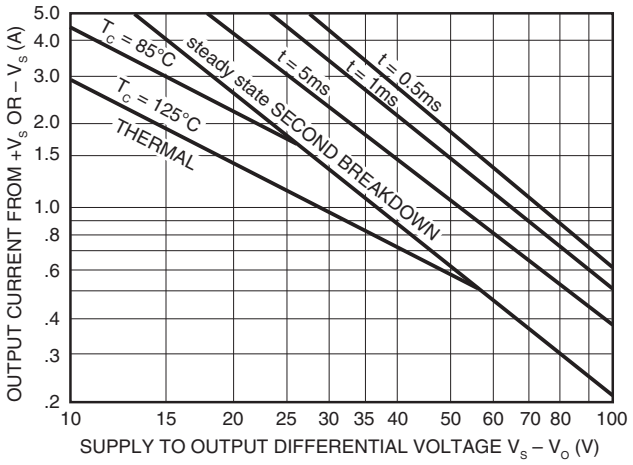
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



3. The junction temperature of the output transistors.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the new SOA graph.

   For sine wave outputs, use Power Design[1] to plot a load line. Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.

   [1] Note 1. Power Design is a self-extracting Excel spreadsheet available free from www.Cirrus.com

   For other waveform outputs, manual load line plotting is recommended. Applications Note 22, SOA AND LOAD LINES, will be helpful. A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.21A	.61A
40V	.3A	.87A
35V	.36A	1.0A
30V	.46A	1.4A
25V	.61A	1.7A
20V	.87A	2.2A
15V	1.4A	2.9A

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex Precision Power web site at www.Cirrus.com for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/L_{CL} \quad (1)$$

$$I_{CL} = 0.65/R_{CL} \quad (2)$$

Where:
I_{CL} is the current limit in amperes.
R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \quad (4)$$

Where:
Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

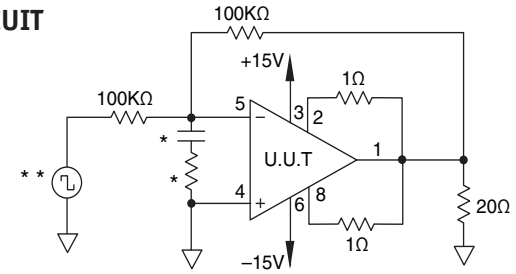
$$R_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

Where:
R_{FO} is in K ohms.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input bias current, –IN	$–I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		75	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input bias current, –IN	$–I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent current	I_Q	125°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input bias current, –IN	$–I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output voltage, I_O = 5A	V_O	25°C	±18V	R_L = 2.07Ω	10		V
4	Output voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current limits	I_{CL}	25°C	±17V	R_L = 12Ω, R_{CL} = 1Ω	.6	.89	A
4	Stability/noise	E_N	25°C	±40V	R_L = 100Ω, A_V = 1, C_L = .33nF		1	mV
4	Slew rate	SR	25°C	±40V	R_L = 500Ω	2	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output voltage, I_O = 5A	V_O	–55°C	±18V	R_L = 2.07Ω	10		V
6	Output voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Output voltage, I_O = 2A	V_O	–55°C	±30V	R_L = 12Ω	24		V
6	Stability/noise	E_N	–55°C	±40V	R_L = 100Ω, A_V = 1, C_L = .33nF		1	mV
6	Slew rate	SR	–55°C	±40V	R_L = 500Ω	2	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	R_L = 500Ω, F = 10Hz	96		db
6	Common mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output voltage, I_O = 3A	V_O	125°C	±14.3V	R_L = 2.07Ω	6.3		V
5	Output voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output voltage, I_O = 2A	V_O	125°C	±30V	R_L = 12Ω	24		V
5	Stability/noise	E_N	125°C	±40V	R_L = 100Ω, A_V = 1, C_L = .33nF		1	mV
5	Slew rate	SR	125°C	±40V	R_L = 500Ω	2	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA12 • PA12A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- LOW THERMAL RESISTANCE — 1.4°C/W
- CURRENT FOLDOVER PROTECTION — NEW
- HIGH TEMPERATURE VERSION — PA12H
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — Up to ±15A Peak

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

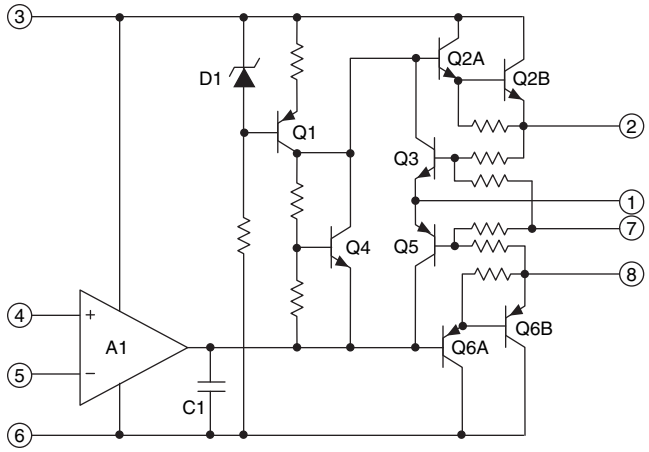
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

DESCRIPTION

The PA12 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. The PA12 is not recommended for gains below –3 (inverting) or +4 (non-inverting).

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



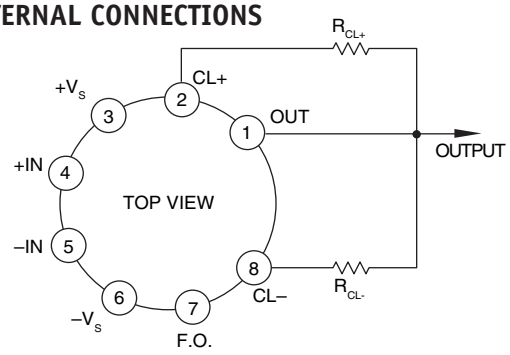
POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. Apex Precision Power rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 125W internal dissipation rating of the PA12 could be expressed as an output rating of 250W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

Apex Precision Power has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by Apex Precision Power in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

	PA12/PA12A
SUPPLY VOLTAGE, +Vs to –Vs	100V
OUTPUT CURRENT, within SOA	15A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

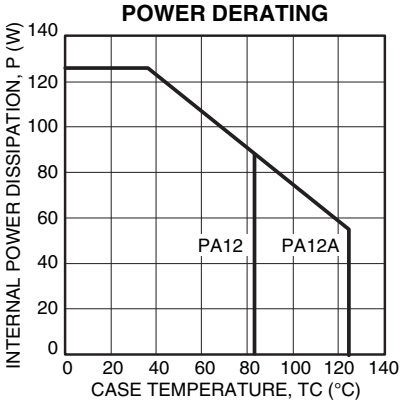
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 5]	PA12 MIN	PA12 TYP	PA12 MAX	PA12A MIN	PA12A TYP	PA12A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±12	±30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±20	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$ –5	$\pm V_S$ –3		*	*		V
COMMON MODE REJECTION, DC	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 8Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 8Ω load	13	20		*	*		kHz
PHASE MARGIN, A_V = +4	Full temp. range, 8Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, PA12 = 10A, PA12A = 15A	$\pm V_S$ –6			*			V
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$ –5			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	10			15			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2.5	4		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 4			1.5			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C		25	50		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		.8	.9		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		1.25	1.4		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		+85	–55		+125	°C

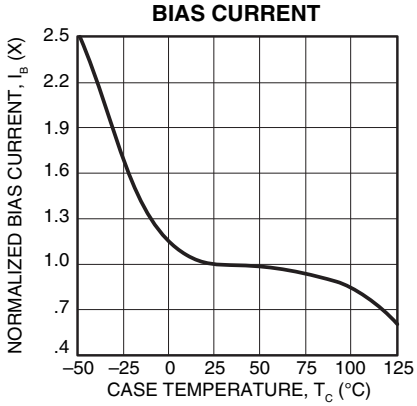
NOTES: * The specification of PA12A is identical to the specification for PA12 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $–V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $–V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not 100% tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

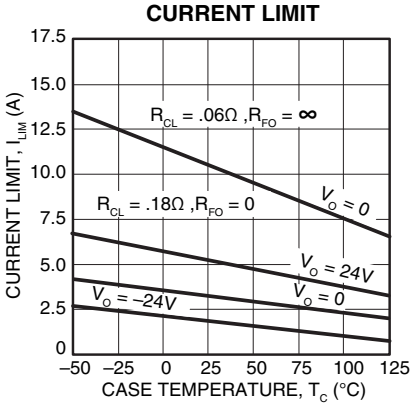
POWER DERATING



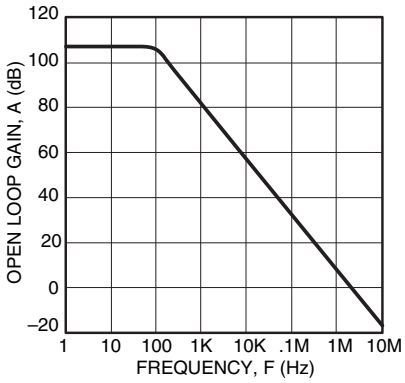
BIAS CURRENT



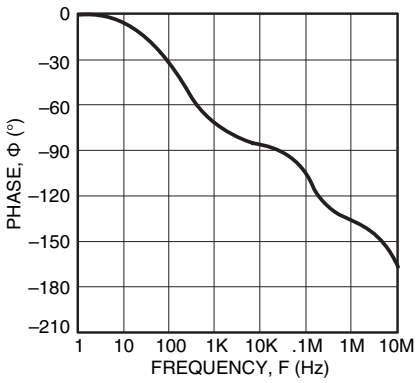
CURRENT LIMIT



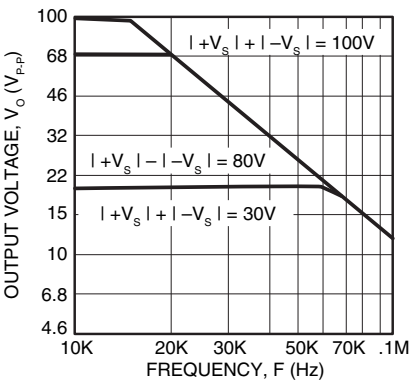
SMALL SIGNAL RESPONSE



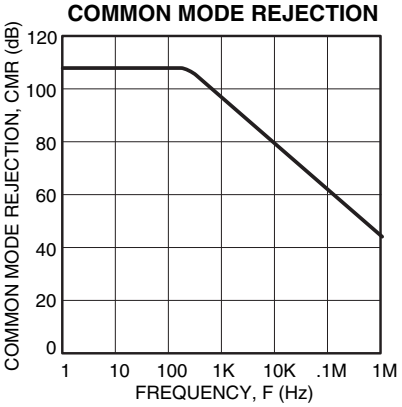
PHASE RESPONSE



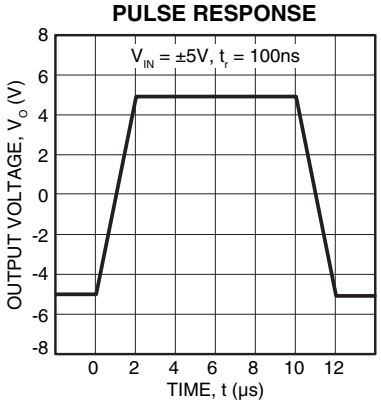
POWER RESPONSE



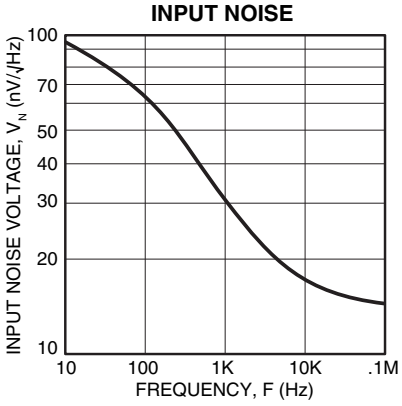
COMMON MODE REJECTION



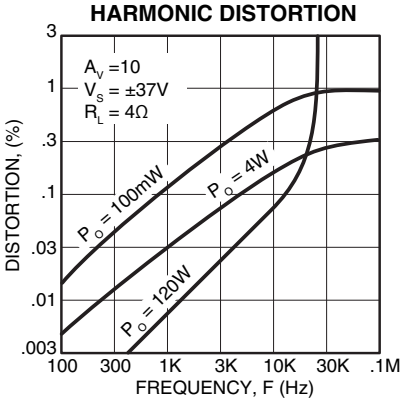
PULSE RESPONSE



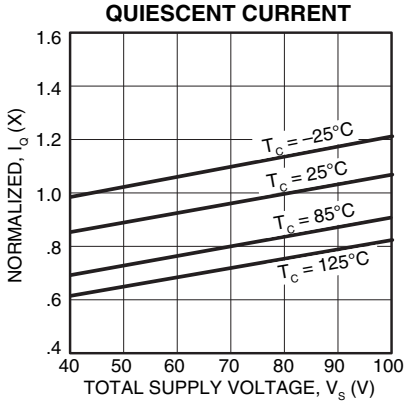
INPUT NOISE



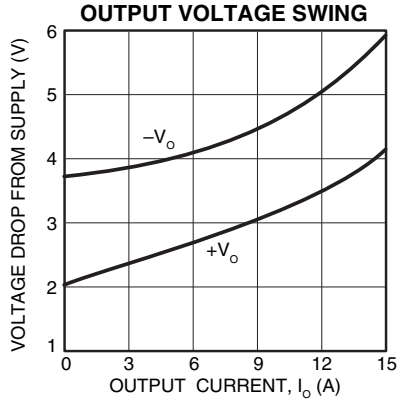
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



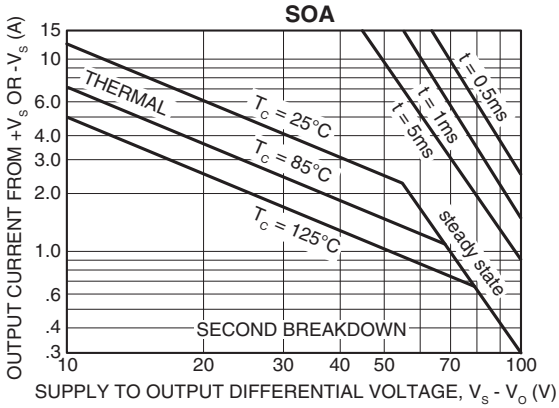
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
50V	200µF	125µF	5mH	2.0mH
40V	500µF	350µF	15mH	3.0mH
35V	2.0mF	850µF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 15A or 25V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 25°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.30A	2.4A
40V	.58A	2.9A
35V	.87A	3.7A
30V	1.5A	4.1A
25V	2.4A	4.9A
20V	2.9A	6.3A
15V	4.2A	8.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex Precision Power web site at www.Cirrus.com for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/I_{CL} \quad (1)$$

$$I_{CL} = 0.65/R_{CL} \quad (2)$$

Where:

I_{CL} is the current limit in amperes.

R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \quad (4)$$

Where:

Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

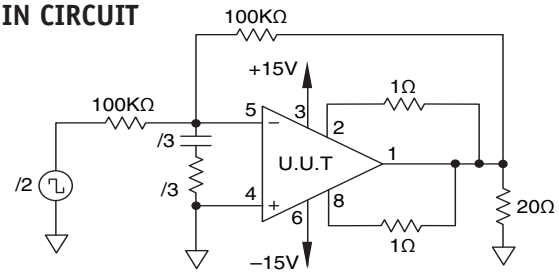
Where:

R_{FO} is in K ohms.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		50	mA
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Inout bias current,–IN	$–I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		100	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input bias current,–IN	$–I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent current	I_Q	125°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		50	mA
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input bias current, –IN	$–I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output voltage, I_O = 10A	V_O	25°C	±16V	R_L = 1Ω	10		V
4	Output voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output voltage, I_O = 5A	V_O	25°C	±35V	R_L = 6Ω	30		V
4	Current limits	I_{CL}	25°C	±14V	R_L = 6Ω, R_{CL} = 1Ω	.6	.89	A
4	Stability/noise	E_N	25°C	±40V	R_L = 500Ω, C_L = 1.5nF, /1		1	mV
4	Slew rate	SR	25°C	±40V	R_L = 500Ω	2.5	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output voltage, I_O = 8A	V_O	–55°C	±14V	R_L = 1Ω	8		V
6	Output voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Stability/noise	E_N	–55°C	±40V	R_L = 500Ω, C_L = 1.5nF, /1		1	mV
6	Slew rate	SR	–55°C	±40V	R_L = 500Ω	2.5	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
6	Common mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output voltage, I_O = 8A	V_O	125°C	±14V	R_L = 1Ω	8		V
5	Output voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Stability/noise	E_N	125°C	±40V	R_L = 500Ω, C_L = 1.5nF, /1		1	mV
5	Slew rate	SR	125°C	±40V	R_L = 500Ω	2.5	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



/1 Minimum gain recommendation is either G = +4 (non-inverting) or G = –3 (inverting).

/2 Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

/3 These components are used to stabilize device due to poor hgh frequency characteristics of burn in board.

PA12H

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- LOW COST 200°C VERSION OF PA12
- OUTPUT CURRENT at 200°C — ±1A
- FULL SPECIFICATIONS — –25°C to +125°C
- WIDE SUPPLY RANGE — ±10 to ±45V
- CURRENT FOLDOVER PROTECTION
- EXCELLENT LINEARITY — Class A/B Output

APPLICATIONS

- MOTOR, VALVE AND ACTUATOR CONTROL
- POWER TRANSDUCERS UP TO 100kHz
- PROGRAMMABLE POWER SUPPLIES UP TO 80V
- TRANSMISSION LINE DRIVER

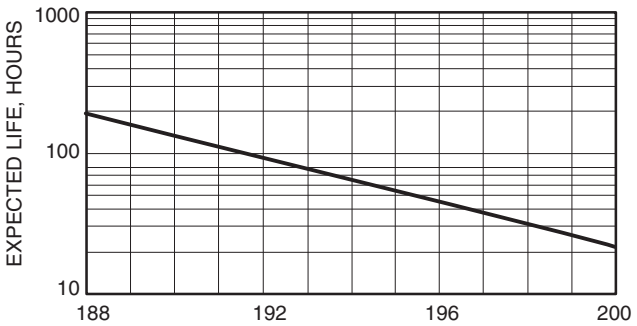
DESCRIPTION

The PA12H is a low cost, high temperature Power Op Amp made especially for short term use in extreme environmental situations such as down hole instrumentation. The amplifier can power mechanical or electronic transducers and can drive the long transmission lines associated with these applications.

The PA12H, based on the standard PA12's very high power level, leaves a six watt capability after being derated for operation at a case temperature of 200°C. To meet the high temperature requirements for up to 200 hours, polyimid has replaced the standard epoxy for attaching the small signal devices.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

CALCULATED LIFE EXPECTANCY



8-PIN TO-3
PACKAGE STYLE CE

SPECIFICATIONS

Specifications of the standard PA12 apply to the PA12H with the exception of the temperature range extensions

1. The operating and storage temperature ABSOLUTE MAXIMUM RATINGS extend to +200°C.
2. Static and dynamic tests are performed at +125°C as shown in SG 2 and SG 5 of the military PA12M data sheet.
3. Additional tests at T_C = 200°C:
   A. Quiescent current = 100mA max at $\pm V_S$ = 45.
   B. Voltage swing = $\pm V_S$ –4 (I_O = 1A, $\pm V_S$ = 15)

GENERAL CONSIDERATIONS

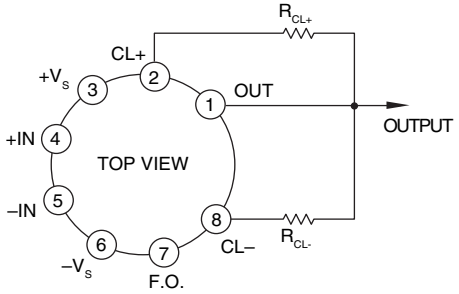
The primary aim of the PA12H is to provide a reasonable level of power output at a minimum cost. To achieve this end, full dynamic tests are performed up to 125°C, with only minimal 100% testing at 200°C. This approach saves nearly an order of magnitude over the cost of a fully tested long life product, but does require recognition of two limitations.

First, input parameters such as voltage offset and bias current are not tested above 125°C. This could lead to accuracy problems if the PA12H is used as a precision computational element. Solutions to this limitation include contacting the factory regarding additional testing at higher temperatures or using high temperature small signal amplifiers for computational tasks.

The second limitation of life span requires the PA12H to be used in short term applications. This requirement is mandated by the low cost design concept. At 200°C component degradation is nearly as severe during storage as during actual operation. This must be taken into account when scheduling actual implementation of the finished package.

Please consult the PA12 data sheet for basic information on this amplifier; the PA12M data sheet for details on +125°C tests, and Power Operational Amplifier handbook section "General Operating Considerations," for recommendations on supplies, stability, heatsinks and bypassing.

EXTERNAL CONNECTIONS



Power Operational Amplifier

FEATURES

- LOW THERMAL RESISTANCE — 1.1°C/W
- CURRENT FOLDOVER PROTECTION
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±45V
- HIGH OUTPUT CURRENT — Up to ±15A Peak

APPLICATIONS

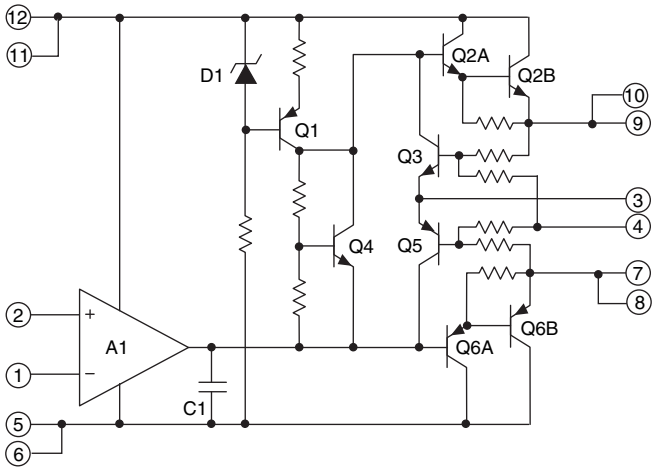
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

DESCRIPTION

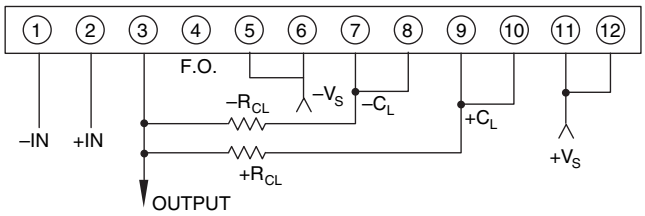
The PA13 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. The PA13 is not recommended for gains below –3 (inverting) or +4 (non-inverting).

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12-pin power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



12-pin SIP PACKAGE STYLE DP

Formed leads avaliable
See package style EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS – PA13/PA13A

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			100	V
OUTPUT CURRENT, within SOA			15	A
POWER DISSIPATION, internal			135	W
INPUT VOLTAGE, differential		-37	37	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 3)			175	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

Parameter	Test Conditions[2,5]	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE, initial			±2	±6		±1	±4	mV
OFFSET VOLTAGE vs. temp	Full temp range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE vs. supply			±30	±200		*	*	µV/V
OFFSET VOLTAGE vs. power			±20			*		µV/W
BIAS CURRENT, initial			±12	±30		±10	±20	nA
BIAS CURRENT, vs. temp	Full temp range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply			±10			*		pA/V
OFFSET CURRENT, initial			±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temp	Full temp range		±50			*		pA/°C
INPUT IMPEDANCE, DC			200			*		MΩ
INPUT CAPACITANCE			3			*		pF
COMMON MODE VOLTAGE RANGE (Note 4)	Full temp range	$\pm V_S$ - 5	$\pm V_S$ - 3		*	*		V
COMMON MODE REJECTION, DC	Full temp range, $V_{CM} = \pm V_S - 6V$	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN @ 10Hz	1KΩ load		110			*		dB
OPEN LOOP GAIN @ 10Hz	Full temp range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	8Ω load		4			*		MHz
POWER BANDWIDTH	8Ω load	13	20		*	*		kHz
PHASE MARGIN, A_V = +4	Full temp range, 8Ω load		20			*		°

Parameter	Test Conditions[2,5]	PA13			PA13A			Units
		Min	Typ	Max	Min	Typ	Max	
OUTPUT								
VOLTAGE SWING (Note 4)	PA13 = 10A, PA13A = 15A	$\pm V_S$ - 6			*			V
VOLTAGE SWING (Note 4)	I_O = 5A	$\pm V_S$ - 5			*			V
VOLTAGE SWING (Note 4)	Full temp range, I_O = 80mA	$\pm V_S$ - 5			*			V
CURRENT, peak		10			15			A
SETTLING TIME to 0.1%	2V step		2			*		µS
SLEW RATE		2.5	4		*	*		V/µS
CAPACITIVE LOAD	Full temp range, A_V = 4			1.5			*	nF
CAPACITIVE LOAD	Full temp range, A_V > 10			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temp range	±10	±40	±45	*	*	*	V
CURRENT, quiescent			25	50		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case (Note 5)	T_C = –55 to +125°C, F > 60Hz		0.6	0.7		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		0.9	1.1		*	*	°C/W
RESISTANCE, DC, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25		+85	*		*	°C

NOTES:
1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
* The specification of PA13A is identical to the specification for PA13 in the applicable column to the left
3. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Full temperature range specifications are guaranteed but not 100% tested.

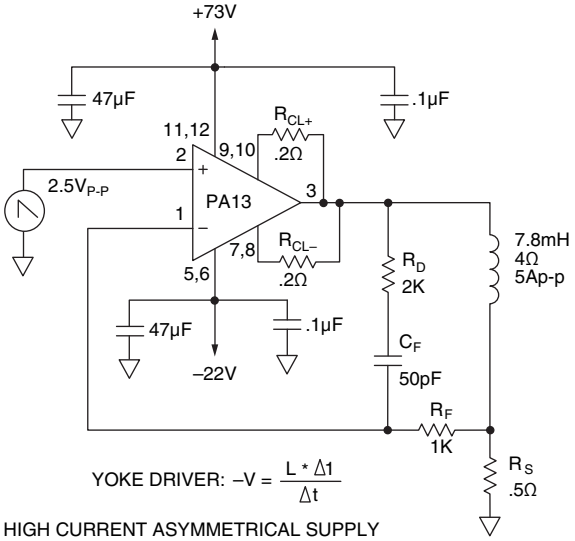
POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. Apex Precision Power rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 135W internal dissipation rating of the PA13 could be expressed as an output rating of 260W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

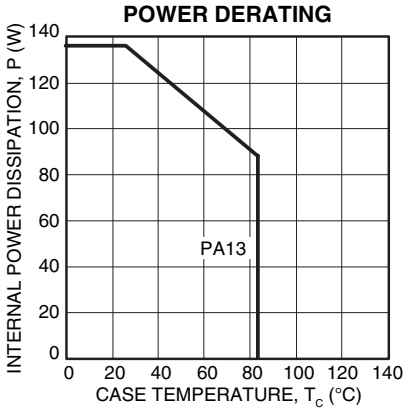
Apex Precision Power has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by Apex Precision Power in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

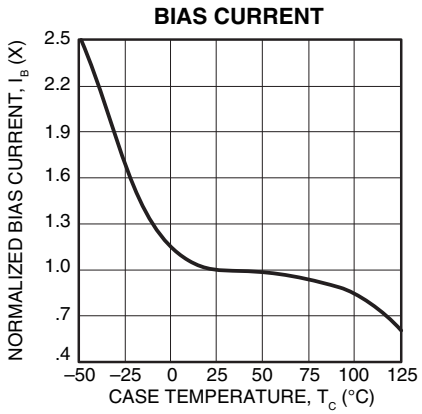
TYPICAL APPLICATION

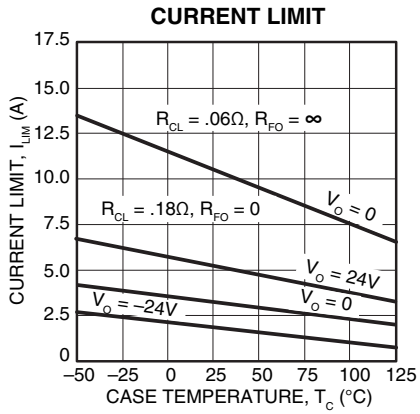


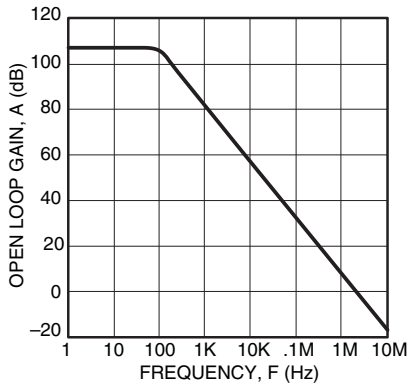
HIGH CURRENT ASYMMETRICAL SUPPLY

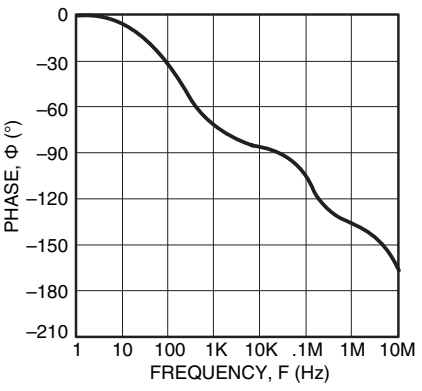
TYPICAL PERFORMANCE GRAPHS

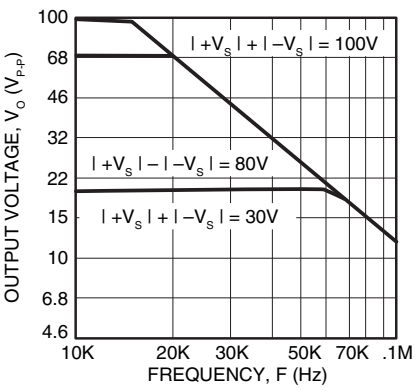




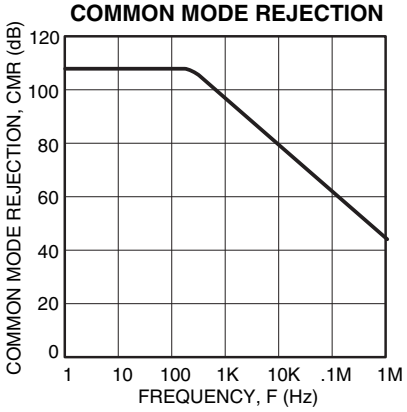




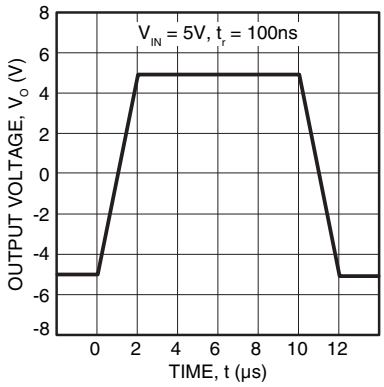




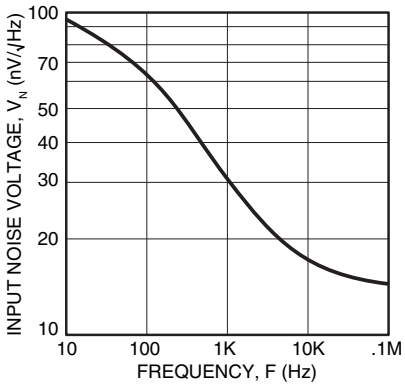
COMMON MODE REJECTION



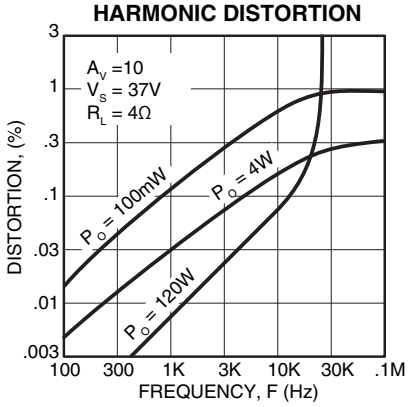
PULSE RESPONSE



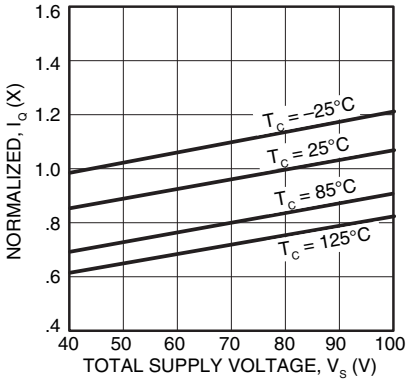
INPUT NOISE



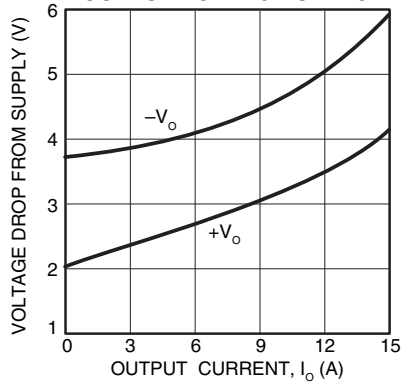
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

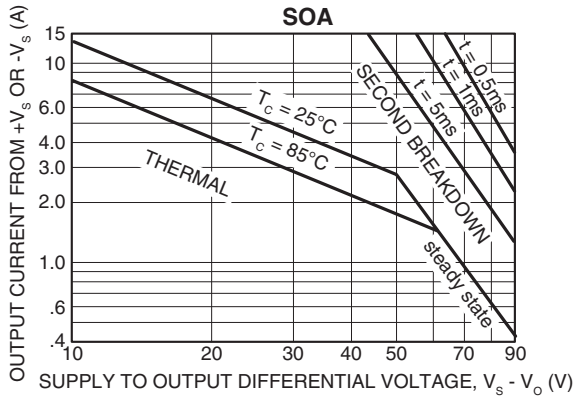
SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

SOA



1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
50V	200µF	125µF	5mH	2.0mH
40V	500µF	350µF	15mH	3.0mH
35V	2.0mF	850µF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12.5V below the supply rail with ILIM = 10A or 27V below the supply rail with ILIM = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at TC = 25°C:

	SHORT TO $\pm V_S$	SHORT TO
$\pm V_S$	C, L, OR EMF LOAD	COMMON
45V	.43A	3.0A
40V	.65A	3.4A
35V	1.0A	3.9A
30V	1.7A	4.5A
25V	2.7A	5.4A
20V	3.4A	6.7A
15V	4.5A	9.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex Precision Power web site at www.cirrus.com for a copy of Power_design.exe which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a ±20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 4 open and use equations 1 and 2.

$$R_{CL} = \frac{0.65}{I_{CL}} \qquad (1)$$

$$I_{CL} = \frac{0.65}{R_{CL}} \qquad (2)$$

Where:

I_{CL} is the current limit in amperes.
R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 4 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (V_O * 0.014)}{R_{CL}} \qquad (3)$$

$$R_{CL} = \frac{0.65 + (V_O * 0.014)}{I_{CL}} \qquad (4)$$

Where:
V_O is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.
In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 4 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{V_O * 0.14}{10.14 + R_{FO}}}{R_{CL}} \qquad (5)$$

$$R_{CL} = \frac{0.65 + \frac{V_O * 0.14}{10.14 + R_{FO}}}{I_{CL}} \qquad (6)$$

Where:
R_{FO} is in K ohms.

E

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

PA15FL • PA15FLA

High Voltage Power Operational Amplifiers

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- LOW COST
- LOW QUIESCENT CURRENT — 3.0mA MAX
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT

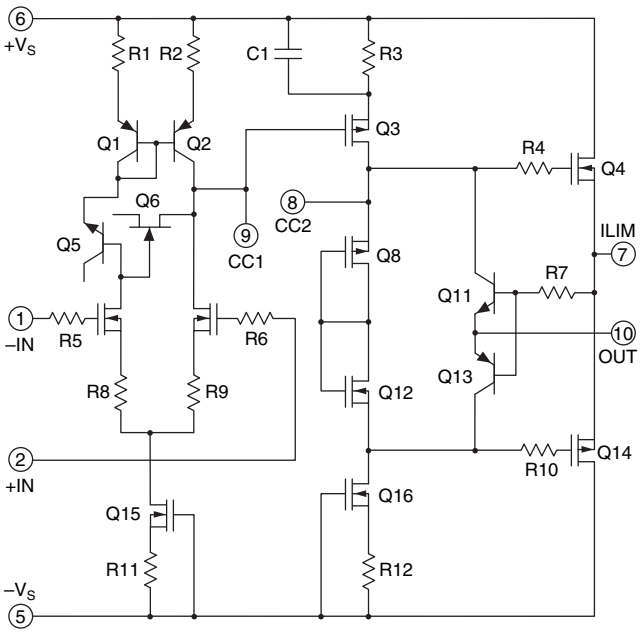
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V

DESCRIPTION

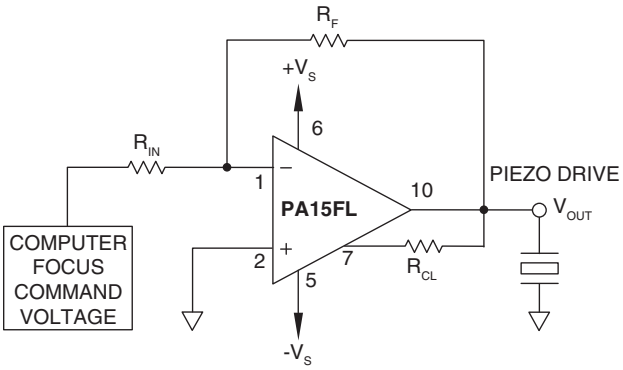
The PA15FL is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET input stage has integrated static and differential mode protection. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. The 10-pin power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



10-PIN SIP
PACKAGE STYLE FL
Formed leads available
See package style FU

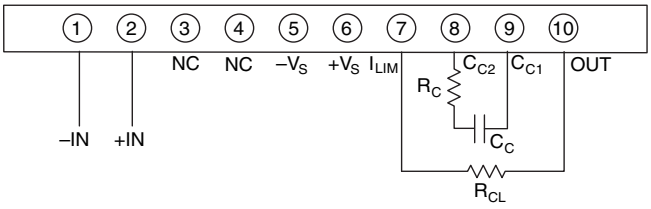
TYPICAL APPLICATION



LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA15FL reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
≥ 1	33pf	1KΩ
≥ 10	OPEN	OPEN

$$R_{CL} \cong \frac{.6}{I_{CL}}$$

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ T_C = 25°C	30W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	260°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE RANGE, storage	–40 to +85°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA15FL MIN	PA15FL TYP	PA15FL MAX	PA15FLA MIN	PA15FLA TYP	PA15FLA MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			2	10		.5	3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50		5	20	µV/°C
OFFSET VOLTAGE, vs. supply			10	50		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial			200	2000		*	*	pA
BIAS CURRENT, vs. supply			4			*		pA/V
OFFSET CURRENT, initial			50	500		30	200	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[3]		$\pm V_S$–15			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		*	*		dB
NOISE	10KHz BW, R_S = 1KΩ, C_C = OPEN		2			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	94	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = OPEN		5.8			*		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = OPEN		24			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[3]	I_O = ±200mA	$\pm V_S$–15	$\pm V_S$–10		*	*		V
CURRENT, continuous		±200			*			mA
SLEW RATE, A_V = 100	C_C = OPEN		20		20	30		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	100			*			pf
SETTLING TIME to .1%	C_C = OPEN, 2V step		2			*		µs
RESISTANCE, no load			50			*		Ω
POWER SUPPLY								
VOLTAGE[5]	See note 5	±50	±150	±225	*	*	*	V
CURRENT, quiescent,			2.0	3.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE , Case	Meets full range specifications	–25		+85	*		*	°C

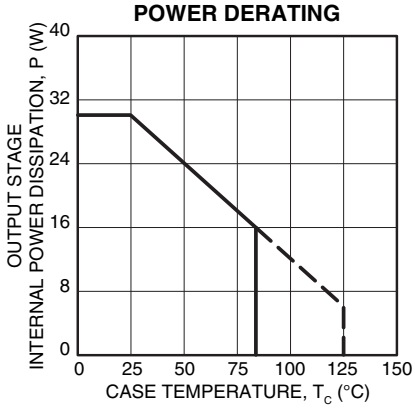
NOTES: * The specification of PA15FLA is identical to the specification for PA15FL in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 33pF, R_C = 1KΩ, R_{CL} = 0. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

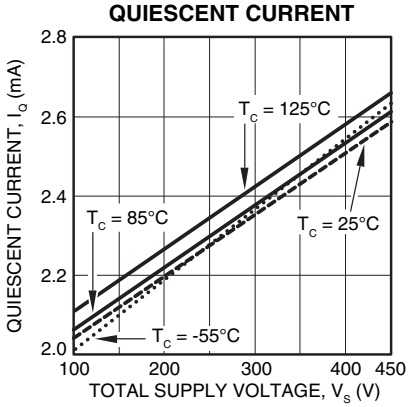
CAUTION The PA15FL is constructed from MOSFET transistors. ESD handling procedures must be observed.

The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

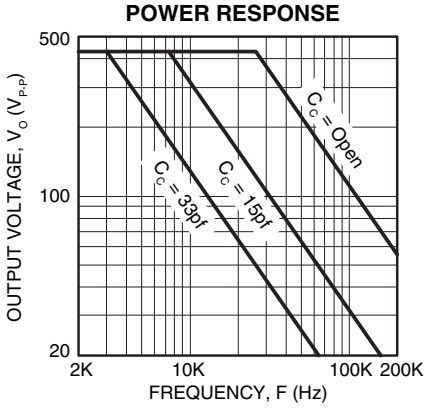
POWER DERATING



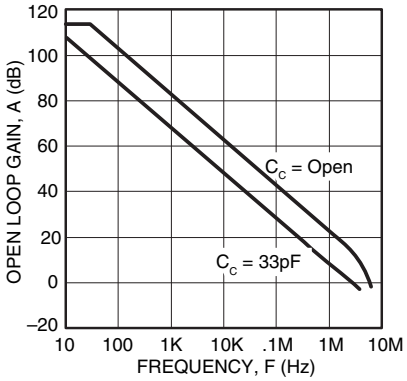
QUIESCENT CURRENT



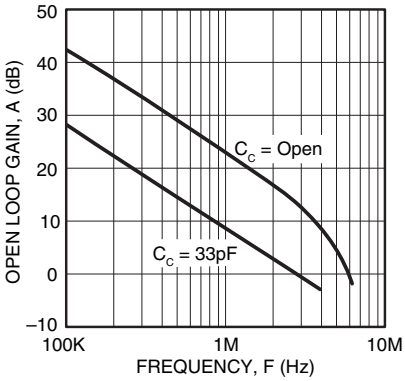
POWER RESPONSE



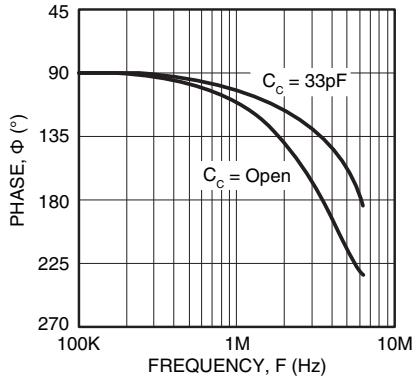
SMALL SIGNAL RESPONSE



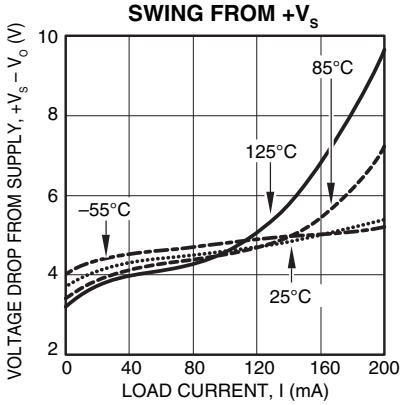
SMALL SIGNAL RESPONSE



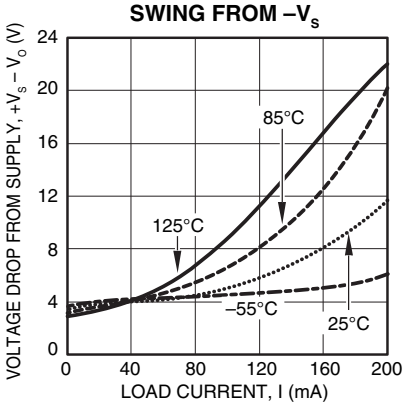
PHASE RESPONSE



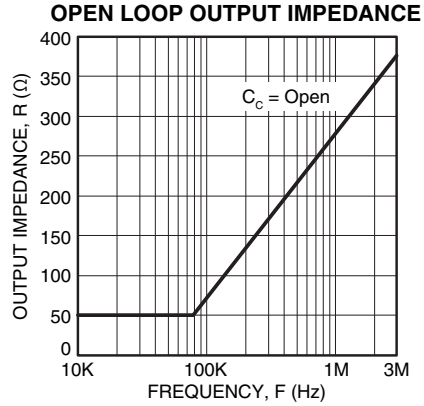
SWING FROM $+V_S$



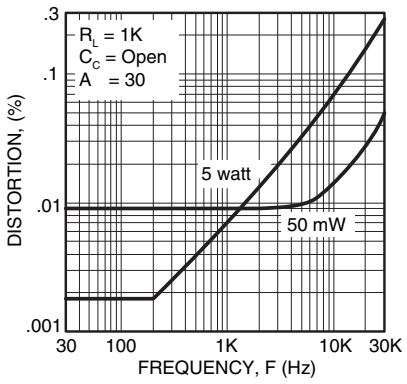
SWING FROM $-V_S$



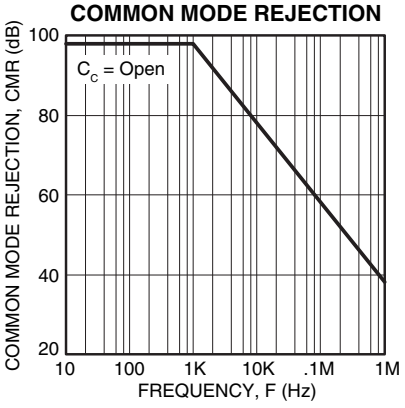
OPEN LOOP OUTPUT IMPEDANCE



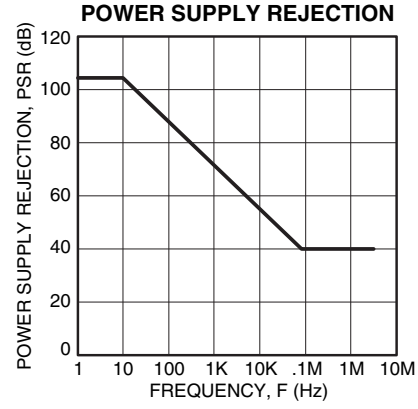
HARMONIC DISTORTION



COMMON MODE REJECTION



POWER SUPPLY REJECTION



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

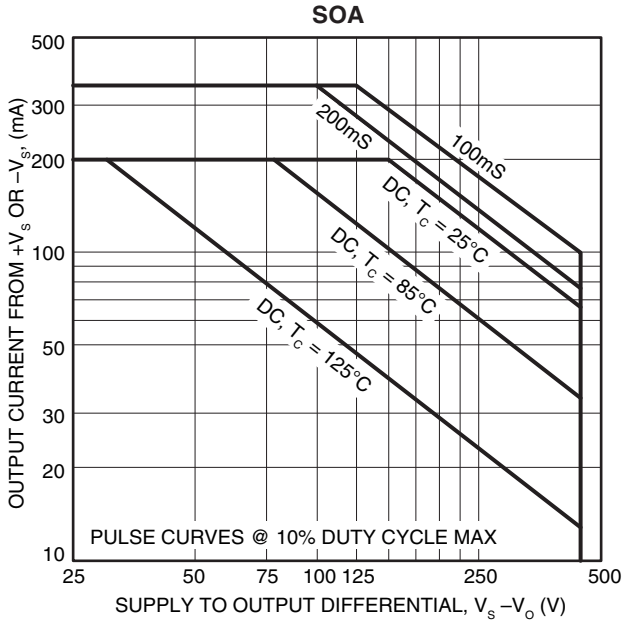
For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 2 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.6}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



INPUT PROTECTION

Although the PA15FL can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1-D4 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1-Q4 in Figure 2b). In either case the input differential voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

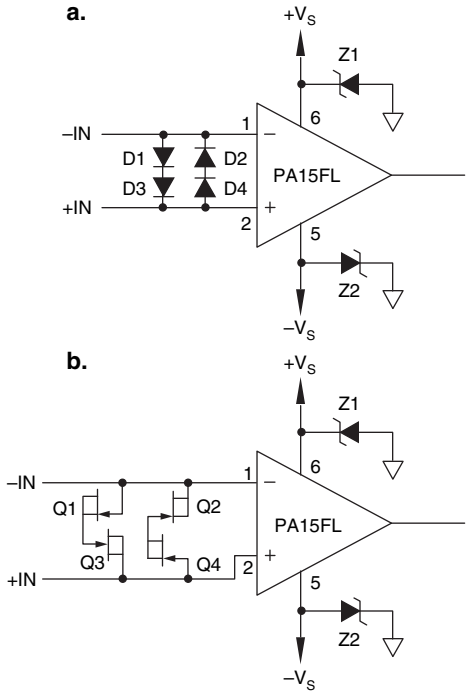
Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA15FL has sufficient phase margin to be stable with most capacitive loads at a gain of 10 or more, using the recommended phase compensation.

The PA15FL is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 8 and 9 to avoid spurious oscillation.

FIGURE 2. OVERVOLTAGE PROTECTION



Power Operational Amplifiers

FEATURES

- HIGH POWER BANDWIDTH — 350kHz
- HIGH SLEW RATE — 20V/µs
- FAST SETTLING TIME — 600ns
- LOW CROSSOVER DISTORTION — Class A/B
- LOW INTERNAL LOSSES — 1.2V at 2A
- HIGH OUTPUT CURRENT — ±5A PEAK
- LOW INPUT BIAS CURRENT — FET Input
- ISOLATED CASE — 300 VDC

APPLICATIONS

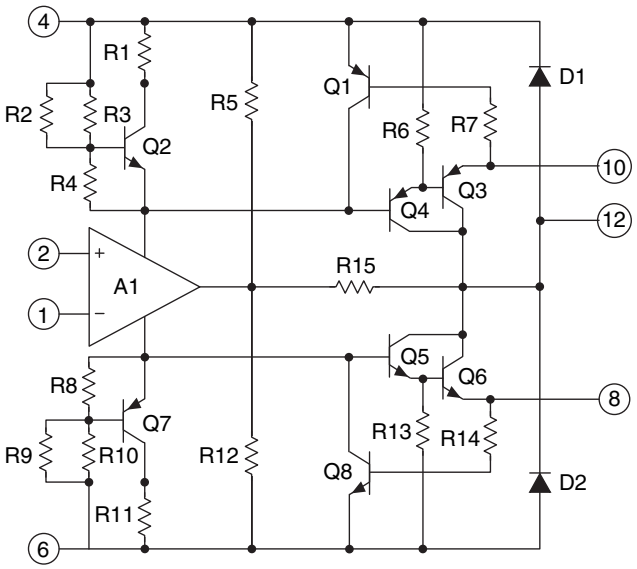
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 kHz
- AUDIO AMPLIFIERS UP TO 44W RMS

DESCRIPTION

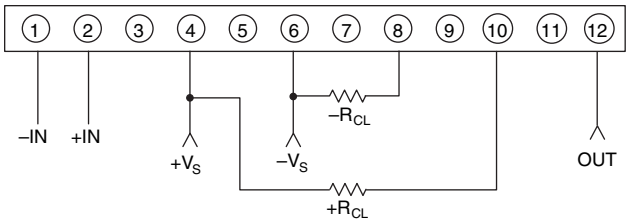
The PA16 and PA16A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting resistors (down to 10mA). Both amplifiers are internally compensated but are not recommended for use as unity gain followers. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The Power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



12-pin SIP PACKAGE STYLE DP
Formed leads available
See package style EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS – PA16/PA16A

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			38	V
OUTPUT CURRENT, within SOA			5	A
POWER DISSIPATION, internal (Note 2)			62.5	W
INPUT VOLTAGE, differential		-30	30	V
INPUT VOLTAGE, common mode		$-V_S + 2$	$+V_S - 2$	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

Parameter	Test Conditions[3,7]	PA16			PA16A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE, initial			±5	±10		±1	±3	mV
OFFSET VOLTAGE vs. temp	Full temp range		±10	±50		*	±25	µV/°C
OFFSET VOLTAGE vs. supply			±10			*		µV/V
OFFSET VOLTAGE vs. power			±6			*		µV/W
BIAS CURRENT, initial			50	200		25	100	pA
BIAS CURRENT, vs. temp				200			*	pA/°C
BIAS CURRENT, vs. supply			0.01			*		pA/V
OFFSET CURRENT, initial			25	100		15	50	pA
OFFSET CURRENT, vs. temp				100			*	pA/°C
INPUT IMPEDANCE, DC			1000			*		GΩ
INPUT CAPACITANCE			3			*		pF

Parameter	Test Conditions[3,7]	PA16			PA16A			Units
		Min	Typ	Max	Min	Typ	Max	
COMMON MODE VOLTAGE RANGE, Pos. (Note 6)	Full temp range	$+V_S$ - 6	$+V_S$ - 3		*	*		V
COMMON MODE VOLTAGE RANGE, Neg. (Note 6)	Full temp range	$-V_S$ + 6	$-V_S$ + 5		*	*		V
COMMON MODE REJECTION, DC	Full temp range	70	100		*	*		dB
GAIN								
OPEN LOOP GAIN @ 10Hz	1KΩ load		103			*		dB
OPEN LOOP GAIN @ 10Hz	Full temp range, 10KΩ load	86	100		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	10Ω load		4.5			*		MHz
POWER BANDWIDTH	10Ω load		350			*		kHz
PHASE MARGIN	Full temp range, 10Ω load		30			*		°
OUTPUT								
VOLTAGE SWING (Note 4)	I_O = 5A, R_{CL} = 0.08Ω	$\pm V_S$ - 4	$\pm V_S$ - 3		$\pm V_S$ - 3	*		V
VOLTAGE SWING (Note 4)	I_O = 2A	$\pm V_S$ - 2	$\pm V_S$ - 1.2		$\pm V_S$ - 1.2	*		V
CURRENT, peak		5			*			A
SETTLING TIME to 0.1%	2V step		0.6			*		µS
SLEW RATE		13	20		*	*		V/µS
CAPACITIVE LOAD	Full temp range, A_V > 10		SOA			*		
HARMONIC DISTORTION	P_O = 5W, F = 1kHz, R_L = 4Ω		0.028			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, A_V = 1		100			*		nS
SMALL SIGNAL overshoot	R_L = 10Ω, A_V = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temp range	±7	±15	±19	*	*	*	V
CURRENT, quiescent			27	40		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case (Note 5)	F > 60Hz		1.4	1.63		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.8	2.0		*	*	°C/W
RESISTANCE, DC, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25		+85	*		*	°C

NOTES:

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

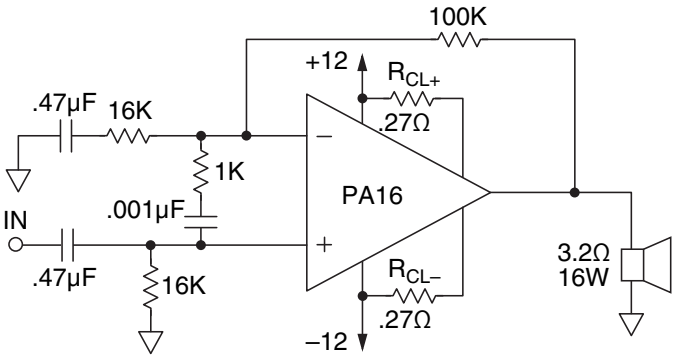
* The specification of PA16A is identical to the specification for PA16 in applicable column to the left.

3. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Exceeding CMV range can cause the output to latch.
7. Full temperature specifications are guaranteed but not 100% tested.
8. The absolute maximum negative input voltage is equal to the negative power supply voltage plus 1V ($-V_S$ + 1V).

TYPICAL APPLICATION

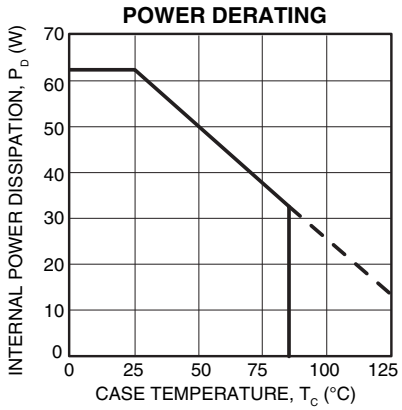
Vehicular Sound System Power Stage

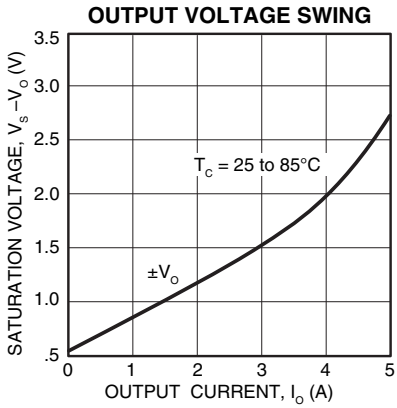
When system voltages are low and power is at a premium, the PA16 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA16, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network. The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

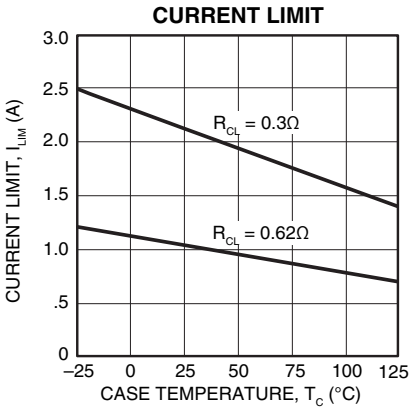


LOW INTERNAL LOSS MAXIMIZES EFFICIENCY

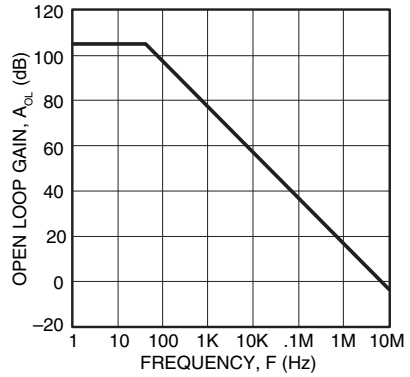
TYPICAL PERFORMANCE GRAPHS



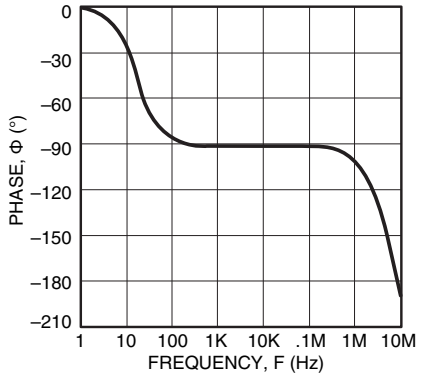




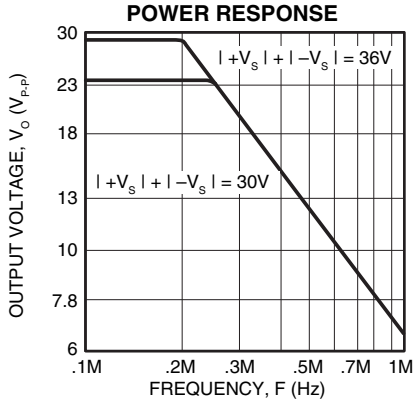
SMALL SIGNAL RESPONSE



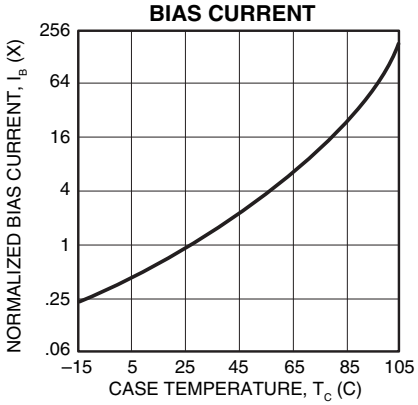
PHASE RESPONSE



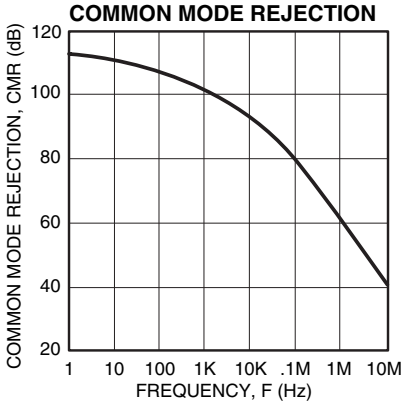
POWER RESPONSE



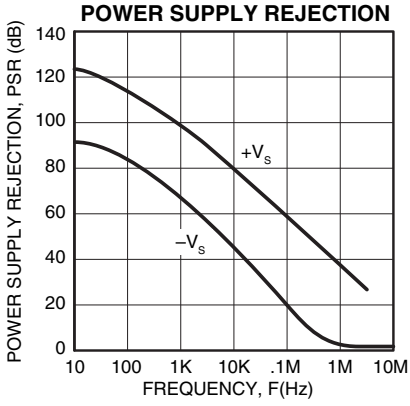
BIAS CURRENT



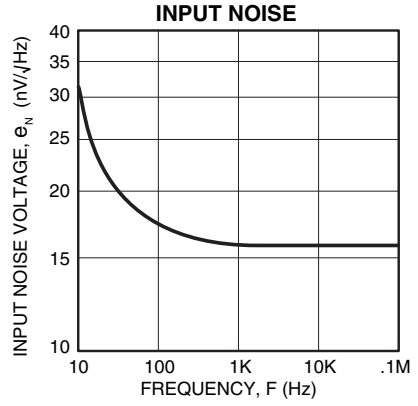
COMMON MODE REJECTION



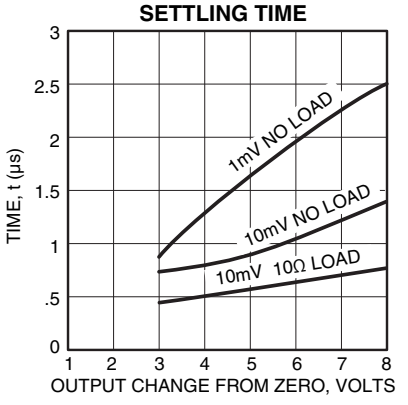
POWER SUPPLY REJECTION



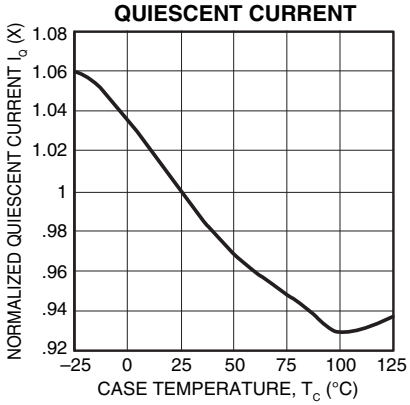
INPUT NOISE



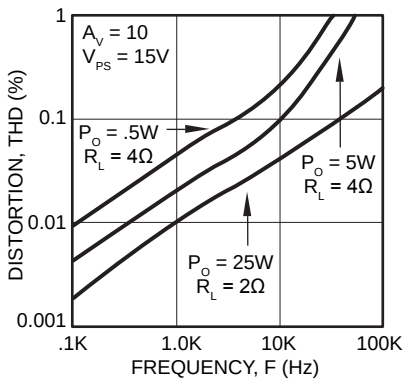
SETTLING TIME



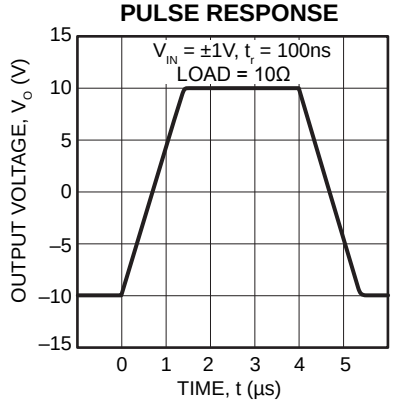
QUIESCENT CURRENT



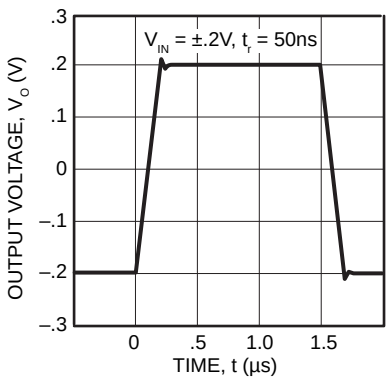
HARMONIC DISTORTION



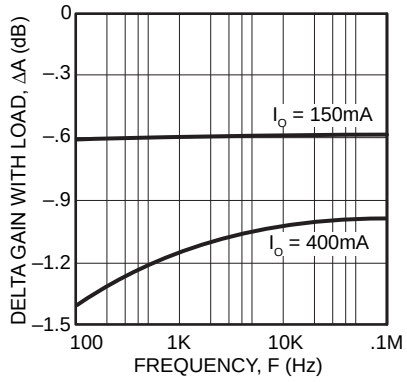
PULSE RESPONSE



PULSE RESPONSE



LOADING EFFECTS



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

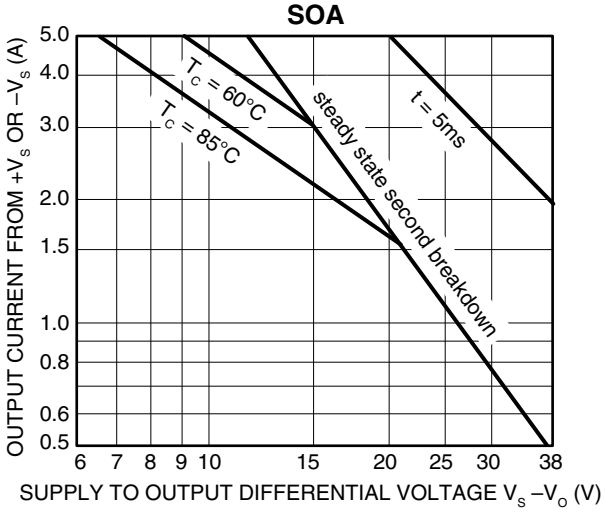
The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T_C = 85°C.

±V_S	SHORT TO ±V_S C, L OR EMF LOAD	SHORT TO COMMON
18V	.9A	1.8A
15V	1.0A	2.1A
10V	1.6A	3.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

SOA



CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

$$R_{CL} = \frac{0.65}{I_{LIM}\,(A)} - 0.01$$

DEVICE MOUNTING

The case (mounting flange) is electrically isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance. Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

PA50 • PA50A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- HIGH INTERNAL DISSIPATION — 400 Watts
- HIGH CURRENT — 40A Continuous, 100A PEAK
- HIGH SLEW RATE — 50V/µs
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

- SEMI-CONDUCTOR TESTING

DESCRIPTION

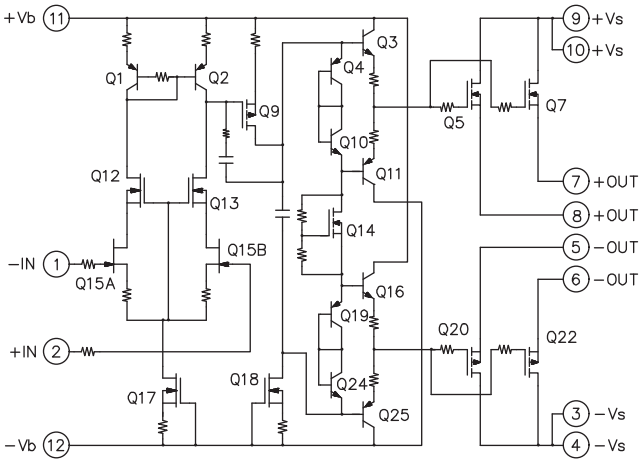
The PA50 is a MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation.

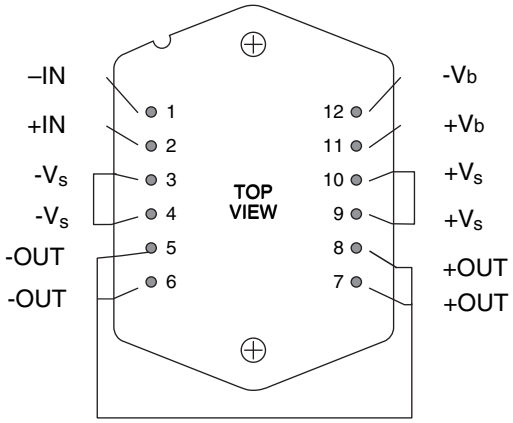
12-PIN DIP
PACKAGE STYLE CR

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE, $+V_b$ to $-V_b$	130V
OUTPUT CURRENT, within SOA	100A
POWER DISSIPATION, internal	400W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_b$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA50 MIN	PA50 TYP	PA50 MAX	PA50A MIN	PA50A TYP	PA50A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20	50		*	*	µV/°V
OFFSET VOLTAGE, vs. supply			10	30		*	*	µV/V
BIAS CURRENT, initial			10	50		*	*	pA
BIAS CURRENT vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		*	*	pA
INPUT IMPEDANCE, DC			10"			*		Ω
IMPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$-V_B$ +12 $+V_B$ -14			*			V
COMMON MODE REJECTION,DC	Full temp, range, V_{CM}= ±20V	90	100			*	*	dB
INPUT NOISE	100KHZ BW, Rs=1KΩ		10			*		µVrms
GAIN								
OPEN LOOP,@ 15Hz	Full temperature range	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L=10Ω		3			*		MHz
POWER BANDWIDTH	R_L=4Ω, V_o=80V_{P-P}, Av=-10 Full temperature range		200			*		kHz
OUTPUT								
VOLTAGE SWING	I_o=40A	$\pm V_S \mp 9.5$	$\pm V_S \mp 8.0$		*	*		V
VOLTAGE SWING, PA50	$\pm V_{BOOST}=\pm V_S \pm 10V$, I_o=40A	$\pm V_S \mp 5.8$	$\pm V_S \mp 4.0$					V
VOLTAGE SWING, PA50A	$\pm V_{BOOST}=\pm V_S \pm 10V$, I_o=50A				$\pm V_S \mp 5.8$	$\pm V_S \mp 5.0$		V
CURRENT, peak	3ms 10% Duty Cycle	100			*			A
SETTLING TIME TO.1%	A_V= -10,10V STEP,R_L=4Ω		1			*		µs
SLEW RATE	A_V=-10	50			*			V/µs
RESISTANCE	I_O=0, NO LOAD, 2MHZ		2.5			*		Ω
POWER SUPPLY								
VOLTAGE, $\pm V_{BOOST}$	Full temperature range	+14, -12	±15	±65	*	*	*	V
VOLTAGE, $\pm V_S$	Full temperature range	±3		±50	*		*	V
CURRENT,quiescent, boost supply			26	32		*	*	mA
CURRENT, quiescent, total			30	36		*	*	mA
THERMAL								
RESISTANCE,AC,junction to case[3]	Full temperature range, F>60HZ		.2	.25		*	*	°C/W
RESISTANCE,DC,junction to case	Full temperature range, F>60HZ		.25	.31		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25		85	*		*	°C

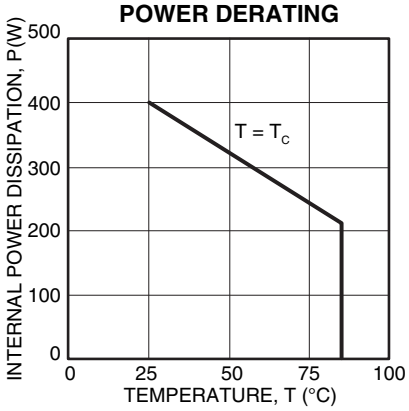
NOTES: * The specification of PA50A is identical to the specification for PA50 in applicable column to the left

1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

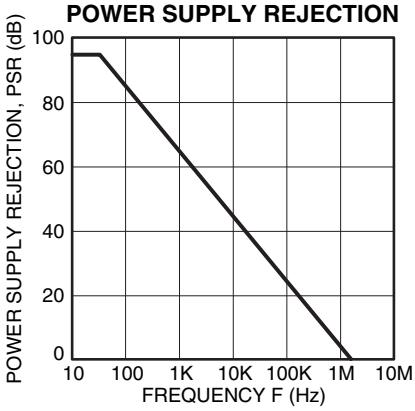
CAUTION The PA50 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

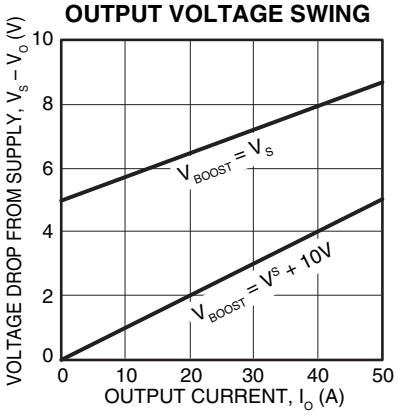
POWER DERATING



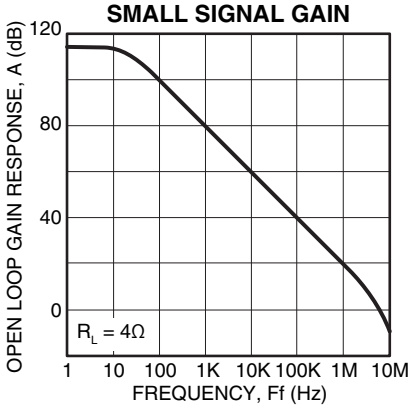
POWER SUPPLY REJECTION



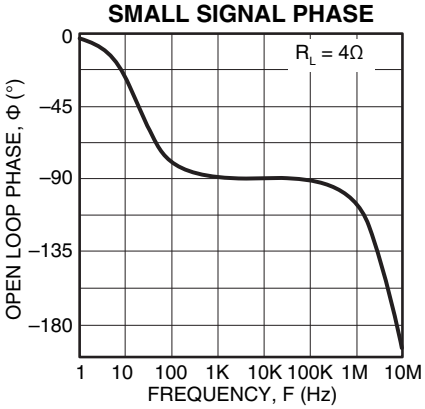
OUTPUT VOLTAGE SWING



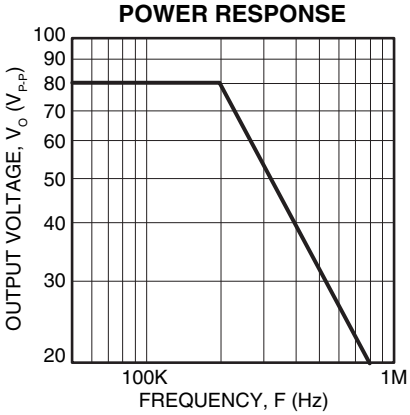
SMALL SIGNAL GAIN



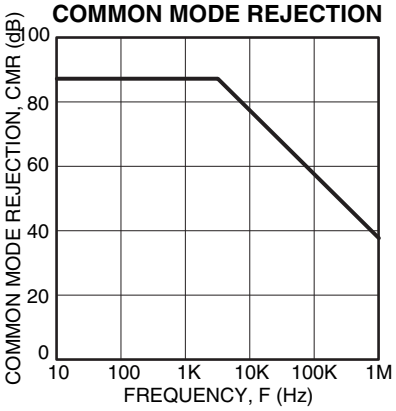
SMALL SIGNAL PHASE



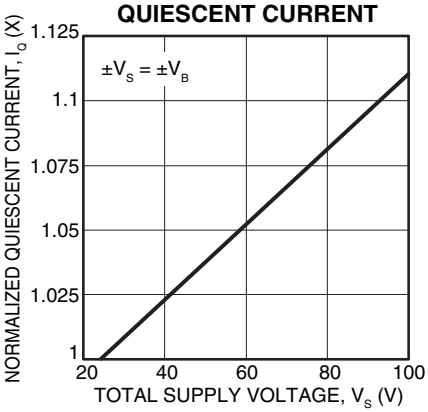
POWER RESPONSE



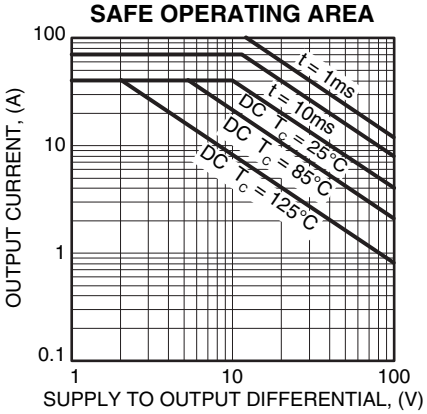
COMMON MODE REJECTION



QUIESCENT CURRENT



SAFE OPERATING AREA



GENERAL

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CURRENT LIMIT

There is no internal circuit provision for current limit in the PA50. However, the PA50 circuit board in the PA50 evaluation kit does provide a means whereby the output current can be sensed. An external circuit current limit can thereby be implemented if needed.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 11) and $-V_{BOOST}$ (pin 12) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 9,10) and $-V_S$ (pin 3,4) are connected to the high current output stage. An additional 10V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

Compensation is internally fixed for a gain of 3 or more and is not adjustable by the user. The PA50 therefore is not unity gain stable.

POWER SUPPLY BYPASSING

Proper and sufficient power supply bypassing is crucial to proper operation of the PA50. Bypass the +Vb and -Vb supply pins with a minimum .1µF ceramic capacitors directly at the supply pins. On the +Vs and -Vs pins use a combination of ceramic and electrolytic capacitors. Use 1µF ceramic capacitors and an electrolytic capacitor at least 10µF for each amp of output current required.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

PA51 • PA51A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±10 to ±40V
- HIGH OUTPUT CURRENT — ±10A Peak
- CLASS "C" OUTPUT — Low Cost
- LOW QUIESCENT CURRENT — 2.6mA

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

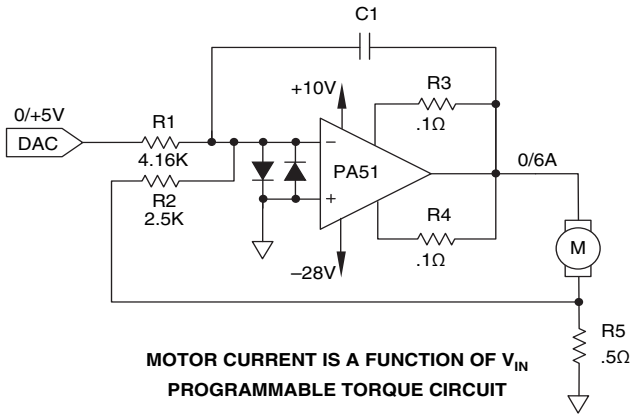
- DC SERVO AMPLIFIER
- MOTOR/SYNCHRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR

DESCRIPTION

The PA51 and PA51A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary common emitter output stage is the simple class C type optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended. Do not use isolation washers!

This hybrid integrated circuit utilizes thick film conductors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

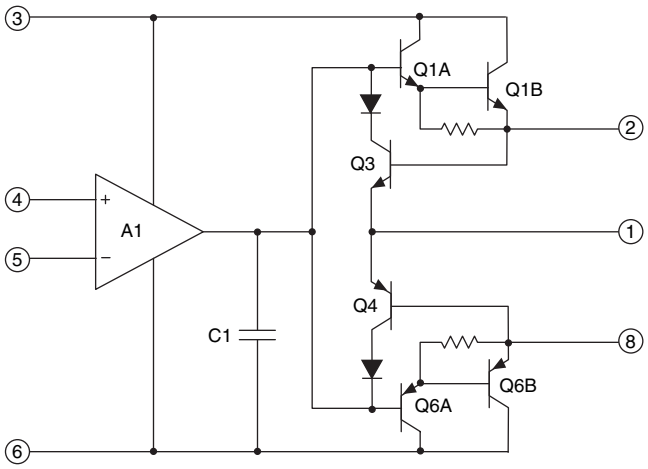
TYPICAL APPLICATION



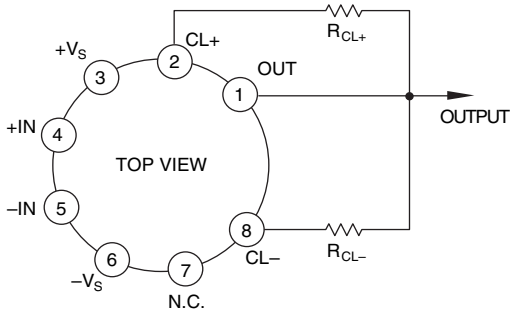
MOTOR CURRENT IS A FUNCTION OF V_{IN}
PROGRAMMABLE TORQUE CIRCUIT

The linear relationship of torque output to current input of the modern torque motor makes this simple control circuit ideal for many material processing and testing applications. The sense resistor develops a feedback voltage proportional to motor current and the small signal properties of the Power Op Amp insure accuracy. With this closed loop operation, temperature induced impedance variations of the motor winding are automatically compensated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction[1]	200°C
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

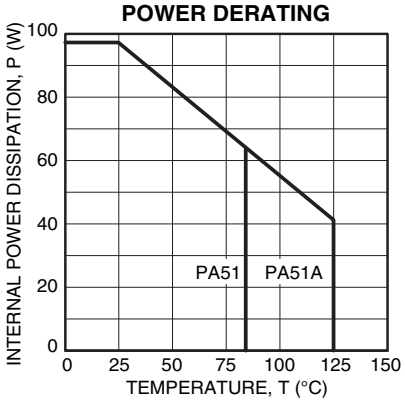
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 5]	PA51 MIN	PA51 TYP	PA51 MAX	PA51A MIN	PA51A TYP	PA51A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±2	±8	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±35			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±15	±40		*	±30	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05			*		nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.02			*		nA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.05			*		nA/°C
INPUT IMPEDANCE, common mode	T_C = 25°C		250			*		MΩ
INPUT IMPEDANCE, differential	T_C = 25°C		10			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–6	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	T_C = 25°C, $V_{CM} = \pm V_S$ –6V	70	110		80	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	94	115		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, $V_O = 40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S$–8	$\pm V_S$–5		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S$–6	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S$–6			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±36	*	±34	±40	V
CURRENT, quiescent	T_C = 25°C		2.6	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

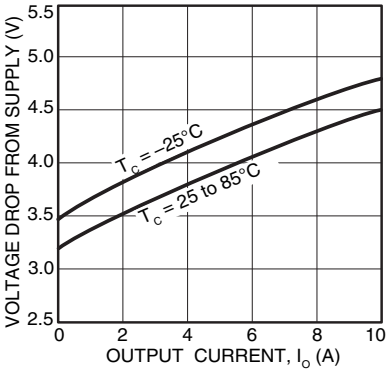
NOTES: * The specification of PA51A is identical to the specification for PA51 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not 100% tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

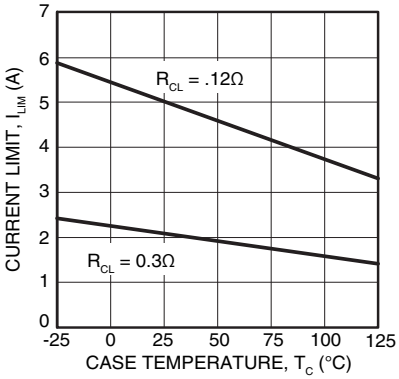
POWER DERATING



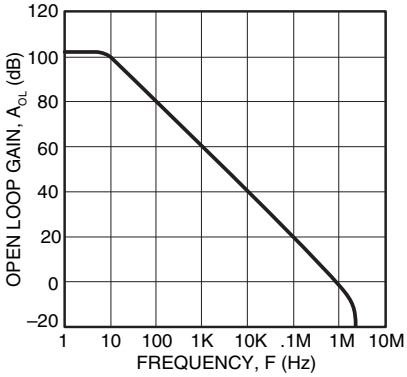
OUTPUT VOLTAGE SWING



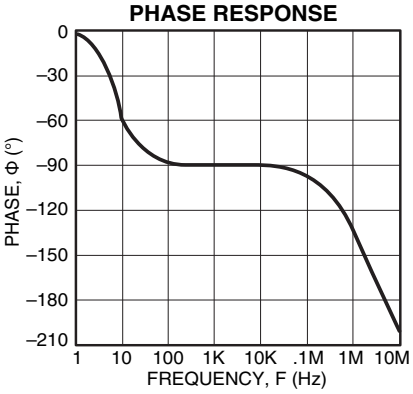
CURRENT LIMIT



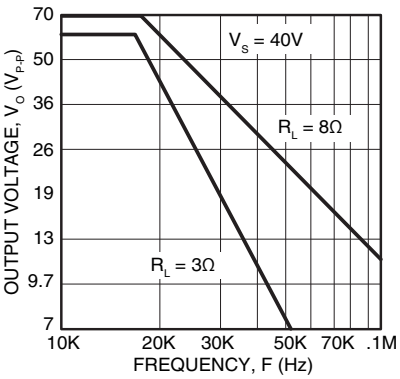
SMALL SIGNAL RESPONSE



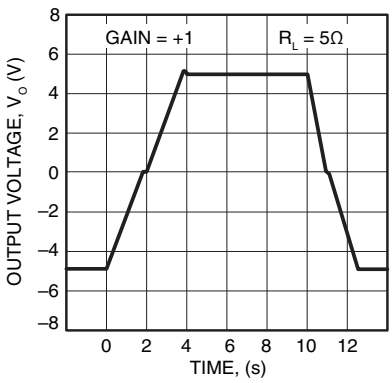
PHASE RESPONSE



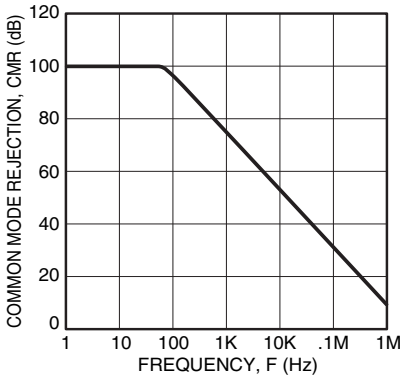
POWER RESPONSE



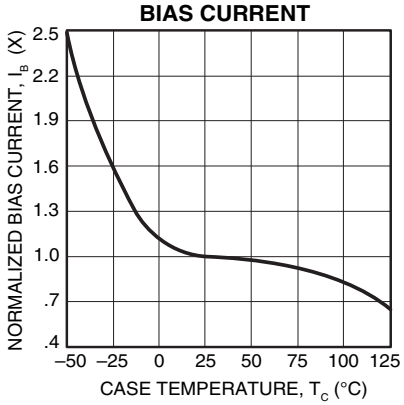
PULSE RESPONSE



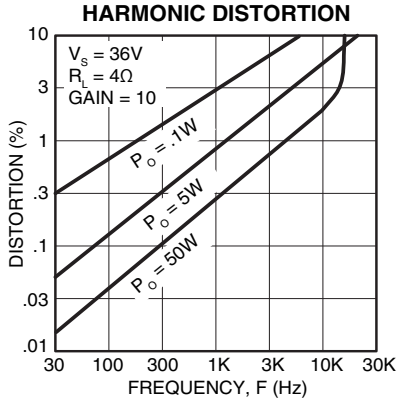
COMMON MODE REJECTION



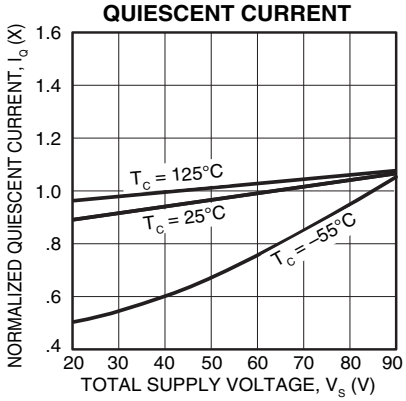
BIAS CURRENT



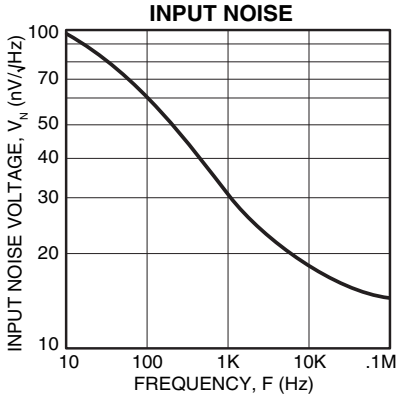
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



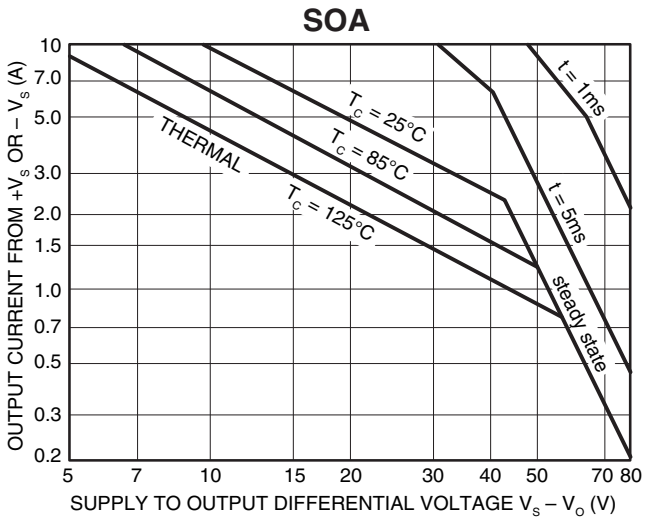
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
40V	400µF	200µF	11mH	4.3mH
35V	800µF	400µF	20mH	5.0mH
30V	1,600µF	800µF	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

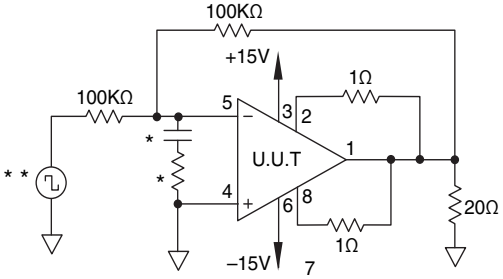
CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is .06 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		10	mA
1	Input offset voltage	V_{OS}	25°C	±34V	V_{IN} = 0, A_V = 100		±10	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±16	mV
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
1	Input bias current, +IN	$+I_B$	25°C	±34V	V_{IN} = 0		±40	nA
1	Input bias current, – IN	$–I_B$	25°C	±34V	V_{IN} = 0		±40	nA
1	Input offset current	I_{OS}	25°C	±34V	V_{IN} = 0		±10	nA
3	Quiescent current	I_Q	–55°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		10	mA
3	Input offset voltage	V_{OS}	–55°C	±34V	V_{IN} = 0, A_V = 100		±15.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±21.2	mV
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±16.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±34V	V_{IN} = 0		±72	nA
3	Input bias current, –IN	$–I_B$	–55°C	±34V	V_{IN} = 0		±72	nA
3	Input offset current	I_{OS}	–55°C	±34V	V_{IN} = 0		±26	nA
2	Quiescent current	I_Q	125°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		13	mA
2	Input offset voltage	V_{OS}	125°C	±34V	V_{IN} = 0, A_V = 100		±16.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±22.5	mV
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±17.7	mV
2	Input bias current, +IN	$+I_B$	125°C	±34V	V_{IN} = 0		±80	nA
2	Input bias current, –IN	$–I_B$	125°C	±34V	V_{IN} = 0		±80	nA
2	Input offset current	I_{OS}	125°C	±34V	V_{IN} = 0		±30	nA
4	Output voltage, I_O =10A	V_O	25°C	±18V	R_L = 1Ω	10		V
4	Output voltage, I_O = 68mA	V_O	25°C	±40V	R_L = 500Ω	34		V
4	Output voltage, I_O = 4A	V_O	25°C	±30V	R_L = 6Ω	24		V
4	Current limits	I_{CL}	25°C	±16V	R_L = 1Ω, R_{CL} = .1Ω	5	7.9	A
4	Stability/noise	E_N	25°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
4	Slew rate	SR	25°C	±34V	R_L = 500Ω	1.0	10	V/µs
4	Open loop gain	A_{OL}	25°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
4	Common-mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
6	Output voltage, I_O =10A	V_O	–55°C	±18V	R_L = 1Ω	10		V
6	Output voltage, I_O = 68mA	V_O	–55°C	±40V	R_L = 500Ω	34		V
6	Output voltage, I_O = 4A	V_O	–55°C	±30V	R_L = 6Ω	24		V
6	Stability/noise	E_N	–55°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
6	Slew rate	SR	–55°C	±34V	R_L = 500Ω	1.0	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
6	Common-mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
5	Output voltage, I_O = 8A	V_O	125°C	±16V	R_L = 1Ω	8		V
5	Output voltage, I_O = 68mA	V_O	125°C	±40V	R_L = 500Ω	34		V
5	Output voltage, I_O = 4A	V_O	125°C	±30V	R_L = 6Ω	24		V
5	Stability/noise	E_N	125°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
5	Slew rate	SR	125°C	±34V	R_L = 500Ω	1.0	10	V/µs
5	Open loop gain	A_{OL}	125°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
5	Common-mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH INTERNAL DISSIPATION — 400 Watts
- HIGH CURRENT — 40A Continuous, 80A PEAK
- HIGH SLEW RATE — 50V/µs
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

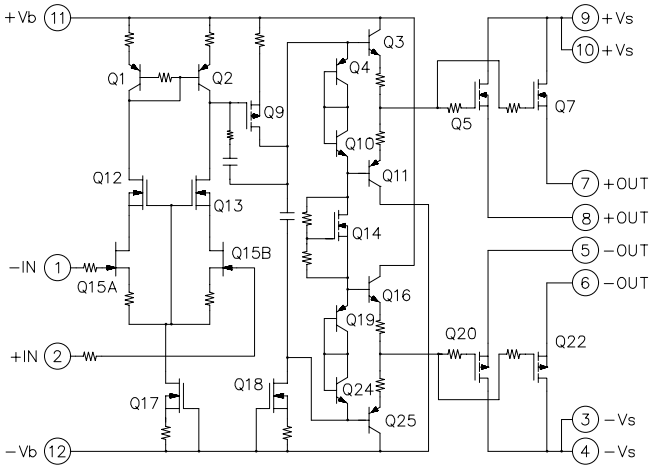
- SEMI-CONDUCTOR TESTING

DESCRIPTION

The PA52 is a MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation.

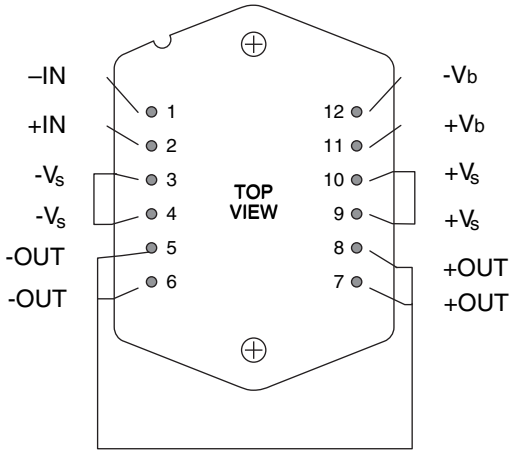
EQUIVALENT SCHEMATIC



12-PIN DIP
PACKAGE STYLE CR

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EXTERNAL CONNECTIONS



E

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE, $+V_b$ to $-V_b$	230V
OUTPUT CURRENT, within SOA	80A
POWER DISSIPATION, internal	400W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_b$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA52 MIN	PA52 TYP	PA52 MAX	PA52A MIN	PA52A TYP	PA52A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20	50		*	*	µV/°V
OFFSET VOLTAGE, vs. supply			10	30		*	*	µV/V
BIAS CURRENT, initial			10	50		*	*	pA
BIAS CURRENT vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		*	*	pA
INPUT IMPEDANCE, DC			10"			*		Ω
IMPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$-V_B$ +12 $+V_B$ -14			*			V
COMMON MODE REJECTION,DC	Full temp, range, V_{CM}= ±20V	90	100			*	*	dB
INPUT NOISE	100KHZ BW, Rs=1KΩ		10			*		µVrms
GAIN								
OPEN LOOP,@ 15Hz	Full temperature range	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L=10Ω		3			*		MHz
POWER BANDWIDTH	R_L=4Ω, V_o=180V_{P-P}, Av=-10 Full temperature range		90			*		kHz
OUTPUT								
VOLTAGE SWING	I_o=40A	$\pm V_S \mp 9.5$	$\pm V_S \mp 8.0$		*	*		V
VOLTAGE SWING, PA52	$\pm V_{BOOST}=\pm V_S \pm 10V$, I_o=40A	$\pm V_S \mp 5.8$	$\pm V_S \mp 4.0$					V
VOLTAGE SWING, PA52A	$\pm V_{BOOST}=\pm V_S \pm 10V$, I_o=50A				$\pm V_S \mp 5.8$	$\pm V_S \mp 5.0$		V
CURRENT, peak	3ms 10% Duty Cycle	80			*			A
SETTLING TIME TO.1%	A_V= -10,10V STEP,R_L=4Ω		1			*		µs
SLEW RATE	A_V=-10	50			*			V/µs
RESISTANCE	I_O=0, NO LOAD, 2MHZ		2.5			*		Ω
POWER SUPPLY								
VOLTAGE, $\pm V_{BOOST}$	Full temperature range	+14, -12	±30	±115	*	*	*	V
VOLTAGE, $\pm V_S$	Full temperature range	±3		±100	*		*	V
CURRENT,quiescent, boost supply			26	32		*	*	mA
CURRENT, quiescent, total			30	36		*	*	mA
THERMAL								
RESISTANCE,AC,junction to case[3]	Full temperature range, F>60HZ		.2	.25		*	*	°C/W
RESISTANCE,DC,junction to case	Full temperature range, F>60HZ		.25	.31		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25		85	*		*	°C

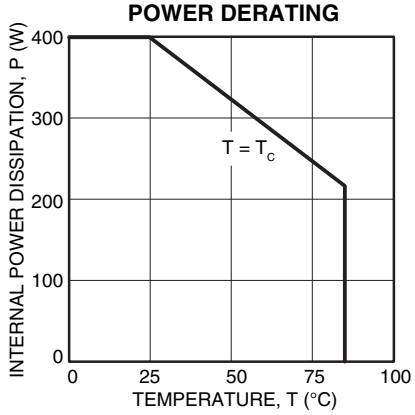
NOTES: * The specification of PA52A is identical to the specification for PA52 in applicable column to the left

1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

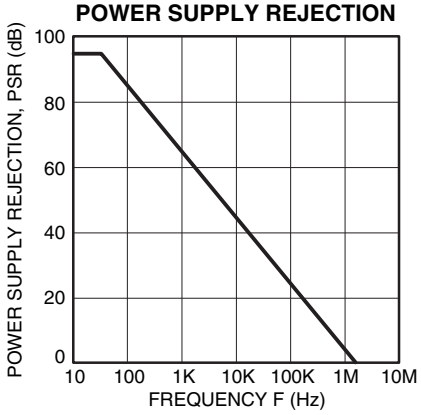
CAUTION The PA52 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

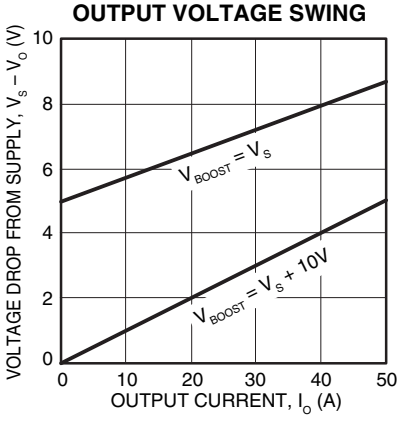
POWER DERATING



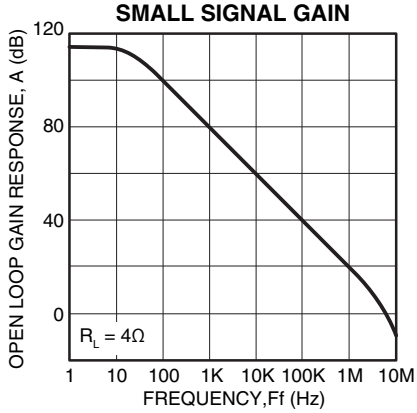
POWER SUPPLY REJECTION



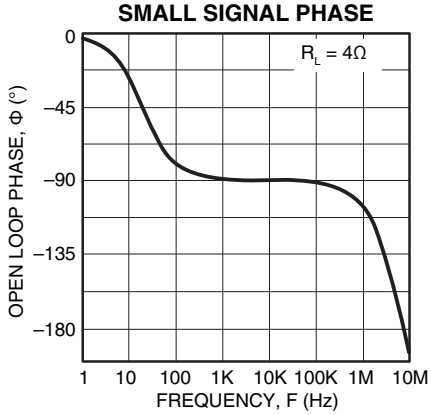
OUTPUT VOLTAGE SWING



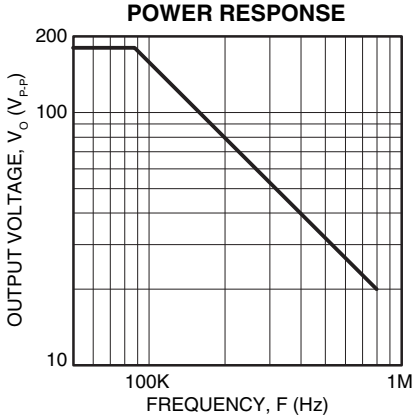
SMALL SIGNAL GAIN



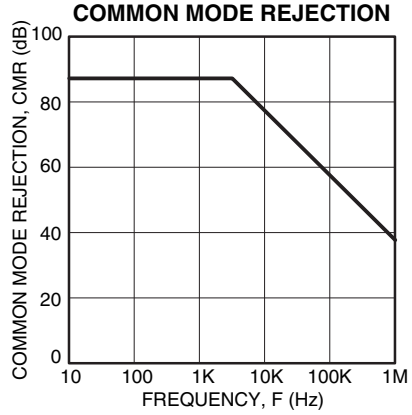
SMALL SIGNAL PHASE



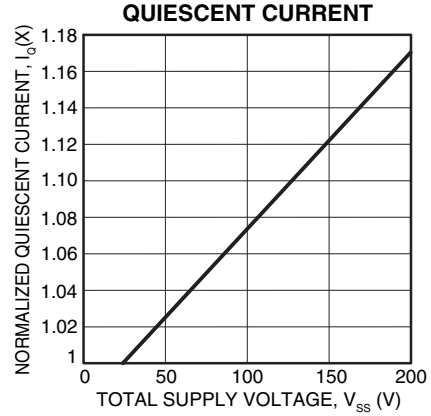
POWER RESPONSE



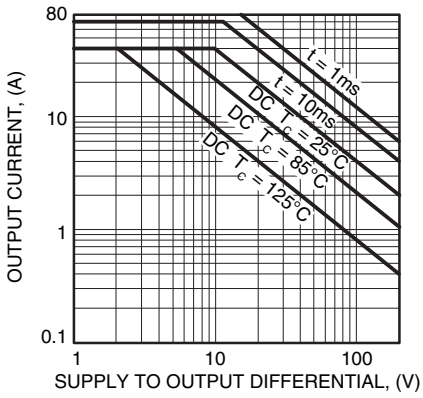
COMMON MODE REJECTION



QUIESCENT CURRENT



SAFE OPERATING AREA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

There is no internal circuit provision for current limit in the PA52. However, the PA52 circuit board in the PA52 evaluation kit does provide a means whereby the output current can be sensed. An external circuit current limit can thereby be implemented if needed.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 11) and $-V_{BOOST}$ (pin 12) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 9,10) and $-V_S$ (pin 3,4) are connected to the high current output stage. An additional 10V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

Compensation is internally fixed for a gain of 3 or more and is not adjustable by the user. The PA52 therefore is not unity gain stable.

POWER SUPPLY BYPASSING

Proper and sufficient power supply bypassing is crucial to proper operation of the PA52. Bypass the +Vb and -Vb supply pins with a minimum .1µF ceramic capacitors directly at the supply pins. On the +Vs and -Vs pins use a combination of ceramic and electrolytic capacitors. Use 1µF ceramic capacitors and an electrolytic capacitor at least 10µF for each amp of output current required.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

High VoltagePower Operational Amplifiers

RoHS COMPLIANT

FEATURES

- RoHS COMPLIANT
- LOW COST
- WIDE BANDWIDTH - 1.1 Mhz
- HIGH OUTPUT CURRENT - 1A per amplifier
- WIDE COMMON MODE RANGE Includes negative supply
- WIDE SUPPLY VOLTAGE RANGE
  - Single supply: 5V to 40V
  - Split supplies: ± 2.5V to ± 20V
- LOW QUIESCIENT CURRENT
- VERY LOW DISTORTION

APPLICATIONS

- HALF AND FULL BRIDGE MOTOR DRIVERS
- AUDIO POWER AMPLIFIER
  - Stereo - 15.91W RMS per channel
  - Bridge - 31.82W RMS per 2 channels
- IDEAL FOR SINGLE SUPPLY SYSTEMS
  - 5V - Peripherals
  - 12V - Automotive
  - 28V - Avionic

DESCRIPTION

The amplifier design is a dual power op amp on a single monolithic die. This approach provides a cost-effective solution to applications where multiple amplifiers are required or a bridge configuration is needed. Very low harmonic distortion of 0.02% THD and low I_Q makes the PA60 a good solution for low power audio applications such as laptops and computer speakers.

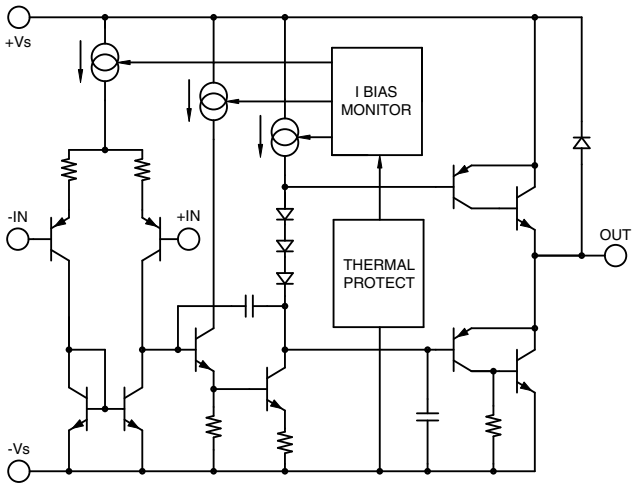


FIGURE 1. Equivalent schematic (one channel)

The dual output PA60EU, is available in a 12-Pin Molded Plastic SIP with standard 100 mil spacing. The heat tab of EU package is tied to $-V_S$.

12-PIN SIP
PACKAGE STYLE EU

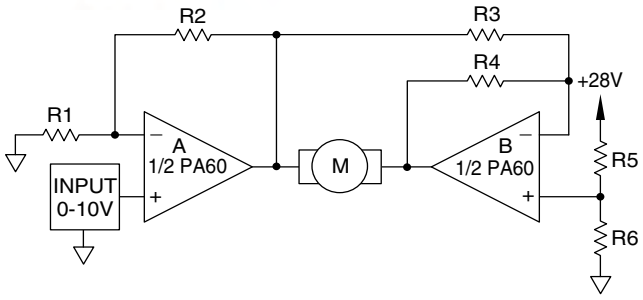


FIGURE 2. Bi-directional speed control from a single supply

TYPICAL APPLICATION

R1 and R2 set up Amplifier A as non-inverting. Amplifier B is set up as a unity gain inverter driven from the output of Amplifier A. Note that Amplifier B inverts the signals about the reference node, which is set at mid-supply by R5 and R6. When the command input is midrange, so is the output of Amplifier A. Since this is also equivalent to the reference node voltage, the output of Amplifier B is the same resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 2). Inputs less than 5V drive the motor in the opposite direction.

The amplifiers are especially well-suited for applications such as this. The extended common mode range allows command inputs as low as 0V. The output swing lets it drive within 2V of the supply at an output of 1A. This means that a command input that ranges from 0 to 10V will drive a 24V motor from full scale CCW to full scale CW at ±1A.

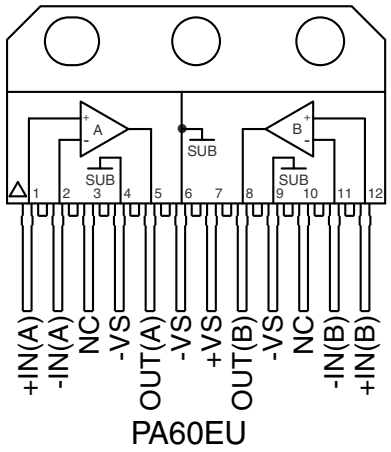


FIGURE 3. External Connections.

ABSOLUTE MAXIMUM RATINGS

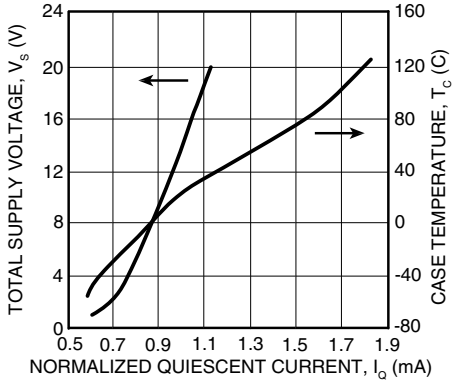
SUPPLY VOLTAGE, total	5V to 40V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (PA60EU, 1 amplifier)	19.89W
POWER DISSIPATION, internal (PA60EU, 2 amplifiers)[4]	31.82W
INPUT VOLTAGE, differential	±Vs
INPUT VOLTAGE, common mode	+Vs,-Vs-.5V
JUNCTION TEMPERATURE, max.[1]	150°C
TEMPERATURE, pin solder - 10 secs max.	220°C
TEMP RANGE STORAGE	-55°C to 150°C
OPERATING TEMP RANGE, case[1]	-40°C to 125°C

SPECIFICATIONS (PER AMPLIFIER)

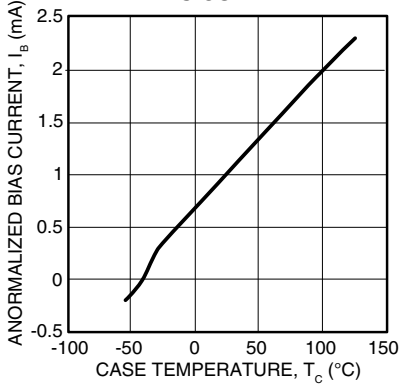
PARAMETER	TEST CONDITIONS[1,2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			1	15	mV
OFFSET VOLTAGE, vs. temperature	Full temp range		20		µV/°C
BIAS CURRENT, initial			100	500	nA
COMMON MODE RANGE	Full temp range	-Vs		+Vs - 1.3	V
COMMON MODE REJECTION, DC		60	90		dB
POWER SUPPLY REJECTION	Full temp range	60	90		dB
CHANNEL SEPARATION	I_{OUT} = 500mA, f = 1kHz	50	68		dB
INPUT NOISE VOLTAGE	R_S = 100Ω, f = 1 to 100kHz		22		nV/√Hz
GAIN					
OPEN LOOP GAIN	V_O = ±10V, R_L = 2.0KΩ	89	100		dB
GAIN BANDWIDTH PRODUCT	f = 100kHz, C_L = 100pF, R_L = 2.0KΩ	0.9	1.4		MHz
PHASE MARGIN	Full temp range, C_L = 100pF, R_L = 2KΩ		65		°C
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6		kHz
OUTPUT					
CURRENT, peak				1.5	A
SLEW RATE		1.0	1.4		V/µS
VOLTAGE SWING	Full temp range, I_O = 100mA	|Vs| -1.1	|Vs| -0.8		V
VOLTAGE SWING	Full temp range, I_O = 1A	|Vs| -1.8	|Vs| -1.4		V
HARMONIC DISTORTION	A_V = 1, R_L = 50Ω, V_O = .5VRMS, f = 1kHz		.02		%
POWER SUPPLY					
VOLTAGE, V_{SS}[3]		5	30	40	V
CURRENT, quiescent total			8	10	mA
THERMAL					
RESISTANCE, junction to case					
DC, 1 amplifier			5.71	6.29	°C/W
DC, 2 amplifiers[4]			3.57	3.93	°C/W
AC, 1 amplifier			4.29	4.71	°C/W
AC, 2 amplifiers[4]			2.68	2.95	°C/W
RESISTANCE, junction to air			30		°C/W

Notes:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: ±V_S = ±15V, T_C =25°C.
3. +V_S and -V_S denote the positive and negative rail respectively. V_{SS} denotes total rail-to-rail supply.
4. Rating applies when power dissipation is equal in each of the amplifiers.
5. If -V_S is disconnected before +V_S, a diode between -V_S and ground is recommended to avoid damage.

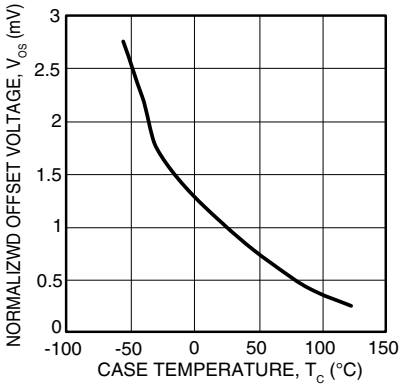
QUIESCENT CURRENT



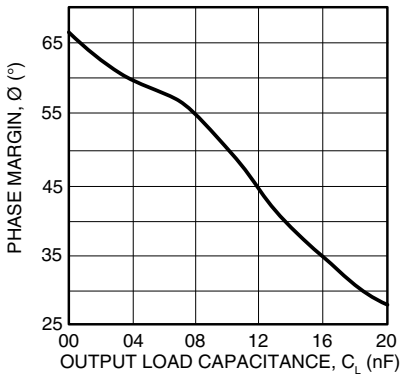
BIAS CURRENT



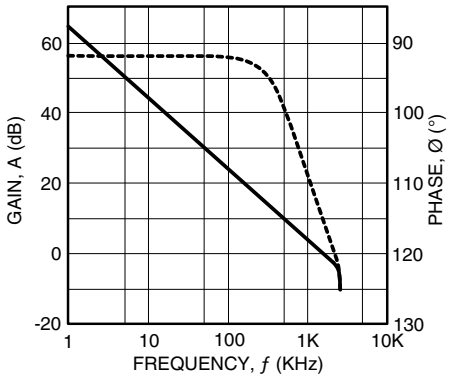
OFFSET VOLTAGE



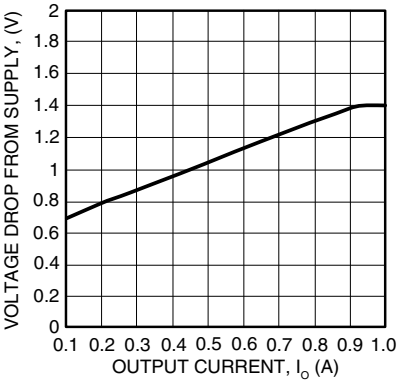
PHASE MARGIN vs. OUTPUT LOAD CAPACITANCE



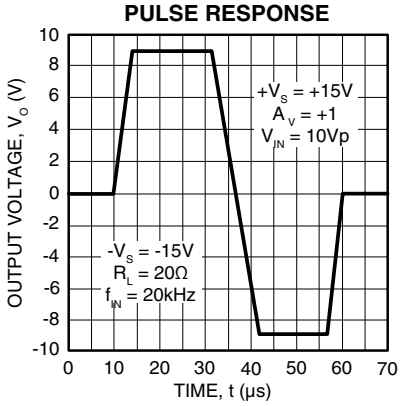
VOLTAGE GAIN & PHASE vs. FREQUENCY



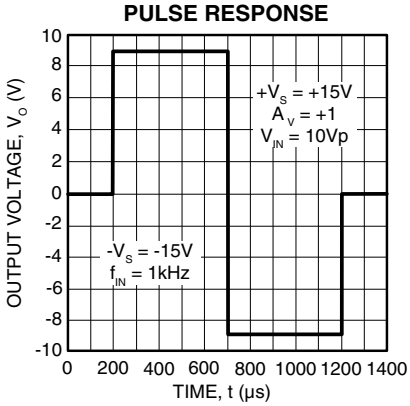
OUTPUT VOLTAGE SWING



PULSE RESPONSE



PULSE RESPONSE



GENERAL

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STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions. For applications with load current exceeding 300mA, oscillation may appear. The oscillation may occur only with the output voltage swing at the negative or positive half cycle. Under most operating and load conditions acceptable stability can be achieved by providing a series RC snubber network connected from the output to ground (see Figure 4). The recommended component values of the of the network are, R_{SN} = 10Ω and C_{SN} = 0.01µF. Please refer to Application Note 1 for further details.

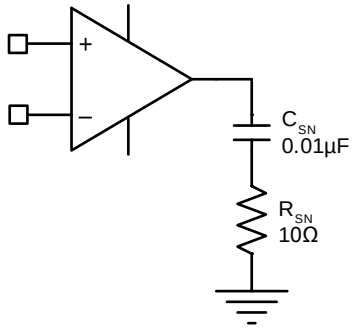


FIGURE 4. R-C Snubber

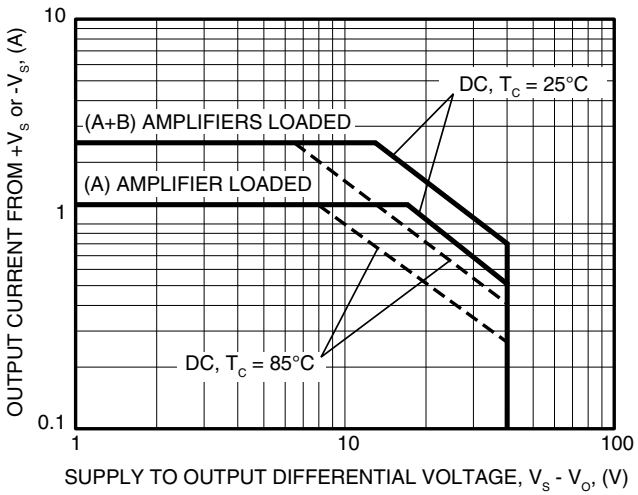
SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

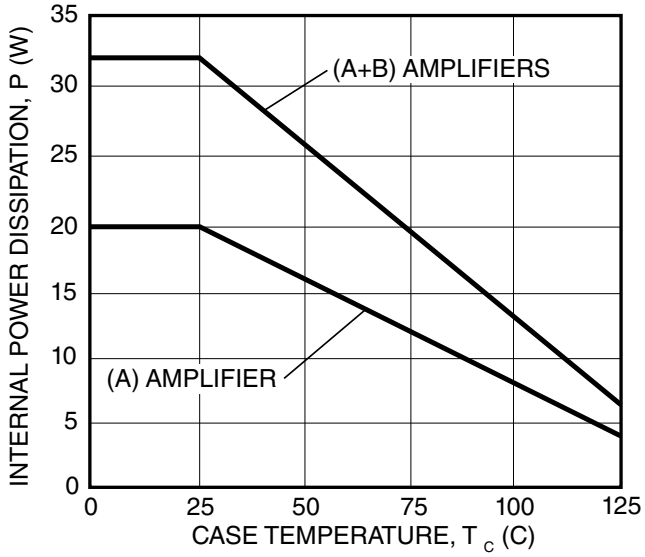
THERMAL CONSIDERATIONS

The PA60EU has a large exposed copper heat tab to which the monolithic is directly attached. The PA60EU may require a thermal washer, which is electrically insulating since the tab is directly tied to $-V_S$. This can result in a thermal impedance R_{CS} of up to 1˚C/W or greater.

SOA PA60EU



POWER DERATING



MOUNTING PRECAUTIONS

1. Always use a heat sink. Even unloaded the PA60EU can dissipate up to .4 watts.
2. Avoid bending the leads. Such action can lead to internal damage.
3. Always fasten the tab of the EU package to the heat sink before the leads are soldered to fixed terminals.
4. Strain relief must be provided if there is any probability of axial stress to the leads.

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±10 to ±45V
- HIGH OUTPUT CURRENT — ±10A Peak
- LOW COST — Class "C" output stage
- LOW QUIESCENT CURRENT — 3mA

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

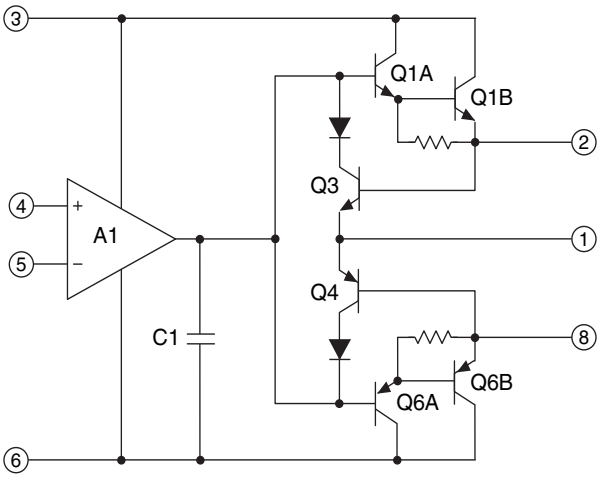
- PROGRAMMABLE POWER SUPPLY
- MOTOR/SYNCRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR
- FIXED FREQUENCY POWER OSCILLATOR

DESCRIPTION

The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary emitter follower output stage is the simple class C type and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film conductors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque voids the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



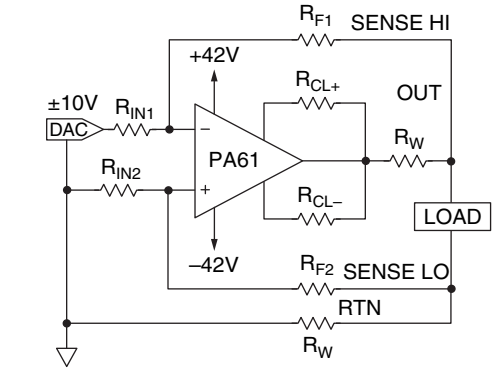


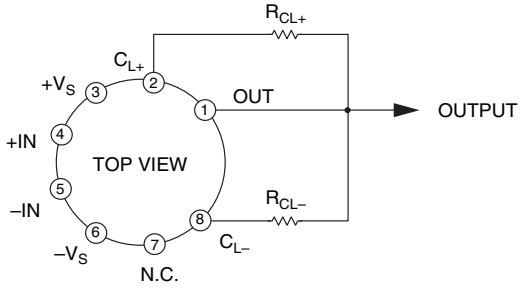
FIGURE 1. PROGRAMMABLE POWER SUPPLY WITH REMOTE SENSING

TYPICAL APPLICATION

Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents, and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75V error at the load.

With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	90V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

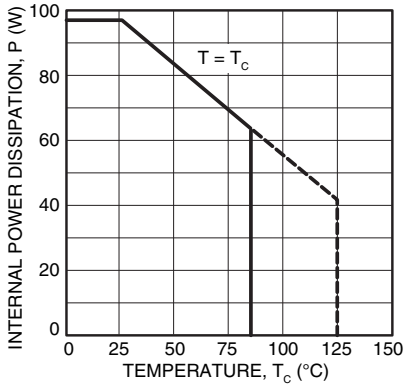
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA61 MIN	PA61 TYP	PA61 MAX	PA61A MIN	PA61A TYP	PA61A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Specified temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Specified temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Specified temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Specified temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Specified temperature range	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, V_O = $40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S$–7	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S$–6	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S$–5			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.8		*	*		V/µs
CAPACITIVE LOAD, unit gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±32	±45	*	*	*	V
CURRENT, quiescent	T_C = 25°C		3	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25	25	+85	*	*	*	°C

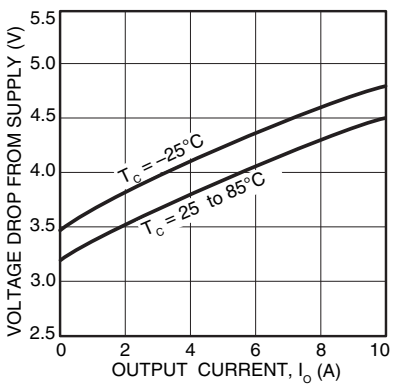
NOTES: * The specification of PA61A is identical to the specification for PA61 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

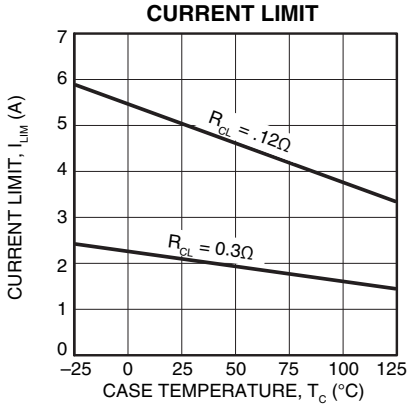
POWER DERATING



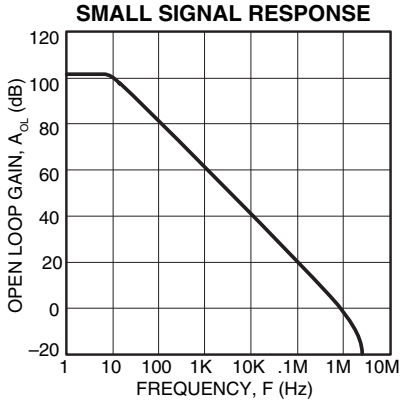
OUTPUT VOLTAGE SWING



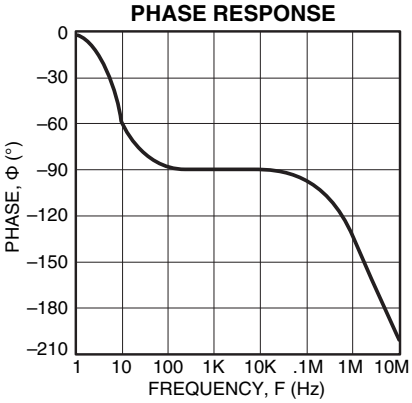
CURRENT LIMIT



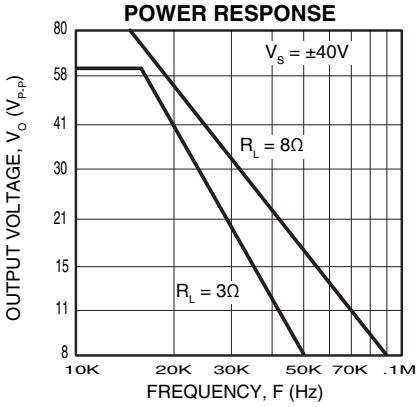
SMALL SIGNAL RESPONSE



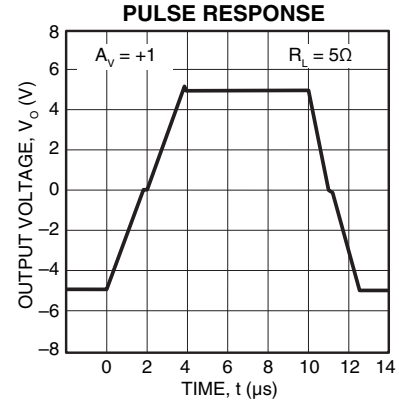
PHASE RESPONSE



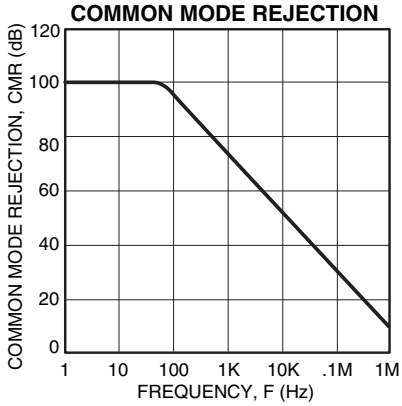
POWER RESPONSE



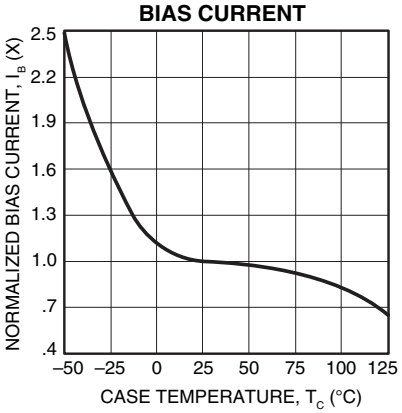
PULSE RESPONSE



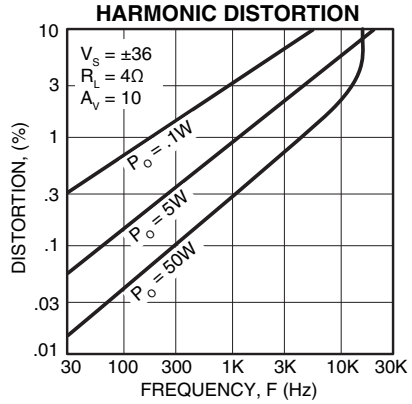
COMMON MODE REJECTION



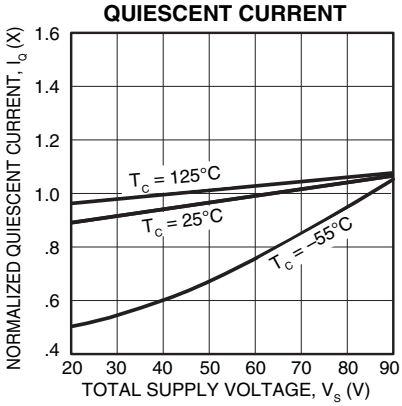
BIAS CURRENT



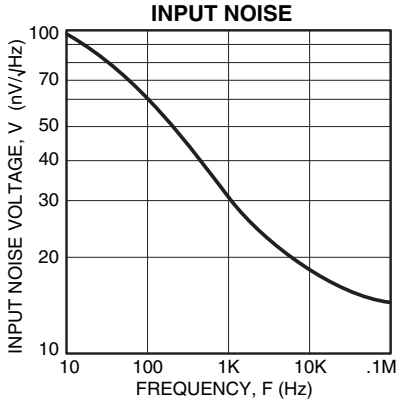
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



GENERAL

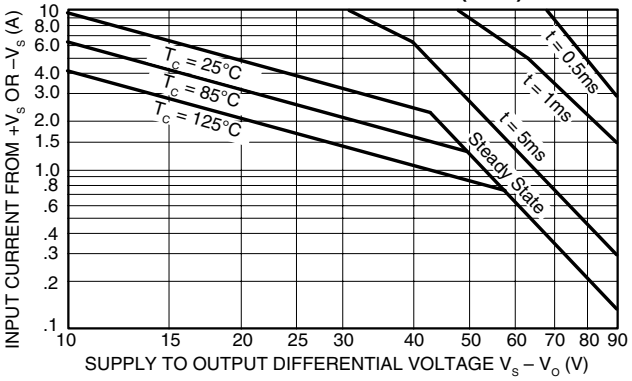
Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.

SAFE OPERATING AREA (SOA)



3. The junction temperature of the output transistors.

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
V_S	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
45V	200 F	150 F	8mH	2.8mH
40V	400 F	200 F	11mH	4.3mH
35V	800 F	400 F	20mH	5.0mH
30V	1600 F	800 F	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C=85°C.

$\pm V_S$	SHORT TO $V_S \pm$ C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

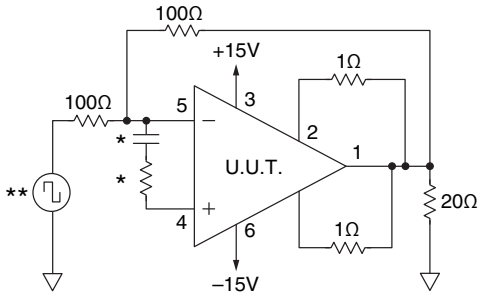
These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±32V	V_{IN} = 0, A_V = 100		10	mA
1	Input Offset Voltage	V_{OS}	25°C	±32V	V_{IN} = 0, A_V = 100		±6	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±10.4	mV
1	Input Offset Voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±8.6	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Offset Current	I_{OS}	25°C	±32V	V_{IN} = 0		±30	nA
3	Quiescent Current	I_Q	–55°C	±32V	V_{IN} = 0, A_V = 100		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±32V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±15.6	mV
3	Input Offset Voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±13.8	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input Offset Current	I_{OS}	–55°C	±32V	V_{IN} = 0		±115	nA
2	Quiescent Current	I_Q	125°C	±32V	V_{IN} = 0, A_V = 100		15	mA
2	Input Offset Voltage	V_{OS}	125°C	±32V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±16.9	mV
2	Input Offset Voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±15.1	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Offset Current	I_{OS}	125°C	±32V	V_{IN} = 0		±70	nA
4	Output Voltage, I_O = 10A	V_O	25°C	±17V	R_L = 1Ω	10		V
4	Output Voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output Voltage, I_O = 4A	V_O	25°C	± 30V	R_L = 6Ω	24		V
4	Current Limits	I_{CL}	25°C	±15V	R_L = 6Ω, R_{CL} = 1Ω	.56	.88	A
4	Stability/Noise	E_N	25°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±32V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output Voltage, I_O = 10A	V_O	–55°C	±17V	R_L = 1Ω	10		V
6	Output Voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Output Voltage, I_O = 4A	V_O	–55°C	±30V	R_L = 6Ω	24		V
6	Stability/Noise	E_N	–55°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±32V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
6	CommonMode Rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output Voltage, I_O = 8A	V_O	125°C	±15V	R_L = 1Ω	8		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output Voltage, I_O = 4A	V_O	125°C	±30V	R_L = 6Ω	24		V
5	Stability/Noise	E_N	125°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±32V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA69

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- A Unique (Patent Pending) Technique for Very Low Quiescent Current
- Over 350 V/µs Slew Rate
- Wide Supply Voltage
  - Single Supply: 20V To 200V
  - Split Supplies: ± 10V To ± 100V
- Output Current – 75mA Cont.; 100mA Pk
- Up to 23 Watt Dissipation Capability
- Over 200 kHz Power Bandwidth

APPLICATIONS

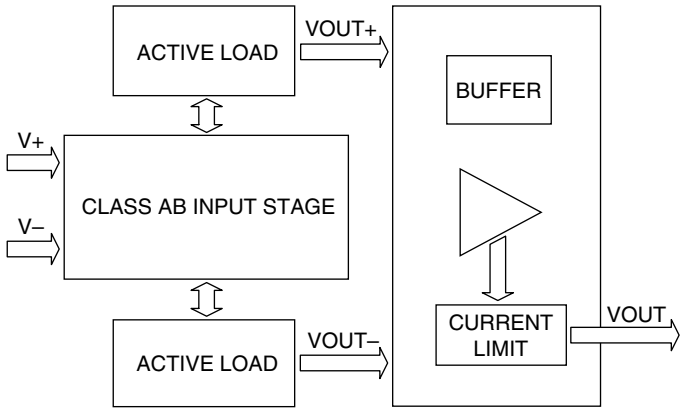
- Piezoelectric Positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

DESCRIPTION

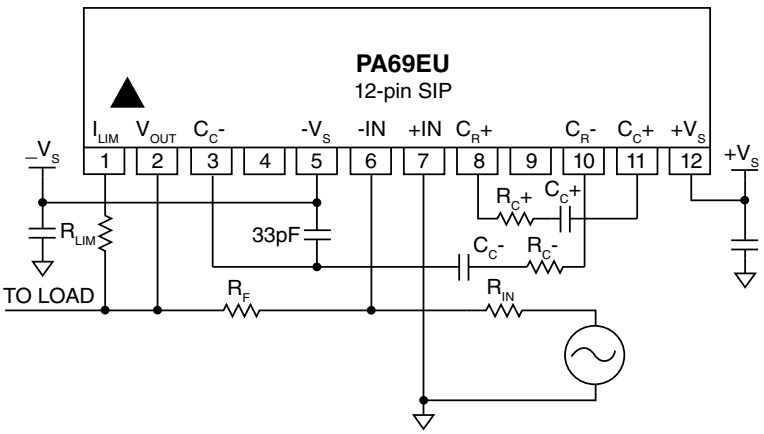
The PA69 is a high voltage, high speed, low idle current op-amp capable of delivering up to 100mA peak output current. Due to the dynamic biasing of the input stage, it can achieve slew rates over 350V/µs, while only consuming less than 1mA of idle current. External phase compensation allows great flexibility for the user to optimize bandwidth and stability.

The output stage is protected with user selected current limit resistor. For the selection of this current limiting resistor, pay close attention to the SOA curves for each package type. Proper heatsinking is required for maximum reliability.

BLOCK DIAGRAM



EXTERNAL CONNECTIONS



12–Pin SIP
PACKAGE STYLE EU
LEAD FORM EW

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			200	V
OUTPUT CURRENT, peak (200ms), within SOA			200	mA
POWER DISSIPATION, internal, DC			23	W
INPUT VOLTAGE, differential		−15	15	V
INPUT VOLTAGE, common mode		$-V_S$	$+V_S$	V
TEMPERATURE, pin solder, 10s			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−55	125	°C
OPERATING TEMPERATURE, case		−40	125	°C

SPECIFICATIONS

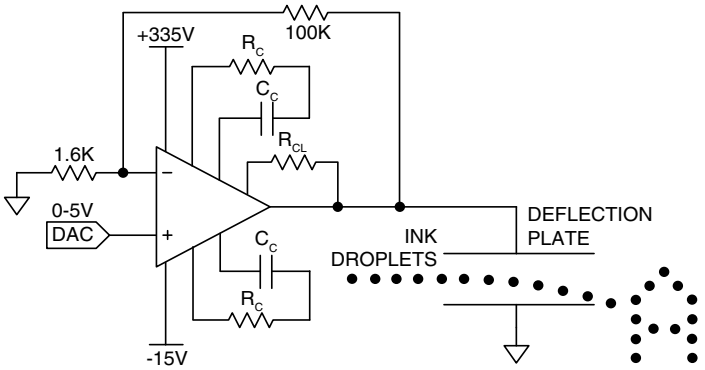
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE		-25	8	25	mV
OFFSET VOLTAGE vs. temperature	0 to 125°C (Case Temperature)		-63		µV/°C
OFFSET VOLTAGE vs. supply				32	µV/V
BIAS CURRENT, initial			8.5	200	pA
OFFSET CURRENT, initial			12	400	pA
INPUT RESISTANCE, DC			10^8		Ω
COMMON MODE VOLTAGE RANGE, pos.			$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC		90	118		dB
NOISE	700KHz		418		µV RMS
NOISE, V_O NOISE			500		nV/√Hz
GAIN					
OPEN LOOP @ 1Hz		89	120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
OUTPUT					
VOLTAGE SWING	I_O = 10mA		$\|V_S\|$ - 2		V
VOLTAGE SWING	I_O = 75mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
CURRENT, continuous, DC		75			mA
SLEW RATE	**Package Tab connected to GND**	100	350		V/µS
SETTLING TIME, to 0.1%	5V Step (No Compensation)		1		µS
POWER BANDWIDTH, $300V_{P-P}$	$+V_S$ = 160V, $-V_S$ = -160V		200		kHz
OUTPUT RESISTANCE, No load	R_{CL} = 6.2Ω		44		Ω
POWER SUPPLY					
VOLTAGE		±10	±50	±100	V
CURRENT, quiescent (Note 5)	±100V Supply	0.2	0.7	2.5	mA

Parameter	Test Conditions	Min	Typ	Max	Units
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range		5.5		ºC/W
RESISTANCE, DC, junction to air	Full temperature range		12.21		ºC/W
TEMPERATURE RANGE, case		-40		125	ºC

NOTES: 1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative supply voltages of the output stage.
4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
5. Supply current increases with signal frequency. See graph on page 4.

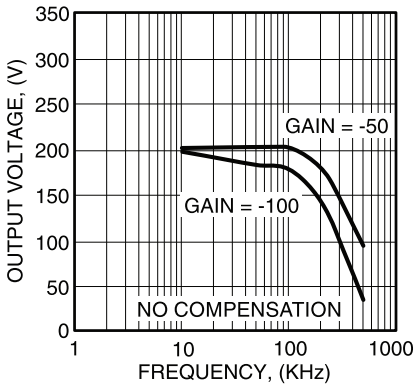
TYPICAL APPLICATION CIRCUIT

The PA69 is ideally suited for driving continuous drop ink jet printers, in both piezo actuation and deflection applications. The high voltage of the amplifier creates an electrostatic field on the deflection plates to control the position of the ink droplets. The rate at which droplets can be printed is directly related to the rate at which the amplifier can drive the plate to a different electrostatic field strength.

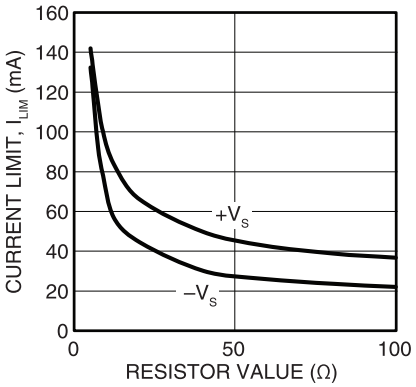


TYPICAL PERFORMANCE GRAPHS

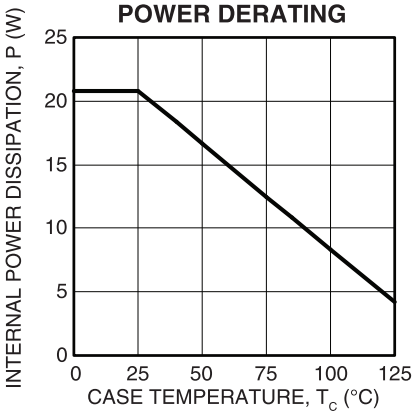
POWER RESPONSE



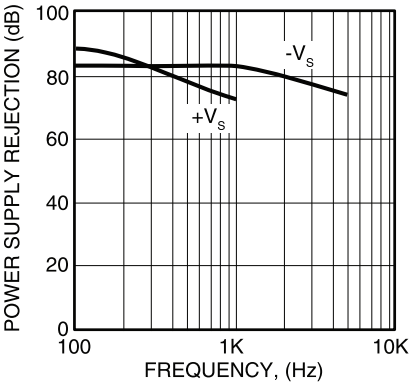
CURRENT LIMIT



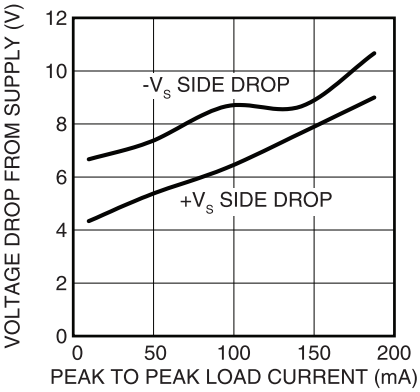
POWER DERATING



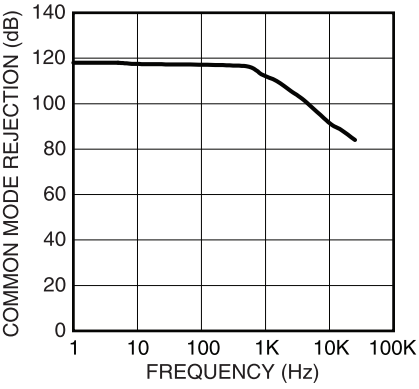
POWER SUPPLY REJECTION



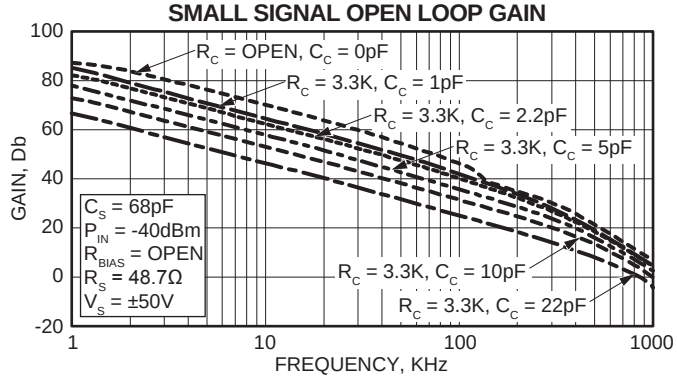
OUTPUT VOLTAGE SWING



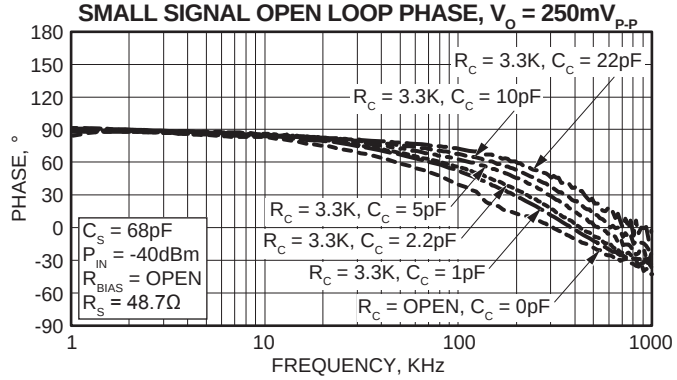
COMMON MODE REJECTION



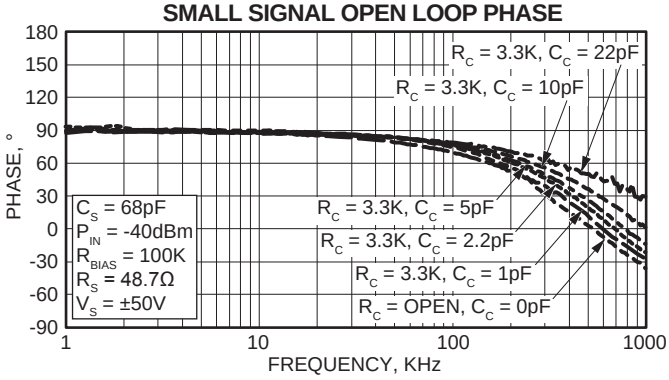
SMALL SIGNAL OPEN LOOP GAIN



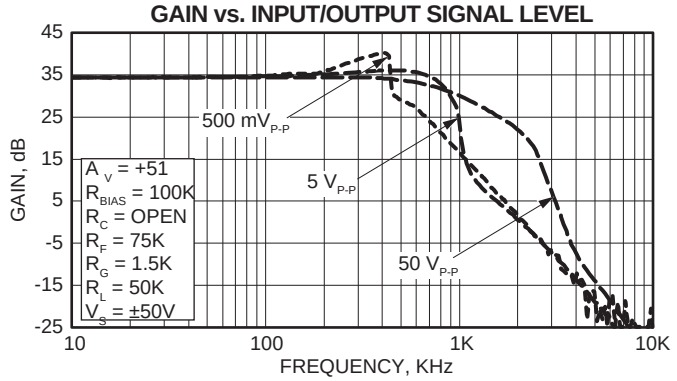
SMALL SIGNAL OPEN LOOP PHASE, V_O = 250mV$_{P-P}$



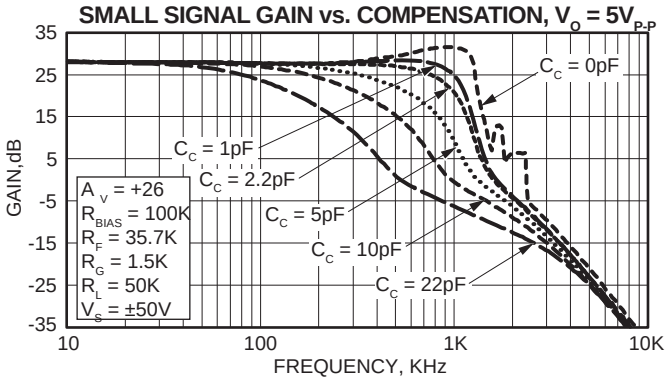
SMALL SIGNAL OPEN LOOP PHASE



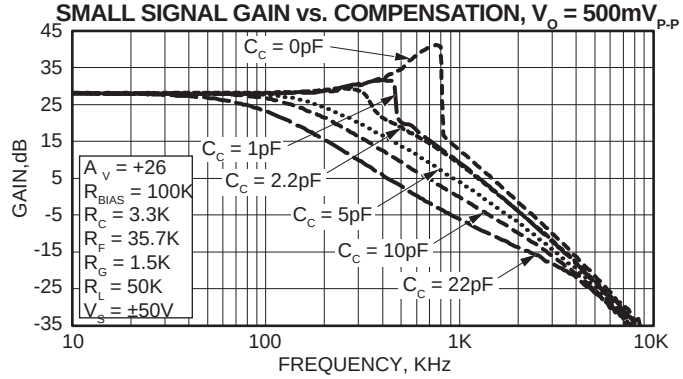
GAIN vs. INPUT/OUTPUT SIGNAL LEVEL



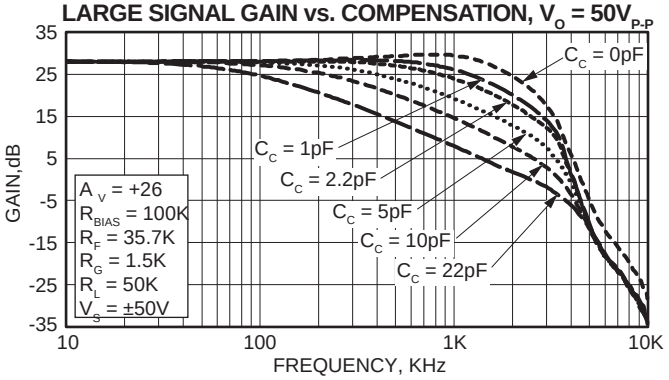
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 5V$_{P-P}$

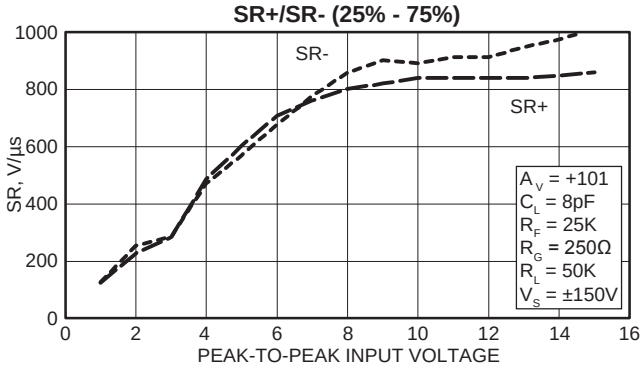


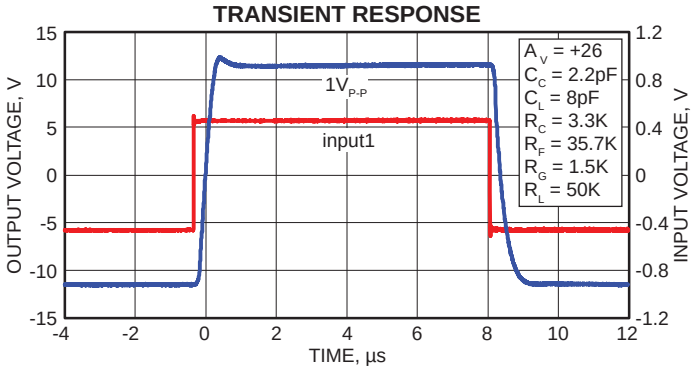
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 500mV$_{P-P}$

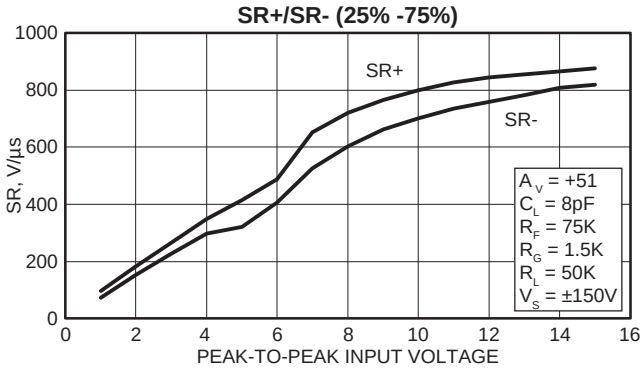


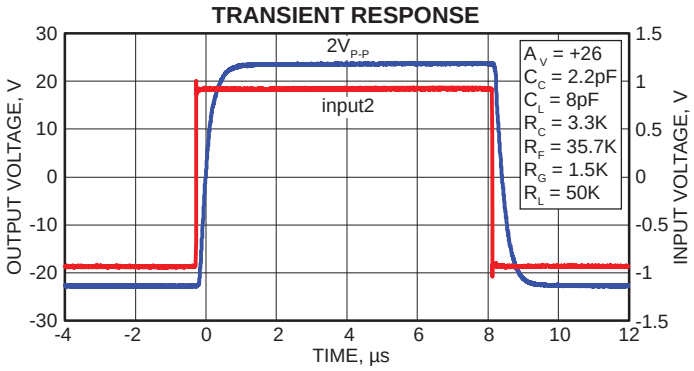
LARGE SIGNAL GAIN vs. COMPENSATION, V_O = 50V$_{P-P}$

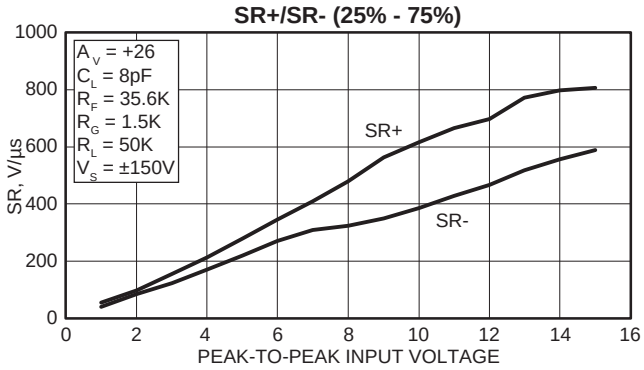


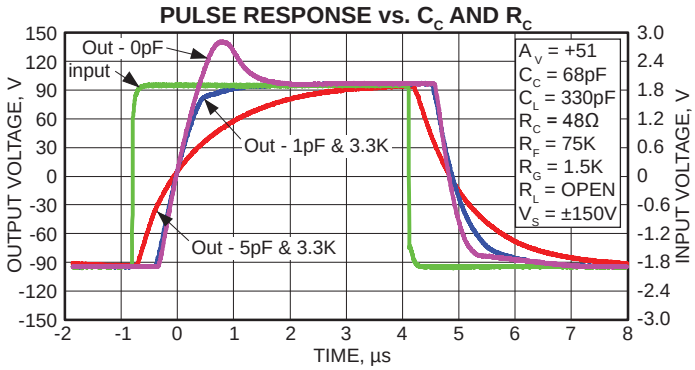

SR+/SR- (25% - 75%)
SR-
SR+
A_V = +101
C_L = 8pF
R_F = 25K
R_G = 250Ω
R_L = 50K
V_S = ±150V
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE


TRANSIENT RESPONSE
1V_P-P
input1
A_V = +26
C_C = 2.2pF
C_L = 8pF
R_C = 3.3K
R_F = 35.7K
R_G = 1.5K
R_L = 50K
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs

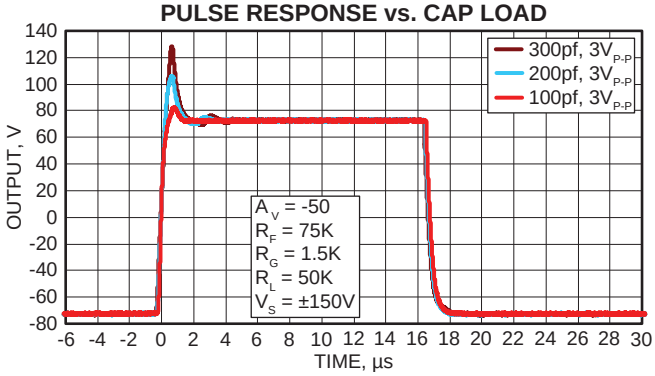

SR+/SR- (25% -75%)
SR+
SR-
A_V = +51
C_L = 8pF
R_F = 75K
R_G = 1.5K
R_L = 50K
V_S = ±150V
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE


TRANSIENT RESPONSE
2V_P-P
input2
A_V = +26
C_C = 2.2pF
C_L = 8pF
R_C = 3.3K
R_F = 35.7K
R_G = 1.5K
R_L = 50K
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs

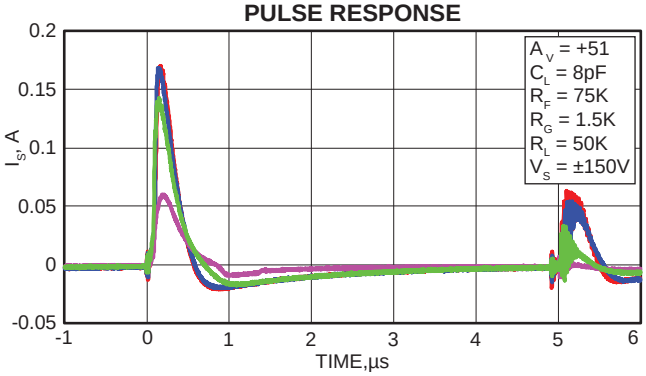

SR+/SR- (25% - 75%)
SR+
SR-
A_V = +26
C_L = 8pF
R_F = 35.6K
R_G = 1.5K
R_L = 50K
V_S = ±150V
SR, V/µs
PEAK-TO-PEAK INPUT VOLTAGE


PULSE RESPONSE vs. C_C AND R_C
Out - 0pF
input
Out - 1pF & 3.3K
Out - 5pF & 3.3K
A_V = +51
C_C = 68pF
C_L = 330pF
R_C = 48Ω
R_F = 75K
R_G = 1.5K
R_L = OPEN
V_S = ±150V
OUTPUT VOLTAGE, V
INPUT VOLTAGE, V
TIME, µs

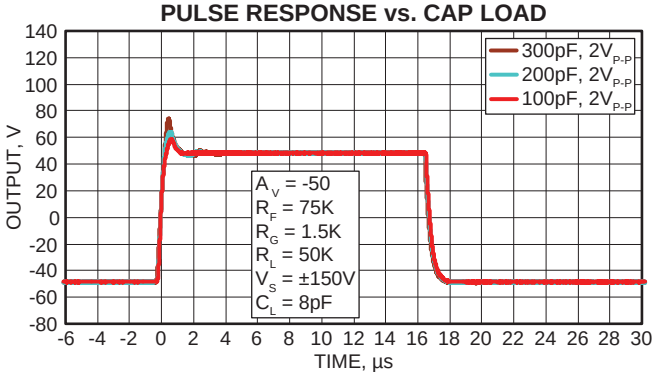
PULSE RESPONSE vs. CAP LOAD



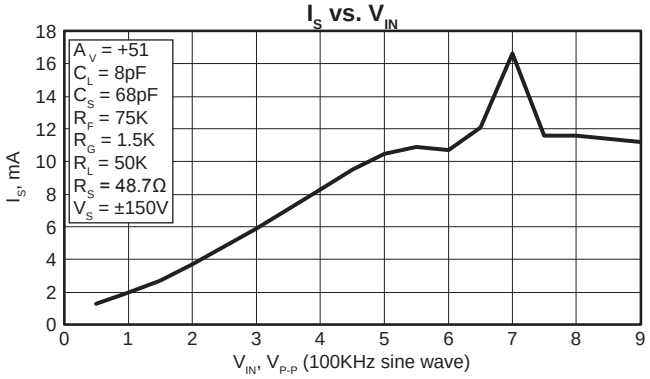
PULSE RESPONSE



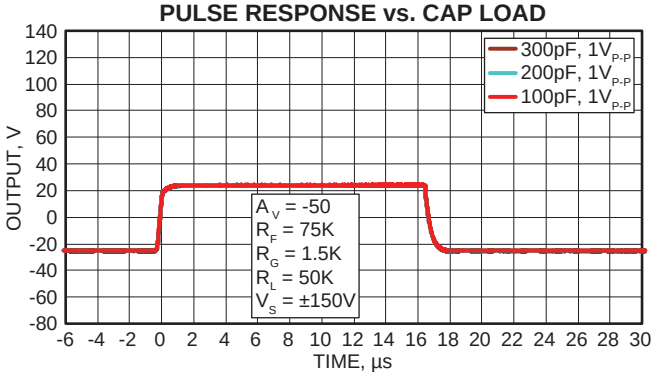
PULSE RESPONSE vs. CAP LOAD



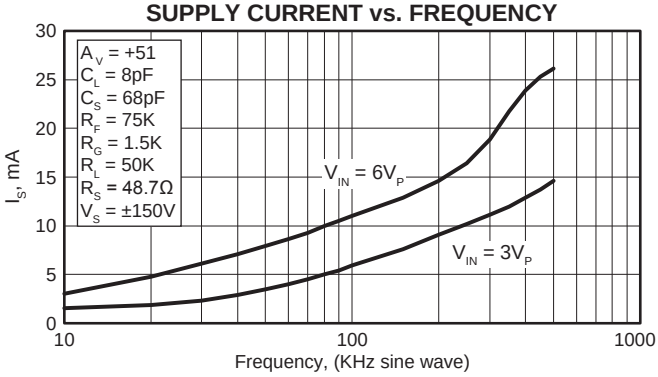
I_S vs. V_{IN}



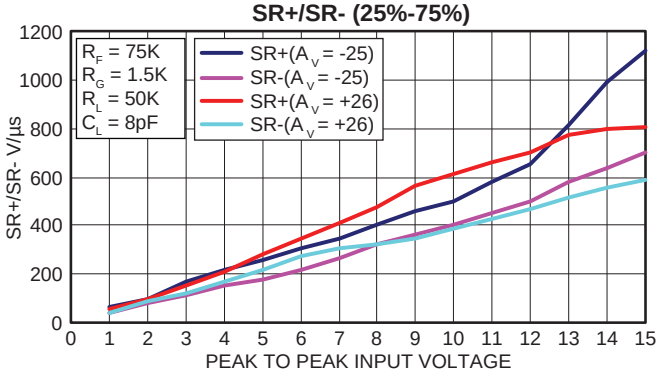
PULSE RESPONSE vs. CAP LOAD



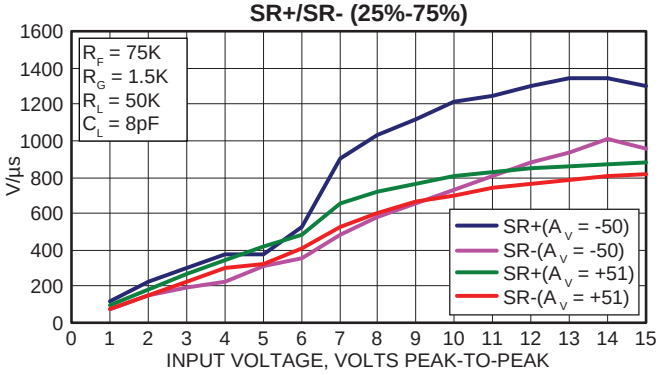
SUPPLY CURRENT vs. FREQUENCY



SR+/SR- (25%-75%)



SR+/SR- (25%-75%)



GENERAL

Please read Application note 1 “General operating considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, and current limit. There you will also find a complete application notes library, technical seminar workbook, and evaluation kits.

THEORY OF OPERATION

The PA69 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.

SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA69 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA69 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA69. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, Rbias, between C_C- and V_S+. The size of Rbias will depend upon the application but 500µA of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA69 is externally compensated and performance can be optimized to the application. Unlike the Rbias technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the tradeoffs between bandwidth and stability. Due to the unique design of the PA69, two symmetric compensation networks are required. The compensation capacitor C_C must be rated for a working voltage of the full operating

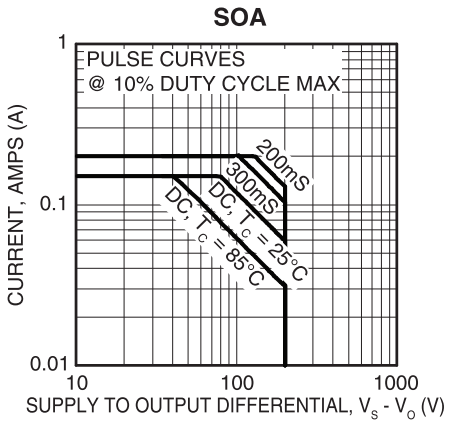
supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature..
The PA69 requires an external 33pF capacitor between C_C- and –Vs to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from $1V_{P-P}$ to $15V_{P-P}$, the slew rate increases from 50V/µs to well over 350V/µs.
The output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA69 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current V_S. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.
The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.



CURRENT LIMIT

For proper operation, the current limit resistor, Rlim, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The minimum practical value for R_{LIM} is about 12Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for R_{LIM} in the intended application.

LAYOUT CONSIDERATIONS

The PA69 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1uF capacitor to GND is also sufficient if a DC connection is undesirable
Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of L_C interactions and oscillations.

ELECTROSTATIC DISCHARGE

Like many high performance MOSFET amplifiers, the PA69 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

PA74/PA76 • PA74A/76A

Power Dual Operational Amplifiers

RoHS COMPLIANT

FEATURES

- LOW COST
- WIDE COMMON MODE RANGE — Includes negative supply
- WIDE SUPPLY VOLTAGE RANGE
  - Single supply: 5V to 40V
  - Split supplies: ±2.5V to ±20V
- HIGH EFFICIENCY — |Vs–2.2V| at 2.5A typ
- HIGH OUTPUT CURRENT — 3A
- LOW DISTORTION

APPLICATIONS

- HALF & FULL BRIDGE MOTOR DRIVERS
- AUDIO POWER AMPLIFIER
  - STEREO — 30W RMS per channel
  - BRIDGE — 60W RMS per package
- IDEAL FOR SINGLE SUPPLY SYSTEMS
  - 5V — Peripherals, 12V — Automotive
  - 28V — Avionic

8-PIN TO-3
PACKAGE STYLE CE

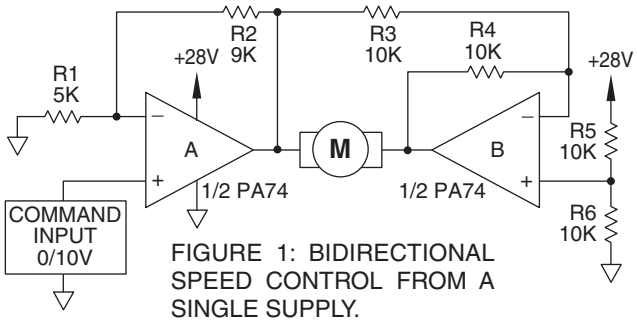


FIGURE 1: BIDIRECTIONAL SPEED CONTROL FROM A SINGLE SUPPLY.

DESCRIPTION

The amplifier design consists of dual monolithic input and output stages to achieve the desired input and output characteristics of the PA74 and PA76. The input stage utilizes a dual power op amp on a single chip monolithic that drives the output stages. The output stages are configured in a non inverting unity gain buffer configuration. The output stages of the amplifier are also compensated for stability. The PA74 and PA76 dual amplifiers are designed with both monolithic and hybrid technologies providing a cost effective solution for applications requiring multiple amplifiers per board or bridge mode configurations. Both amplifiers are internally compensated but are not recommended for use as unity gain followers.

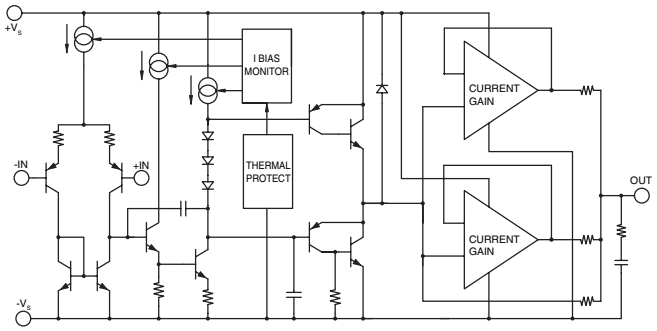
This dual hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and monolithic amplifiers to maximize reliability and power handling capability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-Pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

TYPICAL APPLICATION

R1 and R2 set up amplifier A in a non-inverting gain of 2.8. Amp B is set up as a unity gain inverter driven from the output of amp A. Note that amp B inverts signals about the reference node, which is set at mid-supply (14V) by R5 and R6. When the command input is 5V, the output of amp A is 14V. Since this is equal to the reference node voltage, the output of amp B is also 14V, resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 1). Inputs less positive than 5V drive the motor in the opposite direction.

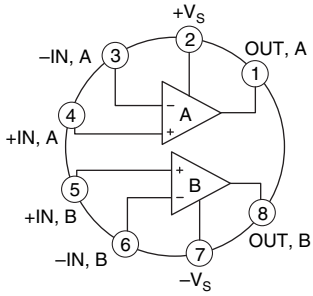
The amplifiers are especially well-suited for this application. The extended common mode range allows command inputs as low as 0V. Its superior output swing abilities let it drive within 2V of supply at an output current of 2A. This means that a command input that ranges from 0.714V to 9.286V will drive a 24V motor from full scale CCW to full scale CW at up to ±2A. A single power op amp with an output swing capability of Vs –6 would require ±30V supplies and would be required to swing 48V p-p at twice the speed to deliver an equivalent drive.

EQUIVALENT SCHEMATIC ONE CHANNEL

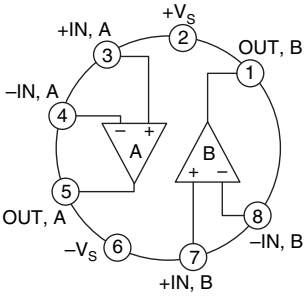


EXTERNAL CONNECTIONS (TOP VIEWS)

PA74



PA76



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, total	5V to 40V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (per amplifier)	36W
POWER DISSIPATION, internal (both amplifiers)	60W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S$–0.5V
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder–10 sec max	300°C
TEMPERATURE RANGE, storage	–65°C to 150°C
OPERATING TEMPERATURE RANGE, case	–55°C to 125°C

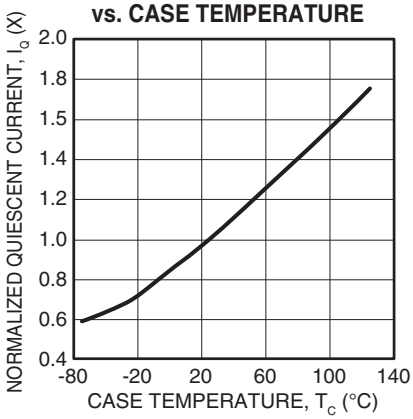
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA74/76 MIN	PA74/76 TYP	PA74/76 MAX	PA74A/PA76A MIN	PA74A/PA76A TYP	PA74A/PA76A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			1.5	10		.5	7	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20			10		µV/°C
BIAS CURRENT, initial			100	500		*	250	nA
COMMON MODE RANGE	Full temperature range	$-V_S$		$+V_S$–1.3	*		*	V
COMMON MODE REJECTION, DC	Full temperature range	60	70		*	*		dB
POWER SUPPLY REJECTION	Full temperature range	60	90		*	*		dB
CHANNEL SEPARATION	I_{OUT} = 1A, F = 1kHz	50	70		*	*		dB
INPUT NOISE VOLTAGE	R_S = 100Ω, f = 1 to 100KHz							
GAIN								
OPEN LOOP GAIN	Full temperature range	89	100		*	*	*	dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB	0.9	1.4		*	*		MHz
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6			*		kHz
OUTPUT								
CURRENT, peak		2.5			3			A
SLEW RATE		0.5	1.4		*	*		V/µs
VOLTAGE SWING	Full temp. range, I_O = 100mA	$\lvert V_S \rvert$ –1.1	$\lvert V_S \rvert$ –0.9		*	*		V
VOLTAGE SWING	Full temp. range, I_O = 1A	$\lvert V_S \rvert$ –2.0	$\lvert V_S \rvert$ –1.7		*	*		V
VOLTAGE SWING	I_O = 2.5A (PA74, 76)	$\lvert V_S \rvert$ –3.5	$\lvert V_S \rvert$ –2.9		*	*		V
VOLTAGE SWING	I_O = 3.0A (PA74A, PA76A)				$\lvert V_S \rvert$ –4.0	$\lvert V_S \rvert$ –3.3		V
POWER SUPPLY								
VOLTAGE, VSS[3]			30	40	*	*	*	V
CURRENT, quiescent, total			18	40		*	*	mA
THERMAL								
RESISTANCE, junction to case								
DC, single amplifier			3.2	3.5		*	*	°C/W
DC, both amplifiers[4]			1.9	2.1		*	*	°C/W
AC, single amplifier			2.4	2.6		*	*	°C/W
AC, both amplifiers[4]			1.4	1.6		*	*	°C/W
RESISTANCE, junction to air			30			*	*	°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	–25		85	°C

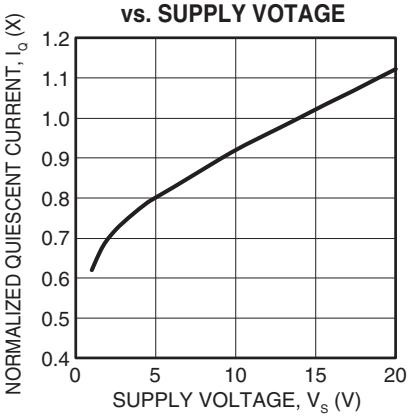
NOTES: * The specification of PA74A/PA76A is identical to the specification for PA74/PA76 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: ±VS = ±15V, TC = 25°C.
3. +VS and –VS denote the positive and negative supply rail respectively. VSS denotes the total rail-to-rail supply voltage.
4. Rating applies when power dissipation is equal in the two amplifiers.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

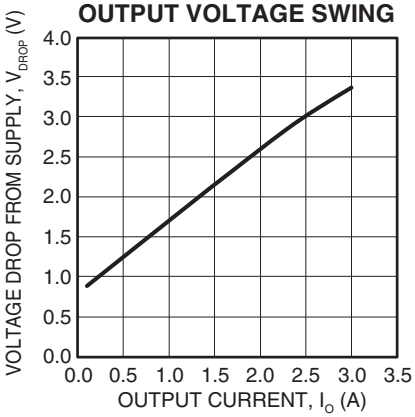
NORMALIZED QUIESCENT CURRENT vs. CASE TEMPERATURE



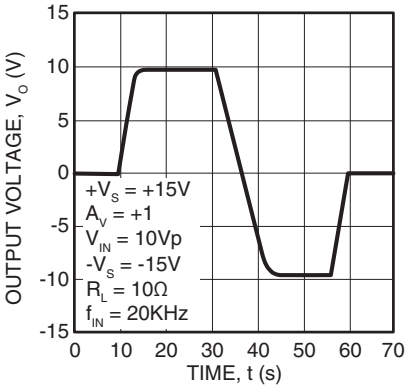
NORMALIZED QUIESCENT CURRENT vs. SUPPLY VOTAGE



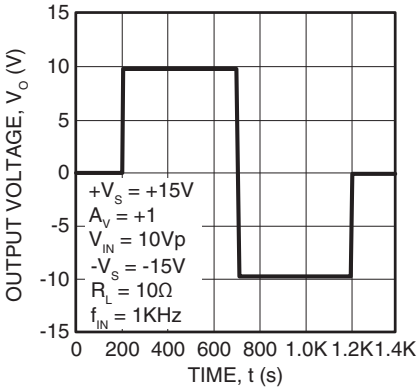
OUTPUT VOLTAGE SWING



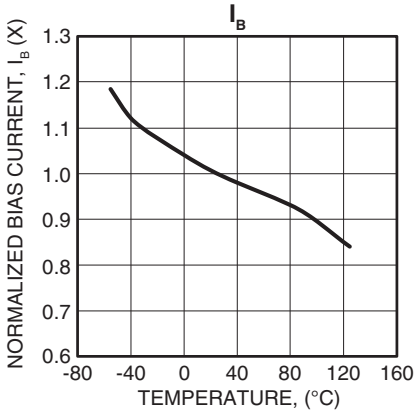
PULSE RESPONSE



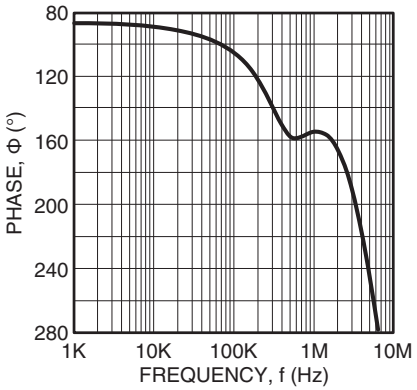
PULSE RESPONSE



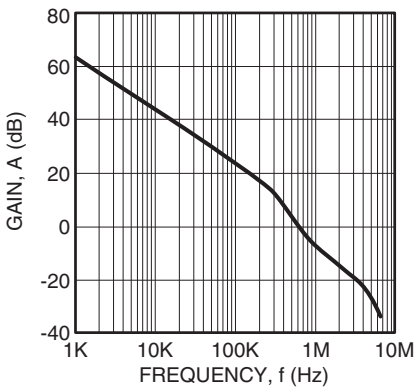
I_B



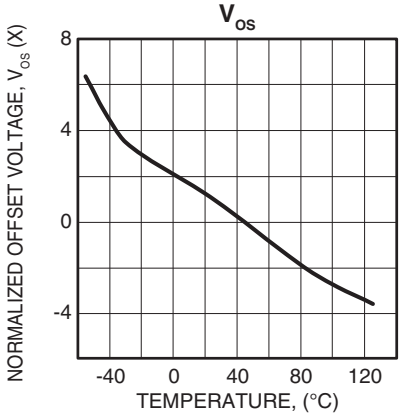
PHASE vs. FREQUENCY



VOLTAGE GAIN vs. FREQUENCY



V_{OS}



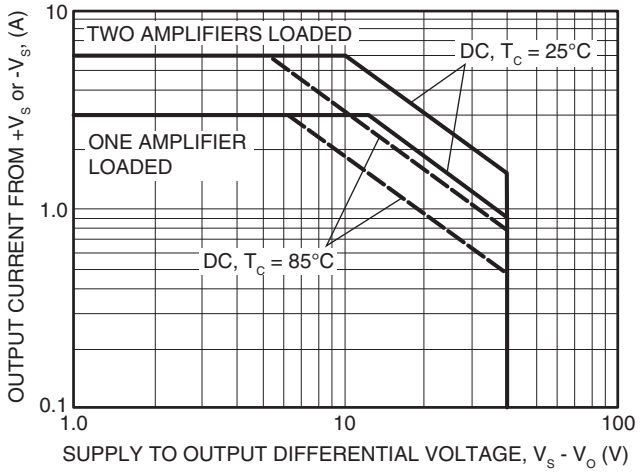
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heatsinking, mounting, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, heatsink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the opamp manufacturer to optimize compensation for all operating conditions.

SOA



SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

THERMAL CONSIDERATIONS

Thermal grease or a Apex Precision Power TW03 thermal washer, RCS = .1 to .2°C/W, is the only recommended interface for the PA74/76. Internal power dissipation increases directly with frequency therefore it is critical to sufficiently heat sink the PA74 and PA76. Even unloaded the PA74 and PA76 can dissipate up to 3 watts while running at higher frequencies.

PARALLEL CONFIGURATION CONSIDERATIONS

LOSSES

The PA74 and PA76 utilize a parallel configuration to achieve the desired current output requirements. The parallel configuration inherently creates internal losses due to circulating currents. The circulating currents generate power losses through the current sharing resistors when delivering current to the load.

SUPPLY CURRENT

The parallel configuration used in the PA74 and PA76 also generates supply currents while high voltage sign waves are seen at the output. Listed below are the supply currents expected while running at a particular frequency and when VO ≈ 15Vpp, note that the outputs are not loaded.

Frequency	Supply Current
100Hz	18mA
1KHz	20mA
5KHz	32mA
10KHz	50mA
15KHz	75mA

SATURATION OPERATION

The parallel configuration used in the PA74 and PA76 is sensitive to operation in the saturation region. The PA74 and PA76 may exhibit large peak currents; this is mainly due to thermal protection limitations.

POWER DERATING

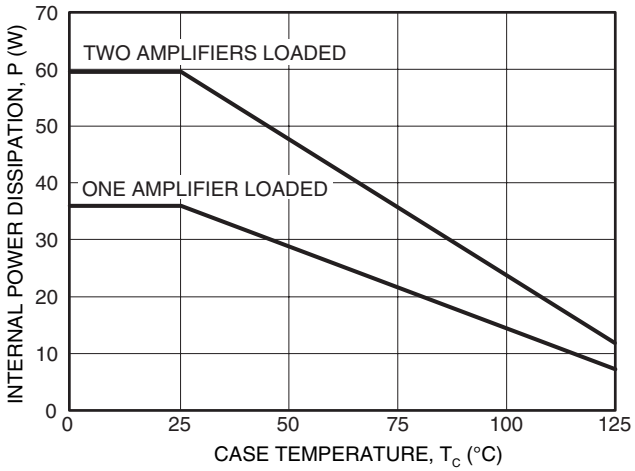
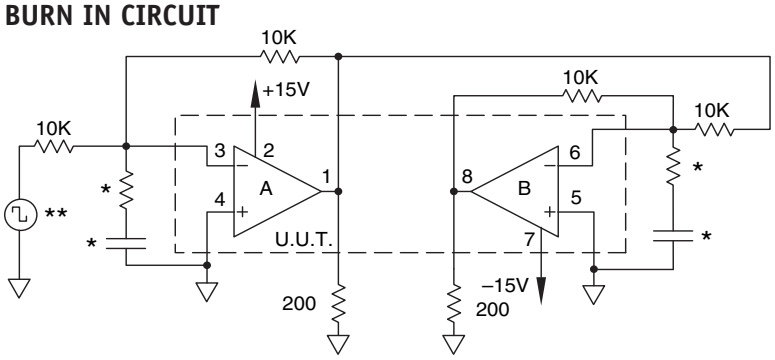


Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiesent Current	I_Q	25°C	±15	V_{IN} = 0, A_V = 100		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±2.5	V_{IN} = 0, A_V = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±15	V_{IN} = 0, A_V = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±20	V_{IN} = 0, A_V = 100		14	mV
1	Input Bias Current + IN	$+I_B$	25°C	±15	V_{IN} = 0		1000	nA
1	Input Bias Current –IN	$–I_B$	25°C	±15	V_{IN} = 0		1000	nA
1	Input Offset Current	I_{OS}	25°C	±15	V_{IN} = 0		500	nA
3	Quiesent Current	I_Q	–55°C	±15	V_{IN} = 0, A_V = 100		30	mA
3	Input Offset Voltage	V_{OS}	–55°C	±2.5	V_{IN} = 0, A_V = 100		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15	V_{IN} = 0, A_V = 100		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	±20	V_{IN} = 0, A_V = 100		18	mV
3	Input Bias Current + IN	$+I_B$	–55°C	±15	V_{IN} = 0		1000	nA
3	Input Bias Current –IN	$–I_B$	–55°C	±15	V_{IN} = 0		1000	nA
3	Input Offset Current	I_{OS}	–55°C	±15	V_{IN} = 0		500	nA
2	Quiesent Current	I_Q	125°C	±15	V_{IN} = 0, A_V = 100		40	mA
2	Input Offset Voltage	V_{OS}	125°C	±2.5	V_{IN} = 0, A_V = 100		15	mV
2	Input Offset Voltage	V_{OS}	125°C	±15	V_{IN} = 0, A_V = 100		15	mV
2	Input Offset Voltage	V_{OS}	125°C	±20	V_{IN} = 0, A_V = 100		19	mV
2	Input Bias Current + IN	$+I_B$	125°C	±15	V_{IN} = 0		1000	nA
2	Input Bias Current –IN	$–I_B$	125°C	±15	V_{IN} = 0		1000	nA
2	Input Offset Current	I_{OS}	125°C	±15	V_{IN} = 0		500	nA
4	Output Voltage I_O= 2A	V_O	25°C	±9.5	R_L = 3Ω	6.0		V
4	Output Voltage I_O= 100mA	V_O	25°C	±11	R_L = 100Ω	9.9		V
4	Output Voltage I_O= 1A	V_O	25°C	±4.8	R_L = 3Ω	2.8		V
4	Stability/Noise	E_N	25°C	±15	R_L = 500Ω, A_V = 1 C_L = 1.5nF		1.0	mV
4	Crosstalk	XTLK	25°C	±15	R_L = 3Ω	50		dB
4	Slew Rate	SR	25°C	±15	R_L = 500Ω	.5		V/µS
4	Open Loop Gain	A_{OL}	25°C	±15	R_L = 500Ω, F =10Hz	75		dB
4	Common-mode Rejection	CMR	25°C	±17	R_L = 500Ω, V_{CM} = ±14V	60		dB
6	Output Voltage I_O= 2A	V_O	–55°C	±9.5	R_L = 3Ω	6.0		V
6	Output Voltage I_O= 100mA	V_O	–55°C	±11	R_L = 100Ω	9.9		V
6	Output Voltage I_O= 1A	V_O	–55°C	±4.8	R_L = 3Ω	2.8		V
6	Stability/Noise	E_N	–55°C	±15	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1.0	mV
6	Slew Rate	SR	–55°C	±15	R_L = 500Ω	.5		V/µS
6	Open Loop Gain	A_{OL}	–55°C	±15	R_L = 500Ω, F = 10Hz	75		dB
6	Common-mode Rejection	CMR	–55°C	±17	R_L = 500Ω, V_{CM} = ±14V	60		dB
5	Output Voltage I_O= 1A	V_O	125°C	±4.8	R_L = 3Ω	2.8		V
5	Output Voltage I_O= 100mA	V_O	125°C	±11	R_L = 100Ω	9.9		V
5	Output Voltage I_O= 750mA	V_O	125°C	±4.0	R_L = 3Ω	2.25		V
5	Stability/Noise	E_N	125°C	±15	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1.0	mV
5	Slew Rate	SR	125°C	±15	R_L = 500Ω	.5		V/µS
5	Open Loop Gain	A_{OL}	125°C	±15	R_L = 500Ω, F = 10Hz	75		dB
5	Common-mode Rejection	CMR	125°C	±17	R_L = 500Ω, V_{CM} = ±14V	60		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

Dual Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- RoHS COMPLIANT
- LOW COST
- WIDE BANDWIDTH - 1.1 Mhz
- HIGH OUTPUT CURRENT - 2.5A (Combined)
- WIDE COMMON MODE RANGE Includes negative supply
- WIDE SUPPLY VOLTAGE RANGE Single supply: 5V to 40V
  Split supplies: ± 2.5V to ± 20V
- LOW QUIESCIENT CURRENT
- VERY LOW DISTORTION

APPLICATIONS

- HALF AND FULL BRIDGE MOTOR DRIVERS
- AUDIO POWER AMPLIFIER
- IDEAL FOR SINGLE SUPPLY SYSTEMS
  5V Peripherals, 12V Automotive, 28V Avionic

PACKAGING OPTIONS

- 7 TO-220 Plastic Package (PA75CD)
- 7 TO-220 with Staggered Lead Form (PA75CX)
- 7 DDPAK Surface Mount Package (PA75CC)

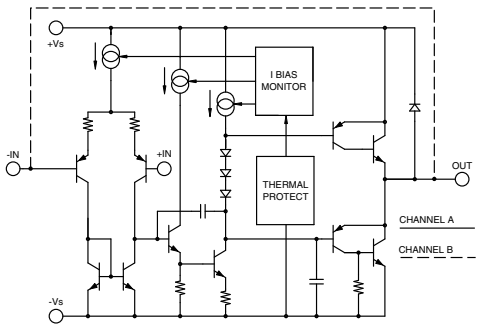
DESCRIPTION

The amplifier design consists of dual power op amp on a single monolithic die. Side B of the dual monolithic is configured as a unity gain buffer to increase the current capability of the master side A. The use of two PA75 amplifiers provides a cost-effective solution to applications where multiple amplifiers are required or a bridge configuration is needed. Very low harmonic distortion of .02% THD and low I_Q makes the PA75 a good solution for power audio applications.

The PA75 is available in three standard package designs. The surface mount version of the PA75, the PA75CC, is an industry standard non-hermetic plastic 7-pin DDPAK. The through hole version of the PA75, the PA75CD and PA75CX, are industry standard non-hermetic plastic 7-pin TO-220 packages. The PA75CX is staggered lead formed and offers standard 100 mil spacing. This allows for easier PC board layout. (Please refer to the CX lead form package drawing for dimension of the PA75CX).

The monolithic amplifier is directly attached to the metal tabs of the PA75CC, PA75CD, and PA75CX. The metal tabs of the packages are directly tied to -Vs.

EQUIVALENT SCHEMATIC ONE CHANNEL



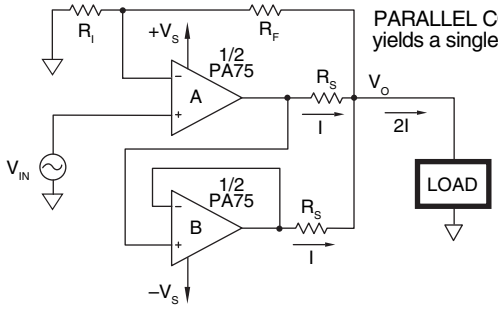
7 PIN DDPAK
PACKAGE STYLE CC

7 PIN TO220
STAGGERED LEADS
PACKAGE STYLE CX

7 PIN TO220
PACKAGE STYLE CD

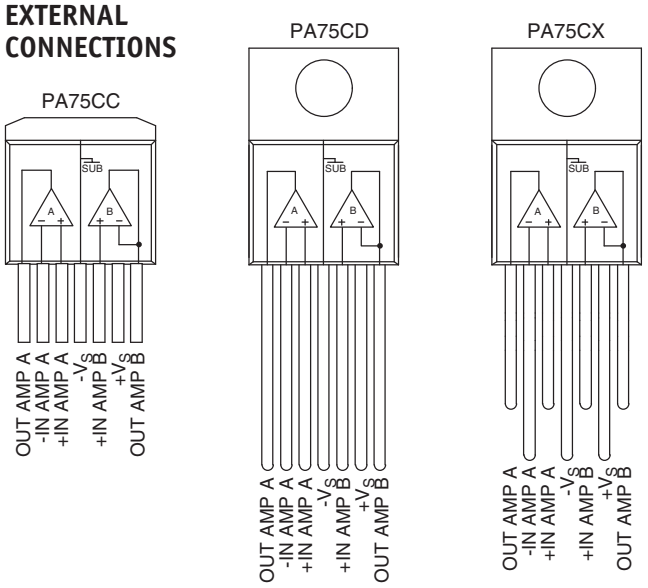
TYPICAL APPLICATION

Ref: APPLICATION NOTES 8, 20, 26



Combining the power op amp (master channel A) and the unity gain buffer (slave channel B) in a parallel connection yields a single 2.5A amplifier. RI and RF can set up channel A for the required gain for the overall circuit. Small values of R_S (sense resistors) are used on the outputs to improve current sharing characteristics. The master amplifier can be configured in inverting or non-inverting gain configurations.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

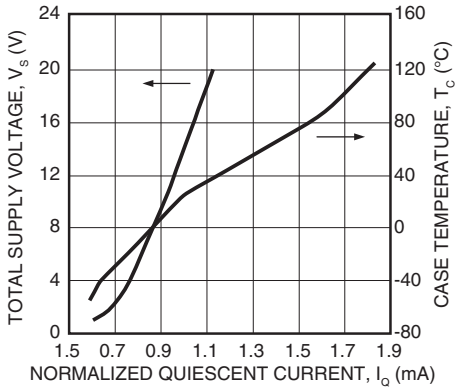
SUPPLY VOLTAGE, total	5V to 40V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal, (per amplifier)	19.5W
POWER DISSIPATION, internal (both amplifiers)	28.6W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S$–0.5V
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder—10 sec max	220°C
TEMPERATURE RANGE, storage	–55°C to 150°C
OPERATING TEMPERATURE RANGE, case	–40°C to 125°C

SPECIFICATIONS

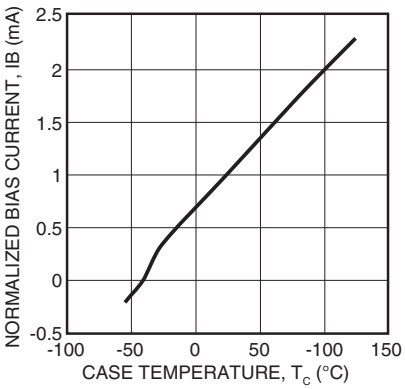
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			1	15	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20		µV/°C
BIAS CURRENT, initial			100	500	nA
COMMON MODE RANGE	Full temperature range	$-V_S$		$+V_S$–1.3	V
COMMON MODE REJECTION, DC	Full temperature range	60	90		dB
POWER SUPPLY REJECTION	Full temperature range	60	90		dB
CHANNEL SEPARATION	I_{OUT} = 500mA, f = 1kHz	50	68		dB
INPUT NOISE VOLTAGE	R_S = 100Ω, f = 1 to 100kHz		22		nV/√Hz
GAIN					
OPEN LOOP GAIN	Full temperature range	89	100		dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB	0.9	1.4		MHz
PHASE MARGIN	Full temperature range, R_L = 2KΩ, C_L = 100pF		65		°
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6		kHz
OUTPUT					
CURRENT, peak				1.5	A
SLEW RATE		1	1.4		V/µs
VOLTAGE SWING	Full Temperature Range, I_O = 100mA	$\|V_S\|$ - 1.1	$\|V_S\|$ - .8		V
VOLTAGE SWING	Full Temperature Range, I_O = 1A	$\|V_S\|$ - 1.8	$\|V_S\|$ - 1.4		V
HARMONIC DISTORTION	A_V = 1, R_2 = 50Ω, V_O = .5V_{RMS}, f = 1kHz		.02		%
POWER SUPPLY					
VOLTAGE, V_{SS}[3]		5	30	40	V
CURRENT, quiescent, total			8	10	mA
THERMAL					
RESISTANCE,DC junction to case (single)			5.84	6.42	°C/W
RESISTANCE,AC junction to case (single)			4.38	4.81	°C/W
RESISTANCE,DC junction to case (both)			3.97	4.36	°C/W
RESISTANCE,AC junction to case (both)			2.98	3.27	°C/W
RESISTANCE,junction to air (CD,CX)			60		°C/W
RESISTANCE,junction to air (CC)[4]			27		°C/W
TEMPERATURE RANGE,case	Meets full range specifications	–25		85	°C

NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $\pm V_S$ = ±15V, T_C = 25°C.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Heat tab attached to 3/32" FR-4 board with 2oz. copper. Topside copper area (heat tab directly attached) = 1000 sq. mm, backside copper area = 2500 sq. mm, board area = 2500 sq. mm.

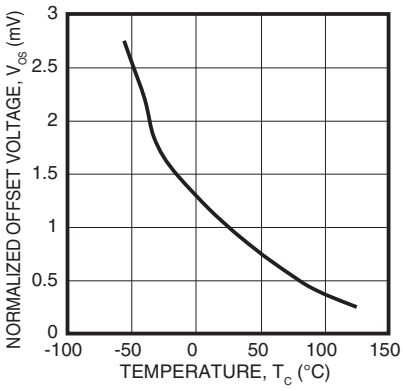
QUIESCENT CURRENT



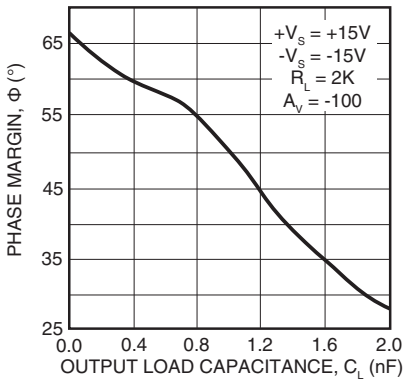
BIAS CURRENT



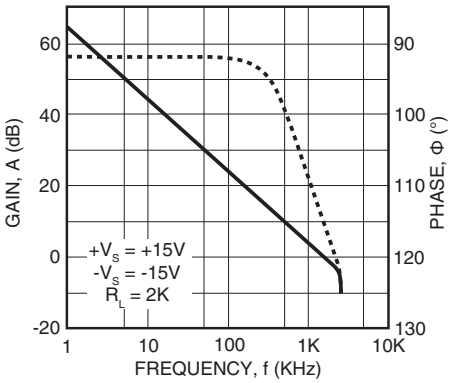
OFFSET VOLTAGE



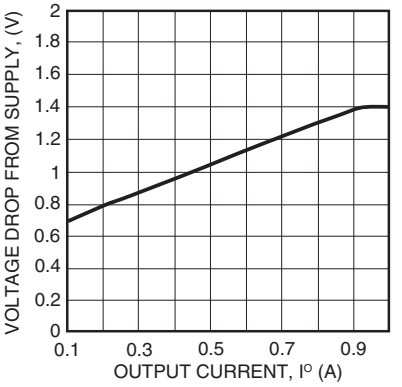
PHASE MARGIN vs. OUTPUT LOAD CAPACITANCE



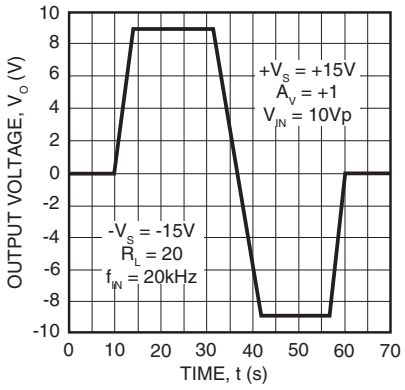
VOLTAGE GAIN & PHASE vs. FREQUENCY



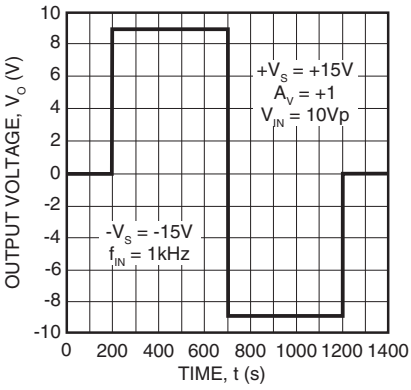
OUTPUT VOLTAGE SWING



PULSE RESPONSE



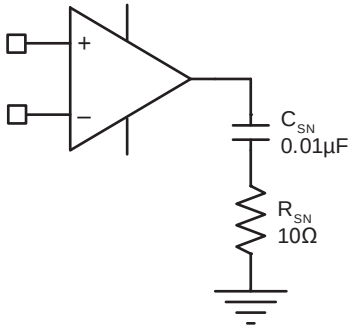
PULSE RESPONSE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heatsinking, mounting, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, heatsink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

STABILITY CONSIDERATIONS

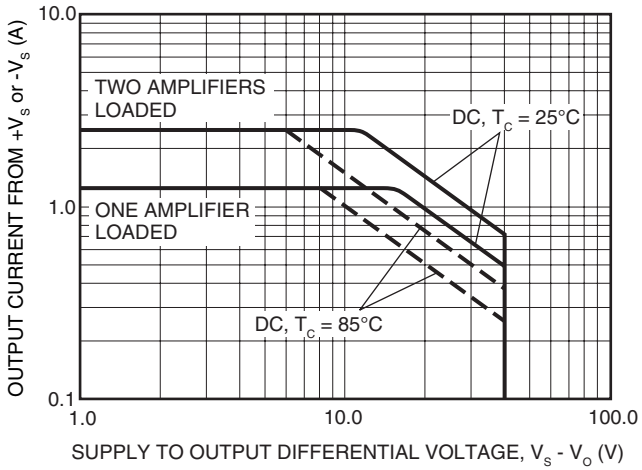


All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions. For applications with load current exceeding 300ma, oscillation may appear. The oscillation may occur only with the output voltage swing at the negative or positive half cycle. Under most operating and load conditions acceptable stability can be achieved by providing a series RC snubber network connected from the output to ground. The recommended component values of the of the network are, R_{SN} = 10Ω and C_{SN} = 0.01µF. Please refer to Application Note 1 for further details.

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

SOA



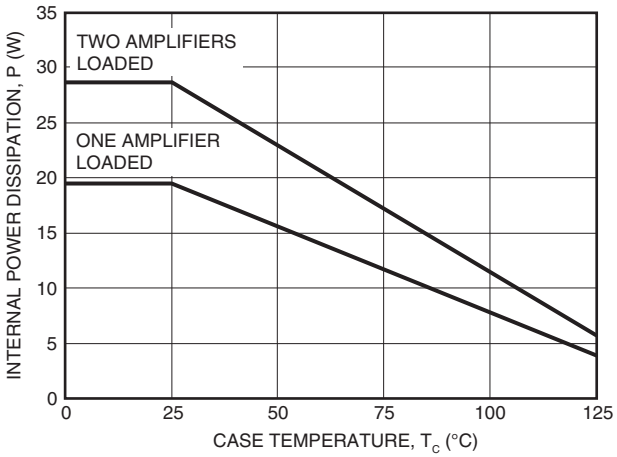
THERMAL CONSIDERATIONS

The PA75CD and CX have a large exposed copper heat tab to which the monolithic is directly attached. The PA75CD and CX may require a thermal washer, which is electrically insulating since the tab is directly tied to -VS. This can result in a thermal impedance RCS of up to 1˚C/W or greater.

The PA75CC has a large exposed integrated copper heatslug to which the monolithic is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area of the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA75CC. Solder connection to an area of 1 to 2 square inches of foil is required for minimal power applications

Where the PA75CC is used in higher power applications, it is necessary to use surface mount techniques of heatsinking. Surface mount techniques include the use of a surface mount fan in combination with a surface mount heatsink on the backside of the FR4/ PC board with through hole thermal vias. Other highly thermal conductive substrate board materials are available for maximum heat sinking.

POWER DERATING



MOUNTING PRECAUTIONS

1. Always use a heat sink. Even unloaded the PA75 can dissipate up to .4 watts.
2. Avoid bending the leads. Such action can lead to internal damage.
3. Always fasten the tab of the CD and CX package to the heat sink before the leads are soldered to fixed terminals.
4. Strain relief must be provided if there is any probability of axial stress to the leads.

High Voltage Power Operational Amplifier

The function of the discontinued PA26 can be replaced with a pair of PA75 amplifiers. The basic technique is to connect the op amp and the buffer sections of the PA75 in parallel to perform as one op amp of the PA26 did. A second PA75 then takes on the duties of the second op amp of the PA26. A new printed circuit layout will be required. While the thermal rating of existing PA26 heatsinking will be adequate for the pair of PA75 amplifiers, and most applications will need modification to heatsink mounting design.

BASIC PARALLEL OPERATION NOT UTILIZING VBOOST OR ISENSE FUNCTIONS.

This substitution requires for each half of the PA26 circuit:

1. Increase the wattage rating of the original snubber resistor to 1.25W or more (the recommended value is still 1Ω) to become a sharing resistor.
2. Tie the buffer input directly to the op amp output.
3. Add a second 1 ohm 1.25W sharing resistor for the PA75 buffer section.
4. To the junction of the sharing resistors and original snubber capacitor, connect the output and feedback.
5. If desired, the original snubber capacitor may be reduced to 10nF (this will possibly save space).

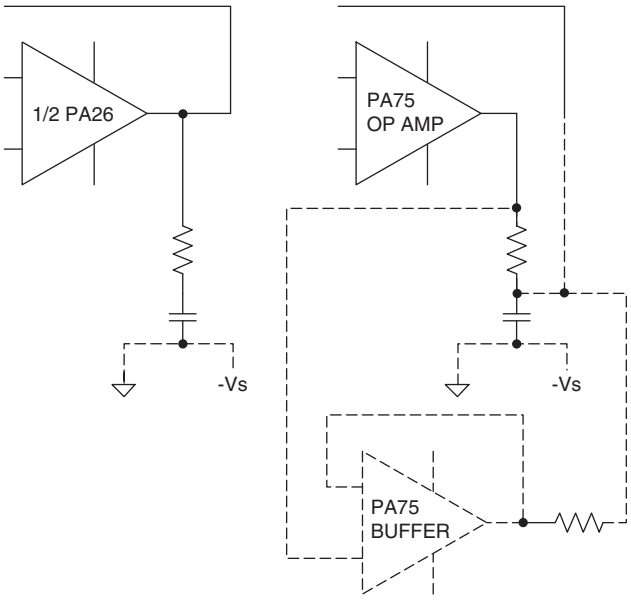


Figure 1. Basic substitution

When this circuit was tested, a single 0.47µF supply bypass capacitor from +Vs to -Vs proved satisfactory for the second PA75 amplifier, even for dual supplies. With 1Ω share resistors, quiescent current was less than the typical for a PA26 and the output voltage swing at 2.5A was equal to PA26.

FOR APPLICATIONS WHERE THE ISENSE FUNCTION WAS IMPLEMENTED

Very nearly equal performance can be obtained because the total quiescent current of the PA75 is roughly equal to the output stage current only of the PA26.

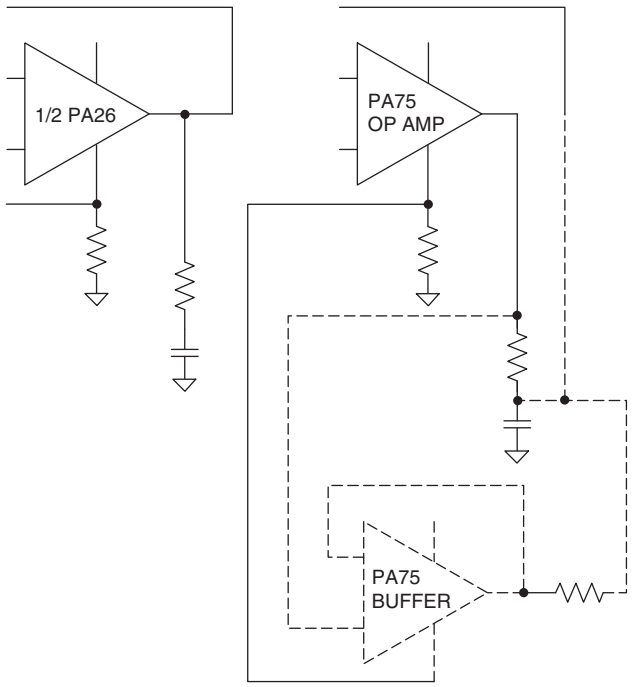


Figure 2. Substitution with Isense

FOR APPLICATIONS WHERE VBOOST WAS IMPLEMENTED

As the PA75 actually swings closer to the rail at 1.25A than the PA26 does at 2.5A, the advantage of the original Vboost circuit can be obtained with PA75 even without Vboost pins. The Vboost capacitors and diodes can be eliminated, the old Vboost pin tied to +Vs and the sharing resistors reduced to 0.5Ω (0.75 W is adequate) in the basic substitution of Figure 1. With the phase shift of the current buffer amplifier generating circulating currents through the two 0.5Ω share resistors, no load supply current will increase as high voltage and high frequency output signals are driven. The test circuit with two PA75 amplifiers drew 215mA while driving ±19Vpeak sine waves at 15KHz. This current will be less as frequency or peak output swing is reduced: Half the frequency will reduce it by almost 2:1; half the amplitude will also reduce it by almost 2:1.

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- A Unique (Patent Pending) Technique for Very Low Quiescent Current
- Over 350 V/µs Slew Rate
- Wide Supply Voltage
  - Single Supply: 20V To 350V
  - Split Supplies: ± 10V To ± 175V
- Output Current – 150mA Cont.; 200mA Pk
- Up to 23 Watt Dissipation Capability
- Over 200 kHz Power Bandwidth

APPLICATIONS

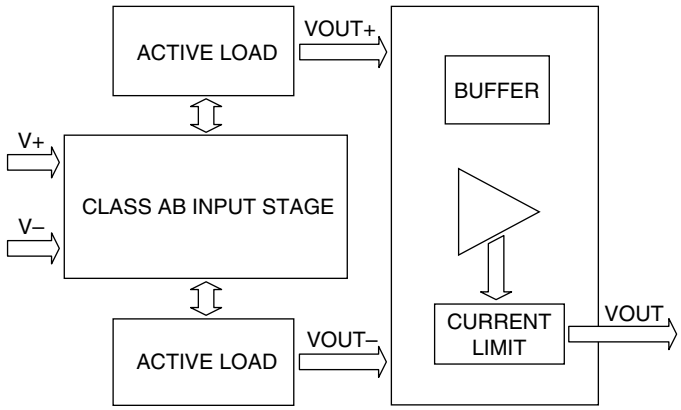
- Piezoelectric Positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

DESCRIPTION

The PA78 is a high voltage, high speed, low idle current op-amp capable of delivering up to 200mA peak output current. Due to the dynamic biasing of the input stage, it can achieve slew rates over 350V/µs, while only consuming less than 1mA of idle current. External phase compensation allows great flexibility for the user to optimize bandwidth and stability.

The output stage is protected with user selected current limit resistor. For the selection of this current limiting resistor, pay close attention to the SOA curves for each package type. Proper heatsinking is required for maximum reliability.

BLOCK DIAGRAM



20–Pin PSOP
PACKAGE STYLE DK

12–Pin SIP
PACKAGE STYLE EU
LEAD FORM EW

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$				350	V
OUTPUT CURRENT, peak (200ms), within SOA				200	mA
POWER DISSIPATION, internal, DC	DK Pkg.			14	W
POWER DISSIPATION, internal, DC	EU Pkg.			23	W
INPUT VOLTAGE, differential			−15	16	V
INPUT VOLTAGE, common mode			$-V_S$	$+V_S$	V
TEMPERATURE, pin solder, 10s	EU Pkg.			260	°C
TEMPERATURE, junction	(Note 2)			150	°C
TEMPERATURE RANGE, storage			−55	125	°C
OPERATING TEMPERATURE, case			−40	125	°C

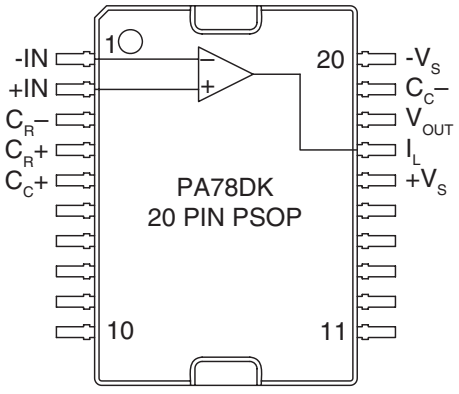
SPECIFICATIONS

Parameter		Test Conditions	Min	Typ	Max	Units
INPUT						
OFFSET VOLTAGE	EU Pkg.		-25	8	25	mV
OFFSET VOLTAGE	DK Pkg.		-40	8	40	mV
OFFSET VOLTAGE vs. temperature		0 to 125°C (Case Temperature)		-63		µV/°C
OFFSET VOLTAGE vs. supply					32	µV/V
BIAS CURRENT, initial				8.5	200	pA
OFFSET CURRENT, initial				12	400	pA
INPUT RESISTANCE, DC				10^8		Ω
COMMON MODE VOLTAGE RANGE, pos.				$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.				$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC			90	118		dB
NOISE		700KHz		418		µV RMS
NOISE, V_O NOISE				500		nV/√Hz
GAIN						
OPEN LOOP @ 1Hz			89	120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz					1	MHz
PHASE MARGIN		Full temperature range		50		°
OUTPUT						
VOLTAGE SWING		I_O = 10mA		$\|V_S\|$ - 2		V
VOLTAGE SWING		I_O = 100mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
VOLTAGE SWING		I_O = 150mA		$\|V_S\|$ - 10		V
CURRENT, continuous, DC			150			mA
SLEW RATE		**Package Tab connected to GND**	100	350		V/µS
SETTLING TIME, to 0.1%		2V Step		1		µS
POWER BANDWIDTH, $300V_{P-P}$		$+V_S$ = 160V, $-V_S$ = -160V		200		kHz
OUTPUT RESISTANCE, No load		R_{CL} = 6.2Ω		44		Ω

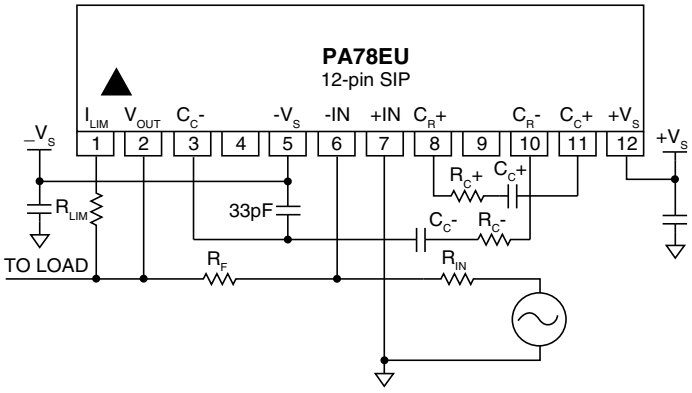
Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE		±10	±150	±175	V
CURRENT, quiescent (Note 5)	±150V Supply	0.2	0.7	2.5	mA
THERMAL					
RESISTANCE, DC, junction to case (PA78EU)	Full temperature range		5.5		ºC/W
RESISTANCE, DC, junction to air (PA78EU)	Full temperature range		12.21		ºC/W
RESISTANCE, DC, junction to case (PA78DK)	Full temperature range		8.3	9.1	ºC/W
RESISTANCE, DC, junction to air (PA78DK) (Note 6)	Full temperature range		25		ºC/W
RESISTANCE, DC, junction to air (PA78DK) (Note 7)	Full temperature range		19.1		ºC/W
TEMPERATURE RANGE, case		-40		125	ºC

NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $–V_S$ denote the positive and negative supply voltages of the output stage.
4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
5. Supply current increases with signal frequency. See graph on page 4.
6. Rating applies when the heatslug of the DK package is soldered to a minimum of 1 square inch foil area of a printed circuit board.
7. Rating applies with the JEDEC conditions outlined in the Heatsinksing section of this datasheet.

EXTERNAL CONNECTIONS
DK Package

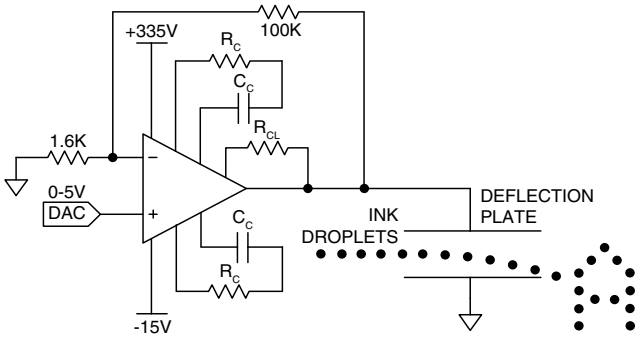


EXTERNAL CONNECTIONS
EU Package



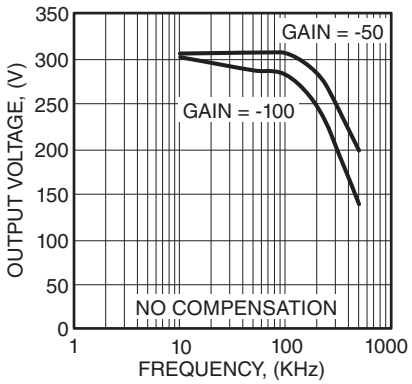
TYPICAL APPLICATION CIRCUIT

The PA78 is ideally suited for driving continuous drop ink jet printers, in both piezo actuation and deflection applications. The high voltage of the amplifier creates an electrostatic field on the deflection plates to control the position of the ink droplets. The rate at which droplets can be printed is directly related to the rate at which the amplifier can drive the plate to a different electrostatic field strength.

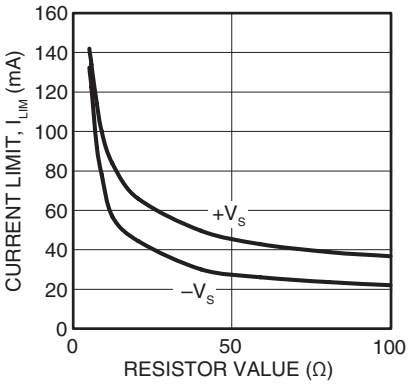


TYPICAL PERFORMANCE GRAPHS

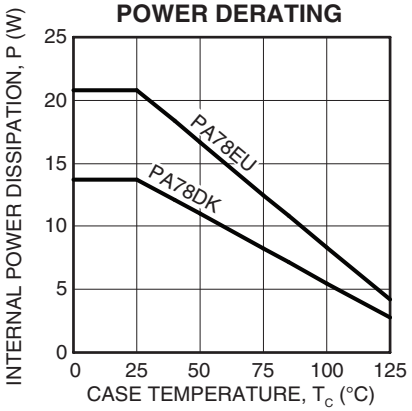
POWER RESPONSE



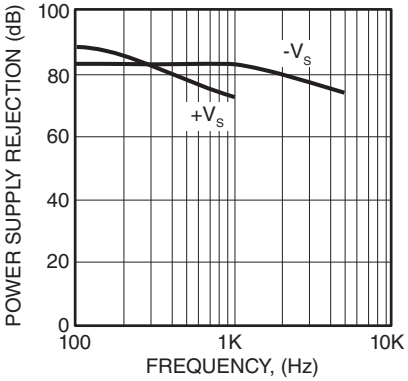
CURRENT LIMIT



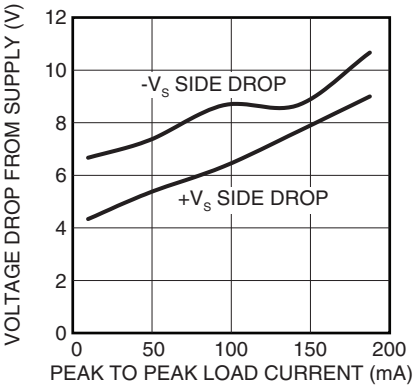
POWER DERATING



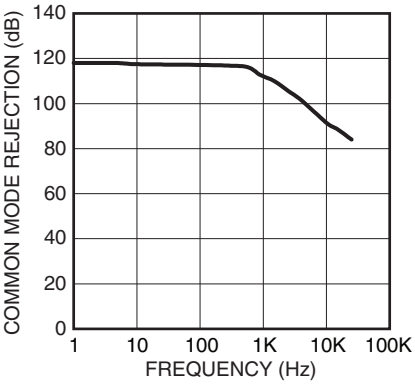
POWER SUPPLY REJECTION



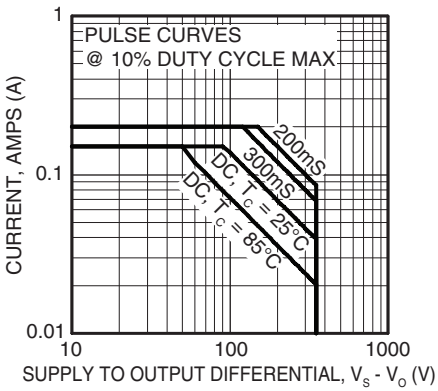
OUTPUT VOLTAGE SWING



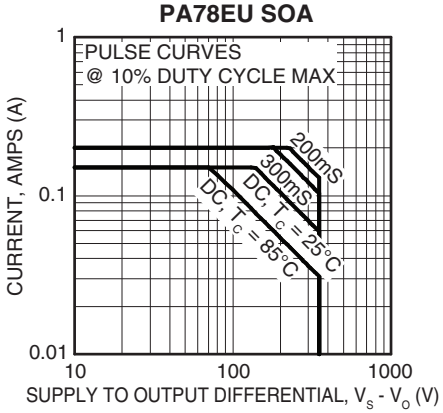
COMMON MODE REJECTION



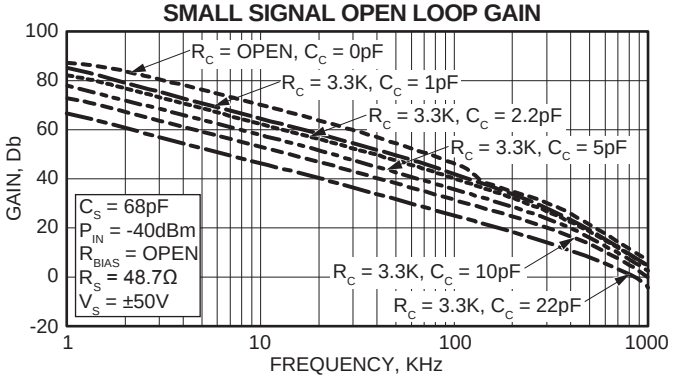
PA78DK SOA



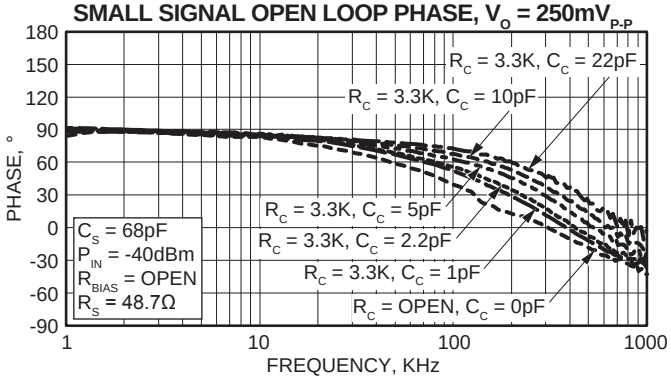
PA78EU SOA



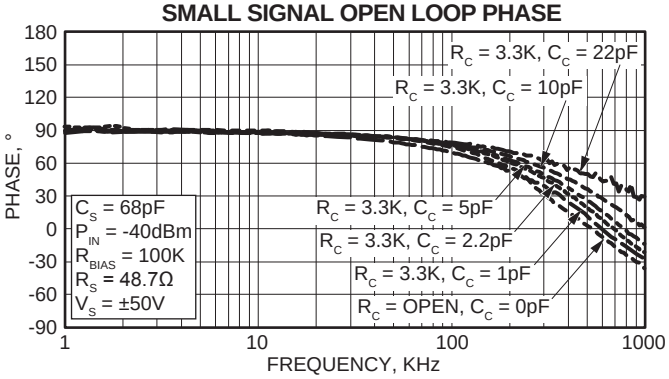
SMALL SIGNAL OPEN LOOP GAIN



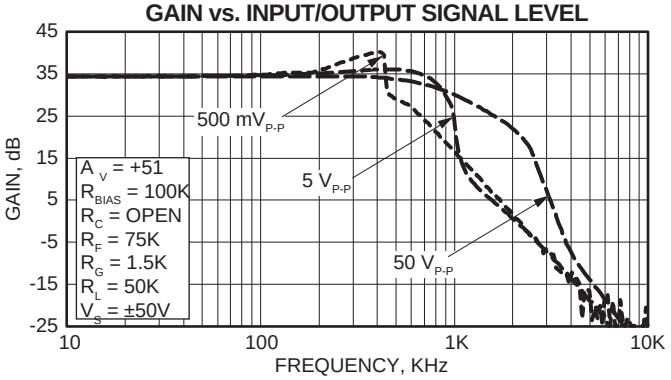
SMALL SIGNAL OPEN LOOP PHASE, V_O = 250mV$_{P-P}$



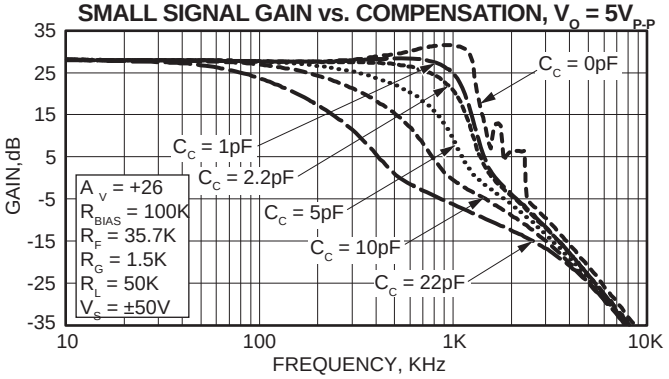
SMALL SIGNAL OPEN LOOP PHASE



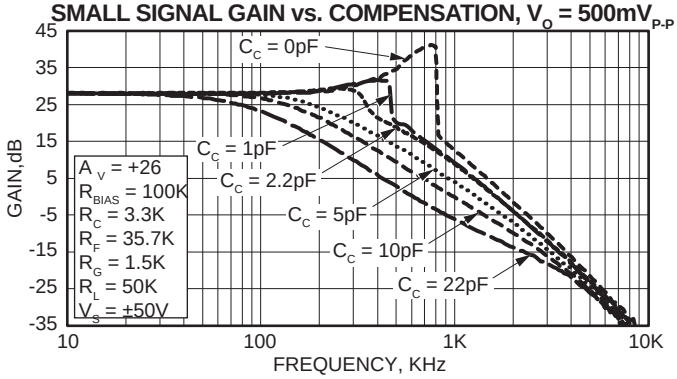
GAIN vs. INPUT/OUTPUT SIGNAL LEVEL



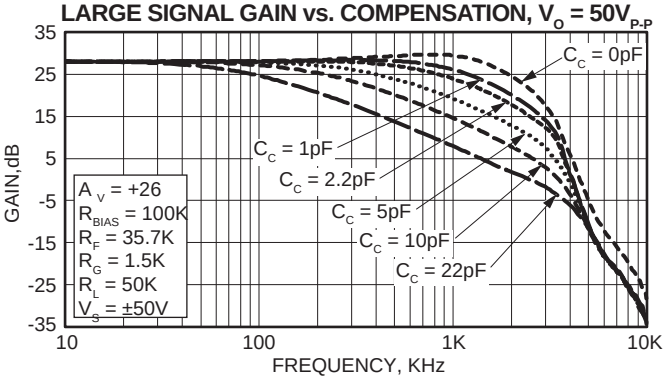
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 5V$_{P-P}$



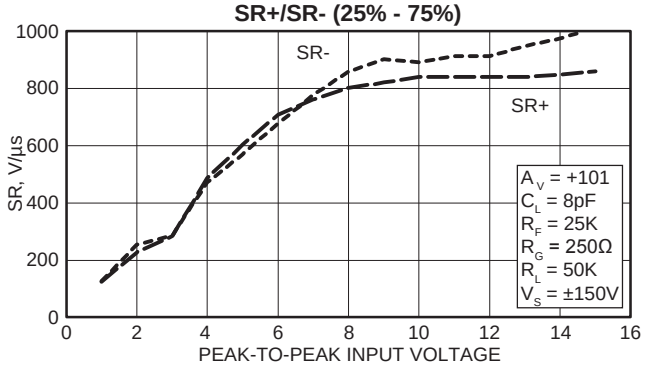
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 500mV$_{P-P}$



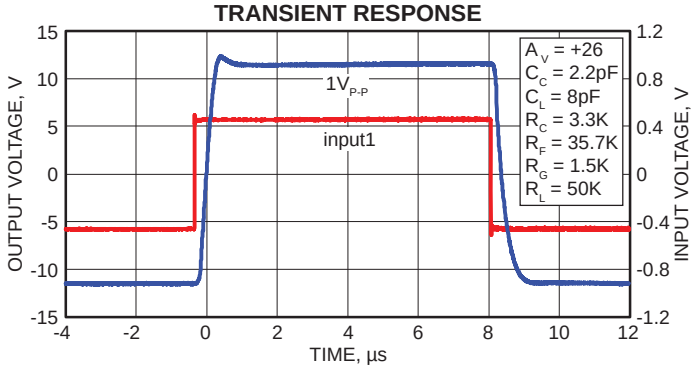
LARGE SIGNAL GAIN vs. COMPENSATION, V_O = 50V$_{P-P}$



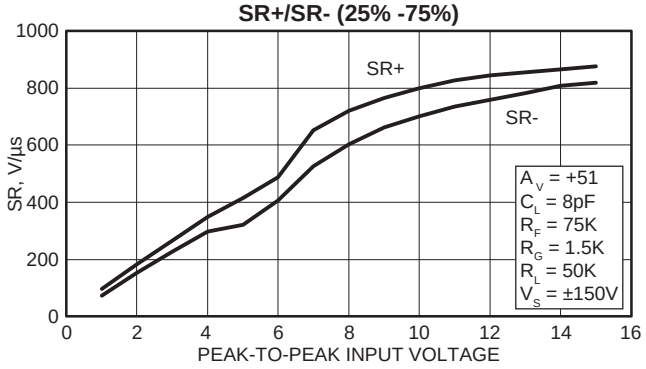
SR+/SR- (25% - 75%)



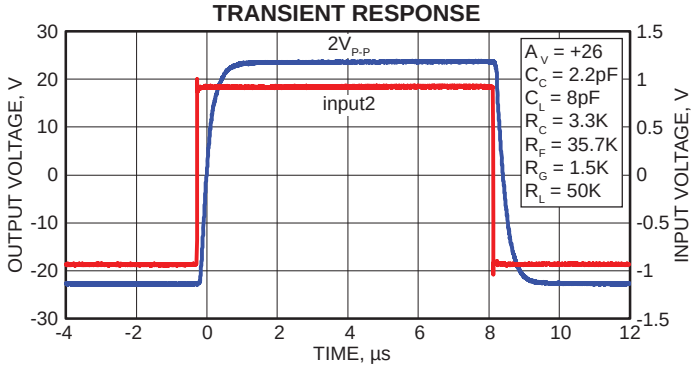
TRANSIENT RESPONSE



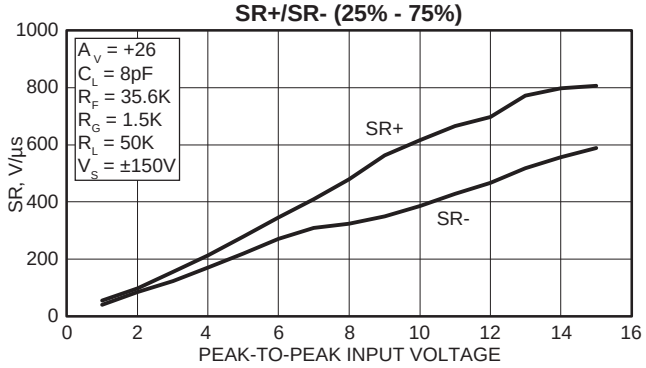
SR+/SR- (25% -75%)



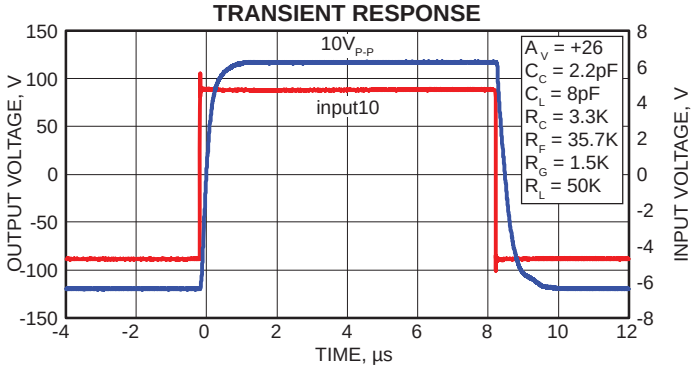
TRANSIENT RESPONSE



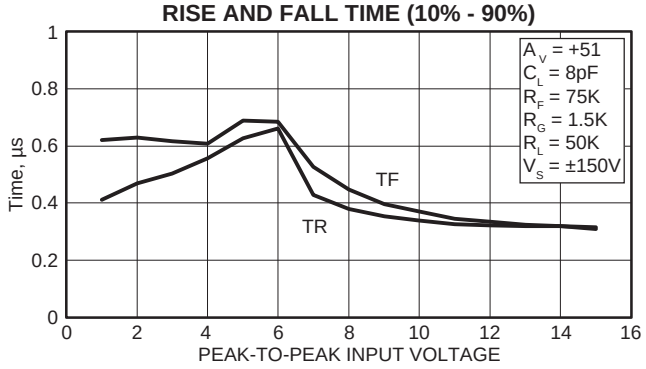
SR+/SR- (25% - 75%)



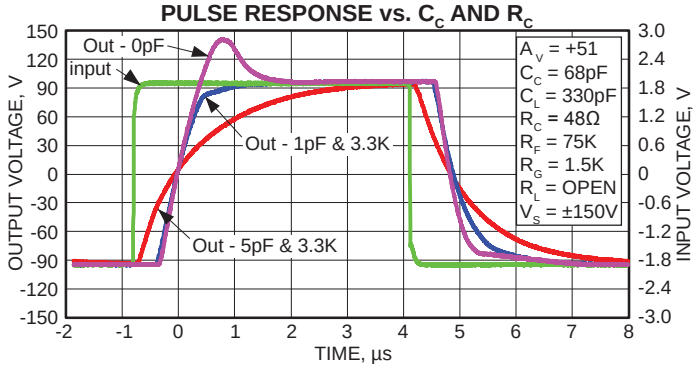
TRANSIENT RESPONSE



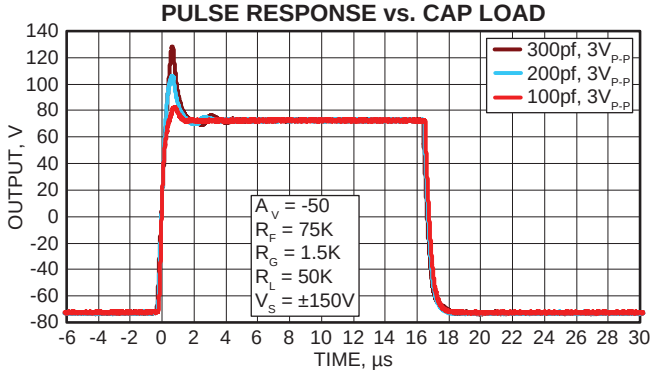
RISE AND FALL TIME (10% - 90%)



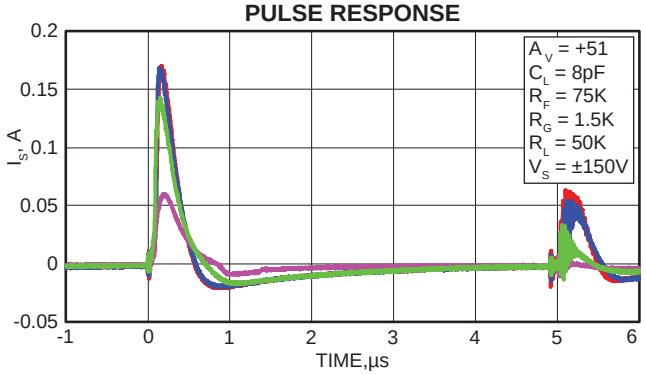
PULSE RESPONSE vs. C_C AND R_C



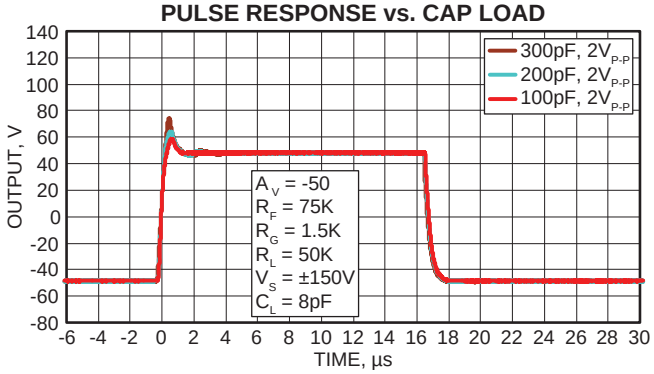
PULSE RESPONSE vs. CAP LOAD



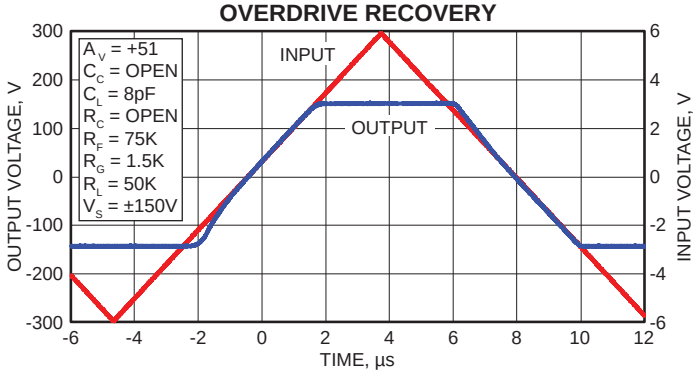
PULSE RESPONSE



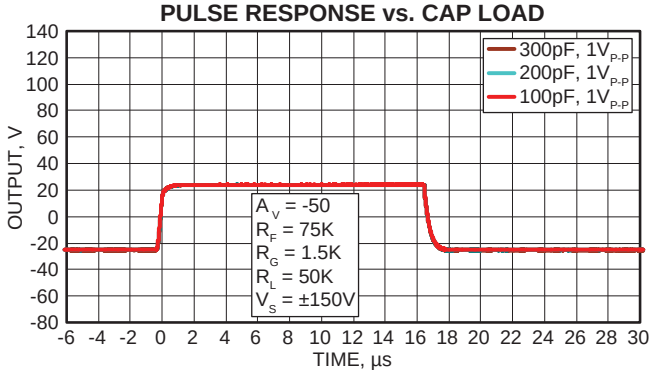
PULSE RESPONSE vs. CAP LOAD



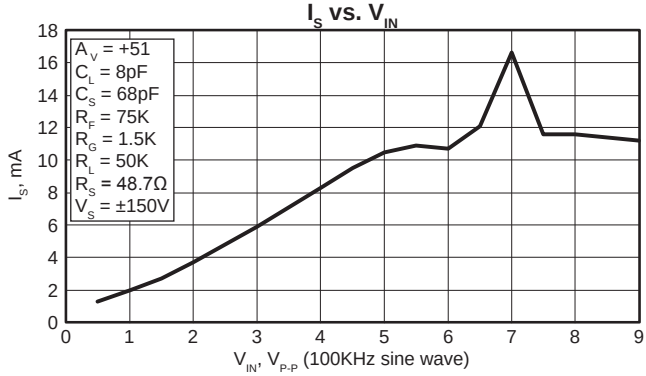
OVERDRIVE RECOVERY



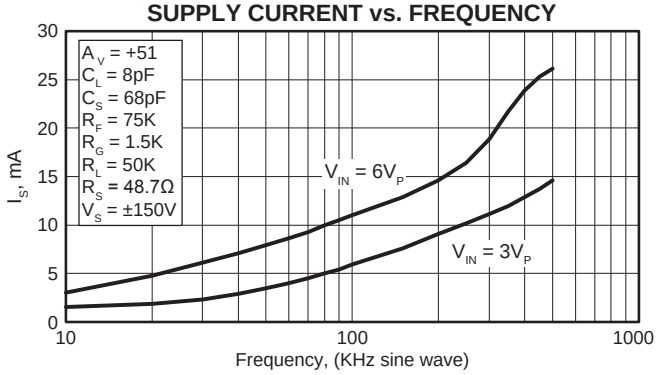
PULSE RESPONSE vs. CAP LOAD



I_S vs. V_{IN}



SUPPLY CURRENT vs. FREQUENCY

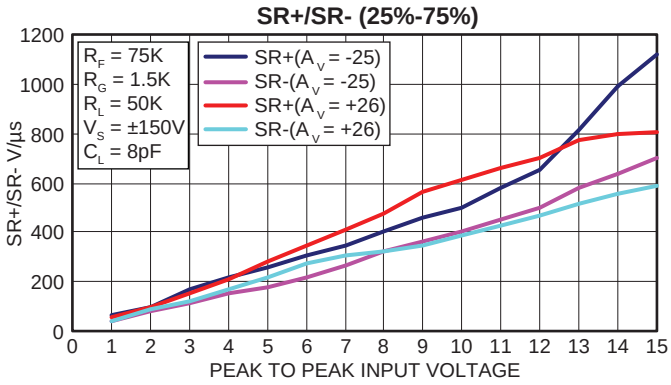


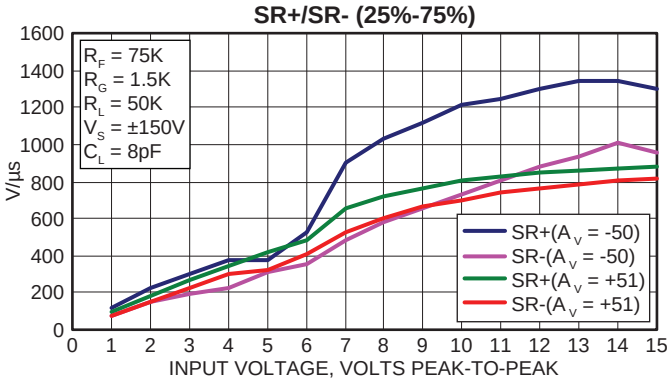
GENERAL

Please read Application note 1 “General operating considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, and current limit. There you will also find a complete application notes library, technical seminar workbook, and evaluation kits.

THEORY OF OPERATION

The PA78 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.





SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA78 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA78 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA78. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in

standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, R_{BIAS}, between C_C- and V_S+. The size of R_{BIAS} will depend upon the application but 500µA (50V V+ supply/100K) of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA78 is externally compensated and performance can be optimized to the application. Unlike the R_{BIAS} technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the tradeoffs between bandwidth and stability. Due to the unique design of the PA78, two symmetric compensation networks are required. The compensation capacitor Cc must be rated for a working voltage of the full operating supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature.

The PA78 requires an external 33pF capacitor between C_C- and $-V_S$ to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from $1V_{P-P}$ to $15V_{P-P}$, the slew rate increases from 50V/µs to well over 350V/µs.

Notice the knee in the Rise and Fall times plot, at approximately $6V_{P-P}$ input voltage. Beyond this point the output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA78 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current vs. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.

The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.

CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The minimum practical value for R_{LIM} is about 12Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for R_{LIM} in the intended application. Current limit may not protect against short circuit conditions with supply voltages over 200V.

LAYOUT CONSIDERATIONS

The PA78 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1µF capacitor to GND is also sufficient if a DC connection is undesirable

Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of LC interactions and oscillations.

The PA78DK package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heat slug to a 1 square inch foil area on the printed circuit board will result in improved thermal performance of 25ºC/W. In order to improve the thermal performance, multiple metal layers in the printed circuit board are recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85ºC.

The junction to ambient thermal resistance of the DK package can achieve a 19.1ºC/W rating by using the PCB conditions outlined in JEDEC standard: (JESD51–5):

PCB Conditions:

- PCB Layers = 4L, Copper, FR–4
- PCB Dimensions = 101.6 x 114.3mm
- PCB Thickness = 1.6mm

Conditions:

- Power dissipation = 2 watt
- Ambient Temperature = 55ºC

ELECTROSTATIC DISCHARGE

Like many high performance MOSFET amplifiers, the PA78 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- A Unique (Patent Pending) Technique for Very Low Quiescent Current
- Over 350 V/µs Slew Rate
- Wide Supply Voltage
  - Single Supply: 20V To 350V
  - Split Supplies: ± 10V To ± 175V
- Output Current – Per Amplifier – 150mA Cont.; 200mA Pk
- Up to 26 Watt Dissipation Capability (Dual)
- Over 200 kHz Power Bandwidth

APPLICATIONS

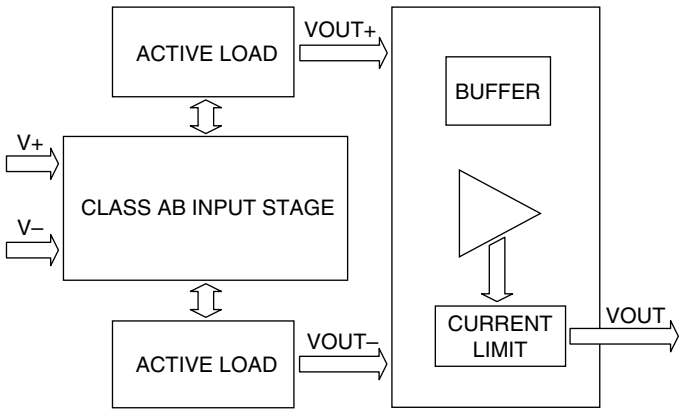
- Piezoelectric Positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

DESCRIPTION

The PA79 is a high voltage, high speed, low idle current op-amp capable of delivering up to 200mA peak output current. Due to the dynamic biasing of the input stage, it can achieve slew rates over 350V/µs, while only consuming less than 1mA of idle current. External phase compensation allows great flexibility for the user to optimize bandwidth and stability.

The output stage is protected with user selected current limit resistor. For the selection of this current limiting resistor, pay close attention to the SOA curves for each package type. Proper heatsinking is required for maximum reliability.

BLOCK DIAGRAM



20–Pin PSOP
PACKAGE STYLE DK

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			350	V
OUTPUT CURRENT, peak (200ms), within SOA			200	mA
POWER DISSIPATION, internal, DC Single			14	W
POWER DISSIPATION, internal, DC Dual			26	W
INPUT VOLTAGE, differential		−15	15	V
INPUT VOLTAGE, common mode		$-V_S$	$+V_S$	V
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−55	125	°C
OPERATING TEMPERATURE, case		−40	125	°C

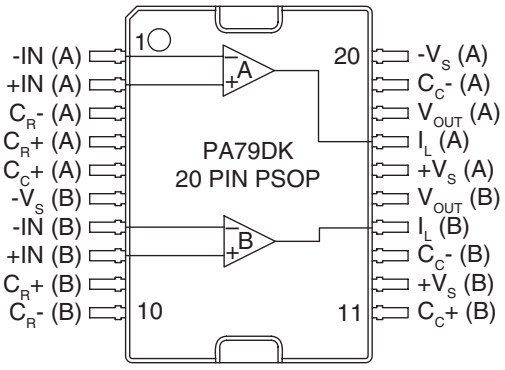
SPECIFICATIONS

Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE		-40	8	40	mV
OFFSET VOLTAGE vs. temperature	0 to 125°C (Case Temperature)		-63		µV/°C
OFFSET VOLTAGE vs. supply				32	µV/V
BIAS CURRENT, initial			8.5	200	pA
OFFSET CURRENT, initial			12	400	pA
INPUT RESISTANCE, DC			10^8		Ω
COMMON MODE VOLTAGE RANGE, pos.			$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC		90	118		dB
NOISE	700KHz		418		µV RMS
NOISE, V_O NOISE			500		nV/√Hz
GAIN					
OPEN LOOP @ 1Hz		89	120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
OUTPUT					
VOLTAGE SWING	I_O = 10mA		$\|V_S\|$ - 2		V
VOLTAGE SWING	I_O = 100mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
VOLTAGE SWING	I_O = 150mA		$\|V_S\|$ - 10		V
CURRENT, continuous, DC		150			mA
SLEW RATE	**Package Tab connected to GND**	100	350		V/µS
SETTLING TIME, to 0.1%	5V Step (No Compensation)		1		µS
POWER BANDWIDTH, $300V_{P-P}$	$+V_S$ = 160V, $-V_S$ = -160V		200		kHz
OUTPUT RESISTANCE, No load	R_{CL} = 6.2Ω		44		Ω
POWER SUPPLY					
VOLTAGE		±10	±150	±175	V
CURRENT, quiescent (Note 5)	±150V Supply	0.2	0.7	2.5	mA

Parameter	Test Conditions	Min	Typ	Max	Units
THERMAL					
RESISTANCE, DC, junction to case, Dual (Note 8)	Full temperature range		5.5		°C/W
RESISTANCE, DC, junction to case, Single	Full temperature range		8.3	9.1	°C/W
RESISTANCE, DC, junction to air, Dual	Full temperature range		25		°C/W
RESISTANCE, DC, junction to air, Single	Full temperature range		19.1		°C/W
TEMPERATURE RANGE, case		-40		125	°C

NOTES: 1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative supply voltages of the output stage.
4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
5. Supply current increases with signal frequency. See graph on page 4. Applies to each amplifier.
6. Rating applies when the heatslug of the DK package is soldered to a minimum of 1 square inch foil area of a printed circuit board.
7. Rating applies with the JEDEC conditions outlined in the Heatsinksing section of this datasheet.
8. Rating applies when power dissipation is equal in two amplifiers.

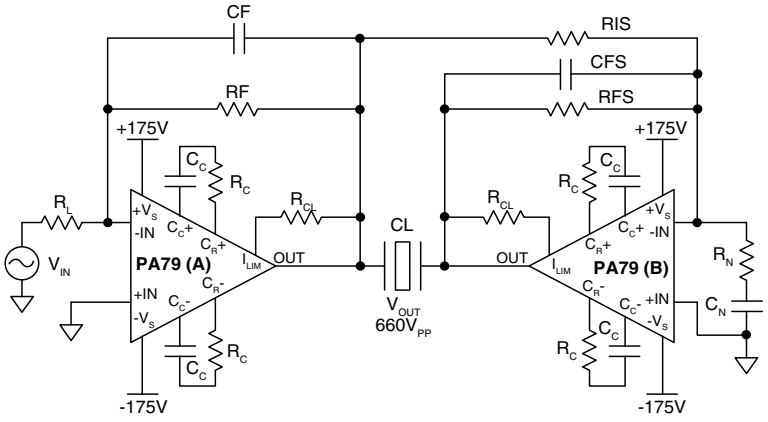
EXTERNAL CONNECTIONS



NOTES:
1. The package heat slug needs to be connected to a stable reference such as gnd for high slew rates. Please refer to special considerations section for details.
2. Supply bypassing required for $-V_S$ and $+V_S$.
3. For C_C and R_C values refer to power supply biasing section.
4. Dimple and ESD triangle denotes pin 1.

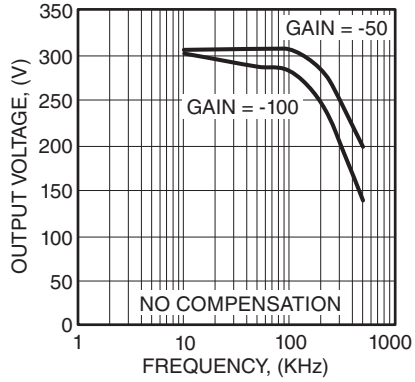
TYPICAL APPLICATION CIRCUIT

The PA79 is ideally suited for driving continuous drop ink jet printers, in both piezo actuation and deflection applications. The high voltage of the amplifier creates an electrostatic field on the deflection plates to control the position of the ink droplets. The rate at which droplets can be printed is directly related to the rate at which the amplifier can drive the plate to a different electrostatic field strength.

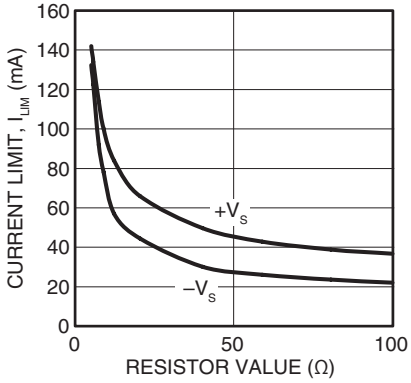


TYPICAL PERFORMANCE GRAPHS

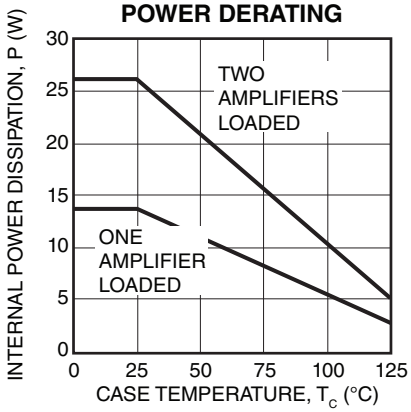
POWER RESPONSE



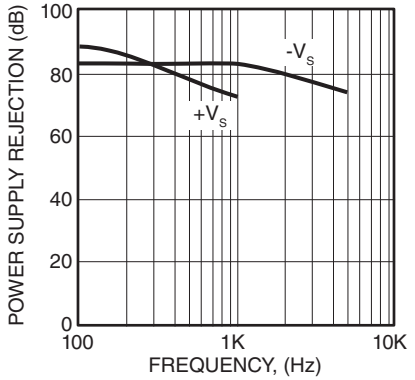
CURRENT LIMIT



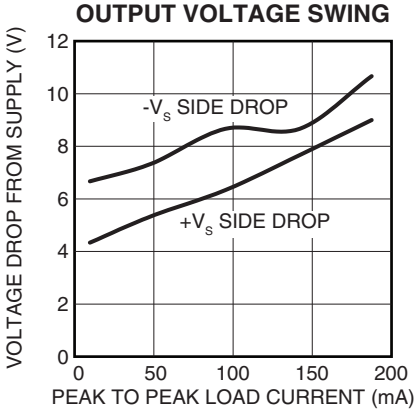
POWER DERATING



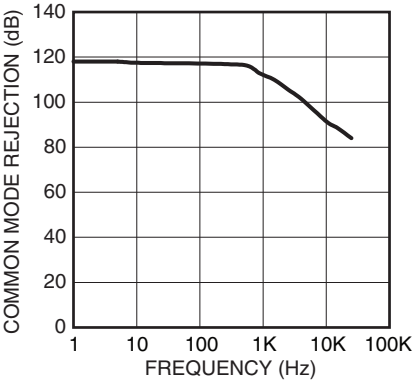
POWER SUPPLY REJECTION



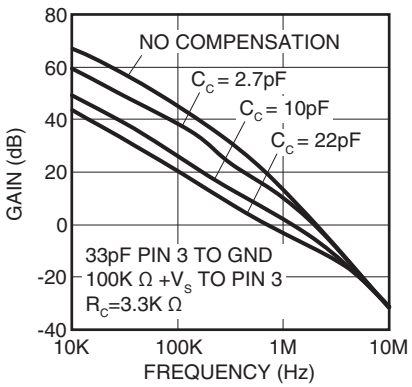
OUTPUT VOLTAGE SWING



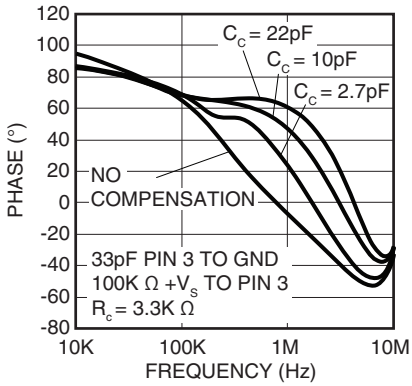
COMMON MODE REJECTION



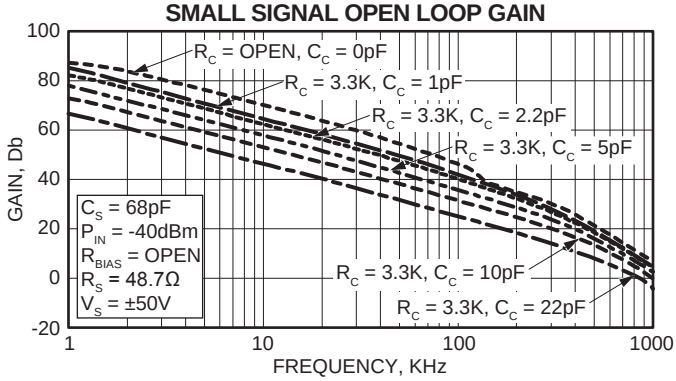
OPEN LOOP GAIN



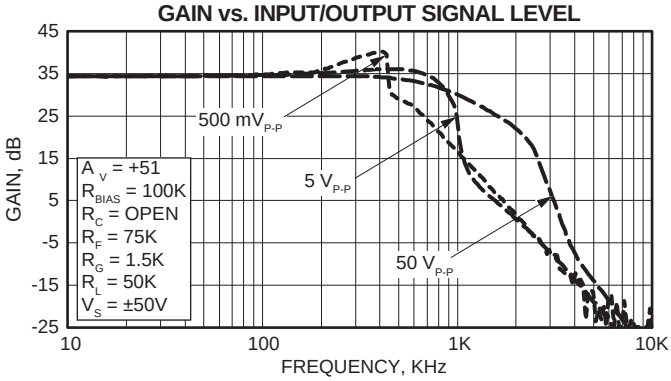
PHASE RESPONSE



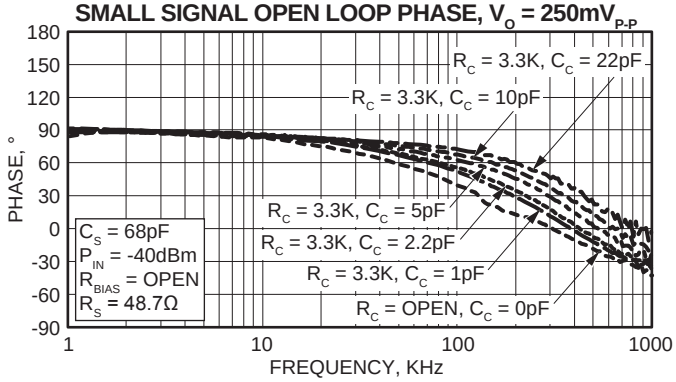
SMALL SIGNAL OPEN LOOP GAIN



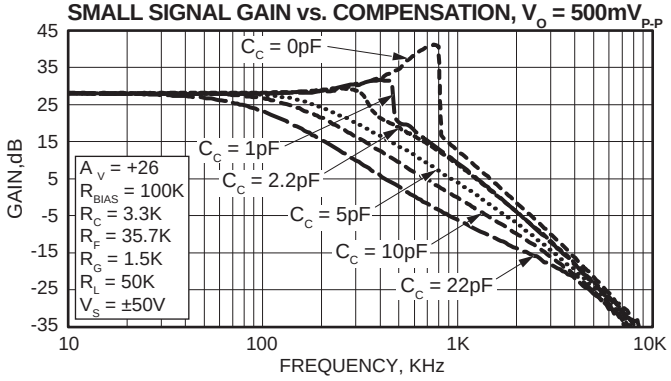
GAIN vs. INPUT/OUTPUT SIGNAL LEVEL



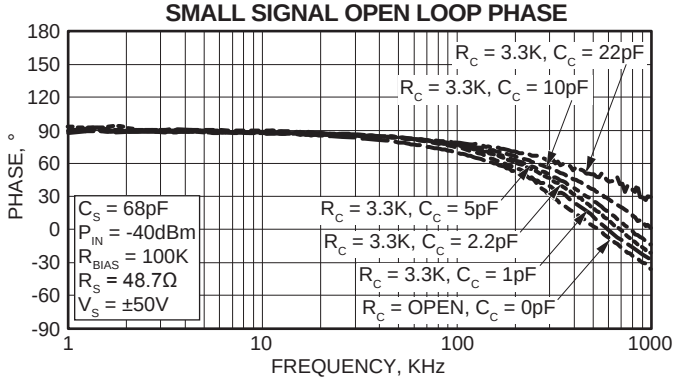
SMALL SIGNAL OPEN LOOP PHASE, V_O = 250mV_{P-P}



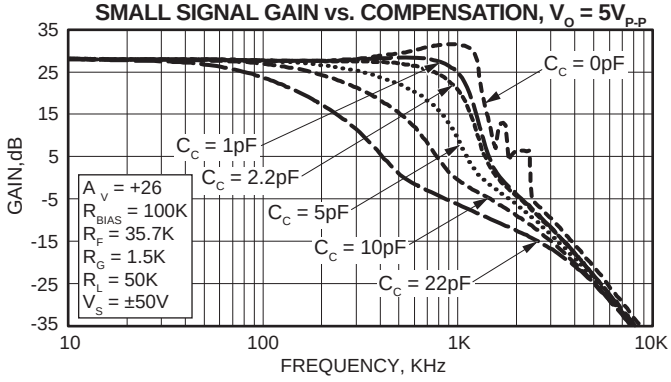
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 500mV_{P-P}



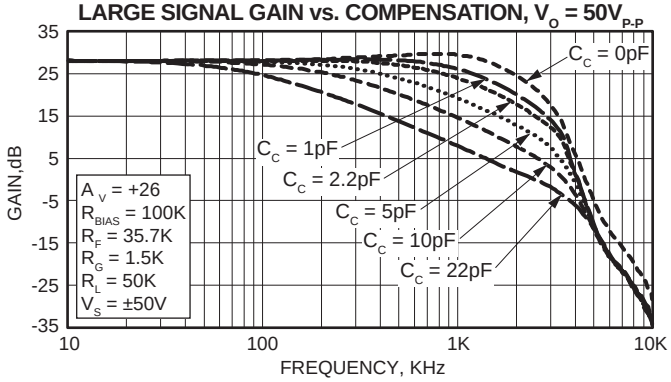
SMALL SIGNAL OPEN LOOP PHASE



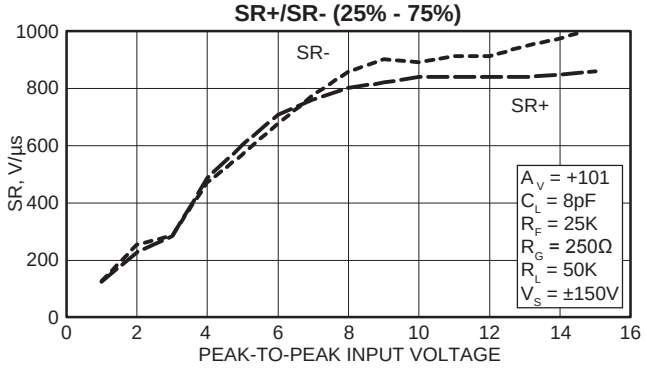
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 5V_{P-P}



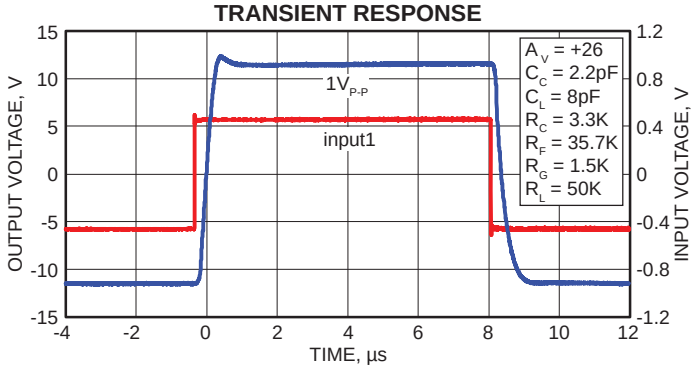
LARGE SIGNAL GAIN vs. COMPENSATION, V_O = 50V_{P-P}



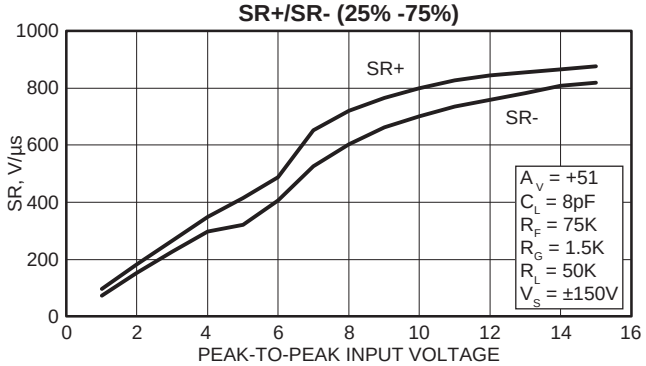
SR+/SR- (25% - 75%)



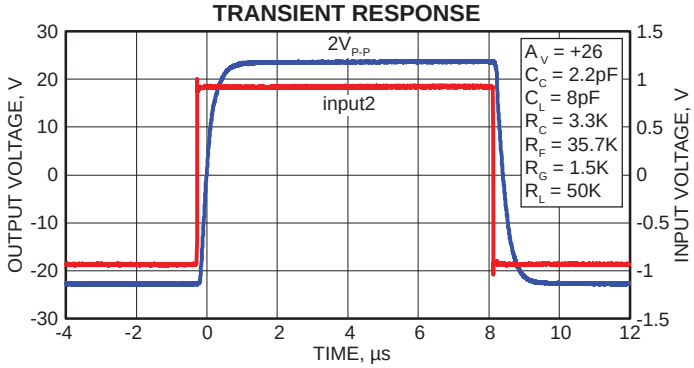
TRANSIENT RESPONSE



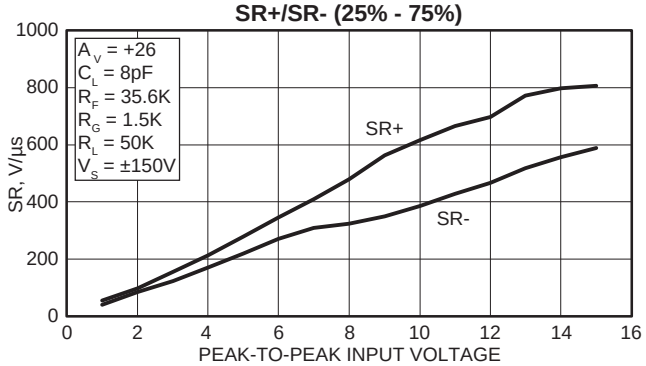
SR+/SR- (25% -75%)



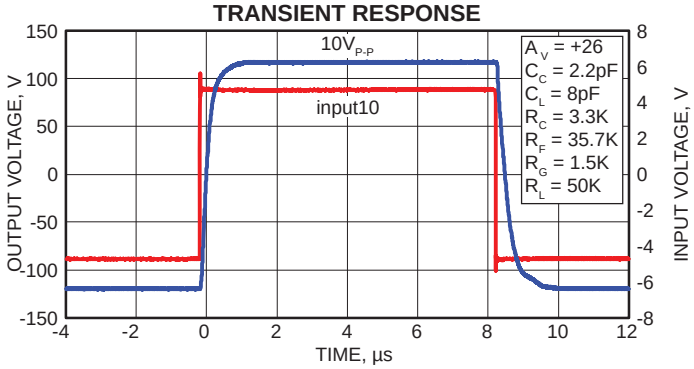
TRANSIENT RESPONSE



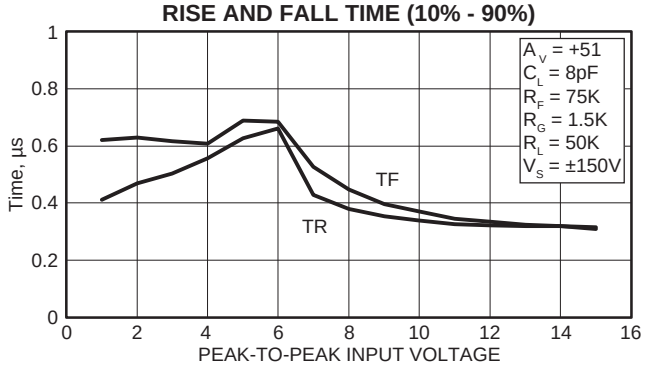
SR+/SR- (25% - 75%)



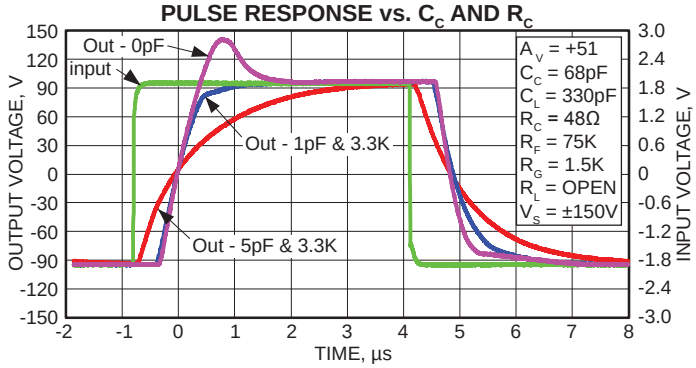
TRANSIENT RESPONSE



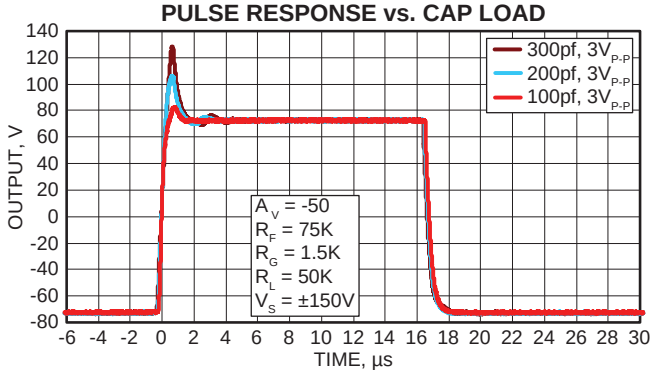
RISE AND FALL TIME (10% - 90%)



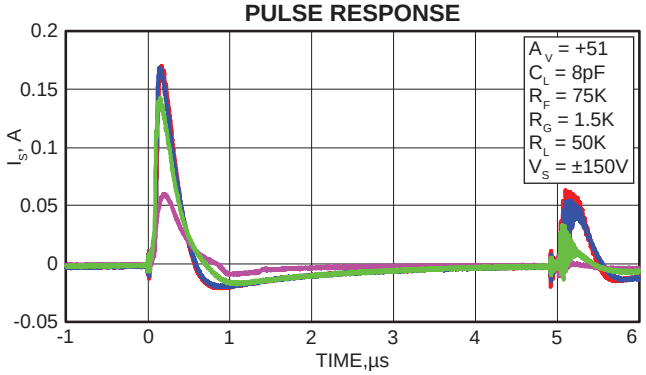
PULSE RESPONSE vs. C_C AND R_C



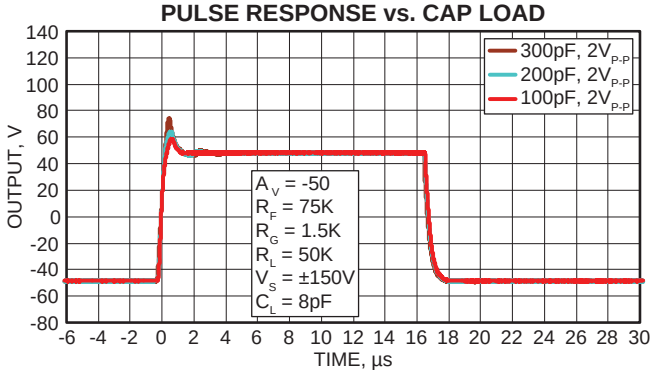
PULSE RESPONSE vs. CAP LOAD



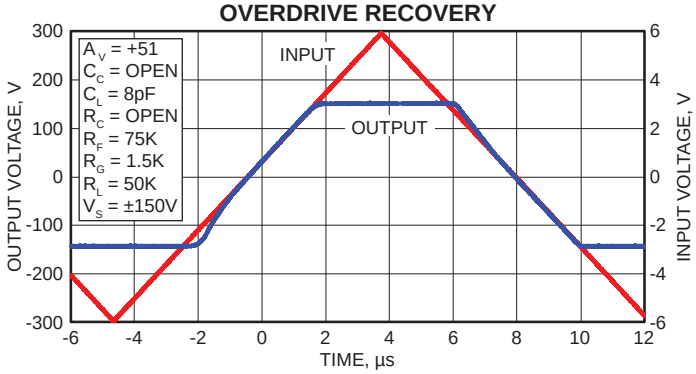
PULSE RESPONSE



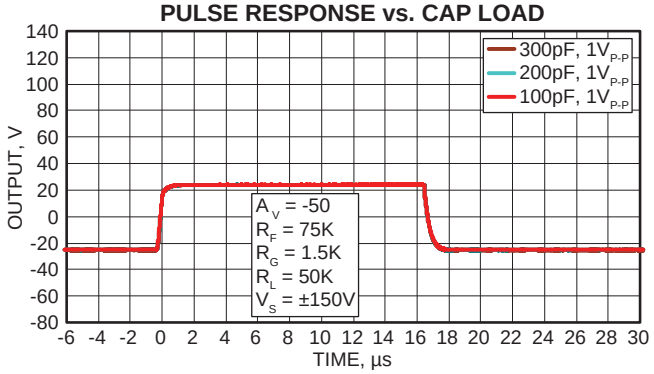
PULSE RESPONSE vs. CAP LOAD



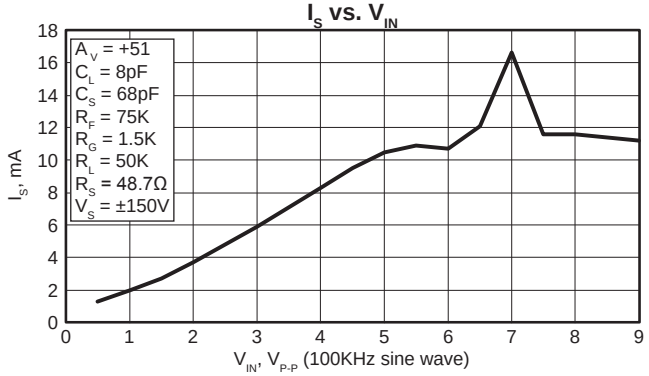
OVERDRIVE RECOVERY



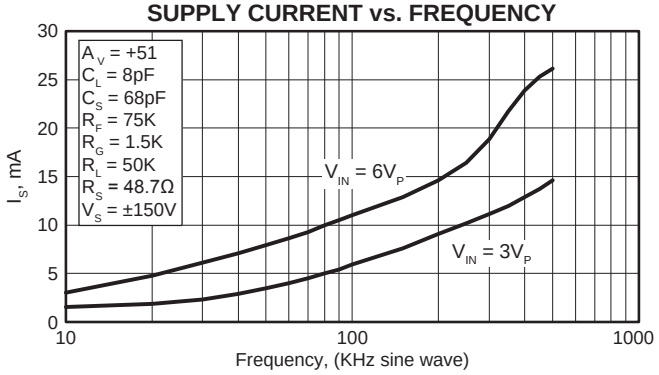
PULSE RESPONSE vs. CAP LOAD



I_S vs. V_{IN}



SUPPLY CURRENT vs. FREQUENCY

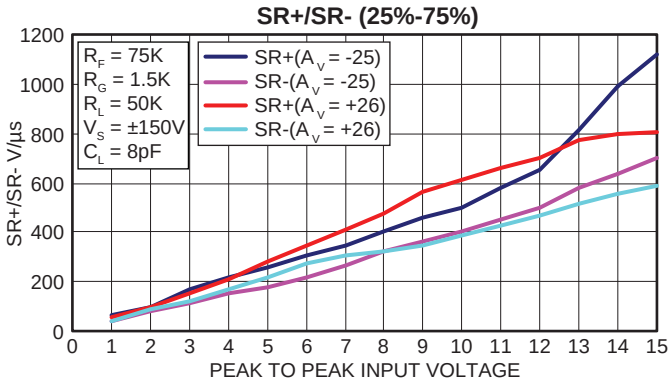


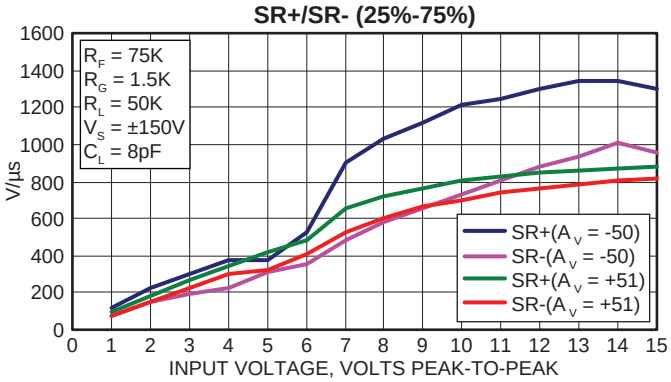
GENERAL

Please read Application note 1 “General operating considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, and current limit. There you will also find a complete application notes library, technical seminar workbook, and evaluation kits.

THEORY OF OPERATION

The PA79 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.





SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA79 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA79 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA79. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in

standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, R_{BIAS}, between C_C- and V_S+. The size of R_{BIAS} will depend upon the application but 500µA (50V V+ supply/100K) of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA79 is externally compensated and performance can be optimized to the application. Unlike the R_{BIAS} technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the tradeoffs between bandwidth and stability. Due to the unique design of the PA79, two symmetric compensation networks are required. The compensation capacitor Cc must be rated for a working voltage of the full operating supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature.

The PA79 requires an external 33pF capacitor between C_C- and $-V_S$ to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from $1V_{P-P}$ to $15V_{P-P}$, the slew rate increases from 50V/µs to well over 350V/µs.

Notice the knee in the Rise and Fall times plot, at approximately $6V_{P-P}$ input voltage. Beyond this point the output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA79 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current vs. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.

The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.

CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The minimum practical value for R_{LIM} is about 12Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for R_{LIM} in the intended application. Current limit may not protect against short circuit conditions with supply voltages over 200V.

LAYOUT CONSIDERATIONS

The PA79 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1µF capacitor to GND is also sufficient if a DC connection is undesirable

Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of L_C interactions and oscillations.

The PA79DK package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heat slug to a 1 square inch foil area on the printed circuit board will result in improved thermal performance of 25ºC/W. In order to improve the thermal performance, multiple metal layers in the printed circuit board are recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85ºC.

The junction to ambient thermal resistance of the DK package can achieve a 19.1ºC/W rating by using the PCB conditions outlined in JEDEC standard: (JESD51–5):

PCB Conditions:

- PCB Layers = 4L, Copper, FR–4
- PCB Dimensions = 101.6 x 114.3mm
- PCB Thickness = 1.6mm

Conditions:

- Power dissipation = 2 watts
- Ambient Temperature = 55ºC

MOISTURE SENSITIVITY

The PA79DK has been qualified according to JEDEC 22-A-113-D, MSL 3. The following conditions were used: IR reflow for Pb-free assembly profile where: package thickness is greater than 2.5mm, package volume is greater than 350mm^2, TP = 245°C.

ELECTROSTATIC DISCHARGE

Like many high performance MOSFET amplifiers, the PA79 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

PA81J • PA82J

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

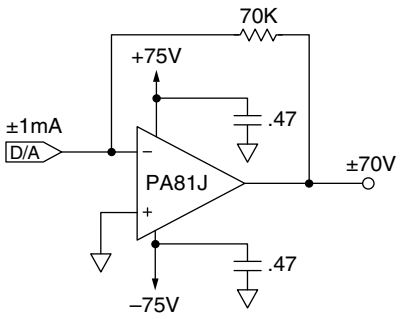
FEATURES

- HIGH VOLTAGE OPERATION — ±150V (PA82J)
- HIGH OUTPUT CURRENT — ±30mA (PA81J)
- LOW BIAS CURRENT, LOW NOISE — FET Input

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- HIGH IMPEDANCE BUFFERS UP TO ±140V
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES TO ±145V
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE



HIGH VOLTAGE PROGRAMMABLE POWER SUPPLY

DESCRIPTION

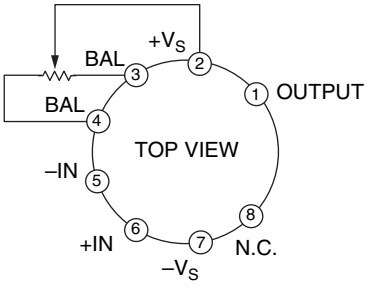
The PA80 series of high voltage operation amplifiers provides an extremely wide range of supply capability with two overlapping products. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode. As a result, these models offer outstanding common mode and power supply rejection. The output stage operates in the class A/B mode for best linearity. Internal phase compensation assures stability at all gain settings without external components. Fixed internal current limits protect these amplifiers against a short circuit to common at most supply voltages. For sustained high energy flyback, external fast recovery diodes should be used. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers voids the warranty.

TYPICAL APPLICATION

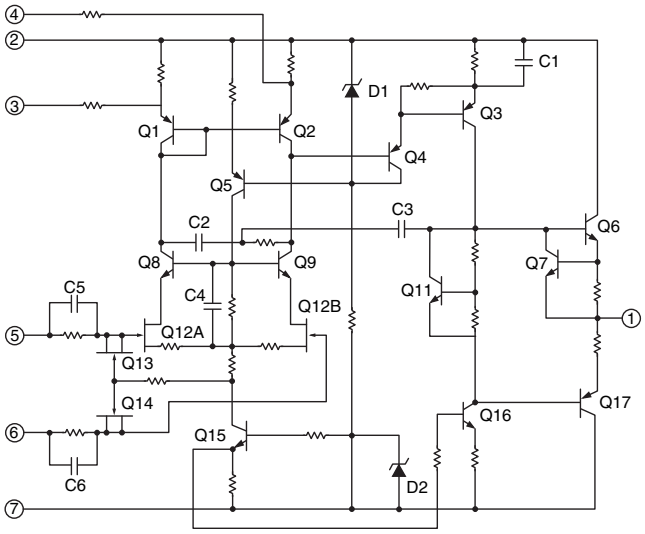
The PA81 and 70K ohm resistor form a current to voltage converter, accepting ±1mA from a 12 bit current output digital to analog converter. The power op amp contribution to the error budget is insignificant. At a case temperature of 70°C, the combination of voltage offset and bias errors amounts to less than 31ppm of full scale range. Incorporation of the optional offset trim can further reduce these errors to under 9ppm.

EXTERNAL CONNECTIONS



NOTE: Input offset trimpot optional.
Recommended value of 100KΩ

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	PA81J	PA82J
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V	300V
OUTPUT CURRENT, within SOA	Internally Limited	
POWER DISSIPATION, internal	11.5W	11.5W
INPUT VOLTAGE, differential	±150V	±300V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder - 10 sec	300°C	300°C
TEMPERATURE, junction	150°C	150°C
TEMPERATURE RANGE, storage	–65 to +125°C	–65 to +125°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C	–55 to +125°C

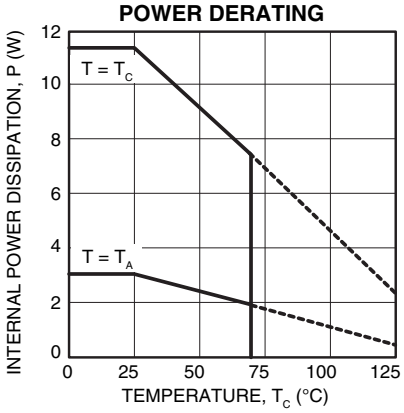
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA81J MIN	PA81J TYP	PA81J MAX	PA82J MIN	PA82J TYP	PA82J MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		*	*	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	25		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		20			*		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		75			*		µV/√kh
BIAS CURRENT, initial	T_C = 25°C		5	50		*	*	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.2			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		*	*	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		10			*		pF
COMMON MODE VOLTAGE RANGE[2]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±20V		110			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full load	94	116		100	118		dB
UNITY GAIN BANDWIDTH	T_C = 25°C		5			*		MHz
POWER BANDWIDTH	T_C = 25°C, full load		60			30		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[2]	T_C = 25°C, I_{PK}	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	30			15			mA
CURRENT, limit	T_C = 25°C		50			25		mA
SETTLING TIME to .1%	T_C = 25°C, 10V step		12			*		µs
SLEW RATE[4]	T_C = 25°C		20			*		V/µs
CAPACITIVE LOAD	A_V = 1		10			*		nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±32	±75	±75	±70	±150	±150	V
CURRENT, quiescent	T_C = 25°C		6.5	8.5		6.5	8.5	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	F > 60Hz		6			*		°C/W
RESISTANCE, DC, junction to case[3]	F < 60Hz		9	10		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, shutdown			150			*		°C
TEMPERATURE RANGE, case	Meets full range specification	0		70	*		*	°C

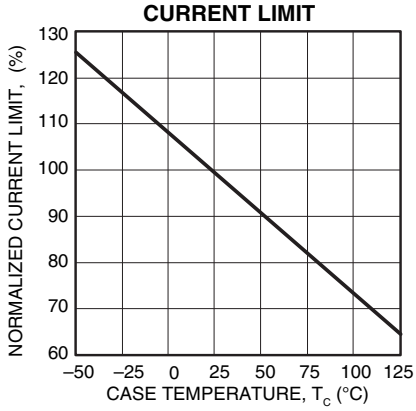
NOTES: * The specification of PA82J is identical to the specification for PA81J in applicable column to the left.
1. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
2. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
4. On the PA81J and PA82J, signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

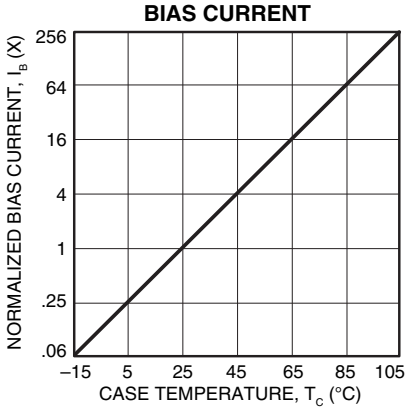
POWER DERATING



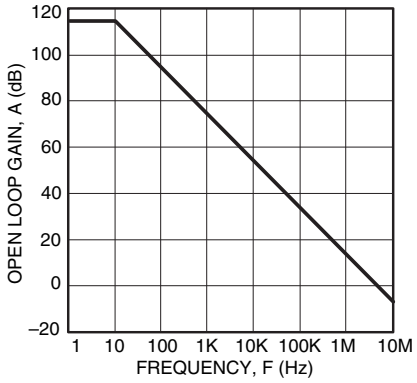
CURRENT LIMIT



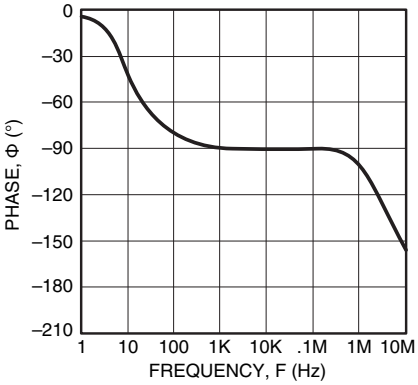
BIAS CURRENT



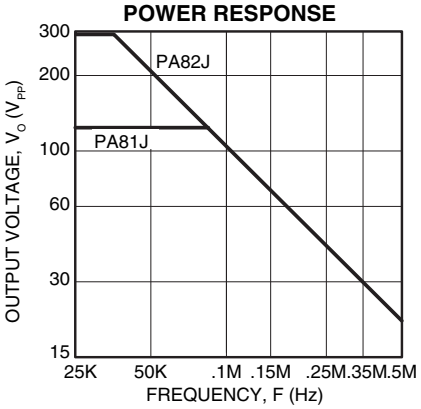
SMALL SIGNAL RESPONSE



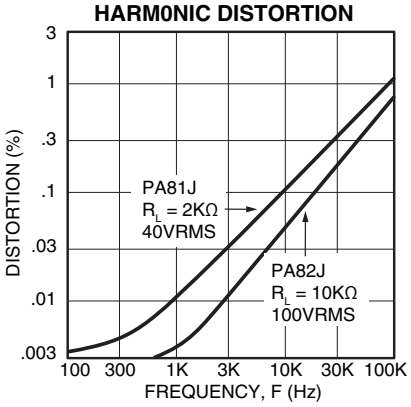
PHASE RESPONSE



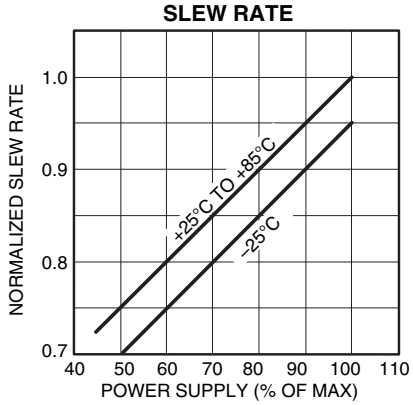
POWER RESPONSE



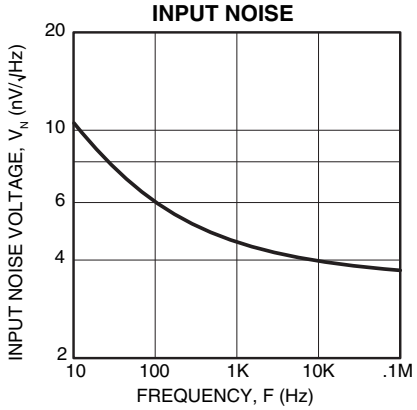
HARM0NIC DISTORTION



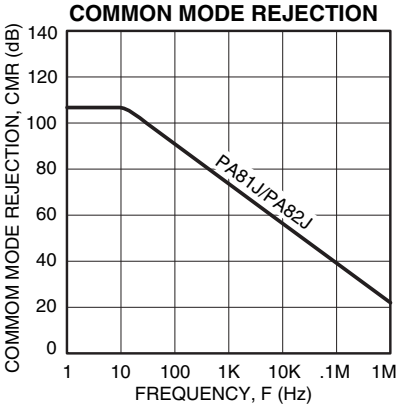
SLEW RATE



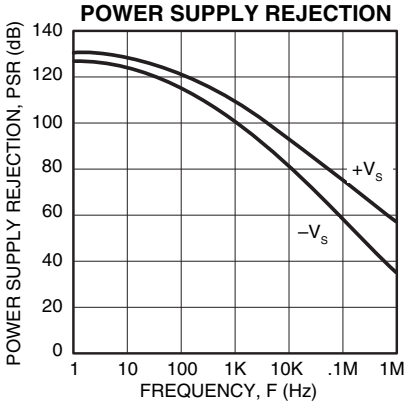
INPUT NOISE



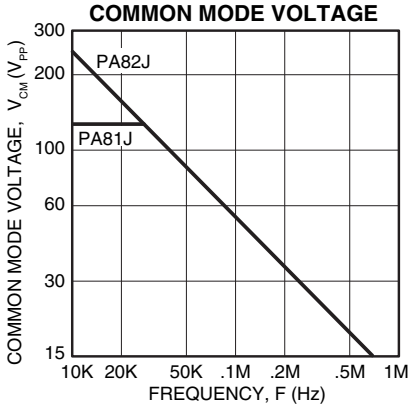
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)

For the PA80J and PA81J, the combination of voltage capability and internal current limits mandate that the devices are safe for all combinations of supply voltage and load. On the PA82J, any load combination is safe up to a total supply of 250 volts. When total supply voltage equals 300 volts, the device will be safe if the output current is limited to 10 milliamps or less. This means that the PA82J used on supplies up to 125 volts will sustain a short to common or either supply without danger. When using supplies above ±125 volts, a short to one of the supplies will be potentially destructive. When using single supply above 250 volts, a short to common will be potentially destructive.

Safe supply voltages do not imply disregard for heatsinking. The thermal calculations and the use of a heatsink are required in many applications to maintain the case temperature within the specified operating range of 0 to 70°C. Exceeding this case temperature range can result in an inoperative circuit due to excessive input errors or activation of the thermal shutdown.

INDUCTIVE LOADS

Two external diodes as shown in Figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltage of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating, or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

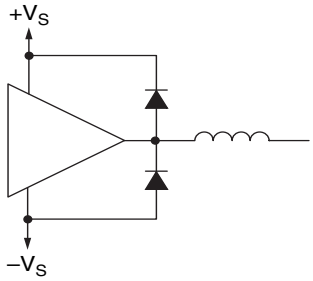


FIGURE 2.
PROTECTION,
INDUCTIVE LOAD

SINGLE SUPPLY OPERATION

These amplifiers are suitable for operation from a single supply voltage. The operating requirements do however, impose the limitation that the input voltages do not approach closer than 10 volts to either supply rail. This is due to the operating voltage requirements of the current sources, the half-dynamic loads and the cascode stage. Refer to the simplified schematics.Thus, single supply operation requires the input signals to be biased at least 10 volts from either supply rail. Figure 3 illustrates one bias technique to achieve this.

Figure 4 illustrates a very common deviation from true single

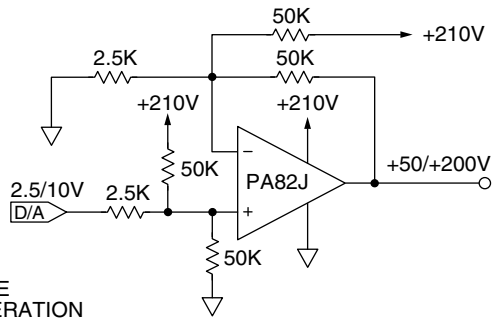


FIGURE 3.
TRUE SINGLE
SUPPLY OPERATION

supply operation. The availibility of two supplies still allows ground (common) referenced signals, but also maximizes the high voltage capability of the unipolar output. This technique can utilize an existing low voltage system power supply and does not place large current demands on that supply. The 12 volt supply in this case must supply only the quiescent current of the PA81J, which is 8.5mA maximum. If the load is reactive or EMF producing, the low voltage supply must also be able to absorb the reverse currents generated by the load.

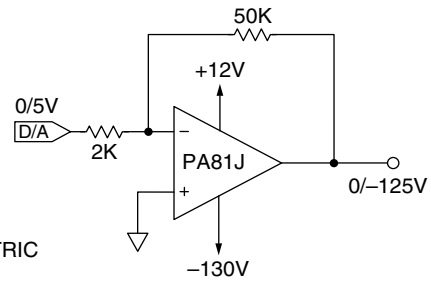


FIGURE 4.
NON-SYMMETRIC
SUPPLIES

PA83 • PA83A

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

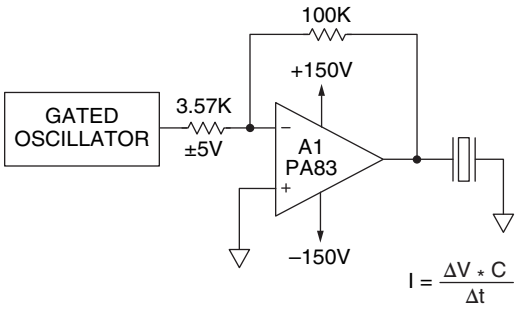
FEATURES

- LOW BIAS CURRENT, LOW NOISE — FET Input
- FULLY PROTECTED INPUT — Up to ±150V
- WIDE SUPPLY RANGE — ±15V to ±150V

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

8-PIN TO-3
PACKAGE STYLE CE



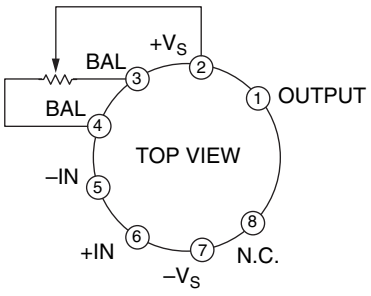
SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

DESCRIPTION

The PA83 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid circuit utilizes beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque voids product warranty. Please see Application Note 1 "General Operating Considerations".

EXTERNAL CONNECTIONS

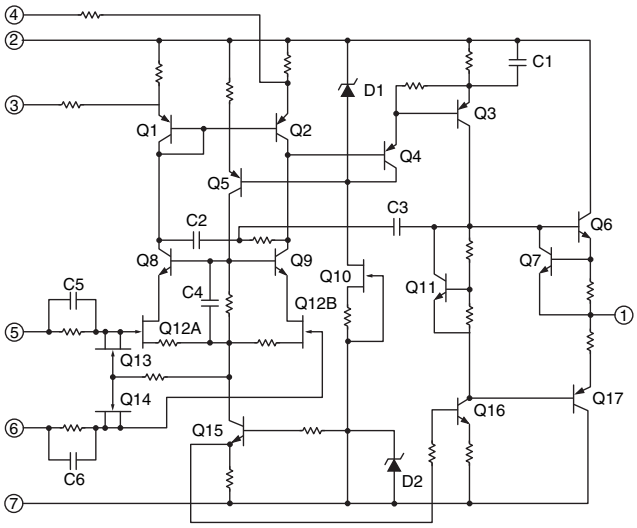


NOTE:
1. Pin 8 not internally connected.
2. Input offset trimpot optional. Recommended value of 100KΩ.

TYPICAL APPLICATION

While piezo electric transducers present a complex impedance, they are often primarily capacitive at useful frequencies. Due to this capacitance, the speed limitation for a given transducer/amplifier combination may well stem from limited current drive rather than power bandwidth restrictions. With its drive capability of 75mA, the PA83 can drive transducers having up to 2nF of capacitance at 40kHz at maximum output voltage. In the event the transducer may be subject to shock or vibration, flyback diodes, voltage clamps or other protection networks must be added to protect the amplifier from high voltages which may be generated.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[1]	17.5W
INPUT VOLTAGE, differential	±300V
INPUT VOLTAGE, common mode	±300V
TEMPERATURE, pin solder - 10s max (solder)	300°C
TEMPERATURE, junction	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

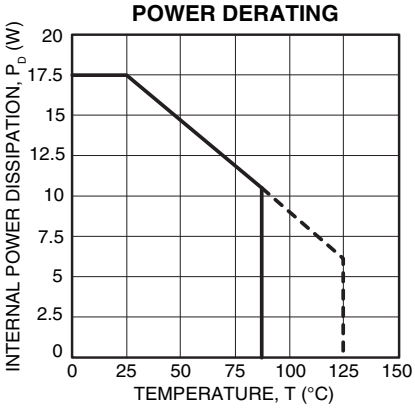
PARAMETER	TEST CONDITIONS[2]	PA83 MIN	PA83 TYP	PA83 MAX	PA83A MIN	PA83A TYP	PA83A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√kh
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	Full temperature range		6			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	Full temperature range		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 2KΩ	96	116		*	*		dB
UNITY GAIN CROSSOVER FREQ.	T_C = 25°C, R_L = 2KΩ		5		3	*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L = 10KΩ		60		40	*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4], full load	Full temp. range, I_O = 75mA	$\pm V_S$–10	$\pm V_S$–5		*	*		V
VOLTAGE SWING[4]	Full temp. range, I_O = 15mA	$\pm V_S$–5	$\pm V_S$–3		*	*		V
CURRENT, peak	T_C = 25°C	75			*			mA
CURRENT, short circuit	T_C = 25°C		100			*		mA
SLEW RATE[6]	T_C = 25°C, R_L = 2KΩ	20	30		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	µF
SETTLING TIME to .1%	T_C = 25°C, R_L = 2KΩ, 10V step		12			*		µs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15	±150	±150	*	*	*	V
CURRENT, quiescent	T_C = 25°C		6	8.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F > 60Hz		4.26			*		°C/W
RESISTANCE, DC, junction to case	F < 60Hz		6.22	8.57		*	*	°C/W
RESISTANCE, case to air			30			*		°C/W
TEMP. RANGE, case (PA83/PA83A)	Meets full range specification	–25		+85	*		*	°C

NOTES: * The specification of PA83A is identical to the specification for PA83 in applicable column to the left.

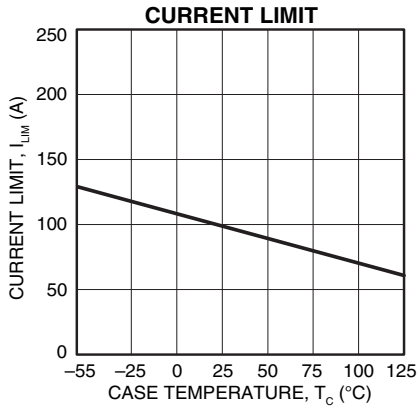
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is the TYP rating, unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

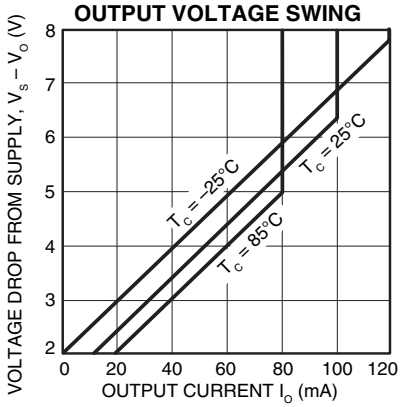
POWER DERATING



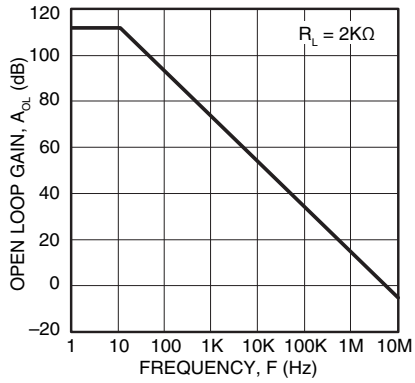
CURRENT LIMIT



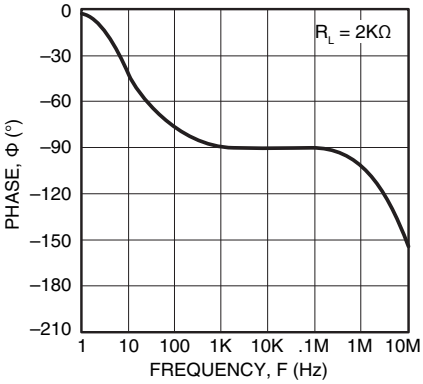
OUTPUT VOLTAGE SWING



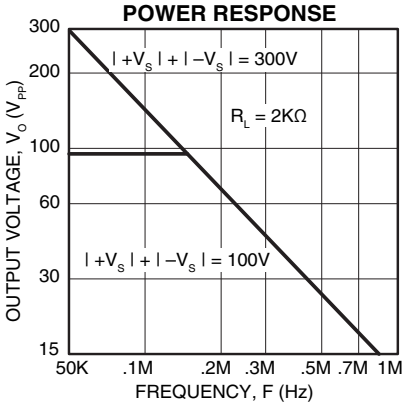
SMALL SIGNAL RESPONSE



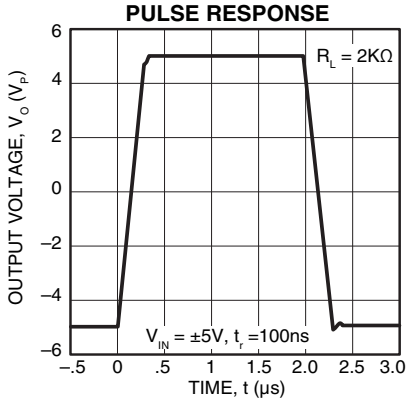
PHASE RESPONSE



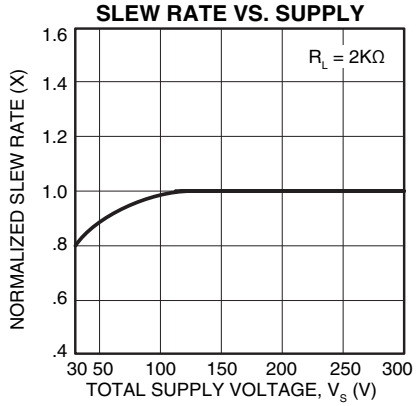
POWER RESPONSE



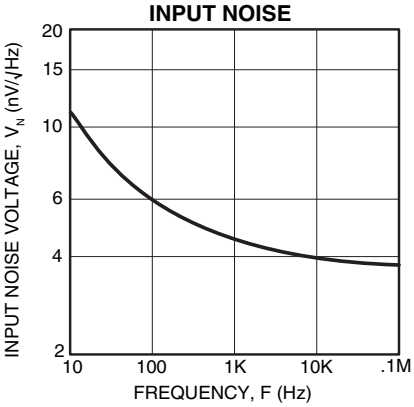
PULSE RESPONSE



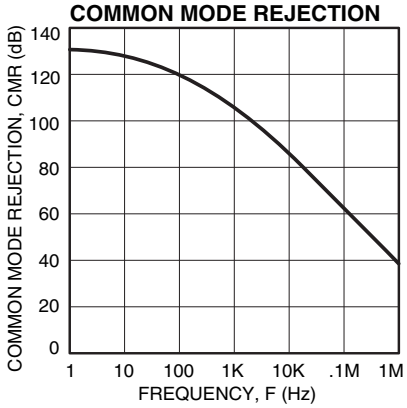
SLEW RATE VS. SUPPLY



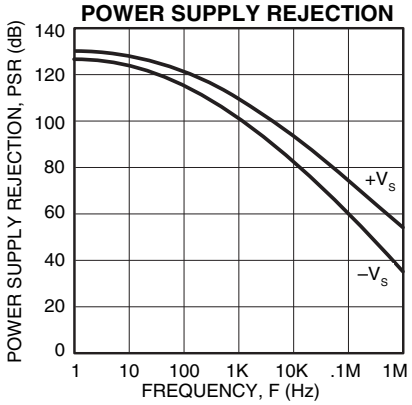
INPUT NOISE



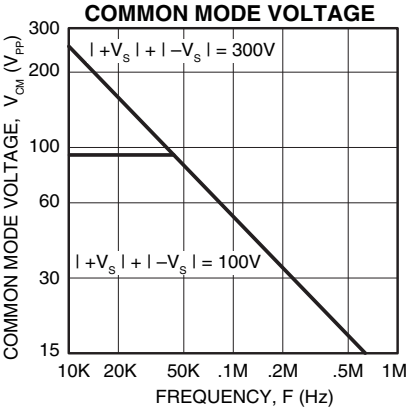
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



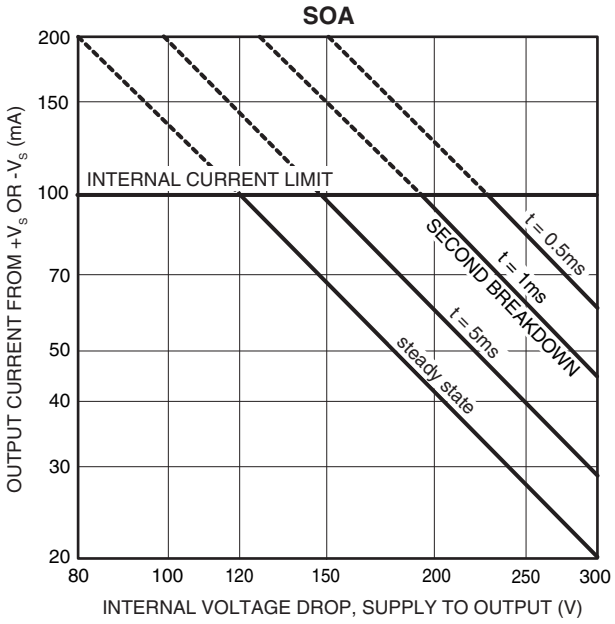
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage amplifier has two distinct limitations.

1. The internal current limit, which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage



exceed specified limits.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_S$	C(MAX)	L(MAX)
150V	.7 F	1.5H
125V	2.0µF	2.5H
100V	5.µF	6.0H
75V	60µF	30H
50V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to 120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V, e.g. ±60V.
4. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INDUCTIVE LOADS

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

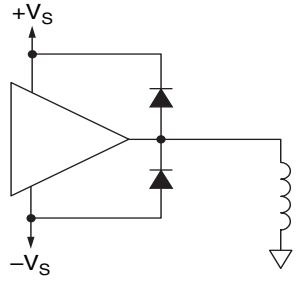
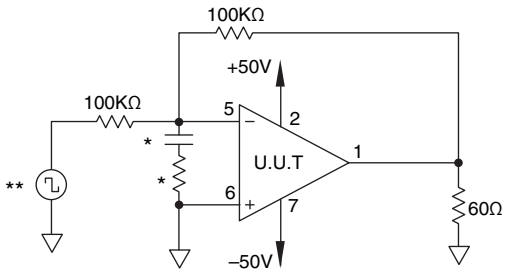


FIGURE 1. PROTECTION, INDUCTIVE LOAD

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$–I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V =100		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$–I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		10	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 75mA	V_O	25°C	±85V	R_L = 1K	75		V
4	Output Voltage, I_O = 29mA	V_O	25°C	±150V	R_L = 5K	145		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K	20	80	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5K, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 40mA	V_O	–55°C	±45V	R_L = 1K	40		V
6	Output Voltage, I_O = 29mA	V_O	–55°C	±150V	R_L = 5K	145		V
6	Stability/Noise	E_N	–55°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±150V	R_L = 5K	20	80	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	R_L = 5K, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 40mA	V_O	125°C	±45V	R_L = 1K	40		V
5	Output Voltage, I_O = 29mA	V_O	125°C	±150V	R_L = 5K	145		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K	20	80	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA84 • PA84A • PA84S

Power Operational Amplifiers

RoHS COMPLIANT

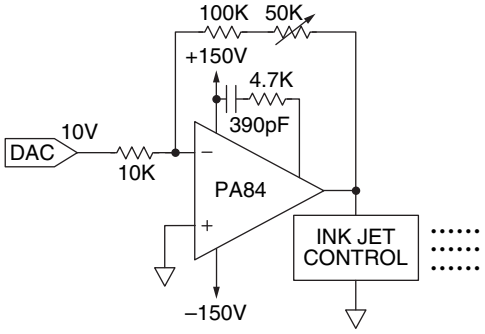
FEATURES

- HIGH SLEW RATE — 200V/µs
- FAST SETTLING TIME — .1% in 1µs (PA84S)
- FULLY PROTECTED INPUT — Up to ±150v
- LOW BIAS CURRENT, LOW NOISE — FET Input
- WIDE SUPPLY RANGE — ±15V to ±150V

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS



DESCRIPTION

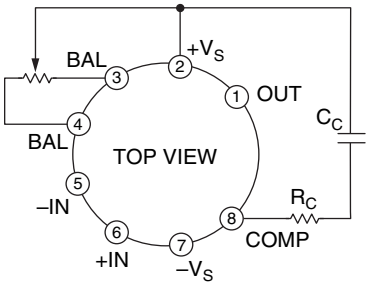
The PA84 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual supply or 290V with a single supply. Two versions are available. The new PA84S, fast settling amplifier can absorb differential input overvoltages up to ±50V while the established PA84 and PA84A can handle differential input overvoltages of up to ±300V. Both versions are protected against common mode transients and overvoltages up to the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA84 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. External phase compensation allows for user flexibility in obtaining the maximum slew rate. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 150V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

TYPICAL APPLICATION

The PA84 is ideally suited to driving ink jet control units (often a piezo electric device) which require precise pulse shape control to deposit crisp clear date or lot code information on product containers. The external compensation network has been optimized to match the gain setting of the circuit and the complex impedance of the ink jet control unit. The combination of speed and high voltage capabilities of the PA84 form ink droplets of uniform volume at high production rates to enhance the value of the printer.

EXTERNAL CONNECTION

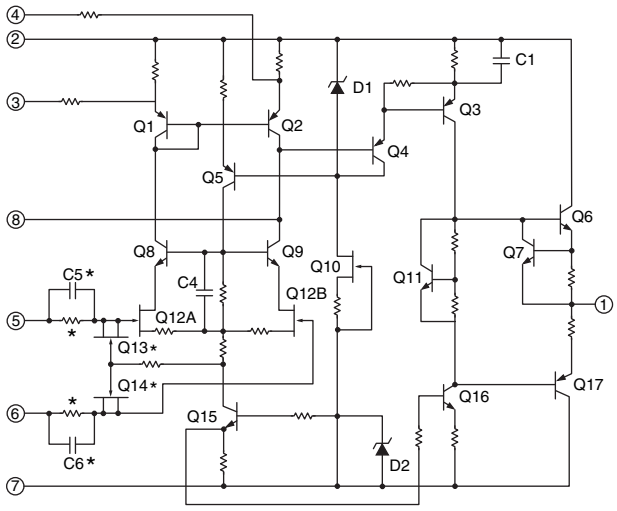


PHASE COMPENSATION

GAIN	C_C	R_C
1	10nF	200Ω
10	500pF	2KΩ
100	50pF	20KΩ
1000	none	none

NOTES:
1. Phase Compensation required for safe operation.
2. Input offset trimpot optional. Recommended value 100KΩ.

EQUIVALENT SCHEMATIC



*Not included in PA84S.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[2]	17.5W
INPUT VOLTAGE, differential PA84/PA84A[1]	±300V
INPUT VOLTAGE, differential PA84S	±50V
INPUT VOLTAGE, common mode[1]	$\pm V_S$
TEMPERATURE, pins for 10s max (solder)	300°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

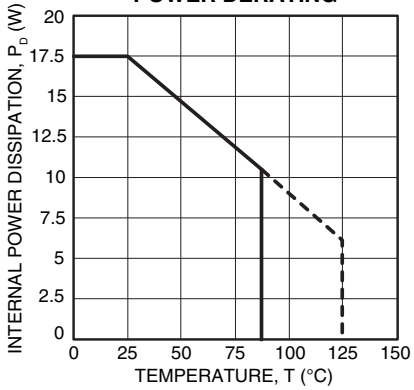
PARAMETER	TEST CONDITIONS[3]	PA84/PA84S MIN	PA84/PA84S TYP	PA84/PA84S MAX	PA84A MIN	PA84A TYP	PA84A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25° to +85°C		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√kh
BIAS CURRENT, initial[4]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[4]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = –25° to +85°C		6			*		pF
COMMON MODE VOLTAGE RANGE[5]	T_C = –25° to +85°C	$\pm V_S$–10	$\pm V_S$–8.5		*	*		V
COMMON MODE REJECTION, DC	T_C = –25° to +85°C		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = ∞		120			*		dB
OPEN LOOP GAIN at 10Hz.	T_C = 25°C, R_L = 3.5KΩ	100	118		*	*		dB
GAIN BANDWIDTH PRODUCT@ 1MHz	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		75			*		MHz
POWER BANDWIDTH, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		250		180	*		kHz
POWER BANDWIDTH, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		120			*		kHz
OUTPUT								
VOLTAGE SWING[5]	T_C = 25°C, I_O = ±40mA	$\pm V_S$–7	$\pm V_S$–3		*	*		V
VOLTAGE SWING[5]	T_C = –25° to +85°C, I_O = ±15mA	$\pm V_S$–5	$\pm V_S$–2		*	*		V
CURRENT, peak	T_C = 25°C	40			*			mA
CURRENT, short circuit	T_C = 25°C		50			*		mA
SLEW RATE, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		200		150	*		V/µs
SLEW RATE, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 2KΩ		125			*		V/µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84S**		2					µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step **ONLY**		1					µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84/84A**		20			20		µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step		12			12		µs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15		±150	*		*	V
CURRENT, quiescent	T_C = 25°C		5.5	7.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[6]	T_C = –55°C to +125°C, F > 60Hz		4.26			*		°C/W
RESISTANCE, DC, junction to case	T_C = –55°C to +125°C, F < 60Hz		6.22	8.57		*	*	°C/W
RESISTANCE, case to air	T_C = –55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA84A is identical to the specification for PA84/PA84S in applicable column to the left.

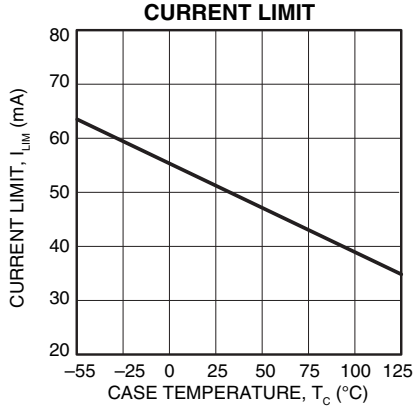
1. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. The power supply voltage for all tests is ±150V, unless otherwise noted as a test condition.
4. Doubles for every 10°C of temperature increase.
5. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

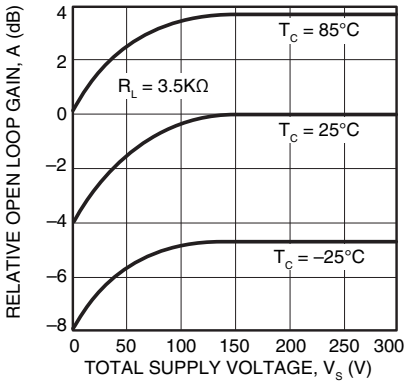
POWER DERATING



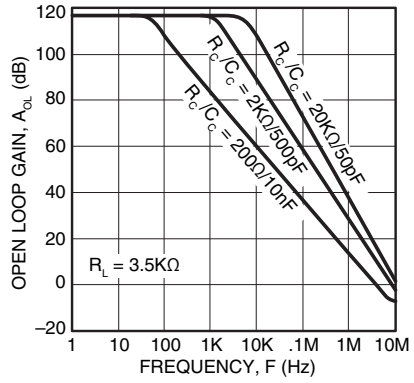
CURRENT LIMIT



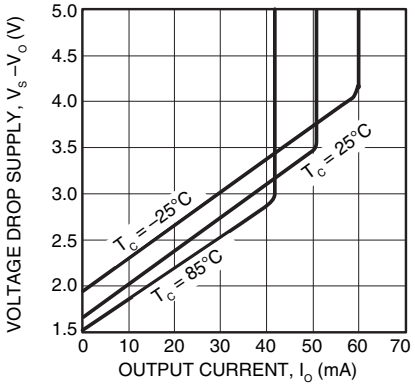
OPEN LOOP GAIN



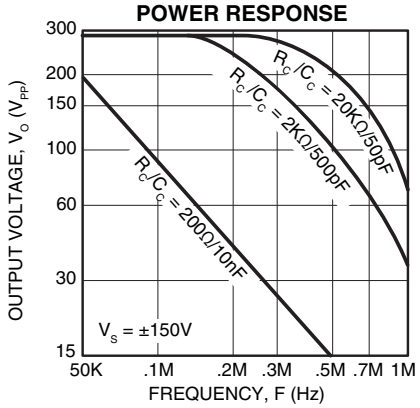
SMALL SIGNAL RESPONSE



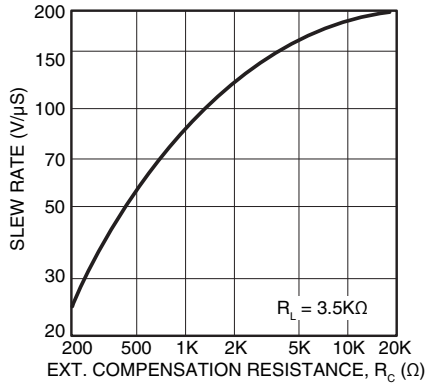
OUTPUT VOLTAGE SWING



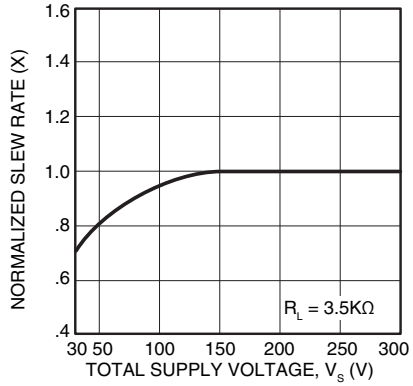
POWER RESPONSE



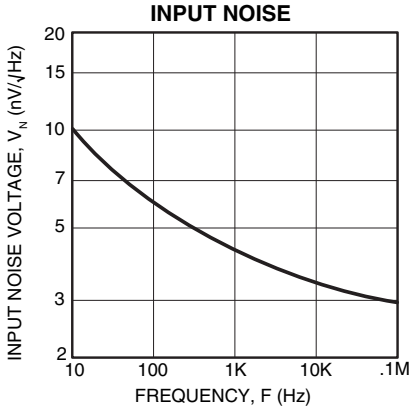
SLEW RATE VS. COMP



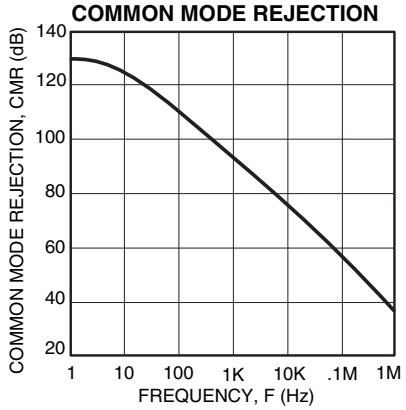
SLEW RATE VS. SUPPLY



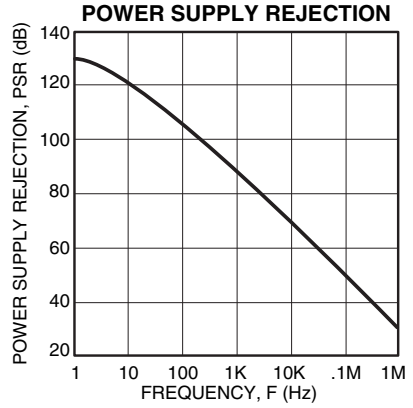
INPUT NOISE



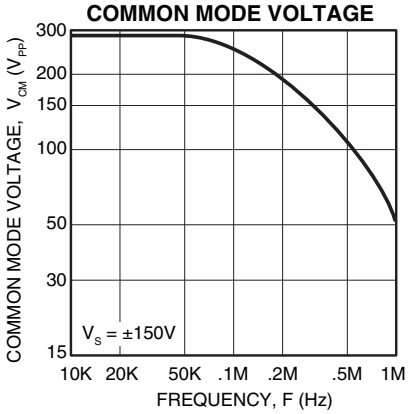
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



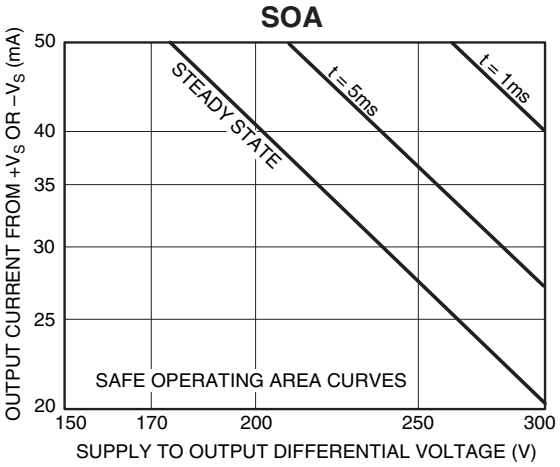
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage operational amplifier has two output limitations:

1. The internal current limit which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

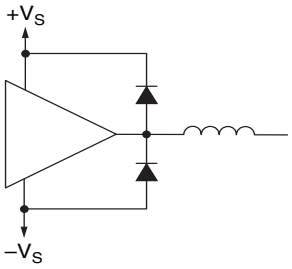
$\pm V_S$	C(MAX)	L(MAX)
150V	1.2µF	.7H
125V	6.0µF	25H
100V	12µF	90H
75V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to ±150V or single supplies up to 150V.
3. Short circuits to the supply rails are safe with total supply voltages up to 150V (i.e. ±75V).

OUTPUT PROTECTION

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

FIGURE 1. PROTECTIVE, INDUCTIVE LOAD



A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

STABILITY

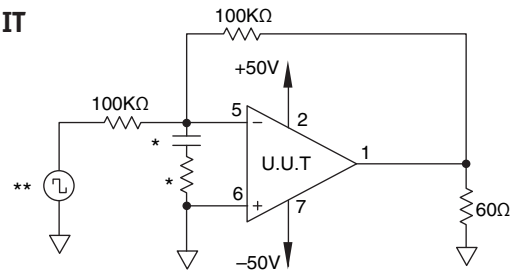
Due to its large bandwidth the PA84 is more likely to oscillate than lower bandwidth Power Operational Amplifiers such as the PA83 or PA08. To prevent oscillations, a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table. The compensation capacitor may be connected to common (in lieu of $+V_S$) if the positive supply is properly bypassed to common. Because the voltage at pin 8 is only a few volts below the positive supply, this ground connection requires the use of a high voltage capacitor.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistance can be used with increased phase compensation (see 1 above).
3. Connecting the amplifier case to a local AC common thus preventing it from acting as an antenna.

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		7.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$–I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$–I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 40mA	V_O	25°C	±47V	R_L = 1K	40		V
4	Output Voltage, I_O = 28.6mA	V_O	25°C	±150V	R_L = 5K	143		V
4	Output Voltage, I_O = 15mA	V_O	25°C	± 80V	R_L = 5K	75		V
4	Current Limits	I_{CL}	25°C	± 20V	R_L = 100Ω	36	70	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5k, F = 10Hz	100		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 40mA	V_O	–55°C	±47V	R_L = 1K	40		V
6	Output Voltage, I_O = 28.6mA	V_O	–55°C	±150V	R_L = 5K	143		V
6	Output Voltage, I_O = 15mA	V_O	–55°C	±80V	R_L = 5K	75		V
6	Stability/Noise	E_N	–55°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	R_L = 5K, F = 10Hz	100		dB
6	Common Mode Rejection	CMR	-55°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 30mA	V_O	125°C	±37V	R_L = 1K	30		V
5	Output Voltage, I_O = 28.6mA	V_O	125°C	±150V	R_L = 5K	143		V
5	Output Voltage, I_O = 15mA	V_O	125°C	±80V	R_L = 5K	75		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5î, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	100		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA85 • PA85A

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- HIGH SLEW RATE — 1000V/µS
- HIGH OUTPUT CURRENT — 200mA

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- PIEZO TRANSDUCER EXCITATION
- PROGRAMMABLE POWER SUPPLIES UP TO 430V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION

PATENTED

8-PIN TO-3
PACKAGE STYLE CE

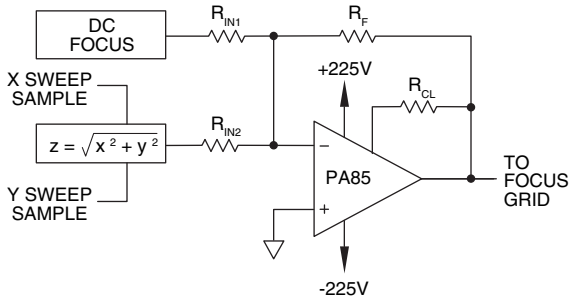
DESCRIPTION

The PA85 is a high voltage, high power bandwidth MOSFET operational amplifier designed for output currents up to 200mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA85 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

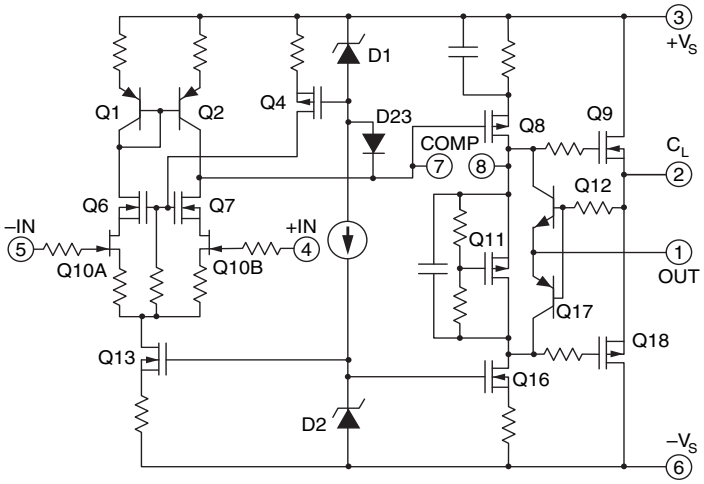
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

TYPICAL APPLICATION

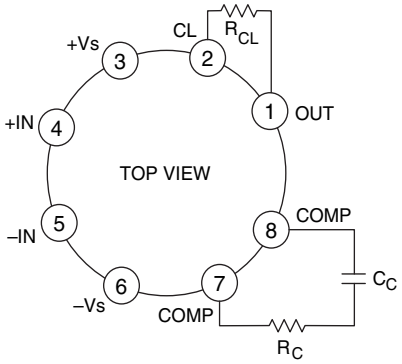
Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA85 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages by calculating the distance of the beam from the center of the display.



EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_c	R_c
1	68pF	100Ω
20	10pF	330Ω
100	3.3pF	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, continuous within SOA	200mA
POWER DISSIPATION, continuous @ T_C = 25°C[2]	30W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA85 MIN	PA85 TYP	PA85 MAX	PA85A MIN	PA85A TYP	PA85A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			3	10		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			10	100		3	30	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S$–15			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 10pf		1			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 3.3pf		100			*		MHz
POWER BANDWIDTH	C_C = 10pf		300			*		kHz
	C_C = 3.3pf		500			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = ±200mA	±Vs–10	±Vs–6.5		*	*		V
VOLTAGE SWING[4]	I_O = ±75mA	±V–8.5	±Vs–6.0		*	*		V
VOLTAGE SWING[4]	I_O = ±20mA	±V–8.0	±Vs–5.5		*	*		V
CURRENT, continuous	T_C = 85°C	±200				*		mA
SLEW RATE, A_V = 20	C_C = 10pf		400			*		V/µs
SLEW RATE, A_V = 100	C_C = OPEN		1000		700	*		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			*		*	pf
SETTLING TIME to .1%	C_C = 10pf, 2V step		1			*		µs
RESISTANCE, no load	R_{CL} = 0		50			*		Ω
POWER SUPPLY								
VOLTAGE[6]	Full temperature range	±15	±150	±225	*	*	*	V
CURRENT, quiescent			21	25		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

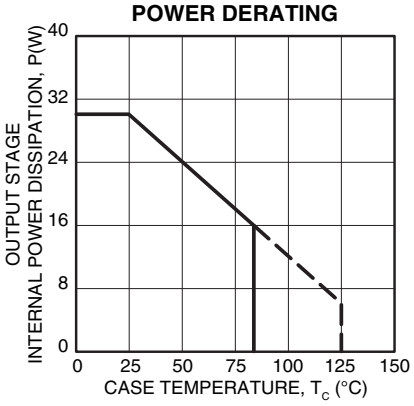
NOTES: * The specification of PA85A is identical to the specification for PA85 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. Ratings apply only to output transistors. An additional 10W may be dissipated due to quiescent power.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

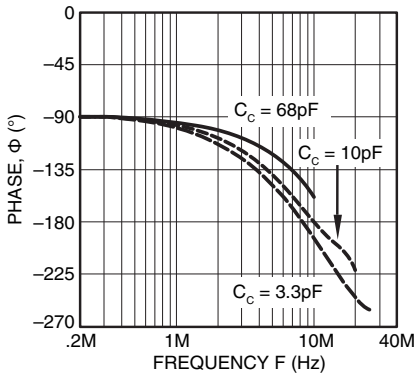
CAUTION The PA85 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

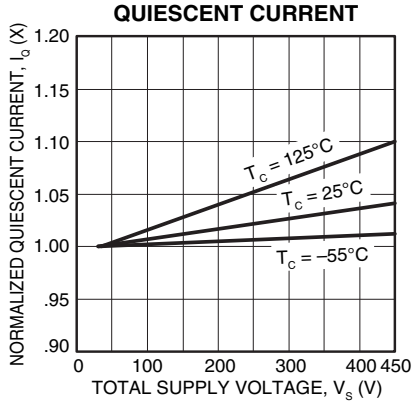
POWER DERATING



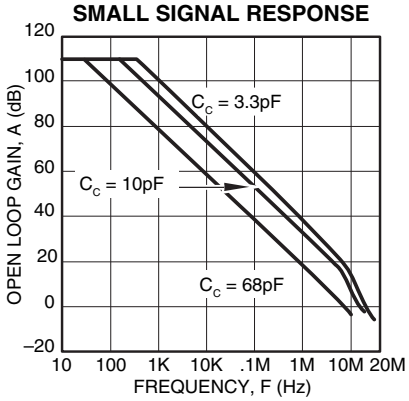
PHASE RESPONSE



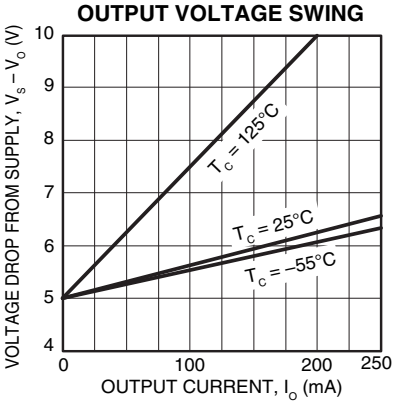
QUIESCENT CURRENT



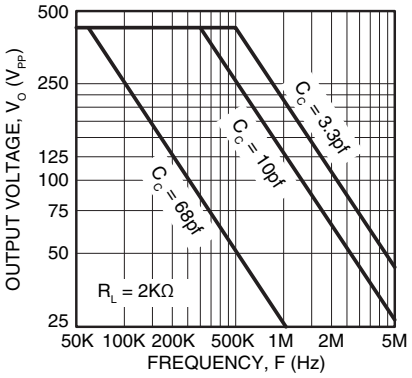
SMALL SIGNAL RESPONSE



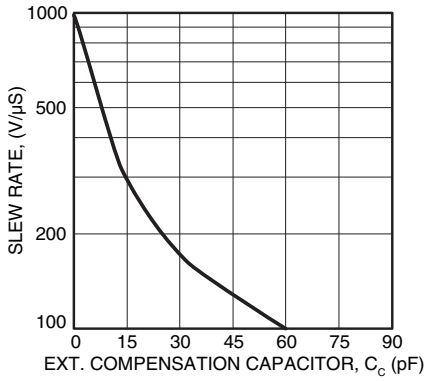
OUTPUT VOLTAGE SWING



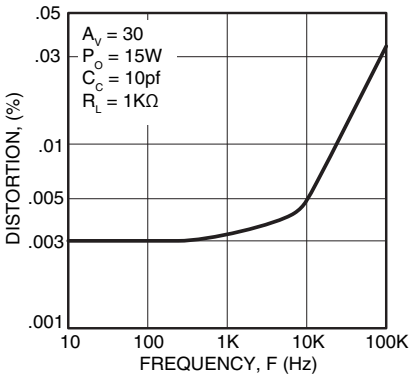
POWER RESPONSE



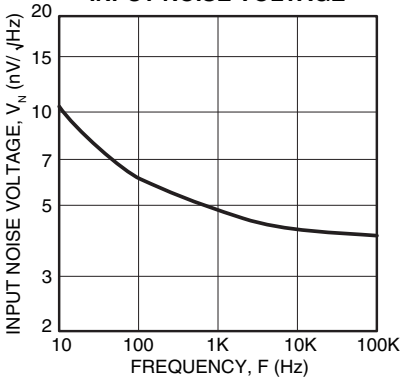
SLEW RATE



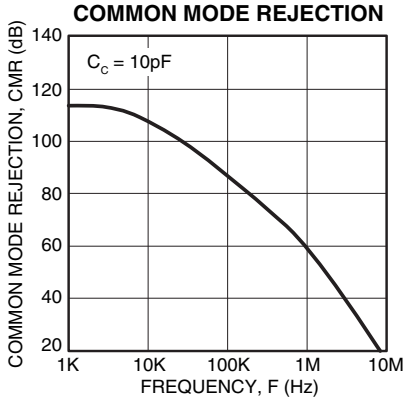
HARMONIC DISTORTION



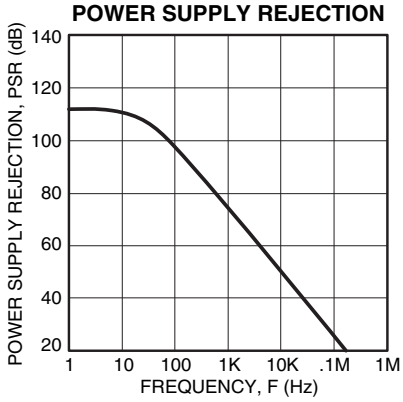
INPUT NOISE VOLTAGE



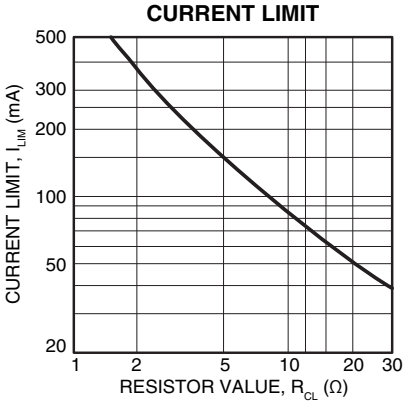
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex Precision Power product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex Precision Power product data sheets, visit www.Cirrus.com.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 1.4 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

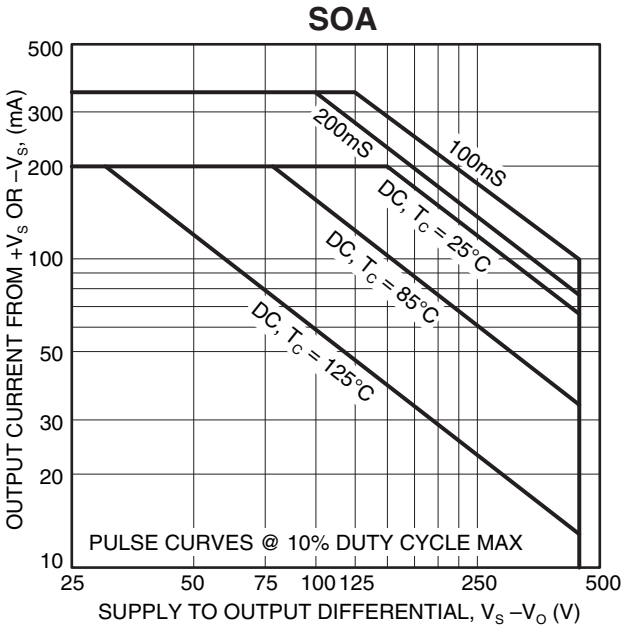
$$R_{CL} = \frac{.7}{I_{LIM} - .016}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

INPUT PROTECTION

Although the PA85 can withstand differential voltages up to ±25V, additional external protection is recommended. Since the PA85 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA85 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

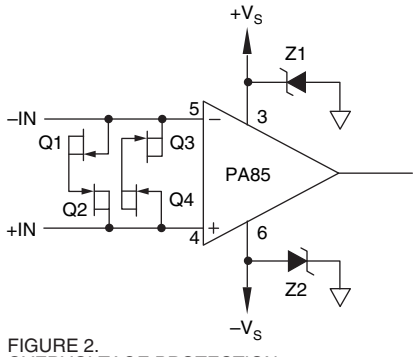
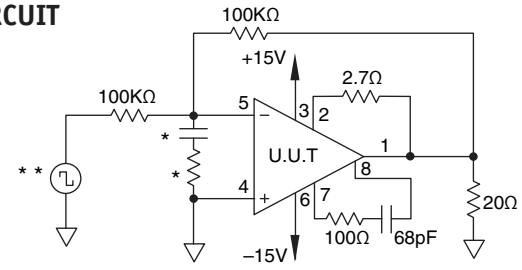


FIGURE 2.
OVERVOLTAGE PROTECTION

Table 4 Group A Inspection

SG	PARAMETER***	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		25	mA
1	Input offset voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		±4	mV
1	Input offset voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		±2	mV
1	Input bias current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input bias current, –IN	$–I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input offset current	I_{OS}	25°C	±150V	V_{IN} = 0		±100	pA
3	Quiescent current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		28	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		±6.4	mV
3	Input offset voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		±4.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input bias current, –IN	$–I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input offset current	I_{OS}	–55°C	±150V	V_{IN} = 0		±50	pA
2	Quiescent current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		28	mA
2	Input offset voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		±7	mV
2	Input offset voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		±5	mV
2	Input bias current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input bias current, –IN	$–I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input offset current	I_{OS}	125°C	±150V	V_{IN} = 0		±10	nA
4	Output voltage, I_O = 200mA	V_O	25°C	±50V	R_L = 200Ω	40		V
4	Output voltage, I_O = 70mA	V_O	25°C	±150V	R_L = 2KΩ	141		V
4	Output voltage, I_O = 20mA	V_O	25°C	±48V	R_L = 2KΩ	40		V
4	Current limits	I_{CL}	25°C	±50V	R_{CL} = 10Ω, R_L = 200Ω	60	112	mA
4	Stability/noise	E_N	25°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
4	Slew rate	SR	25°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
4	Open loop gain	A_{OL}	25°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
4	Common-mode rejection	CMR	25°C	±150V	F = DC, V_{CM} = ±90V	90		dB
6	Output voltage, I_O = 200mA	V_O	–55°C	±50V	R_L = 200Ω	40		V
6	Output voltage, I_O = 70mA	V_O	–55°C	±150V	R_L = 2KΩ	141		V
6	Output voltage, I_O = 20mA	V_O	–55°C	±48V	R_L = 2KΩ	40		V
6	Stability/noise	E_N	–55°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
6	Slew rate	SR	–55°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
6	Open loop gain	A_{OL}	–55°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
6	Common-mode rejection	CMR	–55°C	±150V	F = DC, V_{CM} = ±90V	90		dB
5	Output voltage, I_O = 150mA	V_O	125°C	±40V	R_L = 200Ω	30		V
5	Output voltage, I_O = 70mA	V_O	125°C	±150V	R_L = 2KΩ	141		V
5	Output voltage, I_O = 20mA	V_O	125°C	±48V	R_L = 2KΩ	40		V
5	Stability/noise	E_N	125°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
5	Slew rate	SR	125°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
5	Open loop gain	A_{OL}	125°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
5	Common-mode rejection	CMR	125°C	±150V	F = DC, V_{CM} = ±90V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

*** An additional test is performed manually at T_C = 25°C which stresses power supply, common mode range and output swing to ±225V (450V total).

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- A Unique (Patent Pending) Technique for Very Low Quiescent Current
- Over 350 V/µs Slew Rate
- Wide Supply Voltage
  - Single Supply: 20V To 250V
  - Split Supplies: ± 10V To ± 125V
- Output Current – 150mA Cont.; 200mA Pk
- Up to 23 Watt Dissipation Capability
- Over 200 kHz Power Bandwidth

APPLICATIONS

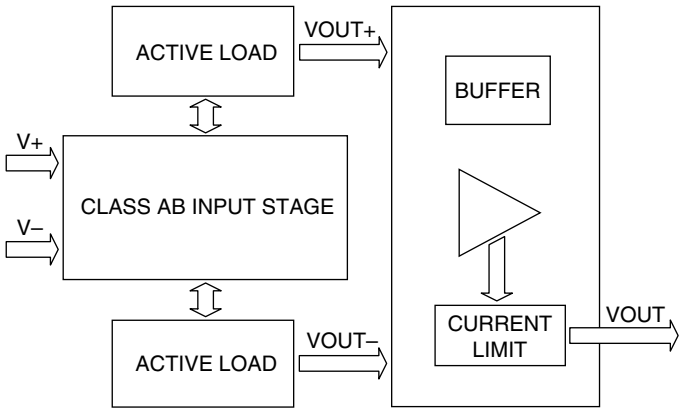
- Piezoelectric Positioning and Actuation
- Electrostatic Deflection
- Deformable Mirror Actuators
- Chemical and Biological Stimulators

DESCRIPTION

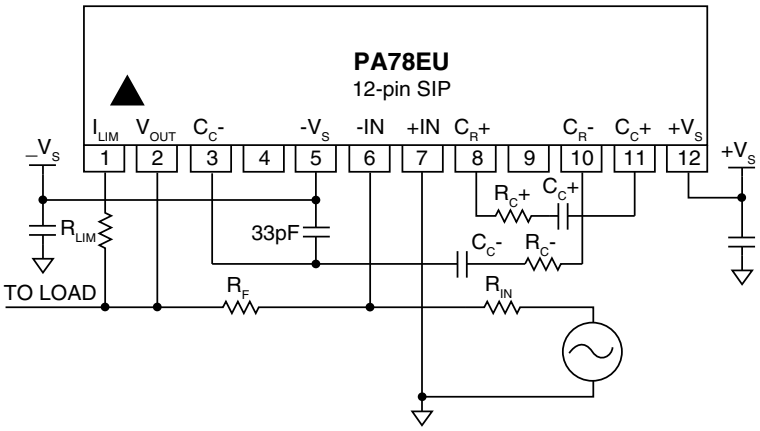
The PA86 is a high voltage, high speed, low idle current op-amp capable of delivering up to 200mA peak output current. Due to the dynamic biasing of the input stage, it can achieve slew rates over 350V/µs, while only consuming less than 1mA of idle current. External phase compensation allows great flexibility for the user to optimize bandwidth and stability.

The output stage is protected with user selected current limit resistor. For the selection of this current limiting resistor, pay close attention to the SOA curves for each package type. Proper heatsinking is required for maximum reliability.

BLOCK DIAGRAM



EXTERNAL CONNECTIONS



12–Pin SIP
PACKAGE STYLE EU
LEAD FORM EW

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			250	V
OUTPUT CURRENT, peak (200ms), within SOA			200	mA
POWER DISSIPATION, internal, DC			23	W
INPUT VOLTAGE, differential		−15	15	V
INPUT VOLTAGE, common mode		$-V_S$	$+V_S$	V
TEMPERATURE, pin solder, 10s			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−55	125	°C
OPERATING TEMPERATURE, case		−40	125	°C

SPECIFICATIONS

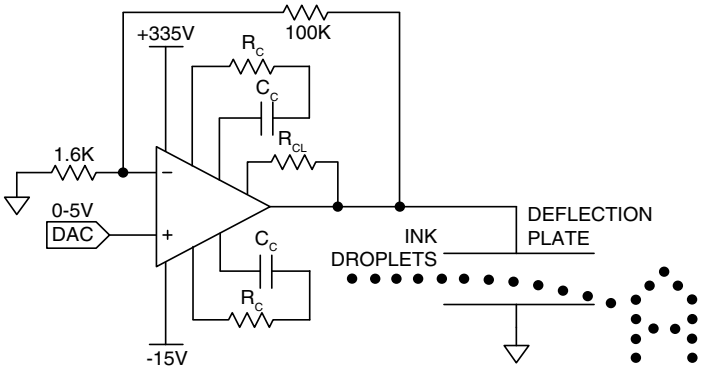
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE		-25	8	25	mV
OFFSET VOLTAGE vs. temperature	0 to 125°C (Case Temperature)		-63		µV/°C
OFFSET VOLTAGE vs. supply				32	µV/V
BIAS CURRENT, initial			8.5	200	pA
OFFSET CURRENT, initial			12	400	pA
INPUT RESISTANCE, DC			10^8		Ω
COMMON MODE VOLTAGE RANGE, pos.			$+V_S$ - 2		V
COMMON MODE VOLTAGE RANGE, neg.			$-V_S$ + 5.5		V
COMMON MODE REJECTION, DC		90	118		dB
NOISE	700KHz		418		µV RMS
NOISE, V_O NOISE			500		nV/√Hz
GAIN					
OPEN LOOP @ 1Hz		89	120		dB
GAIN BANDWIDTH PRODUCT @ 1MHz			1		MHz
PHASE MARGIN	Full temperature range		50		°
OUTPUT					
VOLTAGE SWING	I_O = 10mA		$\|V_S\|$ - 2		V
VOLTAGE SWING	I_O = 100mA		$\|V_S\|$ - 8.6	$\|V_S\|$ - 12	V
VOLTAGE SWING	I_O = 150mA		$\|V_S\|$ - 10		V
CURRENT, continuous, DC		150			mA
SLEW RATE	**Package Tab connected to GND**	100	350		V/µS
SETTLING TIME, to 0.1%	5V Step (No Compensation)		1		µS
POWER BANDWIDTH, $300V_{P-P}$	$+V_S$ = 160V, $-V_S$ = -160V		200		kHz
OUTPUT RESISTANCE, No load	R_{CL} = 6.2Ω		44		Ω
POWER SUPPLY					
VOLTAGE		±10	±50	±125	V
CURRENT, quiescent (Note 5)	±120V Supply	0.2	0.7	2.5	mA

Parameter	Test Conditions	Min	Typ	Max	Units
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range		5.5		ºC/W
RESISTANCE, DC, junction to air	Full temperature range		12.21		ºC/W
TEMPERATURE RANGE, case		-40		125	ºC

NOTES: 1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative supply voltages of the output stage.
4. Rating applies if output current alternates between both output transistors at a rate faster than 60Hz.
5. Supply current increases with signal frequency. See graph on page 4.

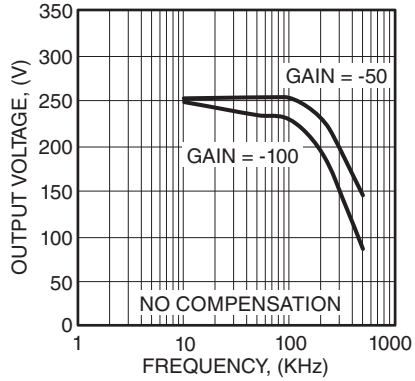
TYPICAL APPLICATION CIRCUIT

The PA86 is ideally suited for driving continuous drop ink jet printers, in both piezo actuation and deflection applications. The high voltage of the amplifier creates an electrostatic field on the deflection plates to control the position of the ink droplets. The rate at which droplets can be printed is directly related to the rate at which the amplifier can drive the plate to a different electrostatic field strength.

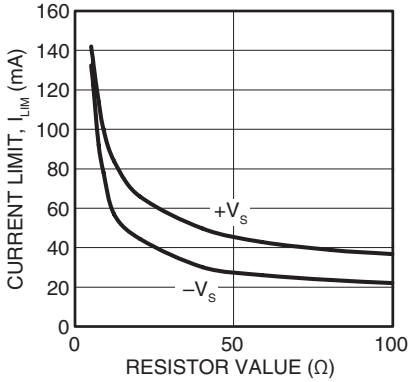


TYPICAL PERFORMANCE GRAPHS

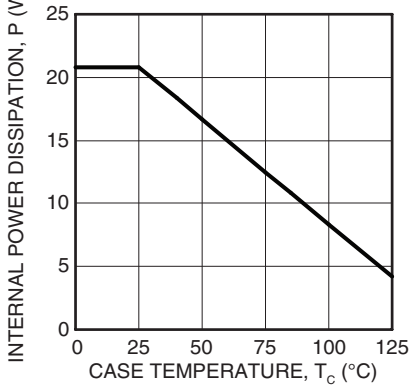
POWER RESPONSE



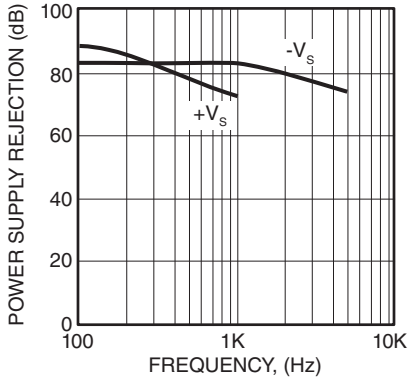
CURRENT LIMIT



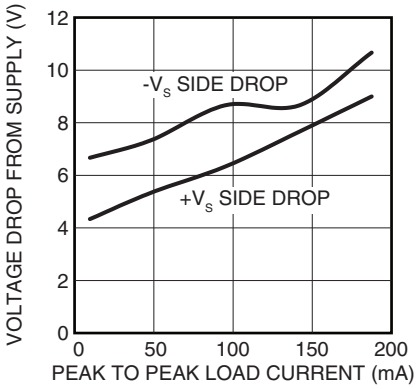
POWER DERATING



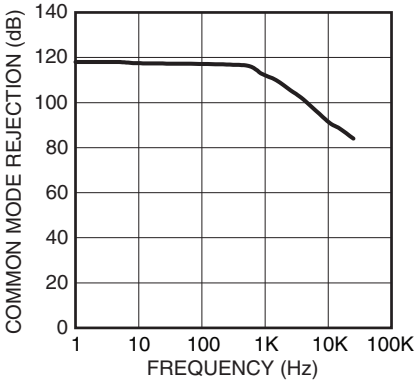
POWER SUPPLY REJECTION



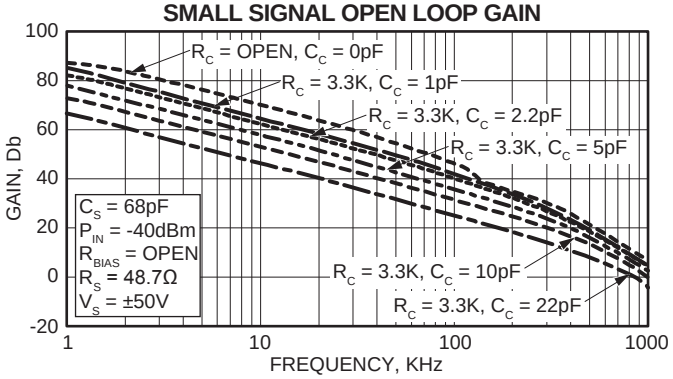
OUTPUT VOLTAGE SWING



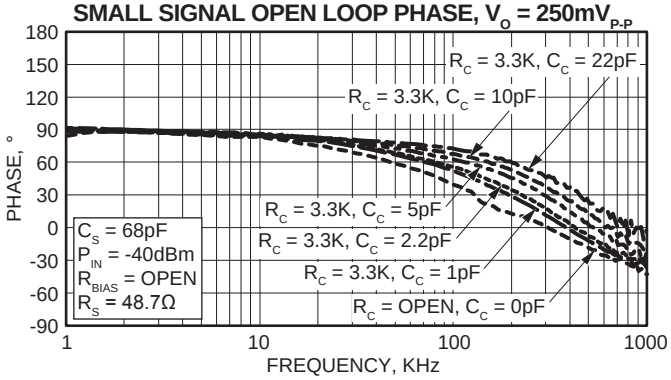
COMMON MODE REJECTION



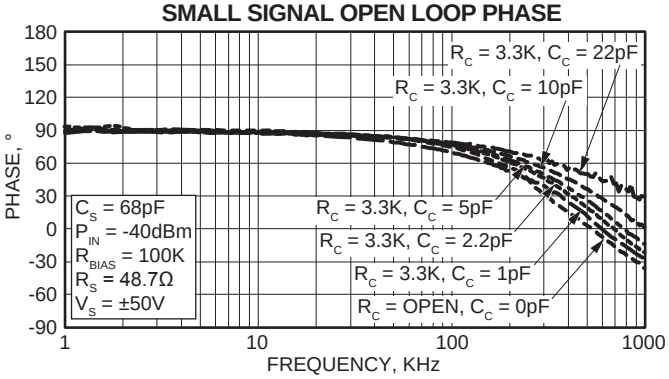
SMALL SIGNAL OPEN LOOP GAIN



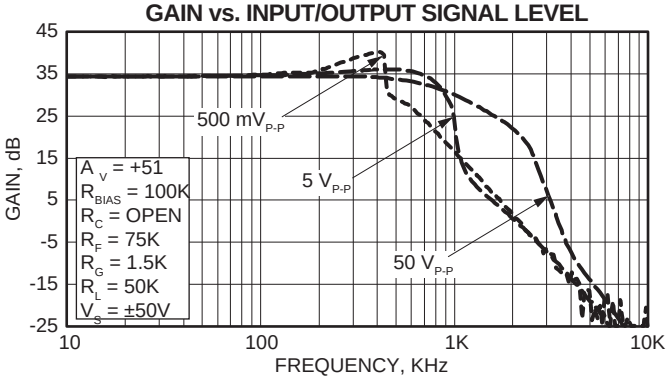
SMALL SIGNAL OPEN LOOP PHASE, V_O = 250mV$_{P-P}$



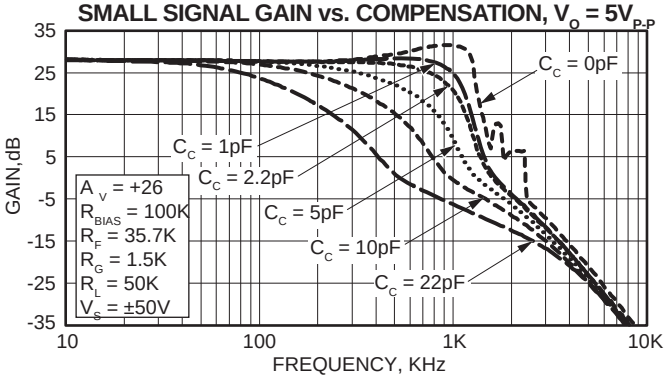
SMALL SIGNAL OPEN LOOP PHASE



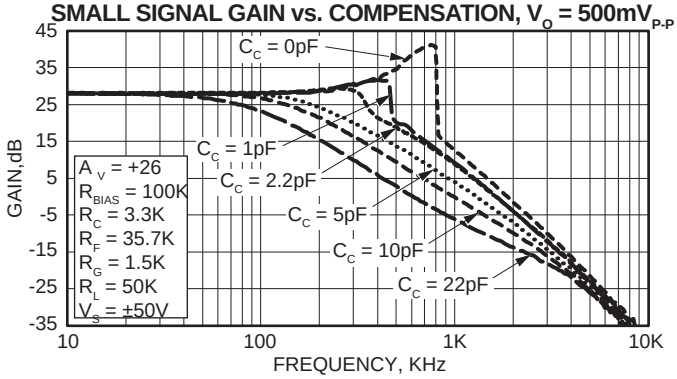
GAIN vs. INPUT/OUTPUT SIGNAL LEVEL



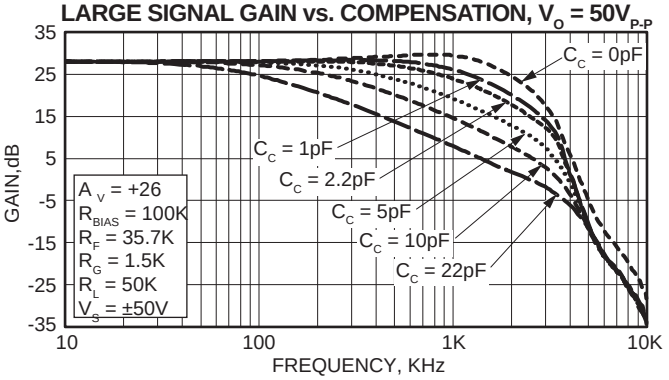
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 5V$_{P-P}$



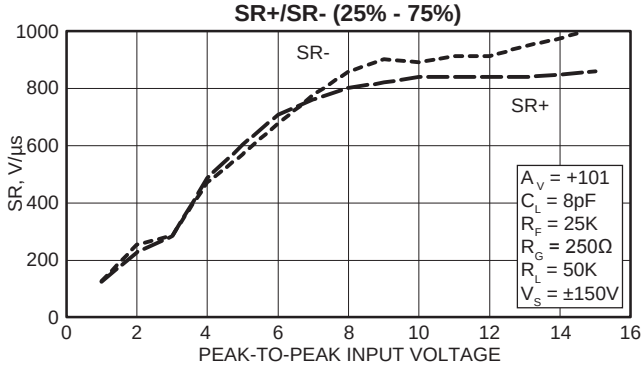
SMALL SIGNAL GAIN vs. COMPENSATION, V_O = 500mV$_{P-P}$



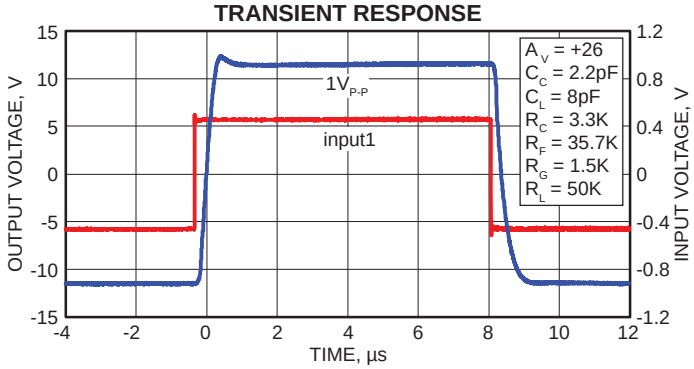
LARGE SIGNAL GAIN vs. COMPENSATION, V_O = 50V$_{P-P}$



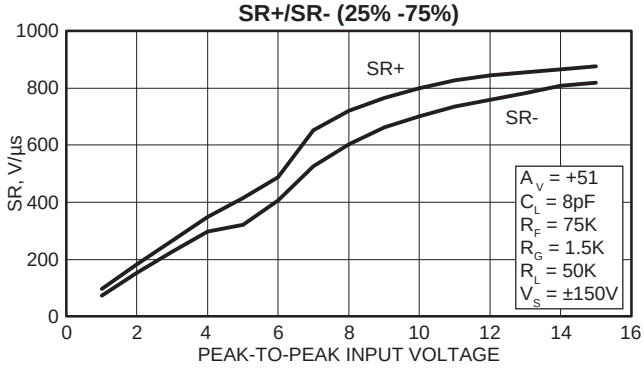
SR+/SR- (25% - 75%)



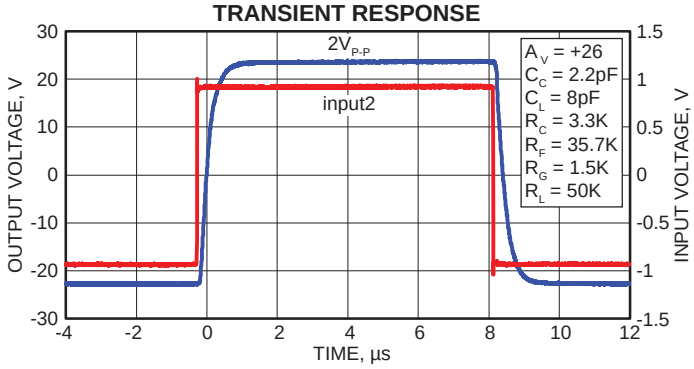
TRANSIENT RESPONSE



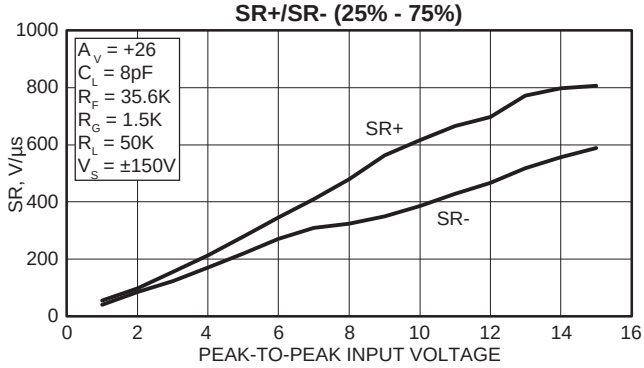
SR+/SR- (25% -75%)



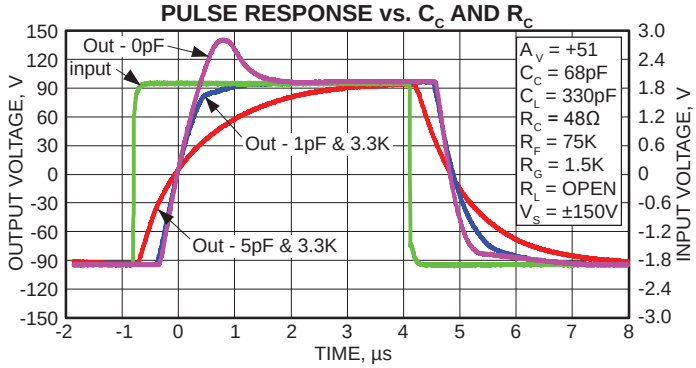
TRANSIENT RESPONSE



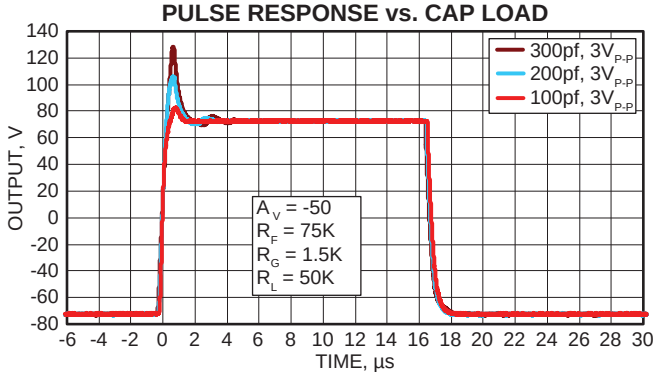
SR+/SR- (25% - 75%)



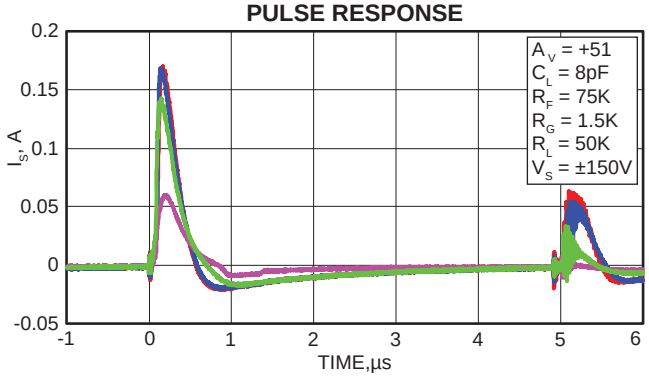
PULSE RESPONSE vs. C_C AND R_C



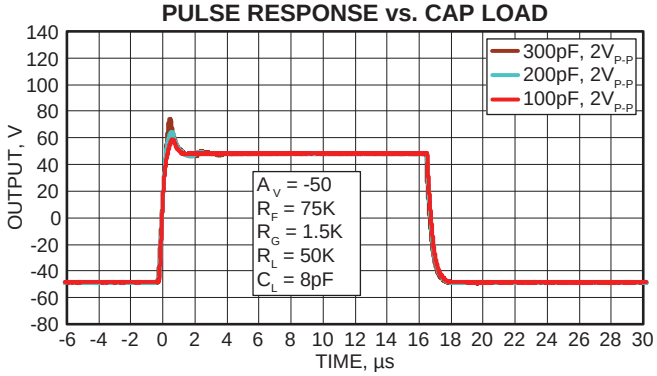
PULSE RESPONSE vs. CAP LOAD



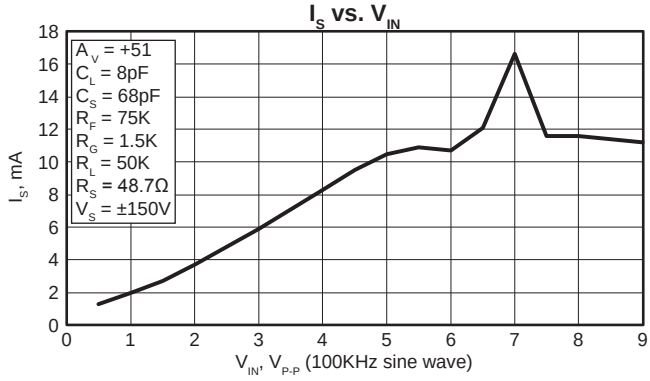
PULSE RESPONSE



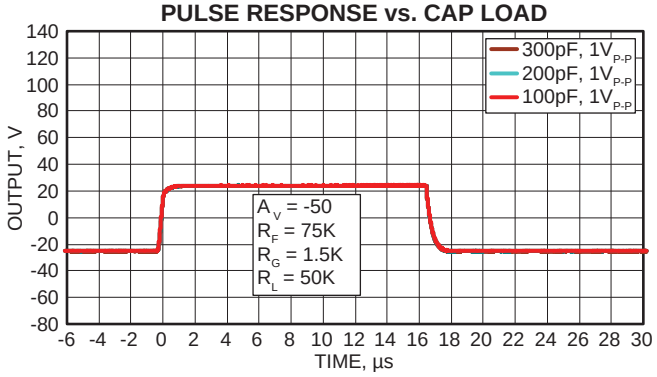
PULSE RESPONSE vs. CAP LOAD



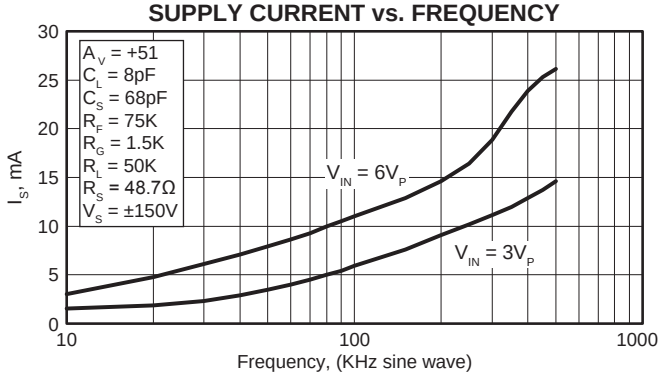
I_S vs. V_{IN}



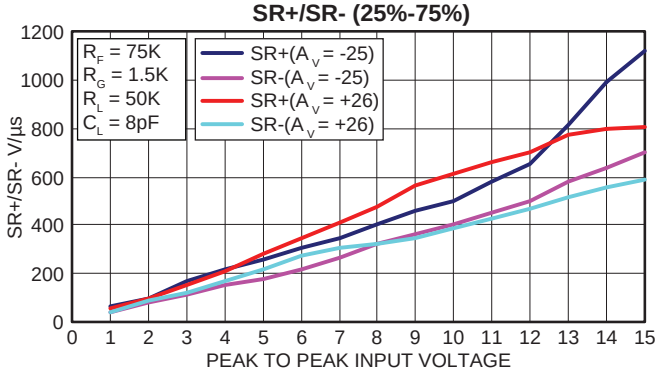
PULSE RESPONSE vs. CAP LOAD



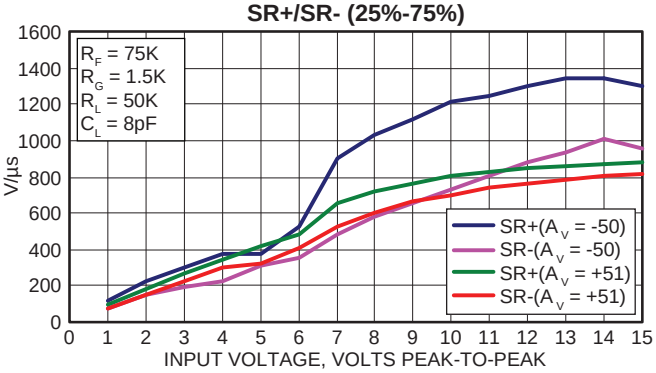
SUPPLY CURRENT vs. FREQUENCY



SR+/SR- (25%-75%)



SR+/SR- (25%-75%)



GENERAL

Please read Application note 1 “General operating considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, and current limit. There you will also find a complete application notes library, technical seminar workbook, and evaluation kits.

THEORY OF OPERATION

The PA86 is designed specifically as a high speed pulse amplifier. In order to achieve high slew rates with low idle current, the internal design is quite different from traditional voltage feedback amplifiers. Basic op amp behaviors like high input impedance and high open loop gain still apply. But there are some notable differences, such as signal dependent supply current, bandwidth and output impedance, among others. The impact of these differences varies depending on application performance requirements and circumstances. These different behaviors are ideal for some applications but can make designs more challenging in other circumstances.

SUPPLY CURRENT AND BYPASS CAPACITANCE

A traditional voltage feedback amplifier relies on fixed current sources in each stage to drive the parasitic capacitances of the next stage. These currents combine to define the idle or quiescent current of the amplifier. By design, these fixed currents are often the limiting parameter for slew rate and bandwidth of the amplifier. Amplifiers which are high voltage and have fast slew rates typically have high idle currents and dissipate notable power with no signal applied to the load. At the heart of the PA86 design is a signal dependent current source which strikes a new balance between supply current and dynamic performance. With small input signals, the supply current of the PA86 is very low, idling at less than 1 mA. With large transient input signals, the supply currents increase dramatically to allow the amplifier stages to respond quickly. The Pulse Response plot in the typical performance section of this datasheet describes the dynamic nature of the supply current with various input transients.

Choosing proper bypass capacitance requires careful consideration of the dynamic supply currents. High frequency ceramic capacitors of 0.1µF or more should be placed as close as possible to the amplifier supply pins. The inductance of the routing from the supply pins to these ceramic capacitors will limit the supply of peak current during transients, thus reducing the slew rate of the PA86. The high frequency capacitance should be supplemented by additional bypass capacitance not more than a few centimeters from the amplifier. This additional bypass can be a slower capacitor technology, such as electrolytic, and is necessary to keep the supplies stable during sustained output currents. Generally, a few microfarad is sufficient.

SMALL SIGNAL PERFORMANCE

The small signal performance plots in the typical performance section of this datasheet describe the behavior when the dynamic current sources described previously are near the idle state. The selection of compensation capacitor directly affects the open loop gain and phase performance.

Depending on the configuration of the amplifier, these plots show that the phase margin can diminish to very low levels when left uncompensated. This is due to the amount of bias current in the input stage when the part is in standby. An increase in the idle current in the output stage of the amplifier will improve phase margin for small signals although will increase the overall supply current.

Current can be injected into the output stage by adding a resistor, R_{BIAS}, between C_C- and V_S+. The size of R_{BIAS} will depend upon the application but 500µA of added bias current shows significant improvement in the small signal phase plots. Adding this resistor has little to no impact on small signal gain or large signal performance as under these conditions the current in the input stage is elevated over its idle value. It should also be noted that connecting a resistor to the upper supply only injects a fixed current and if the upper supply is fixed and well bypassed. If the application includes variable or adjustable supplies, a current source diode could also be used. These two terminal components combine a JFET and resistor connected within the package to behave like a current source.

As a second stability measure, the PA86 is externally compensated and performance can be optimized to the application. Unlike the R_{BIAS} technique, external phase compensation maintains the low idle current but does affect the large signal response of the amplifier. Refer to the small and large signal response plots as a guide in making the tradeoffs between bandwidth and stability. Due to the unique design of the PA86, two symmetric compensation networks are required. The compensation capacitor Cc must be rated for a working voltage of the full operating

supply voltage ($+V_S$ to $-V_S$). NPO capacitors are recommended to maintain the desired level of compensation over temperature.

The PA86 requires an external 33pF capacitor between C_C- and $-V_S$ to prevent oscillations in the falling edge of the output. This capacitor should be rated for the full supply voltage ($+V_S$ to $-V_S$).

LARGE SIGNAL PERFORMANCE

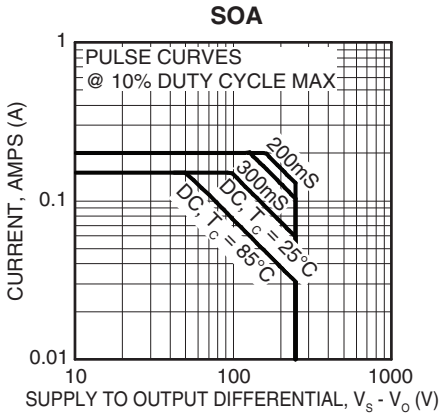
As the amplitude of the input signal increases, the internal dynamic current sources increase the operation bandwidth of the amplifier. This unique performance is apparent in its slew rate, pulse response, and large signal performance plots. Recall the previous discussion about the relationships between signal amplitude, supply current, and slew rate. As the amplitude of the input amplitude increases from $1V_{P-P}$ to $15V_{P-P}$, the slew rate increases from 50V/µs to well over 350V/µs.

The output becomes clipped by the supply rails and the amplifier is no longer operating in a closed loop fashion. The rise and fall times become faster as the dynamic current sources are providing maximum current for slewing. The result of this amplifier architecture is that it slews fast, but allows good control of overshoot for large input signals. This can be seen clearly in the large signal Transient Response plots.

HEATSINKING AND SAFE OPERATING AREA

The MOSFET output stage of the PA86 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations of the package and current handling capabilities limit the Safe Operating Area. The SOA plots include power dissipation limitations which are dependent upon case temperature. Keep in mind that the dynamic current sources which drive high slew rates can increase the operating temperature of the amplifier during periods of repeated slewing. The plot of supply current vs. input signal amplitude for a 100 kHz signal provides an indication of the supply current with repeated slewing conditions. This application dependent condition must be considered carefully.

The output stage is self-protected against transient flyback by the parasitic body diodes of the output stage. However, for protection against sustained high energy flyback, external, fast recovery diodes must be used.



CURRENT LIMIT

For proper operation, the current limit resistor, R_{LIM}, must be connected as shown in the external connections diagram. For maximum reliability and protection, the largest resistor value should be used. The minimum practical value for R_{LIM} is about 12Ω. However, refer to the SOA curves for each package type to assist in selecting the optimum value for R_{LIM} in the intended application. Current limit may not protect against short circuit conditions with supply voltages over 200V.

LAYOUT CONSIDERATIONS

The PA86 is built on a dielectrically isolated process and the package tab is therefore not electrically connected to the amplifier. For high speed operation, the package tab should be connected to a stable reference to reduce capacitive coupling between amplifier nodes and the floating tab. It is often convenient to directly connect the tab to GND or one of the supply rails, but an AC connection through a 1µF capacitor to GND is also sufficient if a DC connection is undesirable

Care should be taken to position the R_C / C_C compensation networks close to the amplifier compensation pins. Long loops in these paths pick up noise and increase the likelihood of LC interactions and oscillations.

ELECTROSTATIC DISCHARGE

Like many high performance MOSFET amplifiers, the PA86 very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operating performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- LOW QUIESCENT CURRENT — 2mA
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT
- LOW BIAS CURRENT — FET Input

PATENTED

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

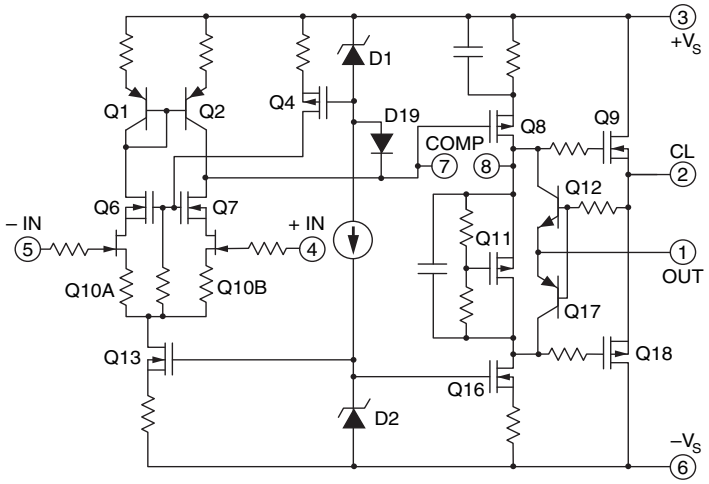
- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V

DESCRIPTION

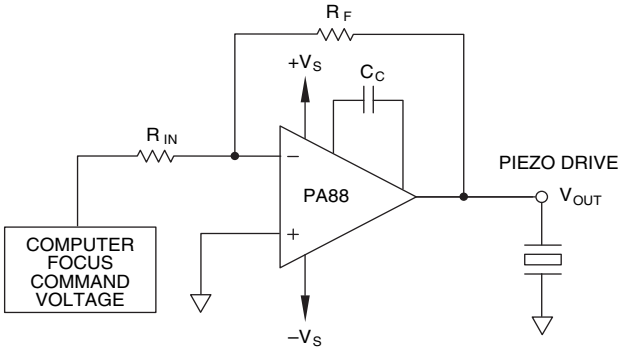
The PA88 is a high voltage, low quiescent current MOSFET operational amplifier designed for output currents up to 100mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA88 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



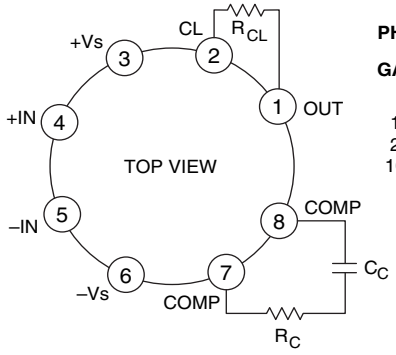
TYPICAL APPLICATION



LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA88's advantage of low quiescent power consumption reduces the costs of power supplies and cooling, while providing the interface between the computer and the high voltage drive to the piezo positioners.

EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	68pf	100W
10	33pf	100W
20	15pf	100W
100	3.3pf	—

$$R_{CL} = \frac{.7}{I_{LIM}}$$

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ T_C = 25°C	15W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA88 MIN	PA88 TYP	PA88 MAX	PA88A MIN	PA88A TYP	PA88A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			1	5		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			2.5	100		3	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S$–15			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 15pf		2			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 15pf, R_C = 100Ω		2.1			*		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = 15pf, R_C = 100Ω		6			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	Full temp. range, I_O = ±75mA	$\pm V_S$–16	$\pm V_S$–14		*	*		V
VOLTAGE SWING[4]	Full temp. range, I_O = ±20mA	$\pm V_S$–10	$\pm V_S$–5.2		*	*		V
CURRENT, continuous	T_C = 85°C	±100				*		mA
SLEW RATE, A_V = 20	C_C = 15pf, R_C = 100Ω		8			*		V/µs
SLEW RATE, A_V = 100	C_C = OPEN		30			*		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			*			pf
SETTLING TIME to .1%	C_C = 15pf, R_C = 100Ω, 2V step		10			*		µs
RESISTANCE, no load	R_{CL} = 0		100			*		Ω
POWER SUPPLY								
VOLTAGE[6]	See note 6	±15	±200	±225	*	*	*	V
CURRENT, quiescent,			1.7	2		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			5.0			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			8.3			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA88A is identical to the specification for PA88 in applicable column to the left.

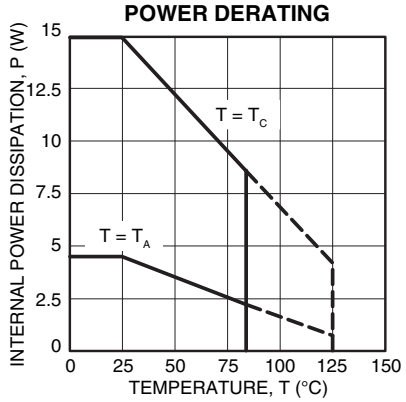
1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION

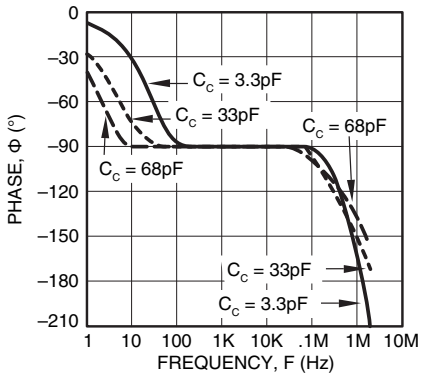
The PA88 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

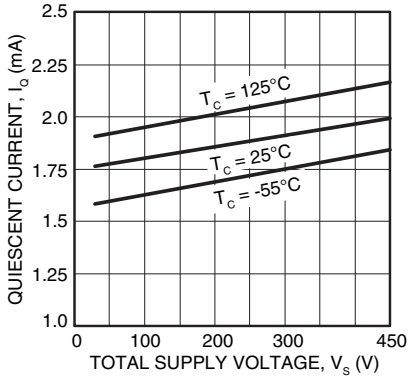
POWER DERATING



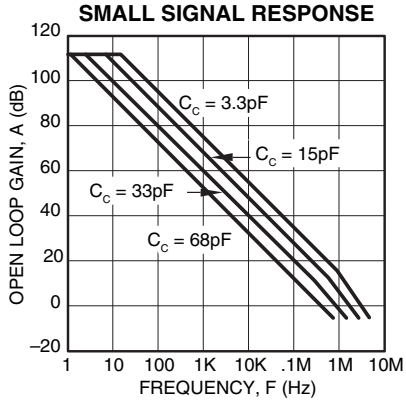
PHASE RESPONSE



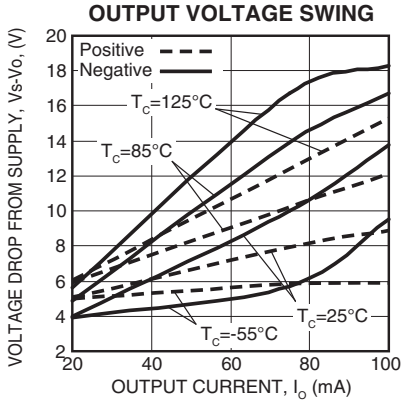
QUIESCENT CURRENT



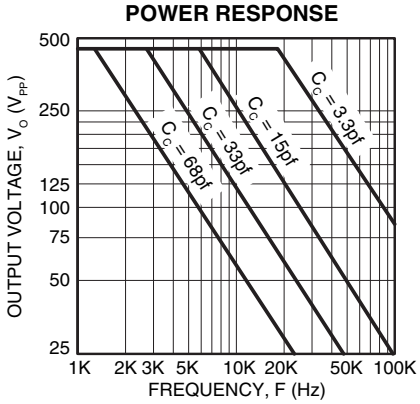
SMALL SIGNAL RESPONSE



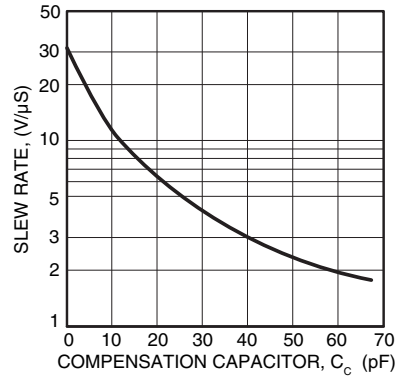
OUTPUT VOLTAGE SWING



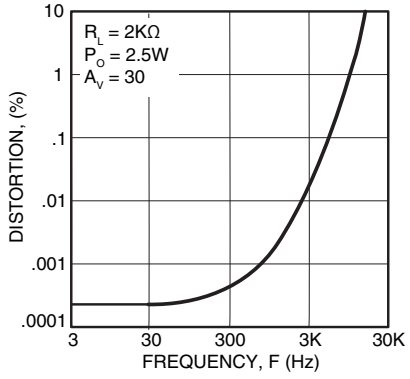
POWER RESPONSE



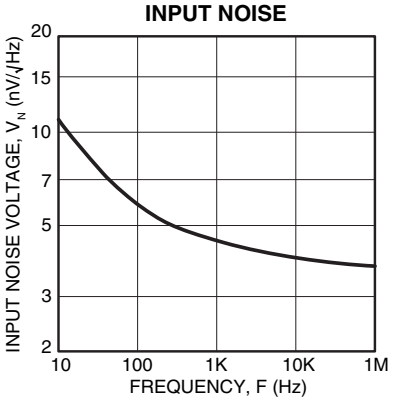
SLEW RATE



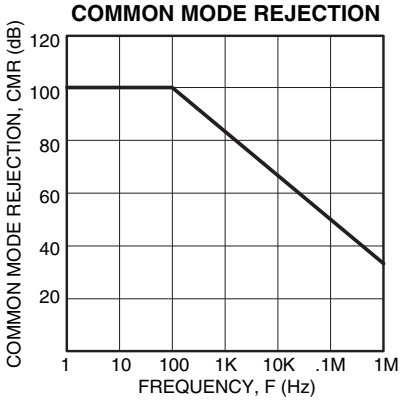
HARMONIC DISTORTION



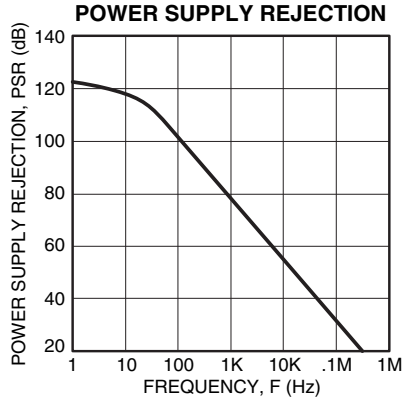
INPUT NOISE



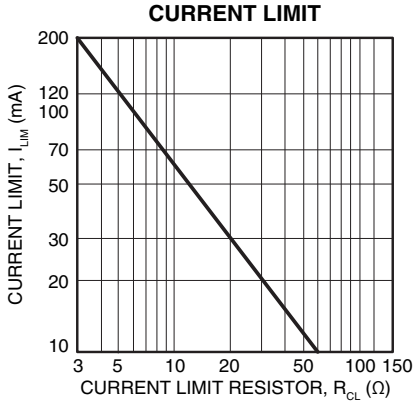
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

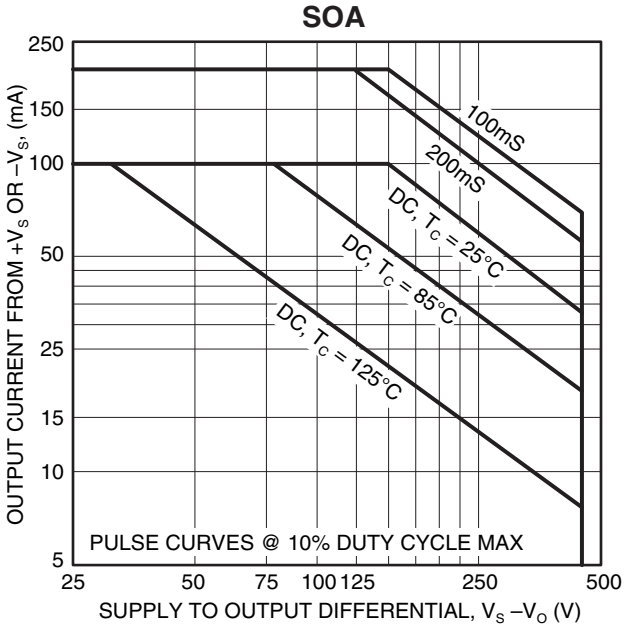
For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INPUT PROTECTION

Although the PA88 can withstand differential input voltages up to ±25V, additional external protection is recommended, and required at total supply voltages above 300 volts. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 2b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA88 has sufficient phase margin to be stable with most capacitive loads at a gain of 4 or more, using the recommended phase compensation.

The PA88 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

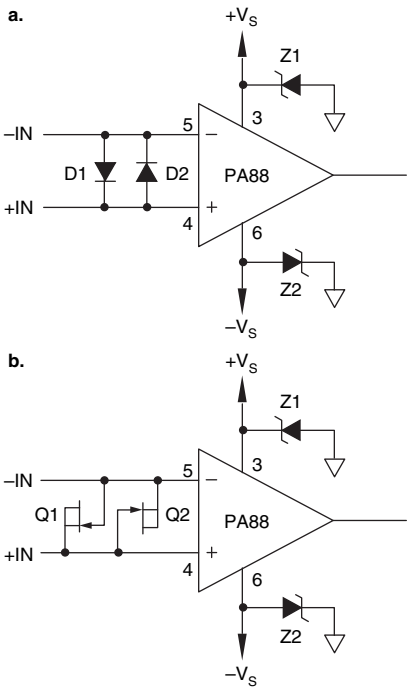


FIGURE 2. OVERVOLTAGE PROTECTION

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- 1140V P-P SIGNAL OUTPUT
- WIDE SUPPLY RANGE — ±75V to ±600V
- PROGRAMMABLE CURRENT LIMIT
- 75 mA CONTINUOUS OUTPUT CURRENT
- HERMETIC SEALED PACKAGE
- INPUT PROTECTION

PATENTED

HIGH VOLTAGE MO-127
PACKAGE STYLE DC

APPLICATIONS

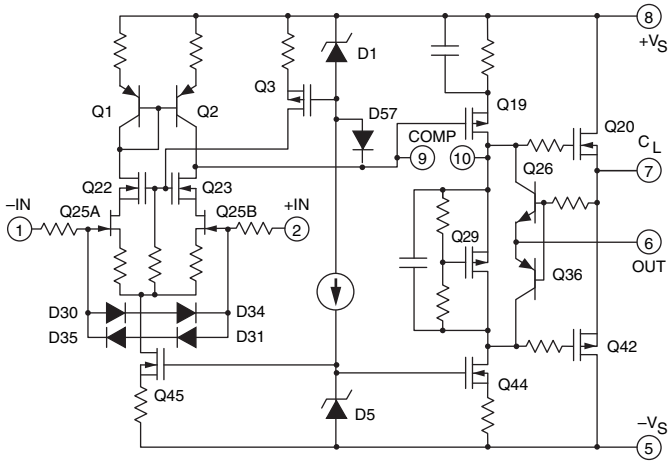
- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC DEFLECTION
- SEMICONDUCTOR TESTING

DESCRIPTION

The PA89 is an ultra high voltage, MOSFET operational amplifier designed for output currents up to 75 mA. Output voltages can swing over 1000V p-p. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration and 120dB open loop gain. All internal biasing is referenced to a bootstrapped zener-MOSFET current source, giving the PA89 a wide supply range and excellent supply rejection. The MOSFET output stage is biased for class A/B linear operation. External compensation provides user flexibility. The PA89 is 100% gross leak tested to military standards for long term reliability.

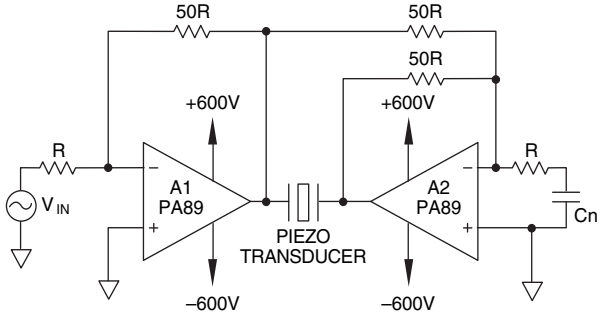
This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 High Voltage, Power Dip™ package is hermetically sealed and electrically isolated. The use of compressible thermal washers will void the product warranty.

SIMPLIFIED SCHEMATIC



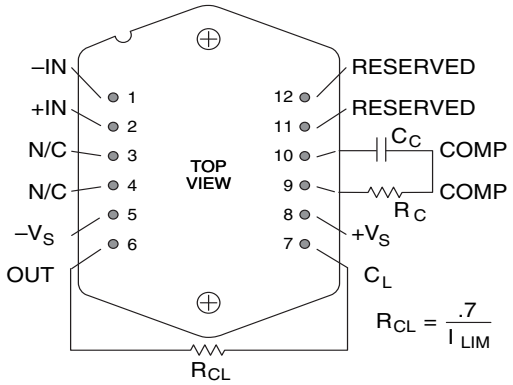
TYPICAL APPLICATION

Ultra-high voltage capability combined with the bridge amplifier configuration makes it possible to develop +/–1000 volt peak swings across a piezo element. A high gain of –50 for A1 insures stability with the capacitive load, while "noise-gain" compensation Rn and Cn on A2 insure the stability of A2 by operating in a noise gain of 50.



SINGLE AXIS MICRO-POSITIONING

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	470Ω
10	68pF	220Ω
15	33pF	220Ω
100	15pF	220Ω

Note: C_C must be rated for full supply voltage –Vs to +Vs. See details under "EXTERNAL COMPONENTS".

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	1200V
OUTPUT CURRENT, within SOA	100mA
POWER DISSIPATION, internal at T_C = 25°C	40W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S \mp 25V$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to 125°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA89 MIN	PA89 TYP	PA89 MAX	PA89A MIN	PA89A TYP	PA89A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			7			*		µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT,vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			5	50		3	20	pA
INPUT IMPEDANCE, DC			10^5			*		MΩ
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S \mp 50$			*			V
COMMON MODE REJECTION, DC	Full temperature range, V_{CM} = ±90V	96	110		*	*		dB
INPUT NOISE	10kHz BW, R_S = 10K, C_C = 15pF		4					µV RMS
GAIN								
OPEN LOOP GAIN at 10Hz	R_L = 10k, C_C = 15pF	108	120		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L = 10k, C_C = 15pF, A_V = 100		10			*		MHz
POWER BANDWIDTH	R_L = 10k, C_C = 15pF, V_O = 500V p-p		5			*		kHz
PHASE MARGIN	Full temperature range, A_V = 10		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = 75mA	$\pm V_S \mp 45$	$\pm V_S \mp 30$		*	*		V
VOLTAGE SWING[4]	Full temperature range, I_O = 20mA	$\pm V_S \mp 20$	$\pm V_S \mp 12$		*	*		V
CURRENT, continuous	Full temperature range	75			*			mA
SLEW RATE	C_C = 15pF, A_V = 100	12	16		*	*		V/µs
CAPACITIVE LOAD, Av = 10	Full temperature range			1			*	nF
CAPACITIVE LOAD, Av>10	Full temperature range			SOA			*	
SETTLING TIME to .1%	R_L = 10KΩ, 10V step, Av = 10		2			*		µs
POWER SUPPLY								
VOLTAGE, V_S[4]	Full temperature range	±75	±500	±600	*	*	*	V
CURRENT, quiescent			4.8	6.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz		2.1	2.3		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz		3.3	3.5		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		15			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA89A is identical to the specification for PA89 in applicable column to the left.

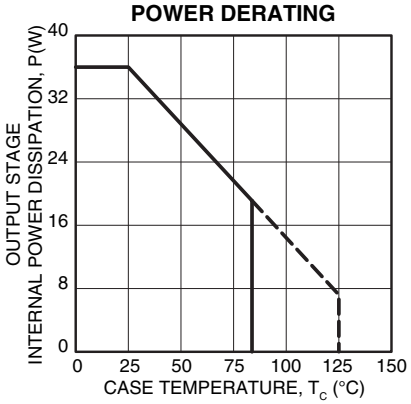
1. Unless otherwise noted: T_C = 25°C, C_C = 68pF, R_C = 220Ω, and V_S = ±500V. Input parameters for bias currents and offset voltage are ± values given.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION

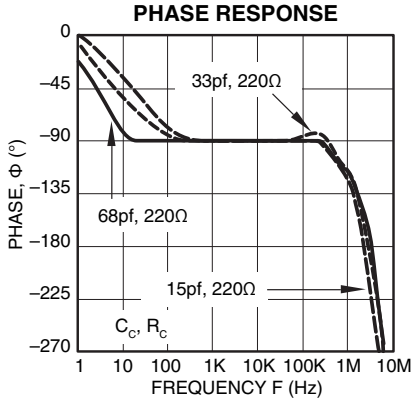
The PA89 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

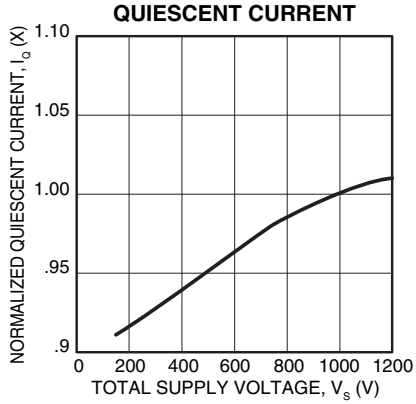
POWER DERATING



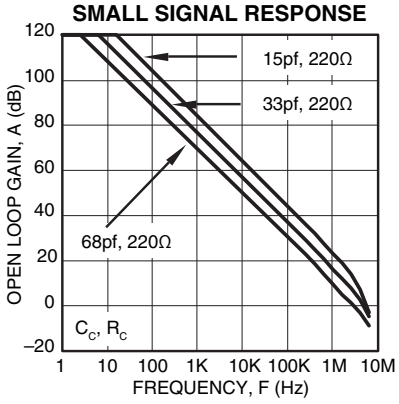
PHASE RESPONSE



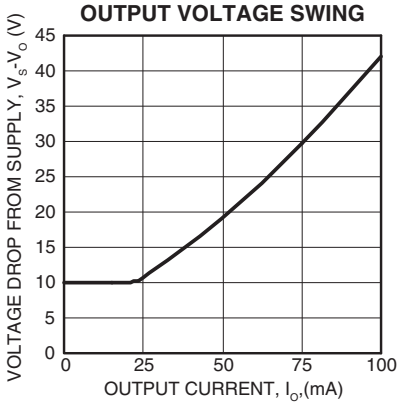
QUIESCENT CURRENT



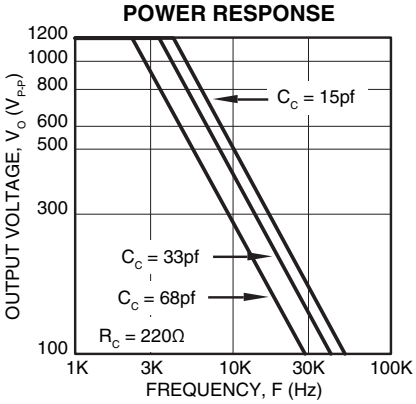
SMALL SIGNAL RESPONSE



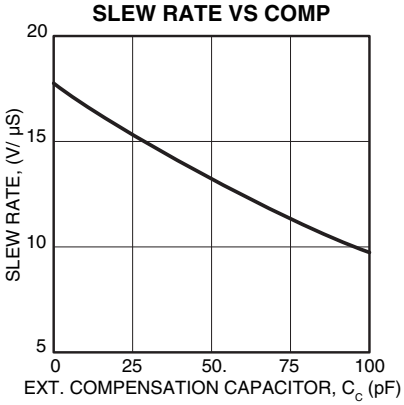
OUTPUT VOLTAGE SWING



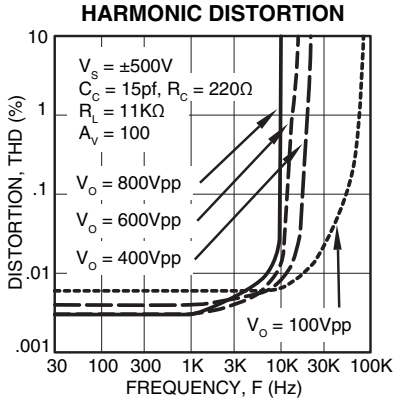
POWER RESPONSE



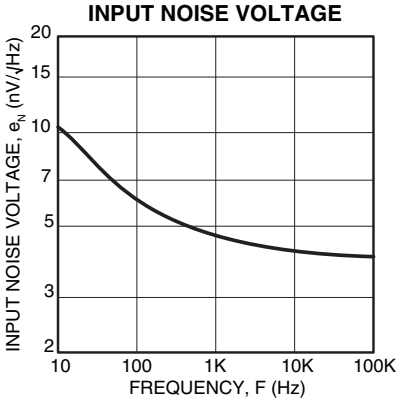
SLEW RATE VS COMP



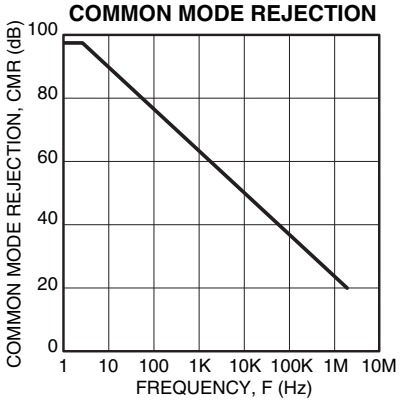
HARMONIC DISTORTION



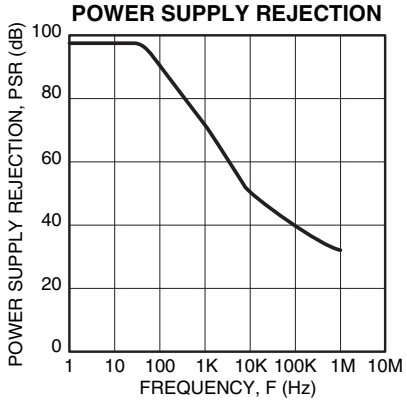
INPUT NOISE VOLTAGE



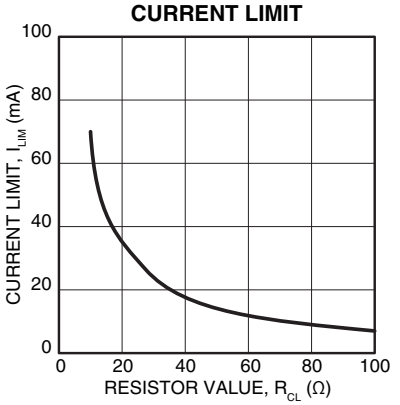
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



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GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

STABILITY

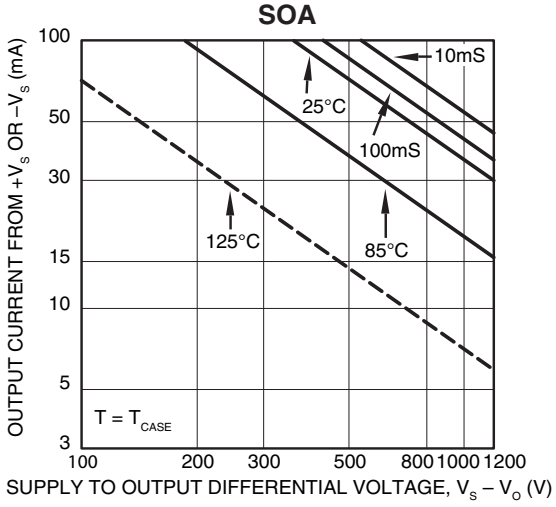
Although the PA89 can be operated at unity gain, maximum slew rate and bandwidth performance was designed to be obtained at gains of 10 or more. Use the small signal response and phase response graphs as a guide. In applications where gains of less than 10 are required, use noise gain compensation to increase the phase margin of the application circuit as illustrated in the typical application drawing.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

EXTERNAL COMPONENTS

The very high operating voltages of the PA89 demand consideration of two component specifications rarely of concern in building op amp circuits: voltage rating and voltage coefficient.

The compensation capacitance C_C must be rated for the full supply voltage range. For example, with supply voltages of ±500V the possible voltage swing across C_C is 1000V. In addition, a voltage coefficient less than 100PPM is recommended to maintain the capacitance variation to less than 5% for this example. It is strongly recommended to use the highest quality capacitor possible rated at least twice the total supply voltage range.

Of equal importance are the voltage rating and voltage coefficient of the gain setting resistances. Typical voltage ratings of low wattage resistors are 150 to 250V. In the above example 1000V could appear across the feedback resistor. This would require several resistors in series to obtain the proper voltage rating. Low voltage coefficient resistors will insure good gain linearity. The wattage rating of the feedback resistor is also of concern. A 1 megohm feedback resistor could easily develop 1 watt of power dissipation.

Though high voltage rated resistors can be obtained, a 1 megohm feedback resistor comprised of five 200Kohm, 1/4 watt metal film resistors in series will produce the proper voltage rating, voltage coefficient and wattage rating.

CURRENT LIMIT

For proper operation the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

When setting the value for R_{CL} allow for the load current as well as the current in the feedback resistor. Also allow for the temperature coefficient of the current limit which is approximately -0.3%/°C of case temperature rise.

CAUTIONS

The operating voltages of the PA89 are potentially lethal. During circuit design, develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient absorbers are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT
- HIGH SLEW RATE — 300V/µs

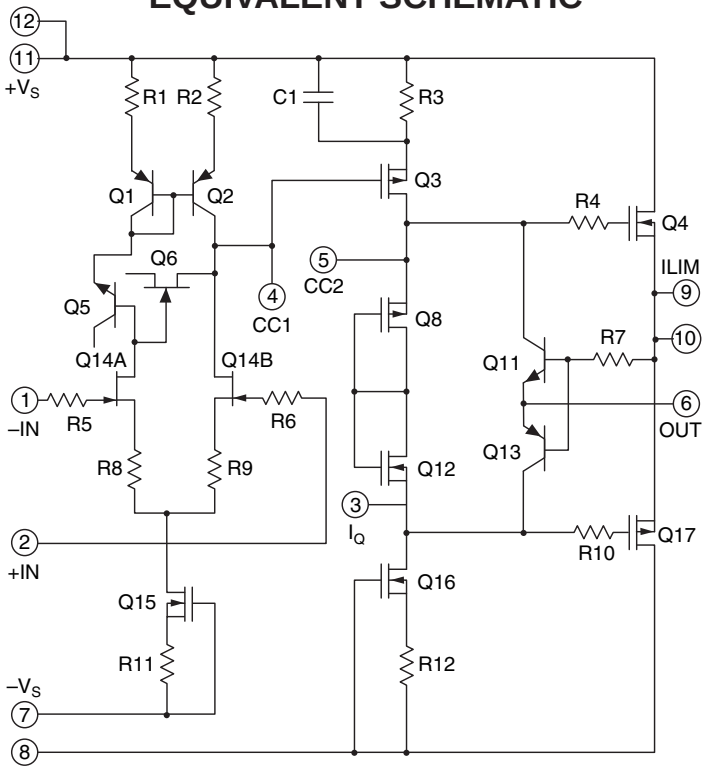
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

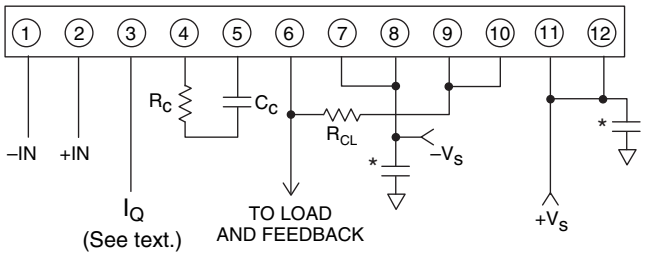
DESCRIPTION

The PA90 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards. The 12-pin PowerSIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



12-pin SIP PACKAGE STYLE DP

Formed leads available

See package EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			400	V
OUTPUT CURRENT, source, sink, peak, within SOA			350	mA
POWER DISSIPATION, continuous @ T_C = 25°C			30	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA90 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

Parameter	Test Conditions[1]	Min	Typ	Max	Units
AMPLIFIER INPUT					
OFFSET VOLTAGE, initial			0.5	2	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		$\pm V_S$ ∓ 15			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	100KHz bandwidth, R_S = 1KΩ, C_C = OPEN		1		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 2KΩ, C_C = OPEN	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 2KΩ, C_C = OPEN		100		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = OPEN		470		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING (Note 3)	I_O = 200mA	$\pm V_S$ ∓ 12	$\pm V_S$ ∓ 10		V
CURRENT, continuous		200			mA
SLEW RATE, A_V = 100	C_C = OPEN	240	300		V/µS
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			pF

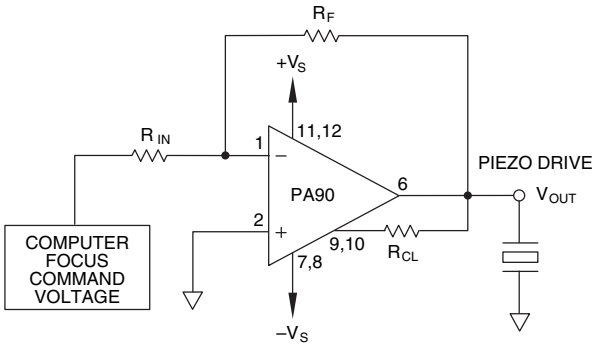
Parameter	Test Conditions[1]	Min	Typ	Max	Units
SETTLING TIME to 0.1%	C_C = OPEN, 2V step		1		µS
RESISTANCE, no load			50		Ω
POWER SUPPLY					
VOLTAGE (Note 5)		±40	±150	±200	V
CURRENT, quiescent			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

TYPICAL APPLICATION

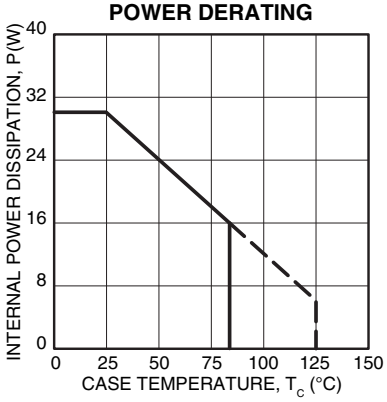
LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA90 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

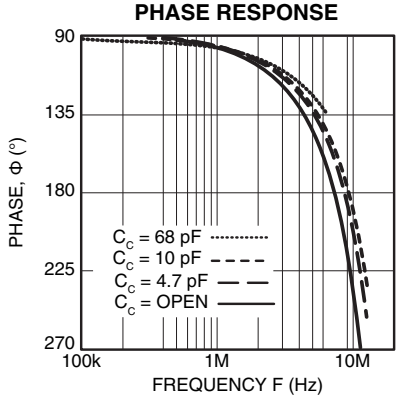


TYPICAL PERFORMANCE GRAPHS

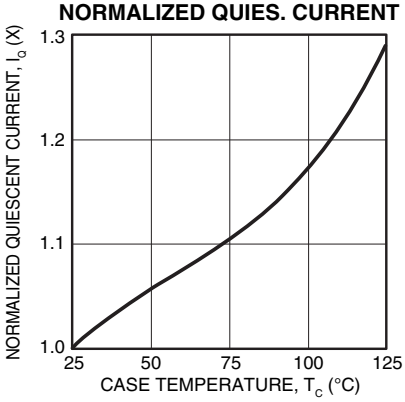
POWER DERATING



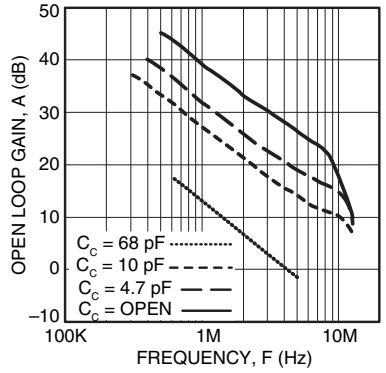
PHASE RESPONSE



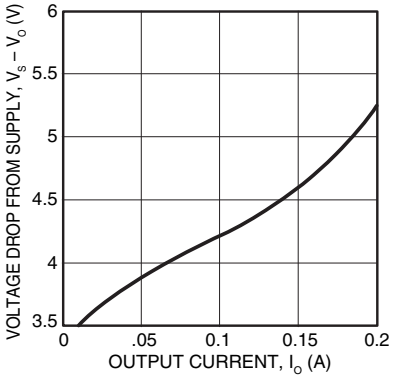
NORMALIZED QUIES. CURRENT



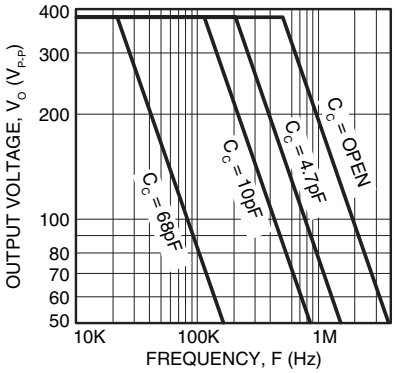
SMALL SIGNAL RESPONSE



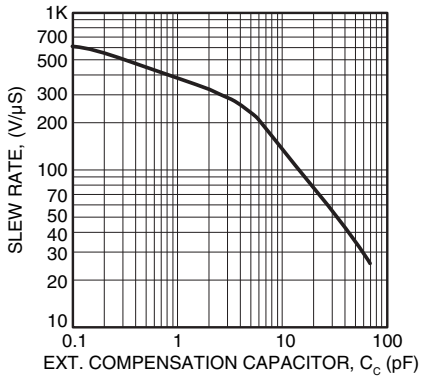
OUTPUT VOLTAGE SWING



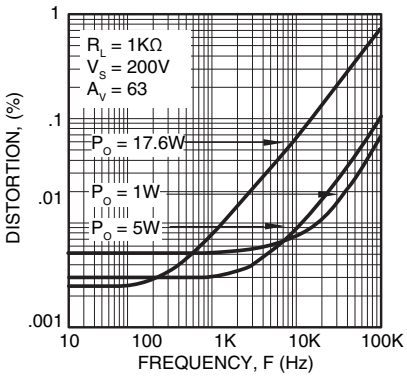
POWER RESPONSE



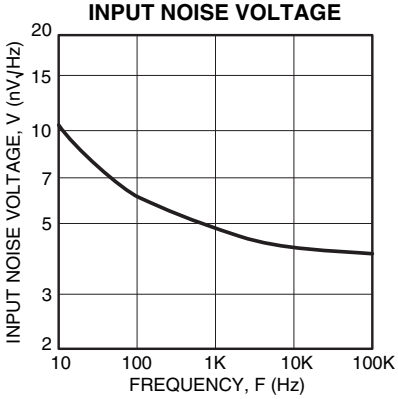
SLEW RATE



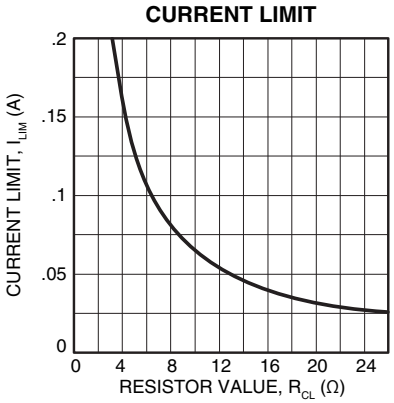
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	68pF	100Ω
≥5	10pF	100Ω
≥10	4.7pF	0Ω
≥30	NONE	0Ω

*C_C To be rated for the full supply voltage +V_S to –V_S. Use NPO ceramic (COG) type.

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 32 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

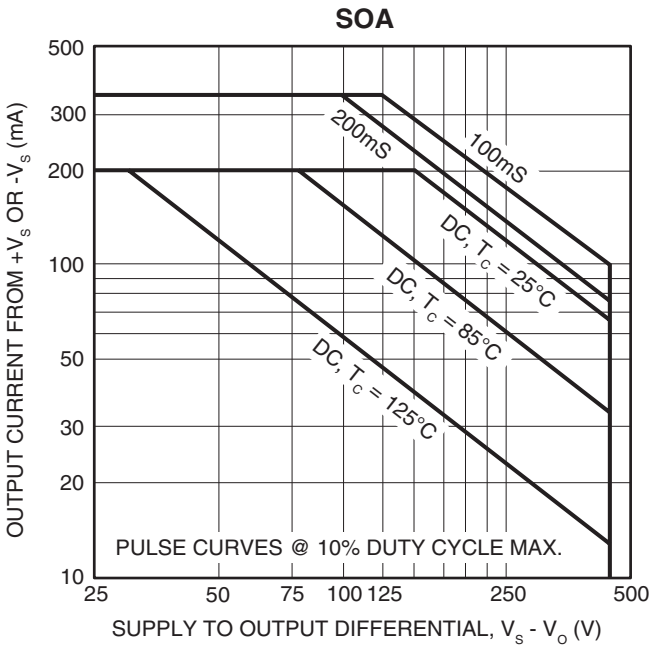
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.



INPUT PROTECTION

Although the PA90 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

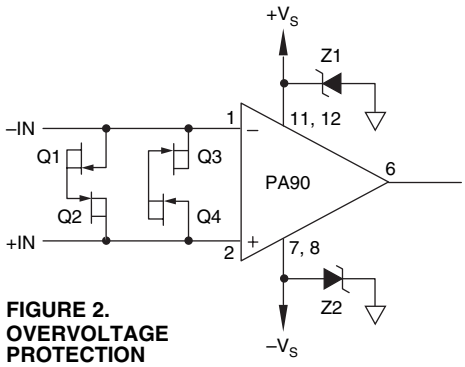


FIGURE 2. OVERVOLTAGE PROTECTION

STABILITY

The PA90 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This raises distortion since the output stage is then class C biased, but reduces the quiescent current by 1mA for a power dissipation savings of 0.4W. Pin 3 may be left open if not used.

PA91

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT
- HIGH SLEW RATE — 300V/µs

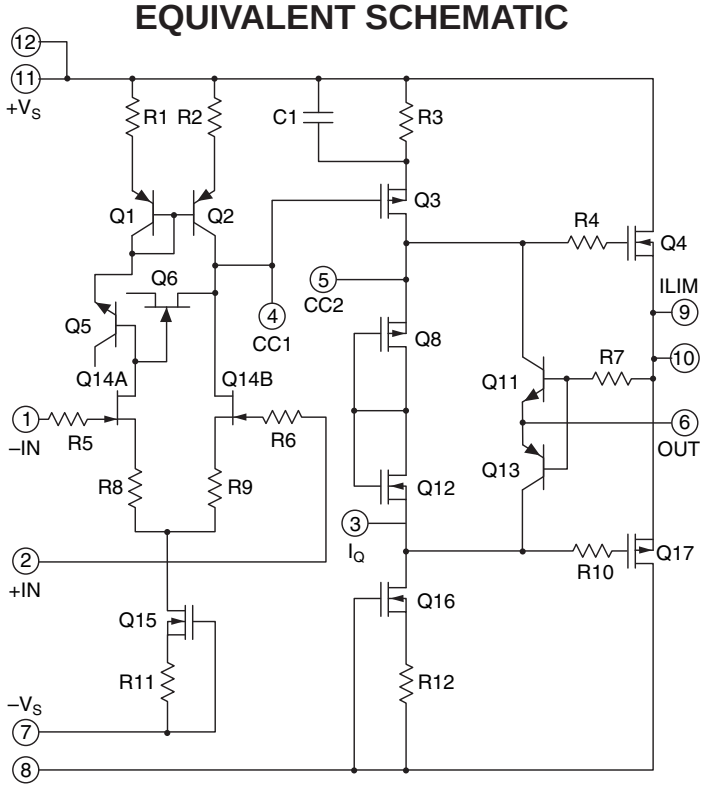
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V

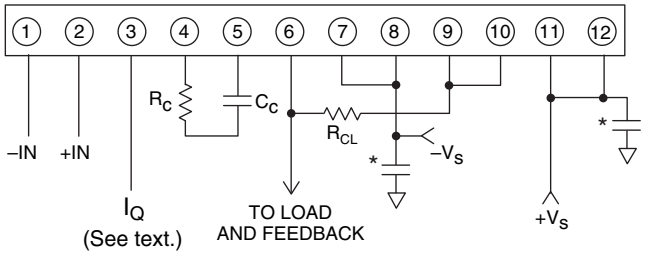
DESCRIPTION

The PA91 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards. The 12-pin PowerSIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



* Bypassing required.

12-pin SIP PACKAGE STYLE DP

Formed leads available
See package style EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			450	V
OUTPUT CURRENT, source, sink, peak, within SOA			350	mA
POWER DISSIPATION, continuous @ T_C = 25°C			30	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE, case		−25	85	°C

CAUTION The PA91 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

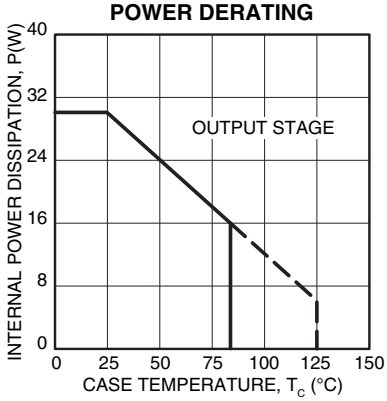
Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			0.5	2	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/KHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		$\pm V_S$ ∓ 15			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	100KHz bandwidth, R_S = 1KΩ, C_C = OPEN		1		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 2KΩ, C_C = OPEN	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 2KΩ, C_C = OPEN		100		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = OPEN		470		KHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING (Note 3)	I_O = 200mA	$\pm V_S$ ∓ 12	$\pm V_S$ ∓ 10		V
CURRENT, continuous		200			mA
SLEW RATE, A_V = 100	C_C = OPEN	240	300		V/µS
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			pF

Parameter	Test Conditions[1]	Min	Typ	Max	Units
SETTLING TIME to 0.1%	C_C = OPEN, 2V step		1		µS
RESISTANCE, no load			50		Ω
POWER SUPPLY					
VOLTAGE (Note 5)		±40	±150	±225	V
CURRENT, quiescent			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

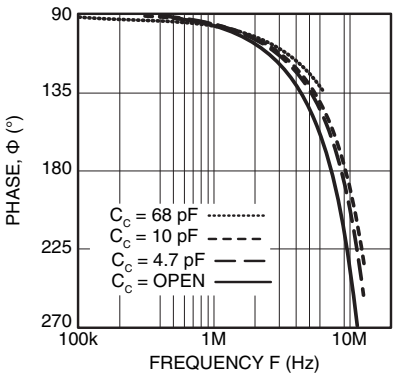
NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

TYPICAL PERFORMANCE GRAPHS

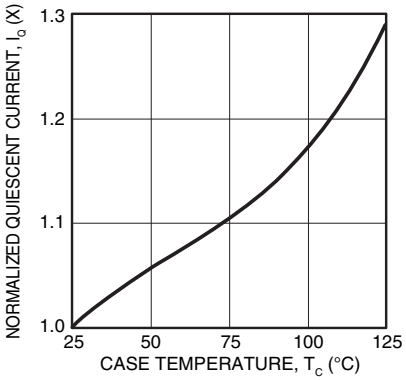
POWER DERATING



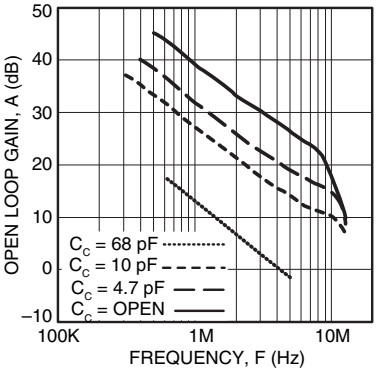
PHASE RESPONSE



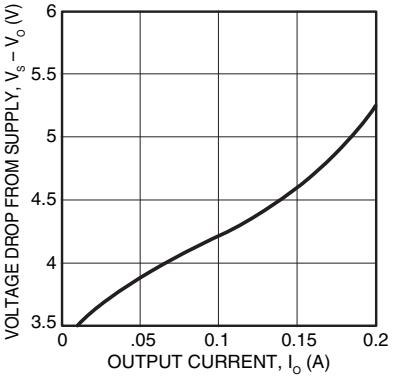
NORMALIZED QUIES. CURRENT



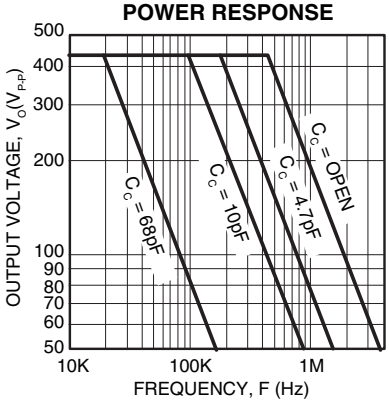
SMALL SIGNAL RESPONSE



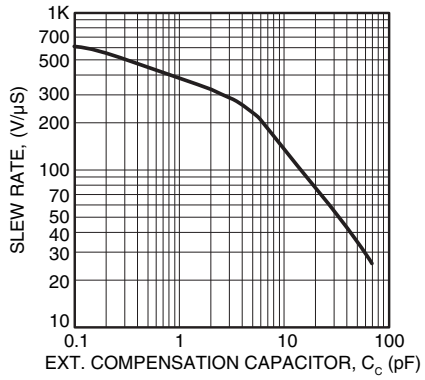
OUTPUT VOLTAGE SWING



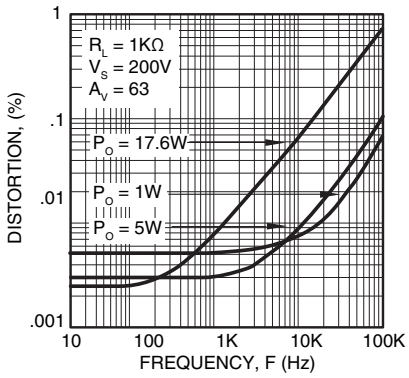
POWER RESPONSE



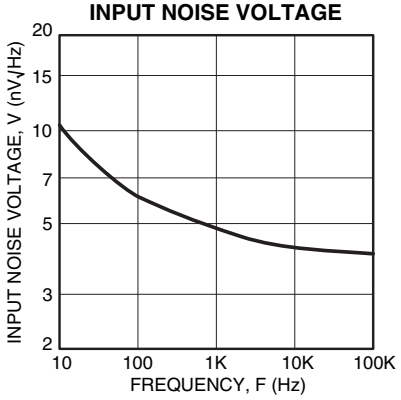
SLEW RATE



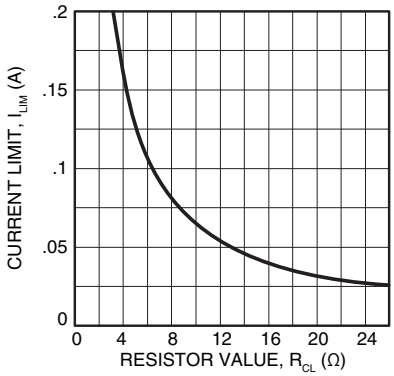
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



PHASE COMPENSATION

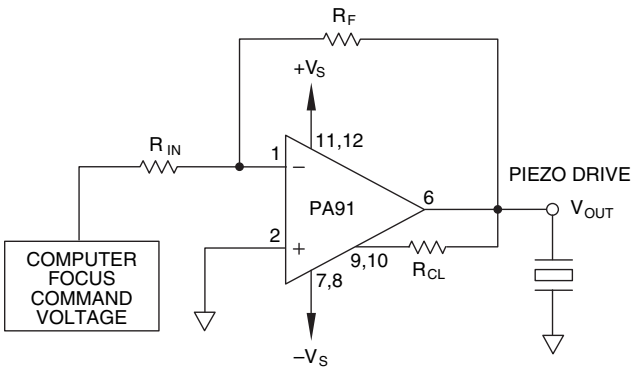
GAIN	C_C*	R_C
≥1	68pF	100Ω
≥5	10pF	100Ω
≥10	4.7pF	0Ω
≥30	NONE	0Ω

*C_C To be rated for the full supply voltage $+V_S$ to $-V_S$. Use NPO ceramic (COG) type.

TYPICAL APPLICATION

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA91 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 32 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

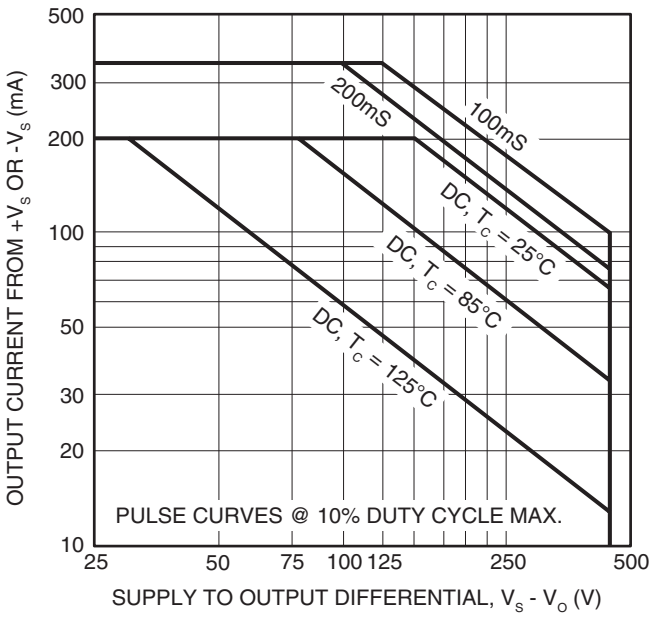
INPUT PROTECTION

Although the PA91 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.



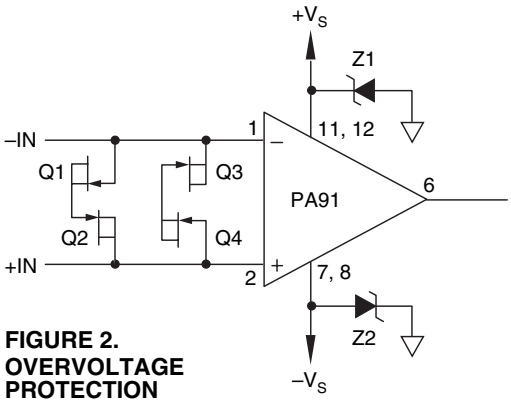


FIGURE 2. OVERVOLTAGE PROTECTION

STABILITY

The PA91 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor CC must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network CCRC must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (IQ) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This raises distortion since the output stage is then class C biased, but reduces the quiescent current by 1mA for a power dissipation savings of 0.4W. Pin 3 may be left open if not used.

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 4A
- PROGRAMMABLE CURRENT LIMIT

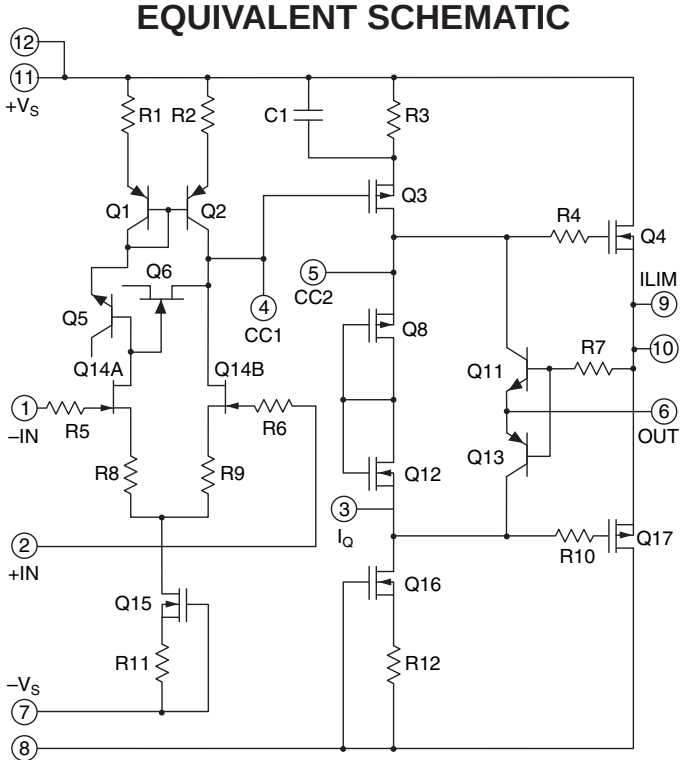
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

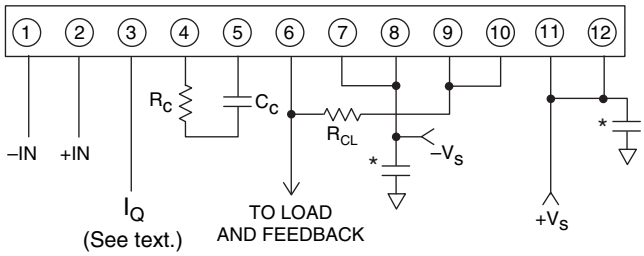
DESCRIPTION

The PA92 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 4A and pulse currents up to 7A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards. The Power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PATENTED

12-pin SIP PACKAGE STYLE DP

Formed leads available
See package style EE

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			400	V
OUTPUT CURRENT, source, sink, peak, within SOA			7	A
POWER DISSIPATION, continuous @ T_C = 25°C			80	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA92 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

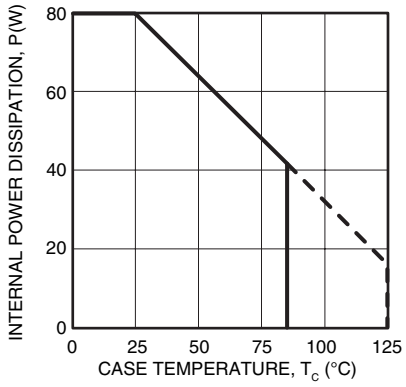
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			2	10	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		$\pm V_S$ ∓ 15			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	100KHz bandwidth, R_S = 1KΩ, C_C = 10pF		1		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 2KΩ, C_C = 10pF	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 2KΩ, C_C = 10pF		18		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = 10pF		30		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING (Note 3)	I_O = 4A	$\pm V_S$ ∓ 12	$\pm V_S$ ∓ 10		V
CURRENT, continuous		4			A
SLEW RATE, A_V = 100	C_C = 10pF		50		V/µS
CAPACITIVE LOAD, A_V = +1	Full temperature range	1			nF

Parameter	Test Conditions	Min	Typ	Max	Units
SETTLING TIME to 0.1%	C_C = 10pF, 2V step		1		µS
RESISTANCE, no load			10		Ω
POWER SUPPLY					
VOLTAGE (Note 5)		±50	±150	±200	V
CURRENT, quiescent			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			1	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			1.5	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

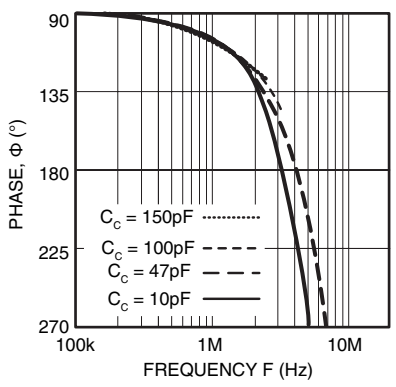
NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

TYPICAL PERFORMANCE GRAPHS

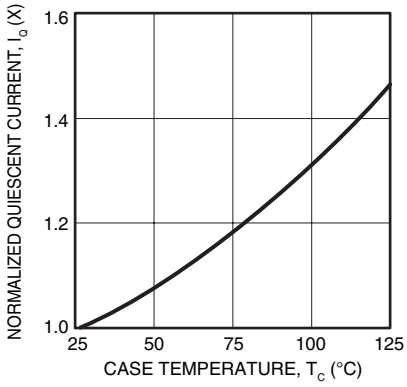
POWER DERATING



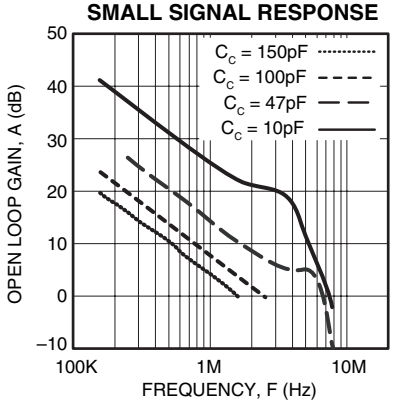
PHASE RESPONSE



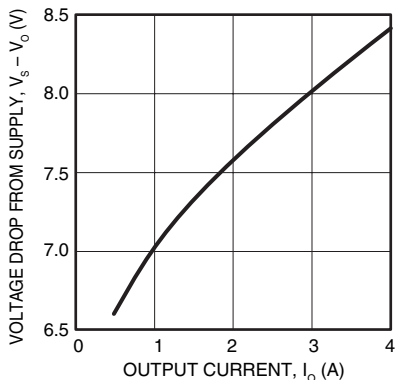
NORMALIZED QUIESCENT CURRENT



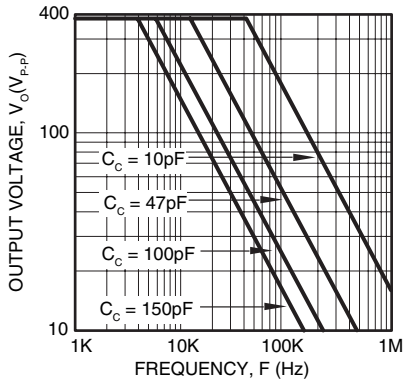
SMALL SIGNAL RESPONSE



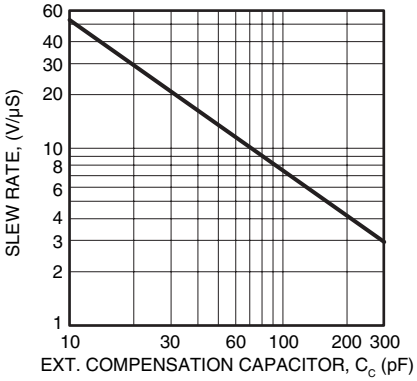
OUTPUT VOLTAGE SWING



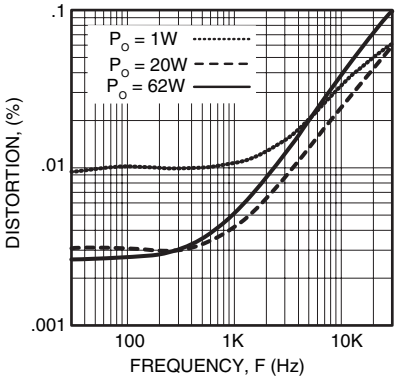
POWER RESPONSE



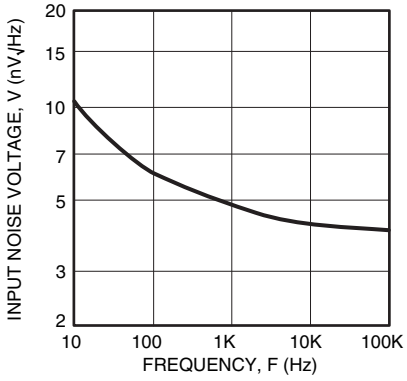
SLEW RATE



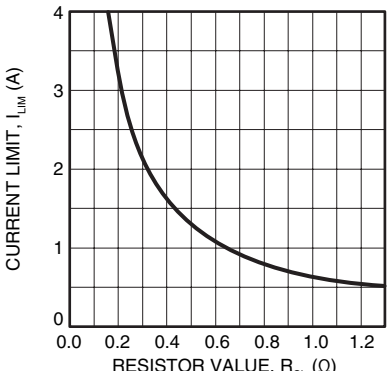
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	150pF	100Ω
≥2	100pF	100Ω
≥3	47pF	0Ω
≥12	10pF	0Ω

*C_C Never to be <10pF. C_C to be rated for the full supply voltage +V to -Vs. Use ceramic NPO (COG) type.

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

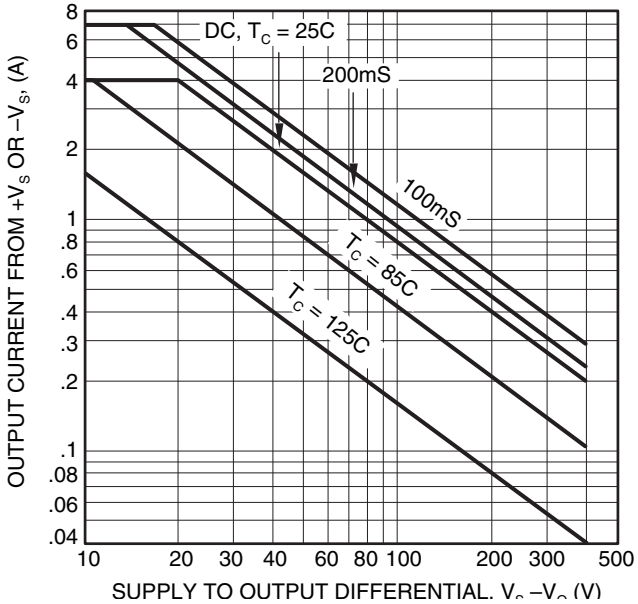
SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SOA



SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

INPUT PROTECTION

Although the PA92 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

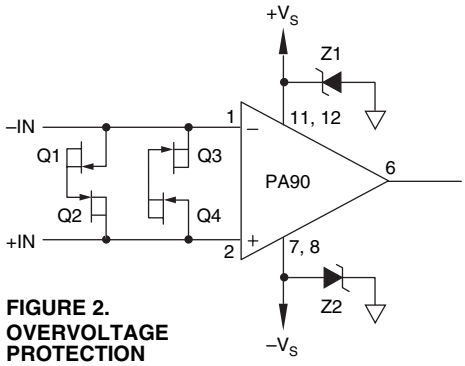


FIGURE 2. OVERVOLTAGE PROTECTION

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA92 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

High Voltage Power Operational Amplifiers

FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 8A
- PROGRAMMABLE CURRENT LIMIT

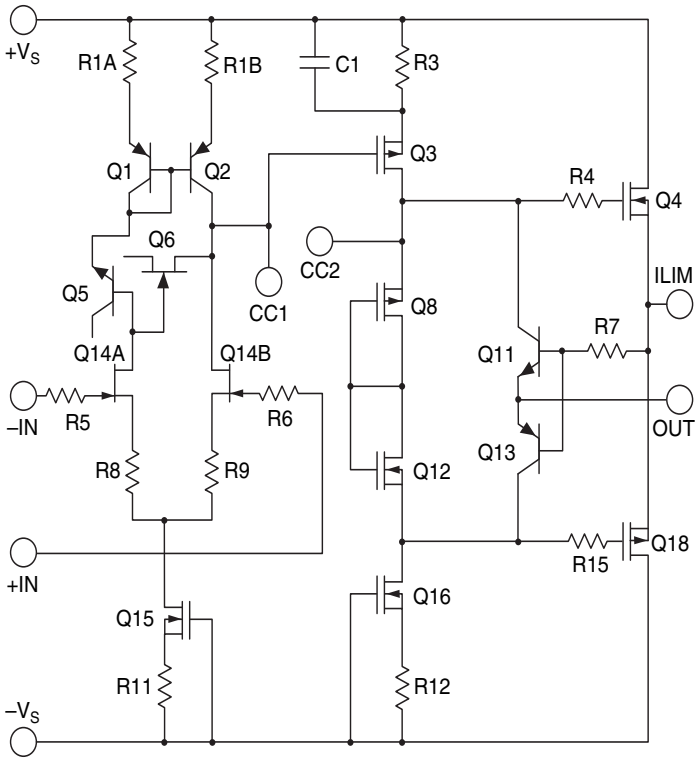
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

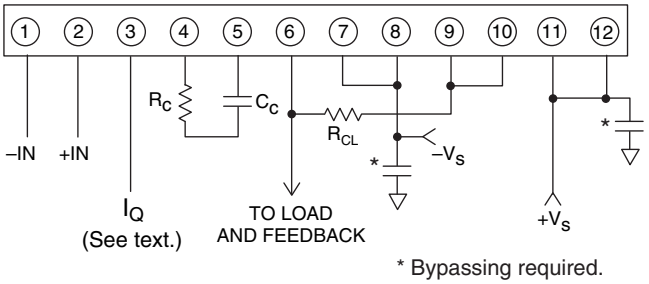
DESCRIPTION

The PA93 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 8A and pulse currents up to 14A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards. The Power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



* Bypassing required.

PATENTED

12-pin SIP PACKAGE STYLE DP

Formed leads available
See package style EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			400	V
OUTPUT CURRENT, source, sink, peak, within SOA			14	A
POWER DISSIPATION, continuous @ T_C = 25ºC			125	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA93 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			2	10	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		±Vs ∓ 15			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	100KHz BW, R_S = 1KΩ, C_C = 10pF		1		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 2KΩ, C_C = 10pF	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 2KΩ, C_C = 10pF		12		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = 10pF		30		KHz
PHASE MARGIN	Full temp range		60		°
OUTPUT					
VOLTAGE SWING (Note 3)	I_O = 8mA	$±V_S$ ∓ 12	$±V_S$ ∓ 10		V
CURRENT, continuous		8			A
SLEW RATE, A_V = 100	C_C = 10pF		50		V/µS
CAPACITIVE LOAD, A_V = +1	Full temp range	1			nF

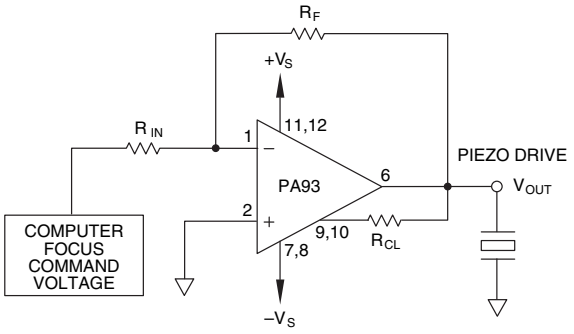
Parameter	Test Conditions[1]	Min	Typ	Max	Units
SETTLING TIME to 0.1%	C_C = 10pF, 2V step		1		µS
RESISTANCE, no load			10		Ω
POWER SUPPLY					
VOLTAGE (Note 5)		±40	±150	±200	V
CURRENT, quiescent			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			0.7	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			1	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. R_C = 100 C_C = 220pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

TYPICAL APPLICATION

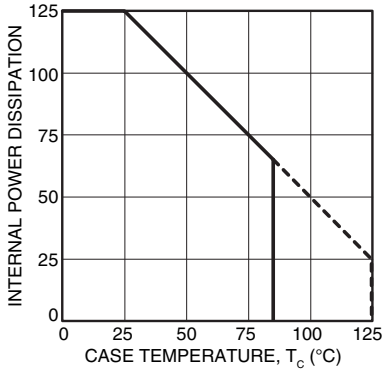
LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA93 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

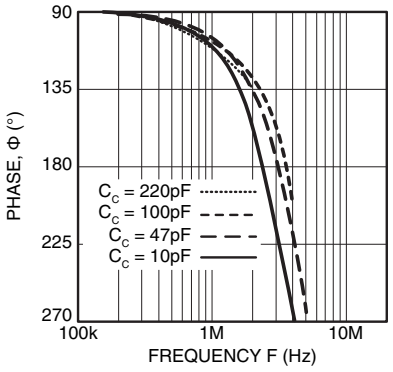


TYPICAL PERFORMANCE GRAPHS

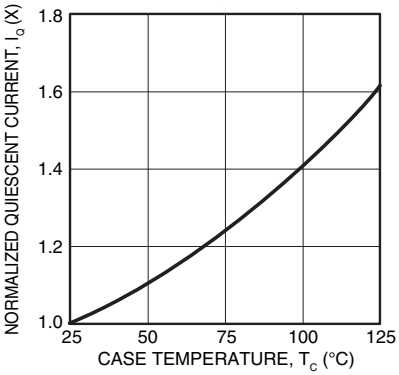
POWER DERATING



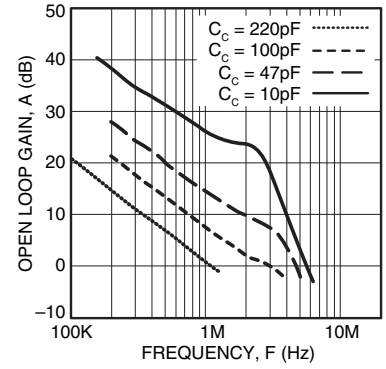
PHASE RESPONSE



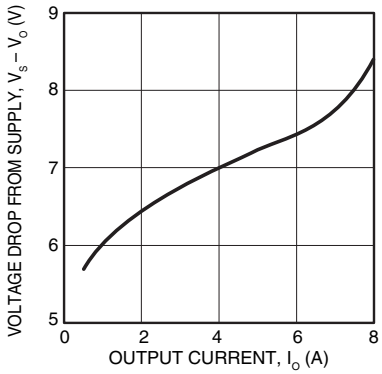
NORMALIZED QUIES. CURRENT



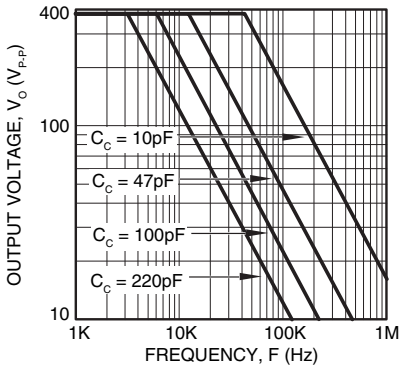
SMALL SIGNAL RESPONSE



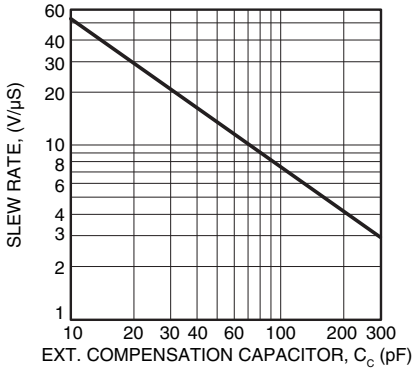
OUTPUT VOLTAGE SWING



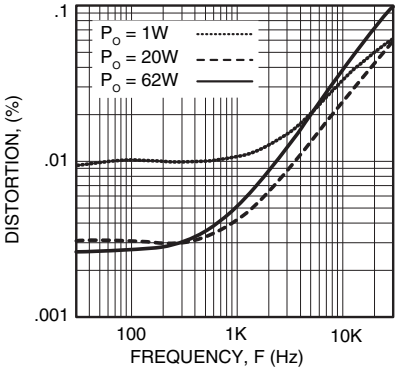
POWER RESPONSE



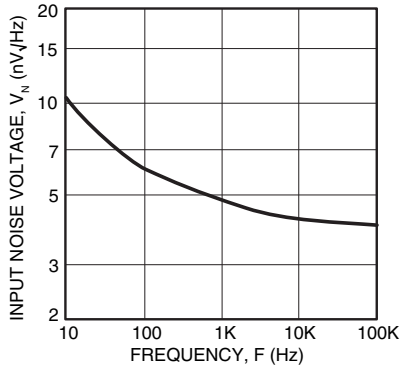
SLEW RATE



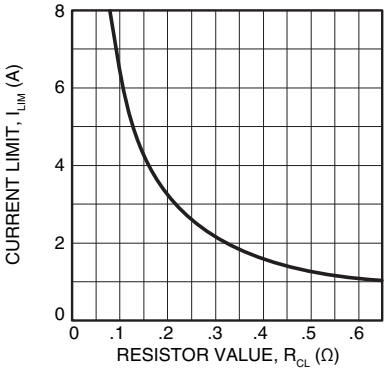
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	220pF	100Ω
≥2	100pF	100Ω
≥4	47pF	0Ω
≥17	10pF	0Ω

*C_C Never to be <10pF. C_C to be rated for the full supply voltage $+V_S$ to $-V_S$. Use ceramic NPO (COG) type.

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 ohms.

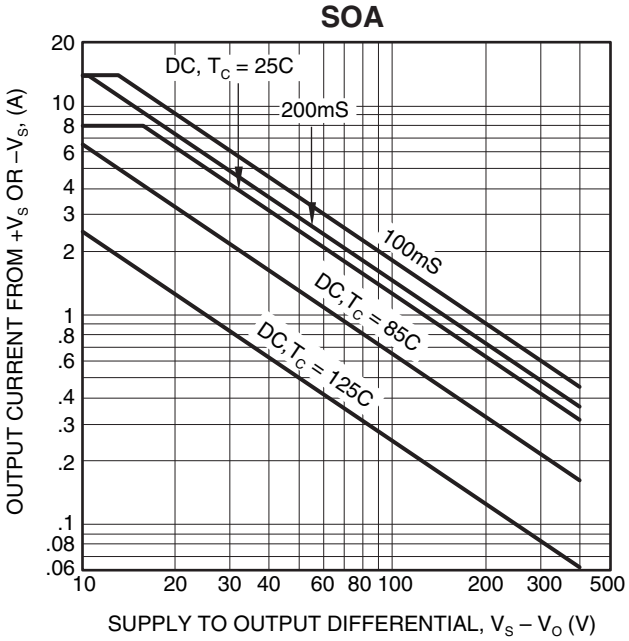
$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

INPUT PROTECTION

Although the PA93 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

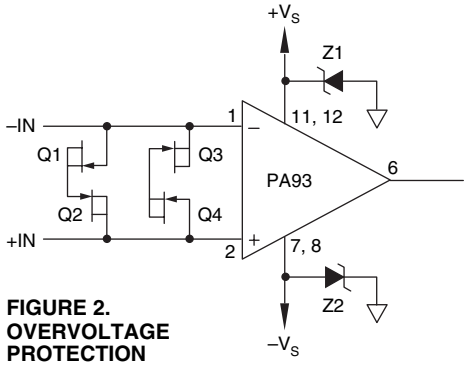


FIGURE 2. OVERVOLTAGE PROTECTION

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA93 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 900V (±450V)
- HIGH SLEW RATE — 500V/µS
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT

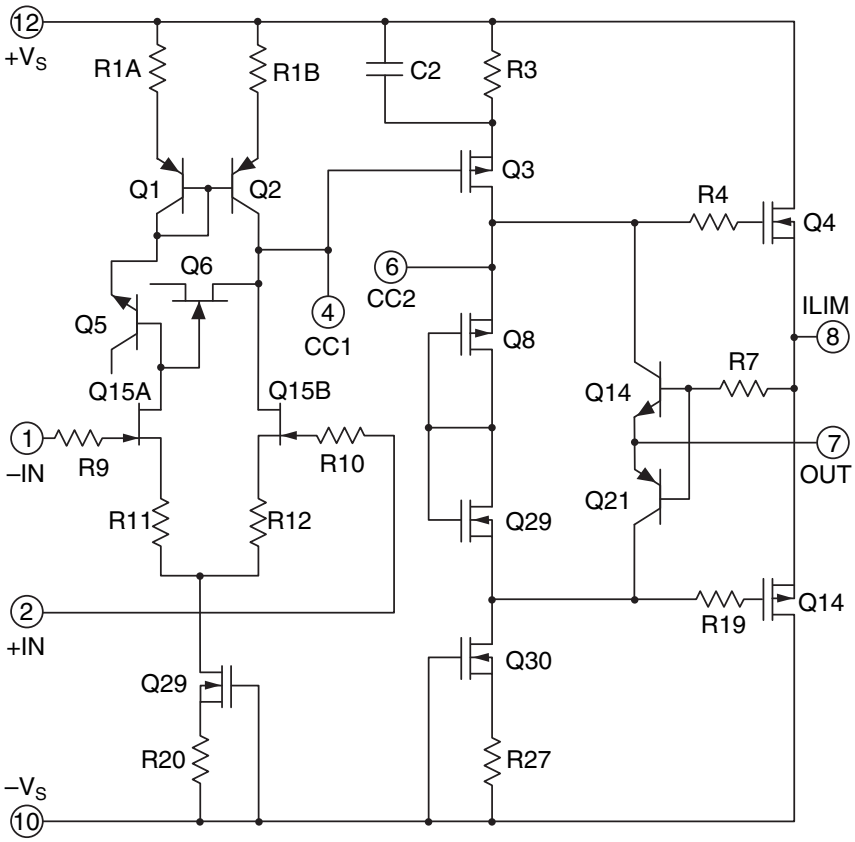
APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO ±430V
- MASS SPECTROMETERS
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

DESCRIPTION

The PA94 is a high voltage, MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 100mA and pulse currents up to 200mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all load types by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards.. The Power SIP package is electrically isolated. Isolating thermal washers (TW13) prevent arcing from pins to heatsink.

EQUIVALENT SCHEMATIC



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			900	V
OUTPUT CURRENT, source, sink, within SOA			200	mA
POWER DISSIPATION, continuous @ T_C = 25°C			30	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode (Note 3)		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA94 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid toxic fumes.

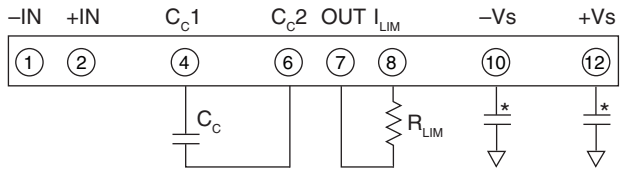
SPECIFICATIONS

Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			0.5	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)	V_S = ±450V	$\pm V_S$ ∓30			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	10KHz bandwidth, R_S = 1KΩ		2		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 5KΩ	94	115		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 5KΩ		140		MHz
POWER BANDWIDTH	R_L = 5KΩ		300		kHz
PHASE MARGIN, A_V = 100	Full temp range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 70mA	$\pm V_S$ ∓ 24	$\pm V_S$ ∓ 20		V
CURRENT, continuous		100			mA
SLEW RATE, A_V = 100	C_C =2.2pF	500	700		V/µS
SETTLING TIME, to 0.1%	2V Step		1		µS
RESISTANCE	no load		100		Ω

Parameter	Test Conditions[1]	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE (Note 5)		±50	±300	±450	V
CURRENT, quiescent total			17	24	mA
CURRENT, quiescent output stage only				120	µA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. C_c= 4.7pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 450V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

EXTERNAL CONNECTIONS



* 0.01µF or greater ceramic power supply bypassing required.

PATENTED

8-pin SIP PACKAGE STYLE DQ

Formed leads available
See package style EC

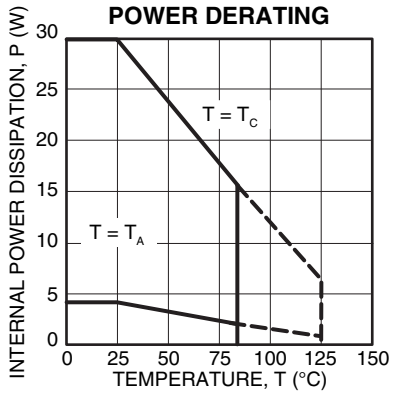
PHASE COMPENSATION

GAIN	C_C
≥100	2.2pF
≥50	4.7pF
≥10	22pF

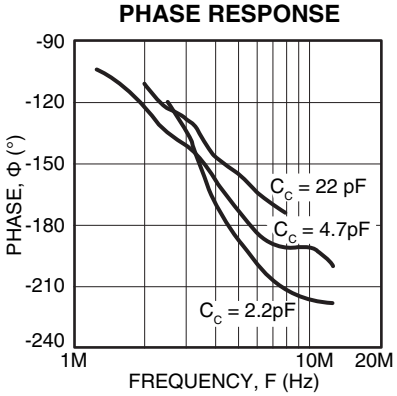
C_C rated for full supply voltage.

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

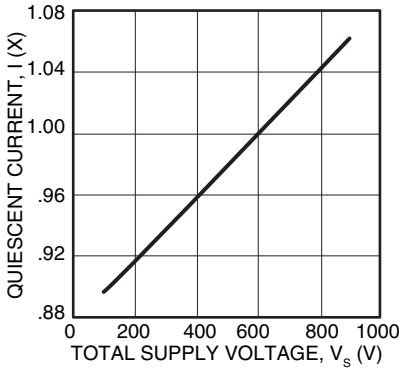
POWER DERATING



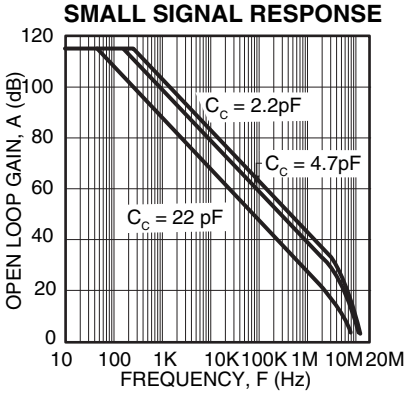
PHASE RESPONSE



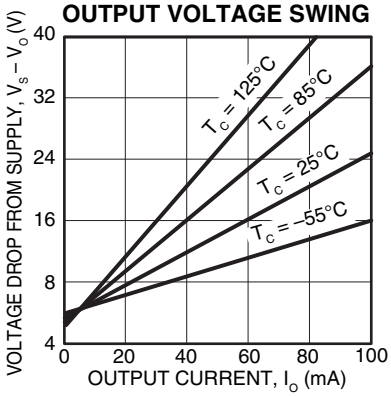
QUIESCENT CURRENT



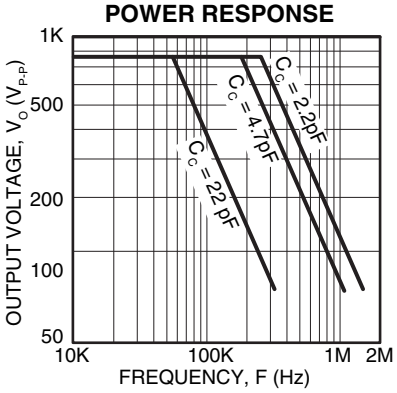
SMALL SIGNAL RESPONSE



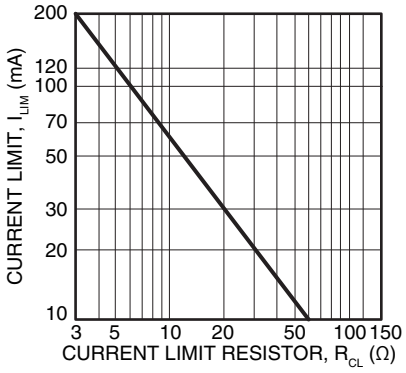
OUTPUT VOLTAGE SWING



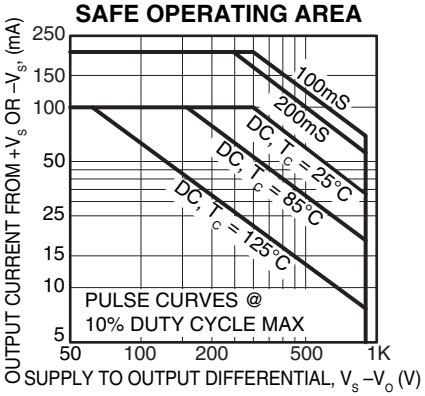
POWER RESPONSE



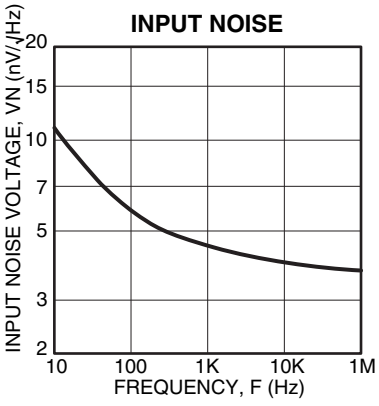
CURRENT LIMIT



SAFE OPERATING AREA

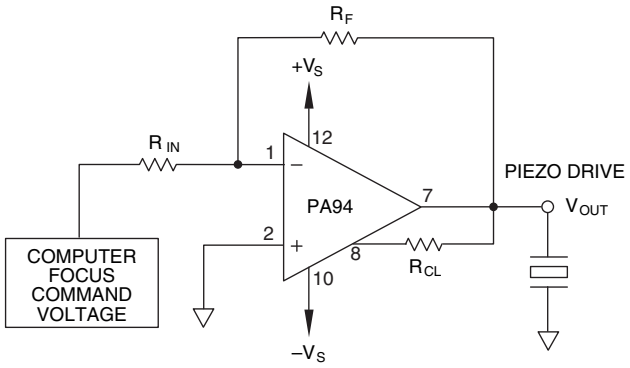


INPUT NOISE



TYPICAL APPLICATION

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA94 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



INTERNAL POWER DISSIPATION AND HEATSINK SELECTION

With the unique combination of high voltage and speed of the PA94, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of this amplifier. To more accurately predict operating temperatures use Power Design[1] revision 10 or higher, or use the following procedure:
Find internal dissipation (PD) resulting from driving the load. Use Power Design or refer to Apex Precision Power Applications Note 1, General Operating Considertaions, paragraph 7. Find total quiescent power (PD_Q) by multiplying 0.024A by V_{SS} (total supply voltage). Find output stage quiescent power (PD_{QOUT}) by multiplying 0.00012 by V_{SS}. Calculate a heatsink rating which will maintain the case at 85°C or lower.

$$R_{\Theta SA} = \frac{T_C - T_A}{PD + PD_Q} - 0.1°C/W$$

Where: T_C = maximum case temperature allowed
T_A = maximum ambient temperature encountered

Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower.

$$R_{\Theta SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) * R_{\Theta JC}}{PD + PD_Q} - 0.1°C/W$$

Where: T_J = maximum junction temperature allowed.
$R_{\Theta JC}$ = AC or DC thermal resistance from the specification table.
Use the larger heatsink of these two calculations.

Power Design is an Excel spreadsheet available free from www.cirrus.com

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

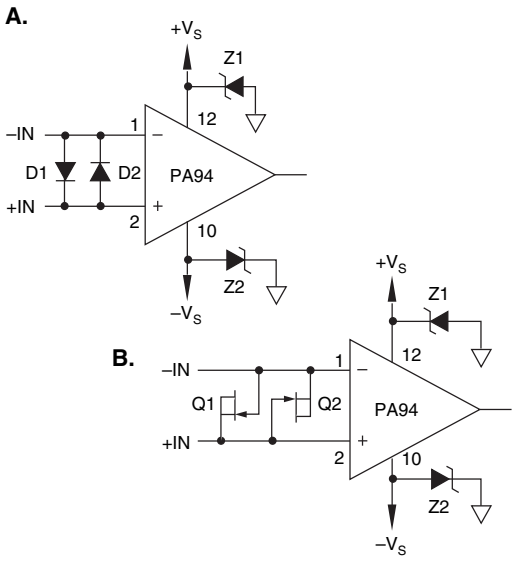
COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA94 is restricted. The input pins must always be a least 30V from either supply voltage but never more than 450V. This means that the PA94 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and –100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +450V and -100V does meet the input common mode voltage range requirements since the maximum difference voltage between the inputs pins and the supply voltage is 450V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA94 can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 1a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 1b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does not automatically protect the amplifier from excessive common mode input voltages.

FIGURE 1. OVERVOLTAGE PROTECTION



POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA94 is stable at gains of 100 or more with a NPO (COG) compensation capacitor of 2.2pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 2.2pF is not recommended.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. An NPO (COG) capacitor rated a 1kV is recommended.

Of equal importance are the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 500 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

CAUTIONS

The operating voltages of the PA94 are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

High Voltage Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE — 900V (±450V)
- LOW QUIESCENT CURRENT — 1.6mA
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT

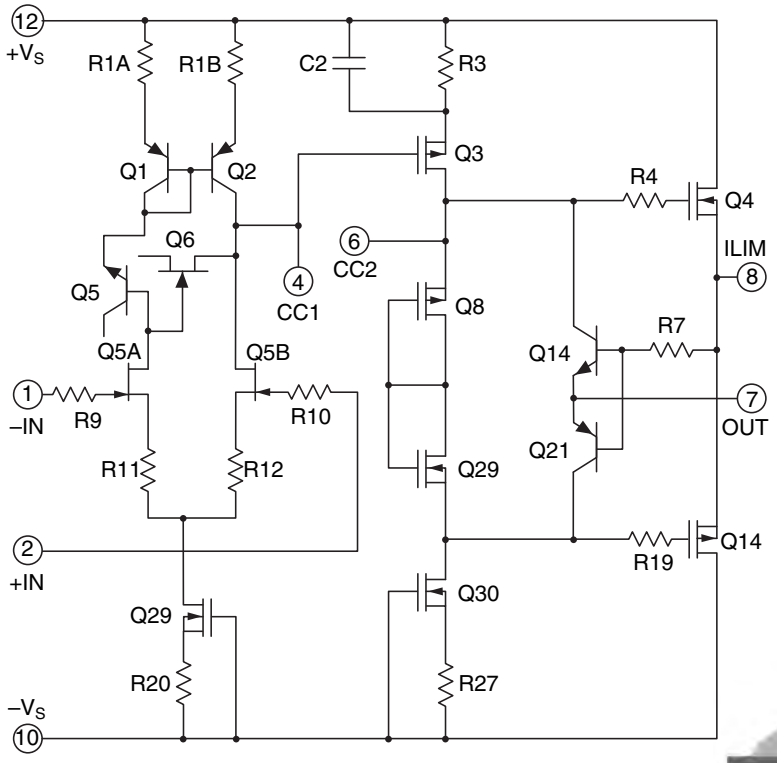
APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO ±430V
- MASS SPECTROMETERS
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

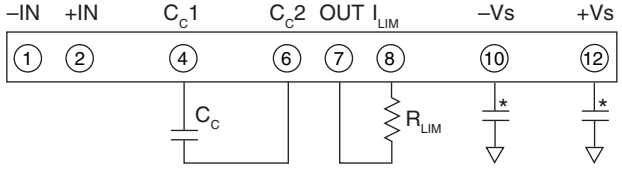
DESCRIPTION

The PA95 is a high voltage, MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 100mA and pulse currents up to 200mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all load types by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's Power SIP package uses a minimum of board space allowing for high density circuit boards. The Power SIP package is electrically isolated. Isolating thermal washers (TW13) are recommended to prevent arcing from pins to heatsink.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



* 0.01µF or greater ceramic power supply bypassing required.

PATENTED

8-pin SIP PACKAGE STYLE DQ

Formed leads available
See package style EC

CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			900	V
OUTPUT CURRENT, source, sink, within SOA			200	mA
POWER DISSIPATION, continuous @ T_C = 25°C			30	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode (Note 3)		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA95 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

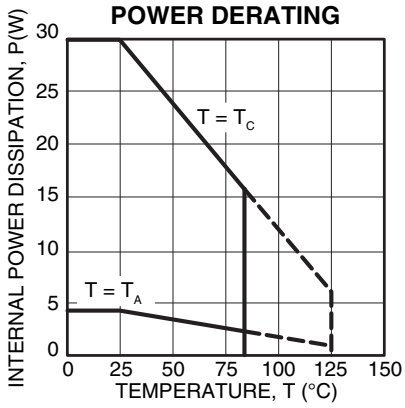
SPECIFICATIONS

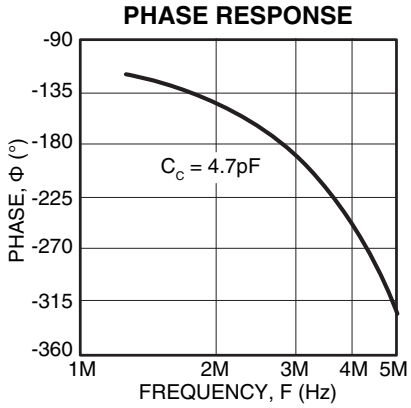
Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			0.5	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT RESISTANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)	V_S=±250V	$\pm V_S$ ∓ 30			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	10KHz bandwidth, R_S = 1KΩ		2		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 5KΩ	94	118		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 5KΩ		10		MHz
POWER BANDWIDTH	R_L = 5KΩ		20		kHz
PHASE MARGIN, A_V = 10	Full temp range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 70mA	$\pm V_S$ ∓ 24	$\pm V_S$ ∓ 20		V
CURRENT, continuous		100			mA
SLEW RATE, A_V = 100	C_C =4.7pF		30		V/µS
SETTLING TIME, to 0.1%	2V Step		1		µS
RESISTANCE	no load		100		Ω

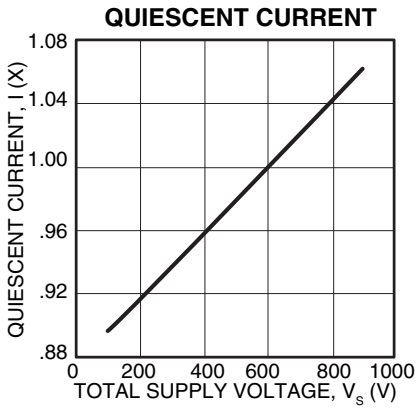
Parameter	Test Conditions[1]	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE (Note 5)		±50	±300	±450	V
CURRENT, quiescent			1.6	2.2	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case		-25		+85	°C

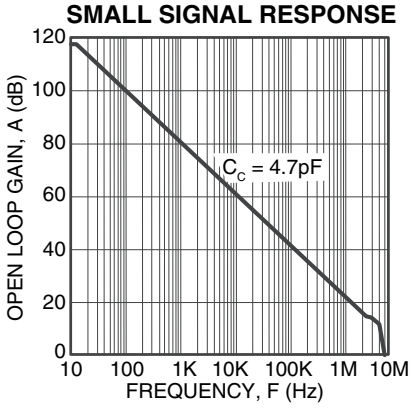
NOTES: 1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. C_c= 4.7pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 500V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

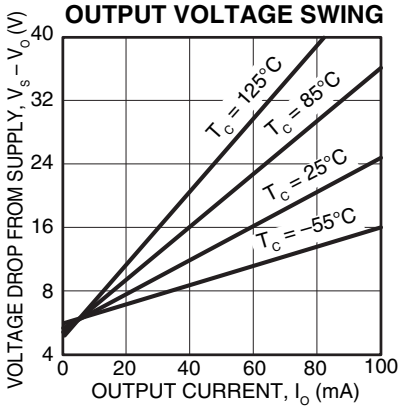
TYPICAL PERFORMANCE GRAPHS

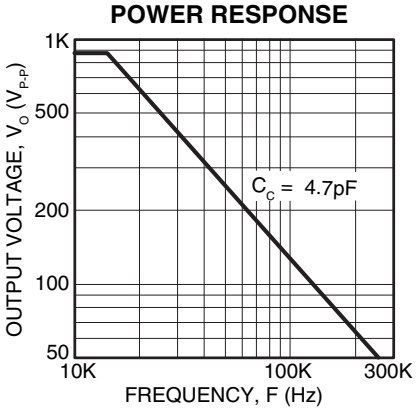


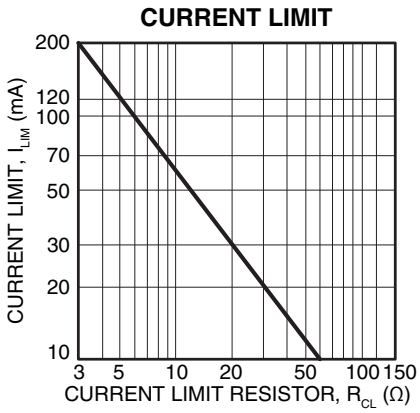


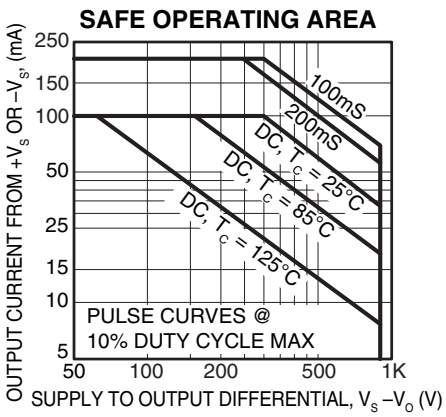


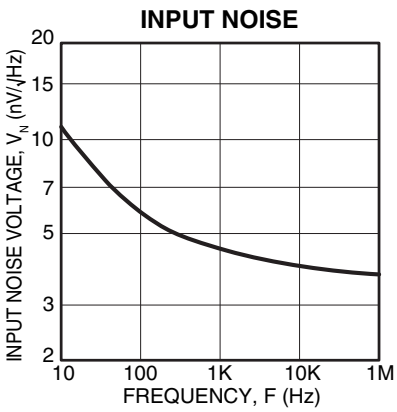






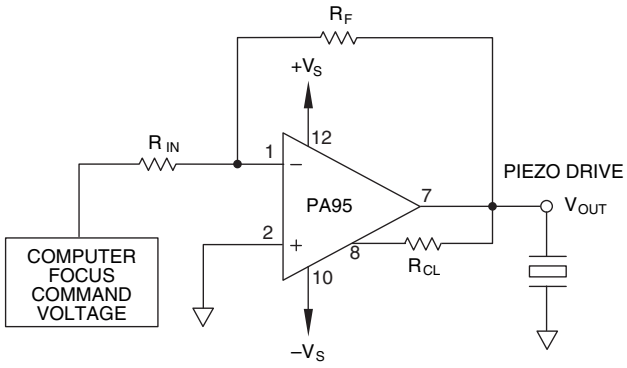






TYPICAL APPLICATION

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA95 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



PHASE COMPENSATION

C_C rated for full supply voltage.

GAIN	C_C
≥100	4.7pF

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA95 is restricted. The input pins must always be a least 30V from either supply voltage but never more than 500V. This means that the PA95 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and –100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +500V and -100V does meet the input common mode voltage range

requirements since the maximum difference voltage between the inputs pins and the supply voltage is 500V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA95 can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 1a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 1b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does not automatically protect the amplifier from excessive common mode input voltages.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

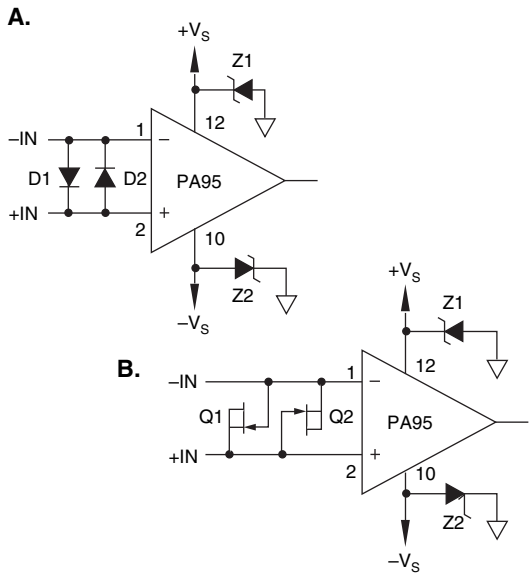


FIGURE 1. OVERVOLTAGE PROTECTION

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA95 is stable at gains of 10 or more with a NPO (COG) compensation capacitor of 4.7pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 4.7pF is not recommended.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. An NPO (COG)capacitor rated a 1kV is recommended.

Of equal importance are the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 500 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

CAUTIONS

The operating voltages of the PA95 are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- HIGH VOLTAGE - 300 VOLTS
- HIGH OUTPUT CURRENT – 1.5 AMPS
- 70 WATT DISSIPATION CAPABILITY
- 175 MHz GAIN BANDWIDTH
- 250 V/µ-SECOND SLEW RATE

APPLICATIONS

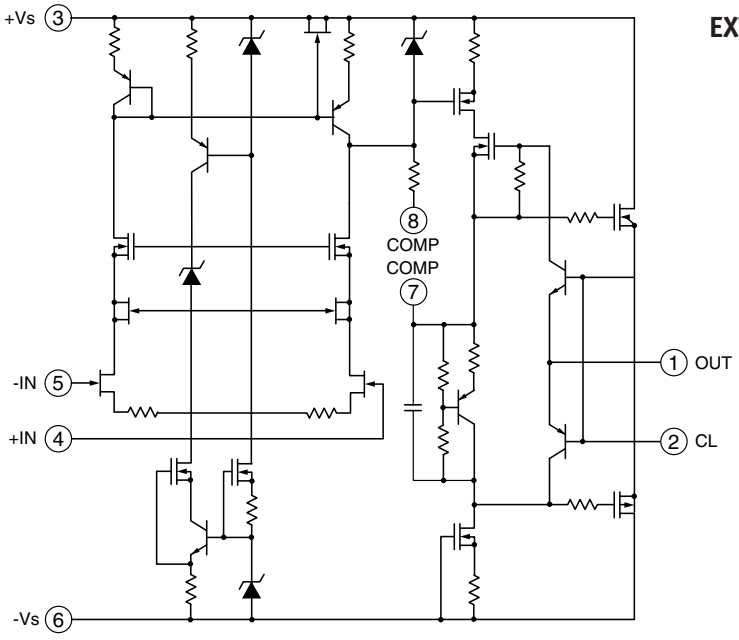
- PZT DRIVE
- MAGNETIC DEFLECTION
- PROGRAMMABLE POWER SUPPLIES
- 70V LINE AUDIO to 70W

DESCRIPTION

The PA96 is a state of the art high voltage, high current operational amplifier designed to drive resistive, capacitive and inductive loads. For optimum linearity, the output stage is biased for class A/B operation. External compensation provides user flexibility in maximizing bandwidth at any gain setting. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit. For continuous operation under load, a heatsink of proper rating is required.

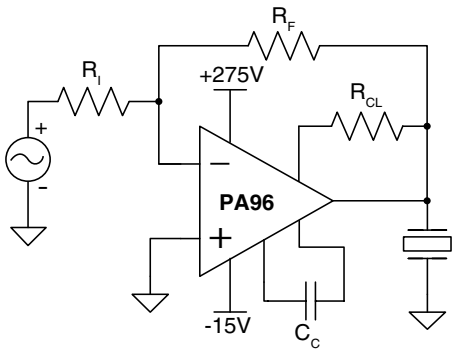
The hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT CIRCUIT DIAGRAM



8-PIN TO-3
PACKAGE STYLE CE

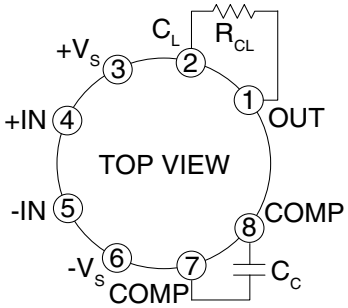
TYPICAL APPLICATION



PZT POSITION CONTROL

The MOSFET output stage of the PA96 provides superior SOA performance compared to bipolar output stages where secondary breakdown is a concern. The extended SOA is ideal in applications where the load is highly reactive and may impose simultaneously both high voltage and high current across the output stage transistors. In the figure above a piezo-electric transducer is driven to high currents and high voltages by the PA96.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, continuous	1.5A,
POWER DISSIPATION, internal, DC	70W
INPUT VOLTAGE, common mode	$+V_S$ to $-V_S$
INPUT VOLTAGE, differential	±15V
TEMPERATURE, pin solder, 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to 150°C
OPERATING TEMPERATURE, case	–55 to 125°C

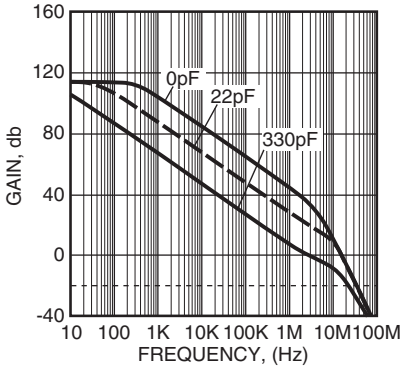
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE			1	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial				200	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT RESISTANCE, DC			100		GΩ
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]		$+V_S$ – 13			V
COMMON MODE VOLTAGE RANGE[3]		$-V_S$ + 13			V
COMMON MODE REJECTION, DC		92			dB
NOISE	100KHz bandwidth, 1kΩ R_s		6		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L= 1kΩ, C_C=100pF	96	114		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	VS = 150V, -VS = 150V, A = -100, RF = 100K	100	175		MHz
PHASE MARGIN	Full temperature range, using recommended C_C for gain.	60			°
PBW	250V p-p output, 100Ω, +150V Supplies, Cc = 0pf		100		KHz
OUTPUT					
VOLTAGE SWING[3]	I_O = 1.5A	$+V_S$ – 12	$+V_S$ – 5.6		V
VOLTAGE SWING[3]	I_O = –1.5A	$-V_S$ + 12	$-V_S$ + 10		V
VOLTAGE SWING[3]	I_O = 0.1A	$+V_S$ – 8			V
VOLTAGE SWING[3]	I_O = –0.1A	$-V_S$ + 8			V
CURRENT, continuous, DC		1.5			A
SLEW RATE	A_V = –100, ±150V Supplies, 250Ω load negative slope, Positiveslope much faster	200	250		V/µS
SETTLING TIME, to 0.1%	A_V = –100, 1V Step, C_C = 0pF		2		µS
RESISTANCE, open loop	DC, 1A Load		7	10	Ω
THERMAL					
RESISTANCE, AC Junction to Case[4]	Full temperature range. f > 60Hz		1.2	1.3	°C/W
RESISTANCE, DC Junction to Case	Full temperature range. f < 60Hz		1.6	1.8	°C/W
RESISTANCE, Junction to Ambient			30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		85	°C
POWER SUPPLY					
VOLTAGE		±15	±100	±150	V
CURRENT, Quiescent total		25	30	35	mA
CURRENT, Quiescent output stage only			10		mA

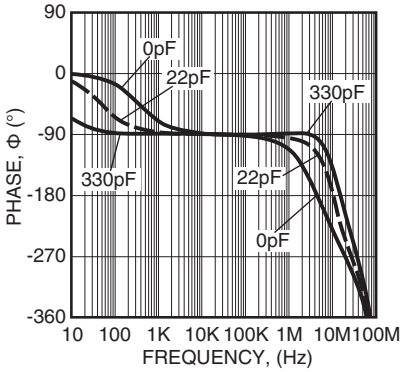
NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage specified under typical (TYP) applies unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

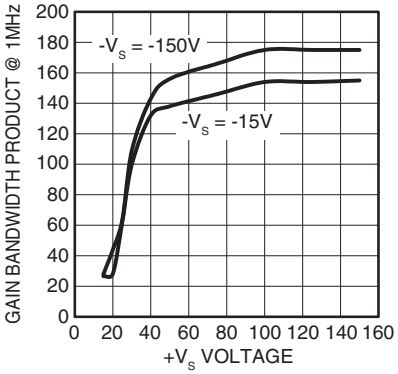
OPEN LOOP FREQUENCY RESPONSE



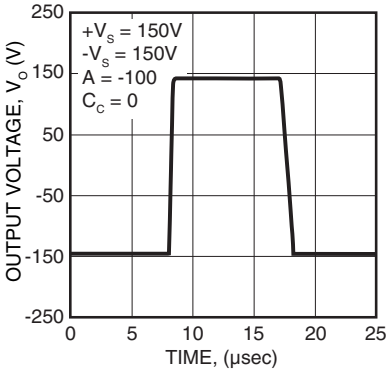
OPEN LOOP PHASE RESPONSE



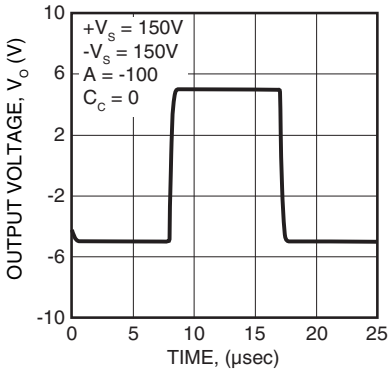
GAIN BANDWIDTH vs. +SUPPLY VOLTAGE



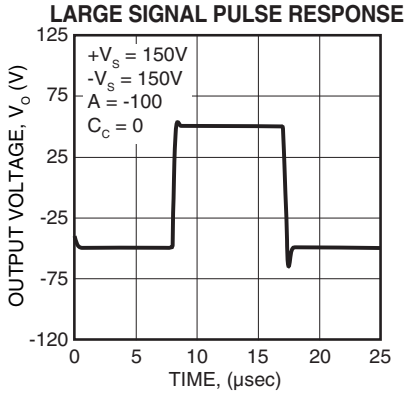
RAIL TO RAIL PULSE RESPONSE



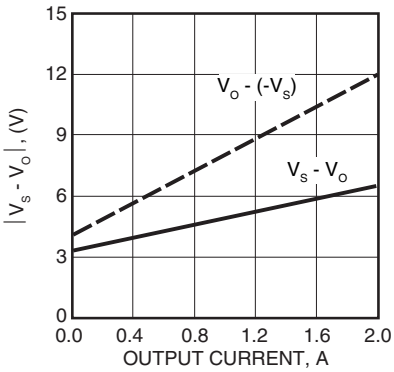
SMALL SIGNAL PULSE RESPONSE



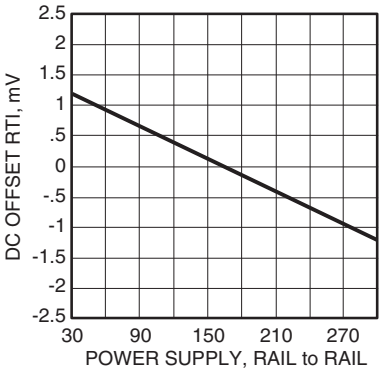
LARGE SIGNAL PULSE RESPONSE



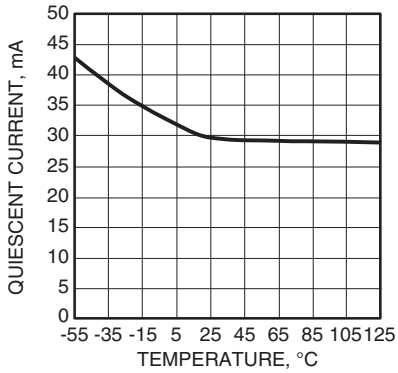
OUTPUT VOLTAGE SWING



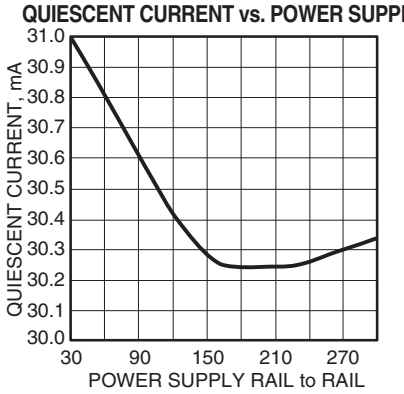
DC OFFSET vs. POWER SUPPLY



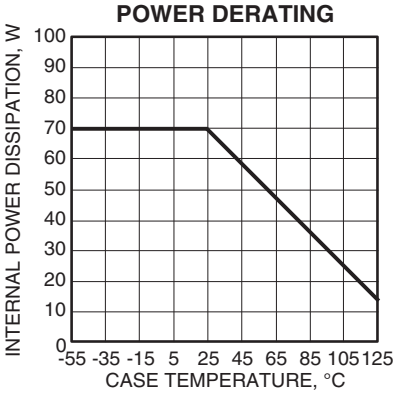
QUIESCENT CURRENT vs. TEMP.



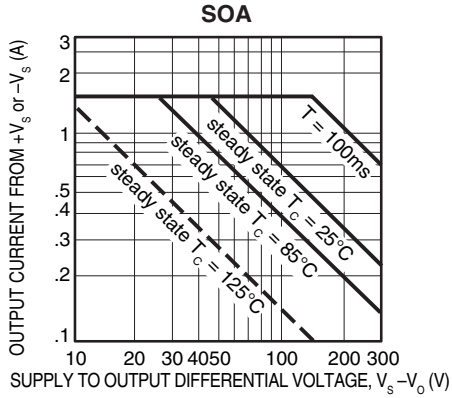
QUIESCENT CURRENT vs. POWER SUPPLY



POWER DERATING



SOA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

SPECIAL PRECAUTIONS

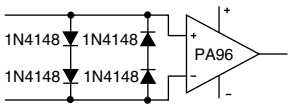
The PA96 operates with up 300V rail to rail voltage, and delivers amperes of current. Precautions should be taken for the safety of the user and the amplifier.

Although the non-operating common mode input range is rail to rail, the differential input voltage must not exceed ±15 V.

Therefore; if the feedback ratio is less than 10, even if caused by disconnecting a signal source , typical power turn on transients can destroy the amplifier.

Similarly in a voltage follower application a large differential transient can be generated if the slew rate of the input is greater than that of the voltage follower.

Therefore it is prudent to clamp the input with series back to back diodes as shown below.



If experimentally optimizing the compensation capacitor, turn off the supplies and let them bleed to low voltage before installing each new value. Otherwise internal current pulses of up to 3 amps can be induced. Also, do you want your fingers around 300V?

Essentially the full rail to rail power supply voltage may be applied to the compensation capacitor. A 400V COG or Mica capacitor is recommended.

POWER BANDWIDTH

The power bandwidth is 1/(π x the negative edge slew time). The slew time is determined by the compensation capacitor, load, and internal device capacitance; it is independent of closed loop gain. The uncompensated power bandwidth is typically 100kHz for a 250Vp-p output signal into 100Ω. It typically increases to above 300KHz with no load.

COMPENSATION TABLE

The following table tabulates recommended compensation capacitor values vs. gain. These values will typically result in less than 2% overshoot and a -3db small signal bandwidth of greater than 1MHz, except under operating conditions where uncompensated gain bandwidth is too low to support a 1MHz bandwidth. (See gain bandwidth vs. Plus power supply curves). Note that other factors such as capacitance in parallel with the feedback resistor may reduce circuit bandwidth from that determined from the gain bandwidth curve.

Cc	Inverting Gain	
	From	To
150pf	1	2
51pf	2	5
33pf	5	10
22pf	10	20
10pf	20	50
5pf	50	100
None	100	up

Cc	Non-Inverting Gain	
	From	To
330 pf	1	2
150pf	2	3
51pf	3	6
33pf	6	10
22pf	10	20
10pf	20	50
5pf	50	100
None	100	up

CURRENT LIMIT

For proper operation the current limit resistor, Rcl, must be connected as shown in the external connections diagram. The minimum value is 0.2Ω, with a maximum practical value of 100Ω. For optimum reliability the resistor should be set as high as possible. The value is calculated as $I_L = 0.68V/Rcl$. Note that the 0.68V is reduced by 2mV every °C rise in temperature.

Also note that the current limit can be set such that the SOA is exceeded on a continuous basis. As an example if the current limit was set at 1.5A and the supply was at 150V, a short to ground would produce 225 watts internal dissipation, greatly exceeding the 83 watt steady state SOA rating.

Under some conditions of load and compensation the amplifier may oscillate at a low level when current limit is active, even though the amplifier is stable otherwise. The current will be limited to the programmed value in this situation. To minimize such occurrences, use a non-reactive resistor to program current limit.

Power Operational Amplifiers

FEATURES

- HIGH VOLTAGE — 900V (±450V)
- LOW QUIESCENT CURRENT — 600µA
- HIGH OUTPUT CURRENT — 10mA

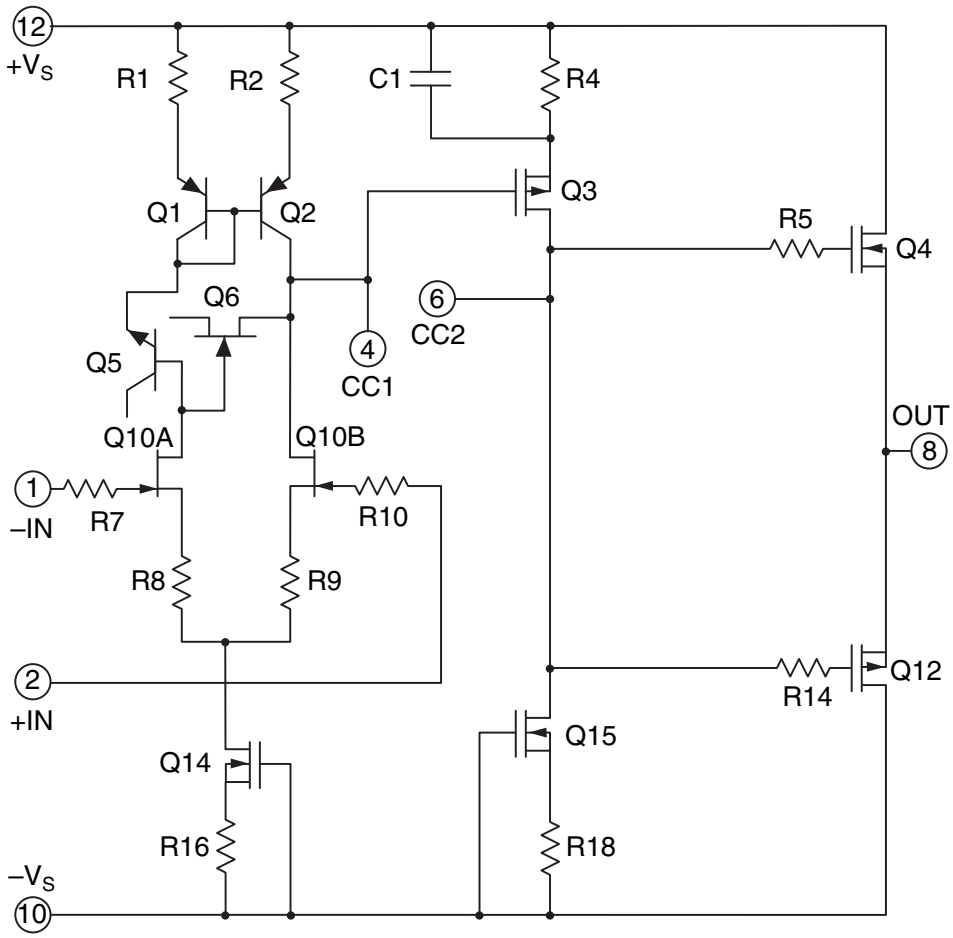
APPLICATIONS

- MASS SPECTROMETERS
- SCANNING COILS
- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO 880V
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

DESCRIPTION

The PA97DR is a high voltage MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 10mA and pulse currents to 15mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations. The MOSFET output stage is biased class C for low quiescent current operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Precision Power's SIP05 package uses a minimum of board space allowing for high density circuit boards.

EQUIVALENT SCHEMATIC



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			900	V
OUTPUT CURRENT, source, sink, within SOA			15	mA
POWER DISSIPATION,continuous @ TC = 25ºC			5	W
INPUT VOLTAGE, differential (Note 3)		-20	20	V
INPUT VOLTAGE, common mode (See Text)		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			220	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−65	150	°C
OPERATING TEMPERATURE, case		−55	125	°C

SPECIFICATIONS

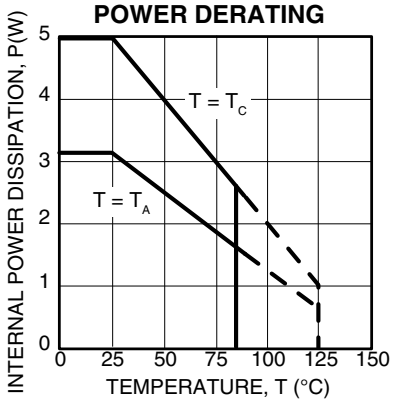
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			0.5	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		10	50	µV/°C
OFFSET VOLTAGE vs. supply			10	25	µV/V
OFFSET VOLTAGE vs. time			75		µV/kHz
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)	V_S=±250V	$\pm V_S$ ∓ 30			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	10KHz BW, R_S = 1KΩ, C_C = 10pF		2		µVRMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 5KΩ, C_C = 10pF	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 5KΩ, C_C = 10pF		1		MHz
POWER BANDWIDTH	R_L = 5KΩ, C_C = 10pF		2		kHz
PHASE MARGIN, A_V = 100	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING (Note 3)	I_O = 10mA	$\pm V_S$ ∓ 24	$\pm V_S$ ∓ 20		V
CURRENT, continuous		10			mA
SLEW RATE, A_V = 100	C_C = 10pF		8		V/µS
SETTLING TIME, to 0.1%	C_C = 10pF, 2V step		2		µS
RESISTANCE	10mA Load		100		Ω

Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE (Note 5)		±50	±300	±450	V
CURRENT, quiescent, amplifier only			0.6	1	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, F > 60Hz			20	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			25	°C/W
RESISTANCE, junction to air	Full temp range		40		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

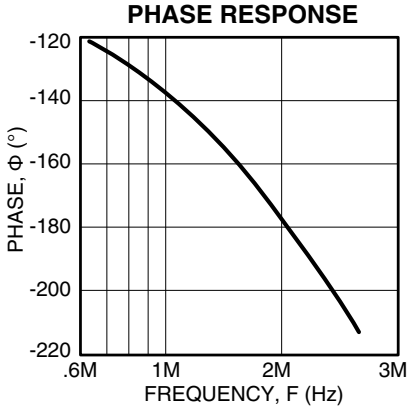
NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. C_C = 10pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 500V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA97DR is constructed from MOSFET transistors. ESD handling procedures must be observed.

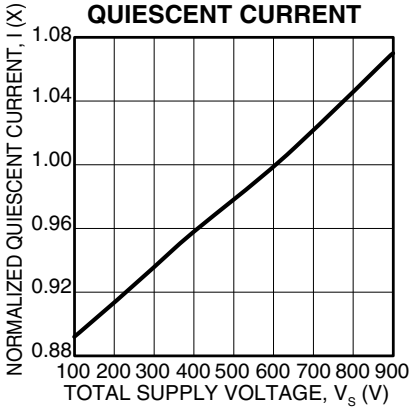
POWER DERATING



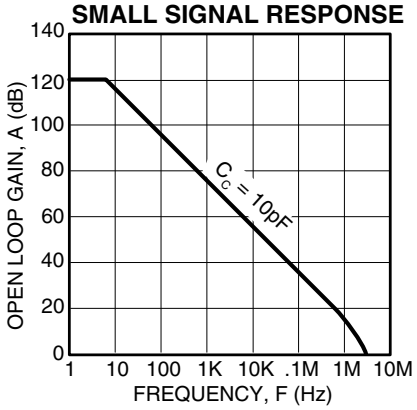
PHASE RESPONSE



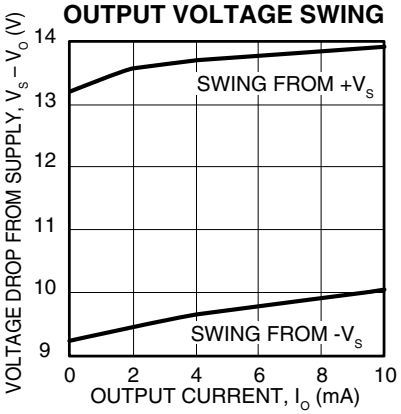
QUIESCENT CURRENT



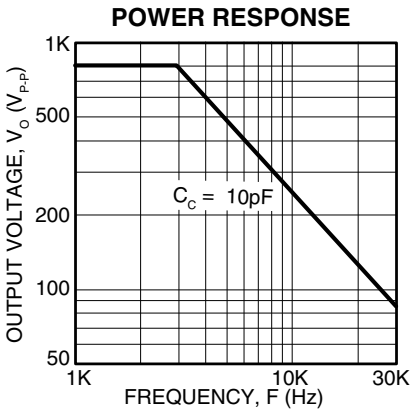
SMALL SIGNAL RESPONSE



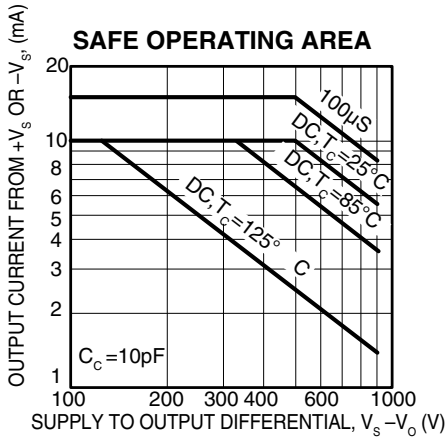
OUTPUT VOLTAGE SWING



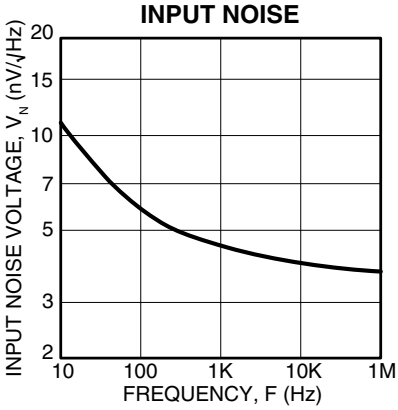
POWER RESPONSE



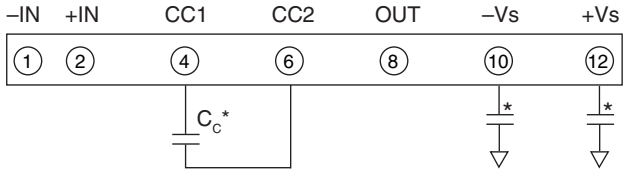
SAFE OPERATING AREA



INPUT NOISE



EXTERNAL CONNECTIONS



* 0.01µF or greater ceramic power supply bypassing required. CC = 10pF minimum, 1kV NPO (COG).

PATENTED

7-pin SIP
PACKAGE STYLE DR

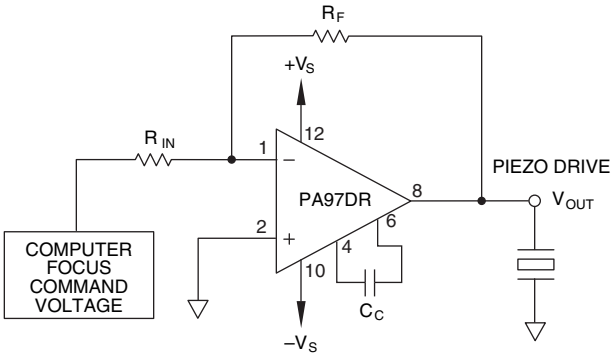
PHASE COMPENSATION

GAIN	C_C
≥10	10pF

TYPICAL APPLICATION

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA97DR reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



GENERAL

Please read the “General Operating Considerations” section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the “Accessory and Package Mechanical Data” section of the handbook.

CURRENT LIMIT

The PA97DR has no provision for current limiting the output.

COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA97DR is restricted. The input pins must always be a least 30V from either supply voltage but never more than 500V. This means that the PA97 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and –100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +500V and -100V does meet the input common mode voltage range requirements since the maximum difference voltage between the inputs pins and the supply voltage is 500V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA97DR can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 2b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does not automatically protect the amplifier from excessive common mode input voltages.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. 10pF NPO (COG)capacitor rated at 1kV is recommended.

Of equal importance is the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 900 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

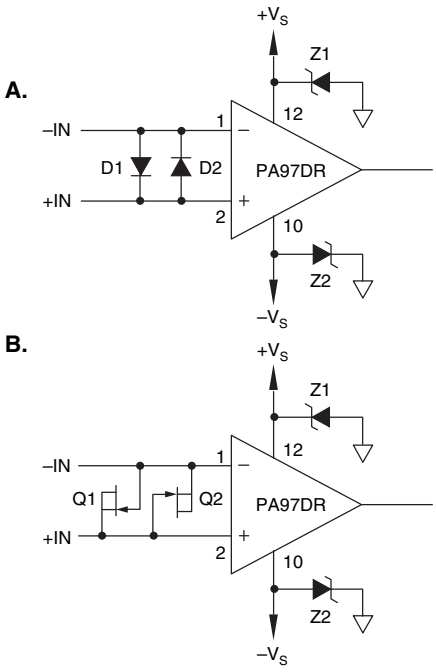


FIGURE 2.

CAUTIONS

The operating voltages of the PA97DR are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting. With no internal current limit, proper choice of load impedance and supply voltage is required to meed SOA limitiations. An output short circuit will destroy the amplifier within milliseconds.

STABILITY

The PA97DR is stable at gains of 10 or more with a NPO (COG) compensation capacitor of 10pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 10pF is not recommended.

Power Operational Amplifiers

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- HIGH SLEW RATE — 1000V/µS
- HIGH OUTPUT CURRENT — 200mA

APPLICATIONS

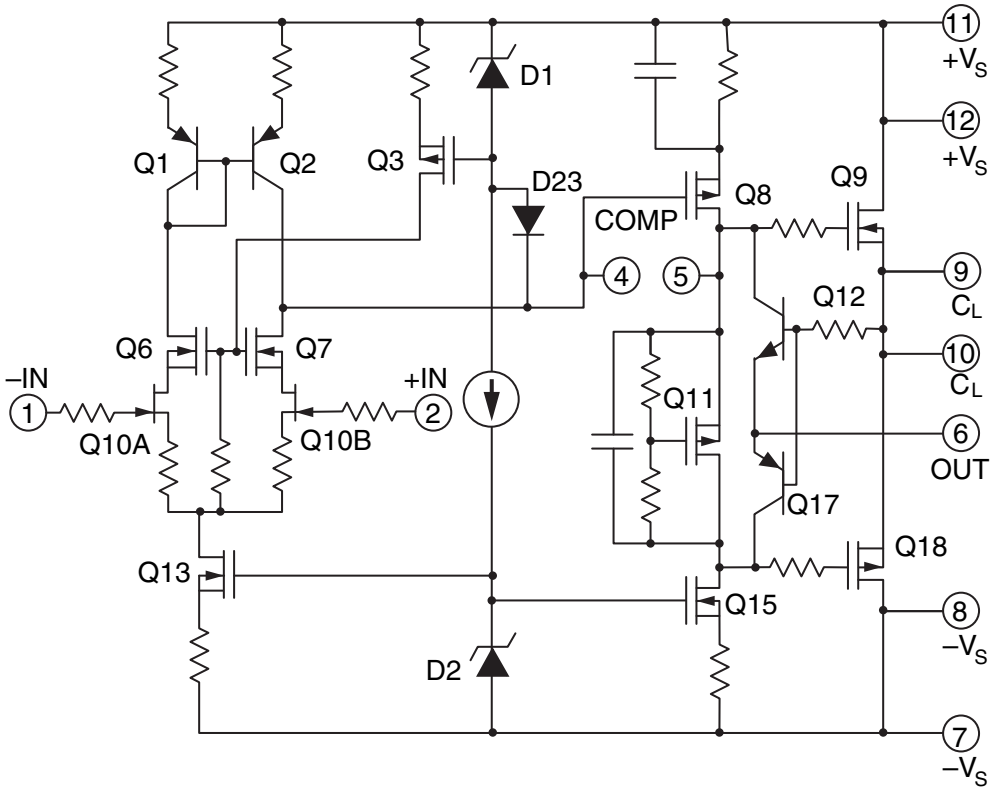
- HIGH VOLTAGE INSTRUMENTATION
- PIEZO TRANSDUCER EXCITATION
- PROGRAMMABLE POWER SUPPLIES UP TO 430V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION

DESCRIPTION

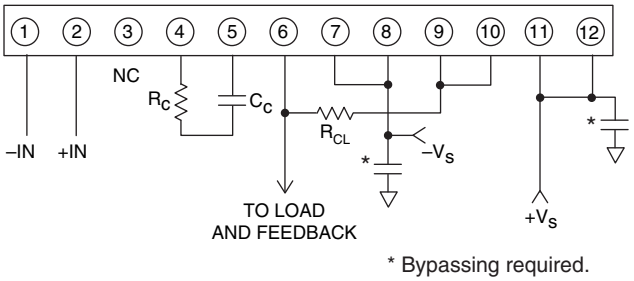
The PA98 is a high voltage, high power bandwidth MOSFET operational amplifier designed for output currents up to 200mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA98 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility. This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The Power SIP package is electrically isolated.

E

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



* Bypassing required.

PATENTED

12-pin SIP PACKAGE STYLE DP
Formed leads available
Package style EE

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			450	V
OUTPUT CURRENT, continuous within SOA			200	mA
POWER DISSIPATION, continuous @ T_C = 25°C (Note 2)			30	W
INPUT VOLTAGE, differential		-25	25	V
INPUT VOLTAGE, common mode		$-V_S$	V_S	V
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−40	85	°C
OPERATING TEMPERATURE RANGE, case		−25	85	°C

CAUTION The PA98 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

SPECIFICATIONS

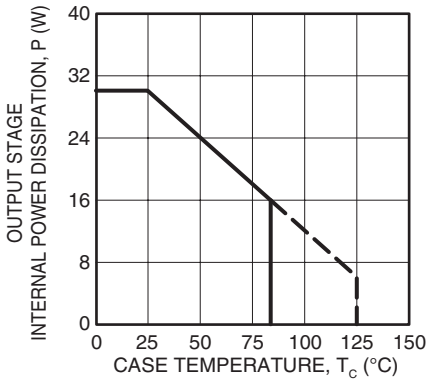
Parameter	Test Conditions[1]	PA98			PA98A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE, initial			0.5	2		0.25	0.5	mV
OFFSET VOLTAGE vs. temp	Full temp range		10	30		5	10	µV/°C
OFFSET VOLTAGE vs. supply			3	10		*	*	µV/V
OFFSET VOLTAGE vs. time			75			*		µV/kHz
BIAS CURRENT, initial (Note 3)			5	50		3	10	pA
BIAS CURRENT, vs. supply			0.01			*		pA/V
OFFSET CURRENT, initial (Note 3)			10	100		3	30	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE (Note 4)		$\pm V_S$ - 15			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB

Parameter	Test Conditions[1]	PA98			PA98A			Units
		Min	Typ	Max	Min	Typ	Max	
NOISE	100kHz BW, R_S = 1KΩ, C_C = 10pf		1			*		µV RMS
GAIN								
OPEN LOOP GAIN @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 2KΩ, C_C = 3.3pf		100			*		MHz
POWER BANDWIDTH	C_C = 10pf		300			*		kHz
	C_C = 3.3pf		500			*		kHz
PHASE MARGIN	Full temp range		60			*		°
OUTPUT								
VOLTAGE SWING (Note 4)	I_O = ±200mA	±V_S - 10	±V_S - 6.5		*	*		V
VOLTAGE SWING (Note 4)	I_O = ±75mA	±V_S - 8.5	±V_S - 6.0		*	*		V
VOLTAGE SWING (Note 4)	I_O = ±20mA	±V_S - 8.0	±V_S - 5.5		*	*		V
CURRENT, continuous	T_C = 85°C	±200				*		mA
SLEW RATE, A_V = 20	C_C = 10pf		400			*		V/µS
SLEW RATE, A_V = 100	C_C = OPEN		1000		700	*		V/µS
CAPACITIVE LOAD, A_V = +1	Full temp range	470			*			pF
SETTLING TIME to 0.1%	C_C = 10pf, 2V step		1			*		µS
RESISTANCE, no load	R_{CL} = 0		50			*		Ω
POWER SUPPLY								
VOLTAGE (Note 6)	Full temp range	±15	±150	±225	*	*	*	V
CURRENT, quiescent			21	25		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case (Note 5)	Full temp range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temp range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temp range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	*		*	°C

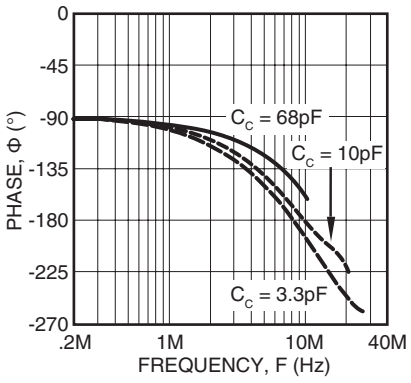
NOTES: * The specification of PA98A is identical to the specification for PA98 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. Ratings apply only to output transistors. An additional 10W may be dissipated due to quiescent power.
3. Doubles for every 10°C of temperature increase.
4. +V_S and –V_S denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating 0.625 V/°C below 25°C case. No derating needed above 25°C case.

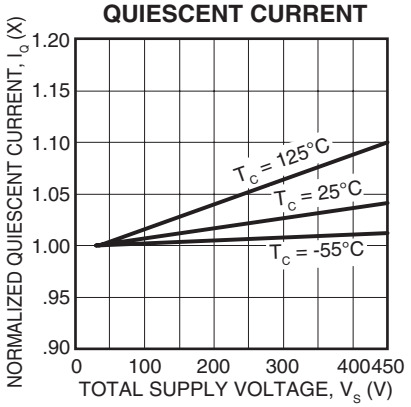
POWER DERATING



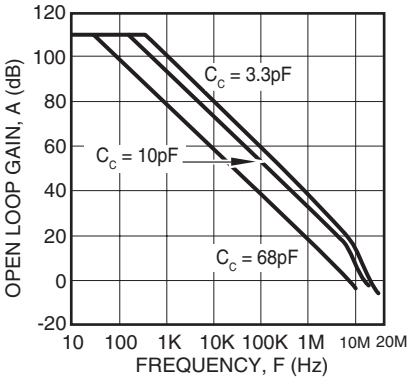
PHASE RESPONSE



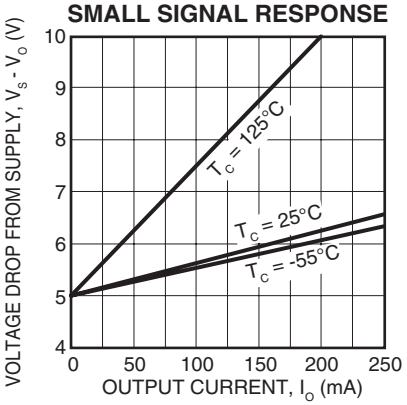
QUIESCENT CURRENT



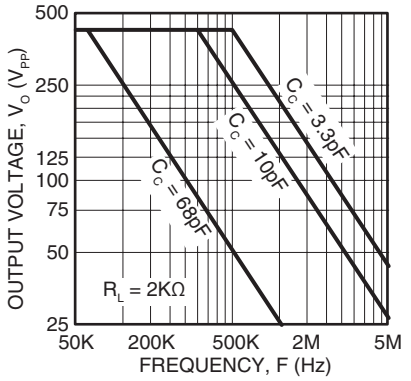
SMALL SIGNAL RESPONSE



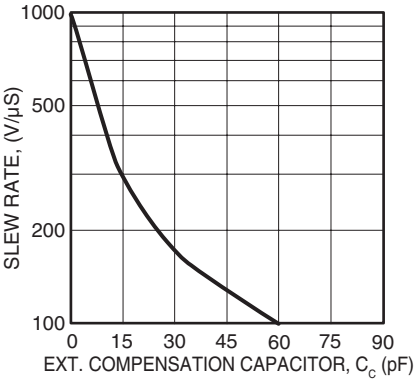
SMALL SIGNAL RESPONSE



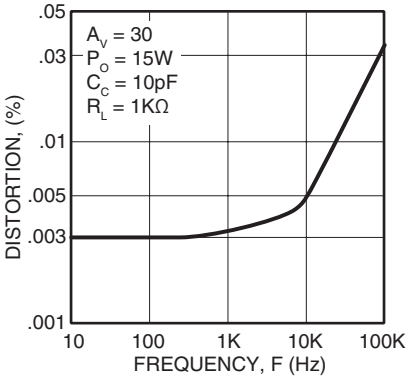
SMALL SIGNAL RESPONSE



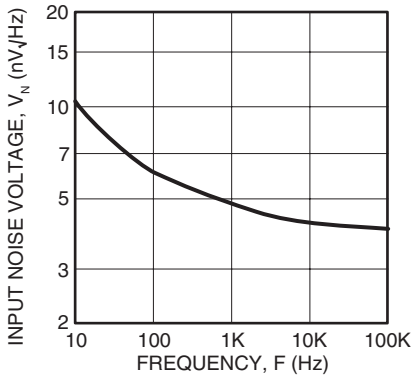
SLEW RATE



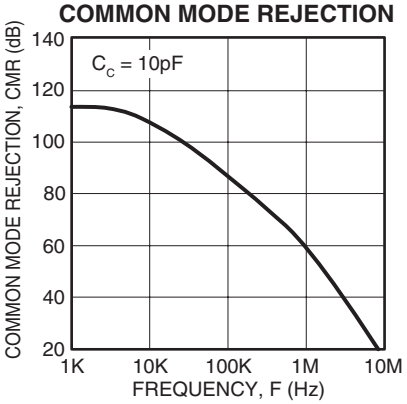
HARMONIC DISTORTION



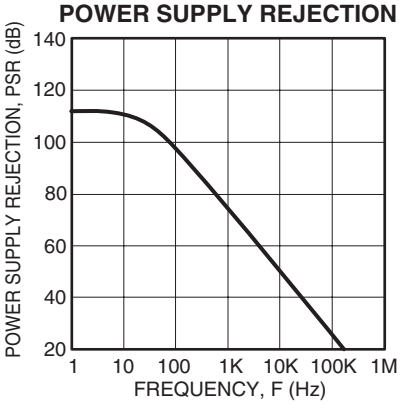
INPUT NOISE VOLTAGE



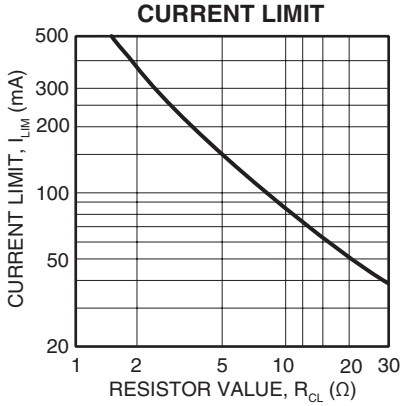
COMMON MODE REJECTION



POWER SUPPLY REJECTION

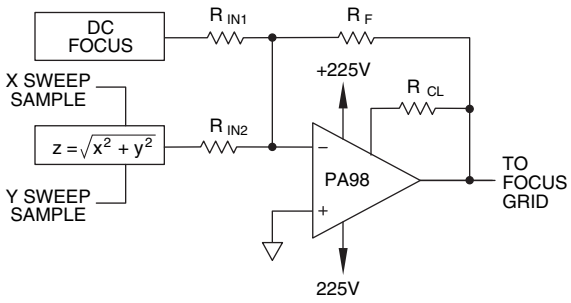


CURRENT LIMIT



TYPICAL APPLICATION

DYNAMIC FOCUSING



Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA98 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages by calculating the distance of the beam from the center of the display.

PHASE COMPENSATION

Gain	C_C	R_C
1	68pF	100Ω
20	10pF	330Ω
100	3.3pF	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 1.4 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{CL} = \frac{.7}{I_{LIM} - .016}$$

SAFE OPERATING AREA (SOA)

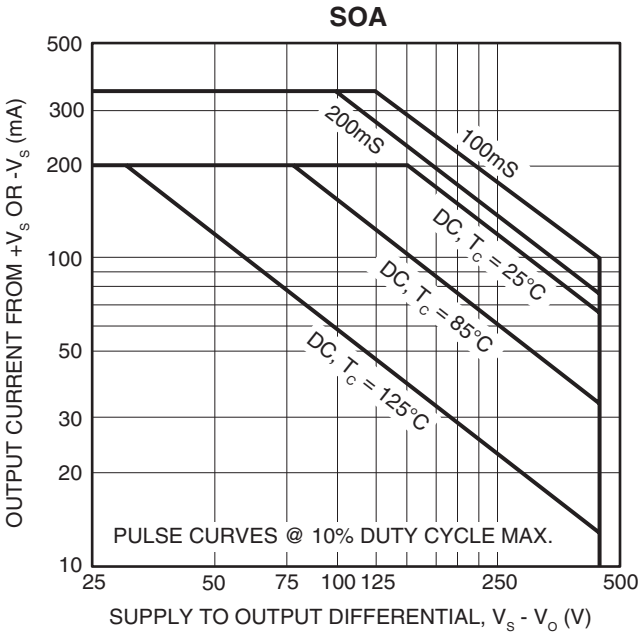
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.



INPUT PROTECTION

Although the PA98 can withstand differential voltages up to ±25V, additional external protection is recommended. Since the PA98 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 1). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

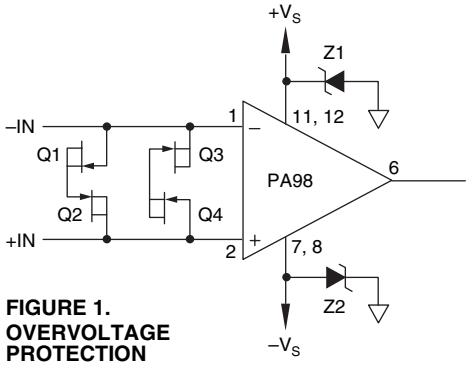


FIGURE 1. OVERVOLTAGE PROTECTION

STABILITY

The PA98 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

INTERNAL POWER DISSIPATION AND HEATSINK SELECTION

With the unique combination of high voltage and speed of the PA98, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of this amplifier. To more accurately predict operating temperatures use Power Design[1] revision 10 or higher, or use the following procedure:

Find internal dissipation (PD) resulting from driving the load. Use Power Design or refer to Apex Precision Power Applications Note 1, General Operating Considertaions, paragraph 7. Find total quiescent power (PD_Q) by multiplying 0.025A by V_{SS} (total supply voltage). Find output stage quiescent power (PD_{QOUT}) by multiplying 0.001 by V_{SS}. Calculate a heatsink rating which will maintain the case at 85°C or lower.

$$R_{\Theta SA} = \frac{T_C - T_A}{PD + PD_Q} \text{-0.1°C/W}$$

Where: T_C = maximum case temperature allowed
T_A = maximum ambient temperature encountered

Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower.

$$R_{\Theta SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) * R_{\Theta JC}}{PD + PD_Q} \text{-0.1°C/W}$$

Where: T_J = maximum junction temperature allowed.
$R_{\Theta JC}$ = AC or DC thermal resistance from the specification table.
Use the larger heatsink of these two calculations.

Power Design is an Excel spreadsheet available free from www.cirrus.com

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- High Voltage 180 Vp-p
- High Slew Rate 2500 V/µs Minimum with A_{CL} = 20
- High Gain Bandwidth 180 MHz
- High Output Current ±1.5 A Steady State Within SOA
- High Peak Output Current ±5 A

APPLICATIONS

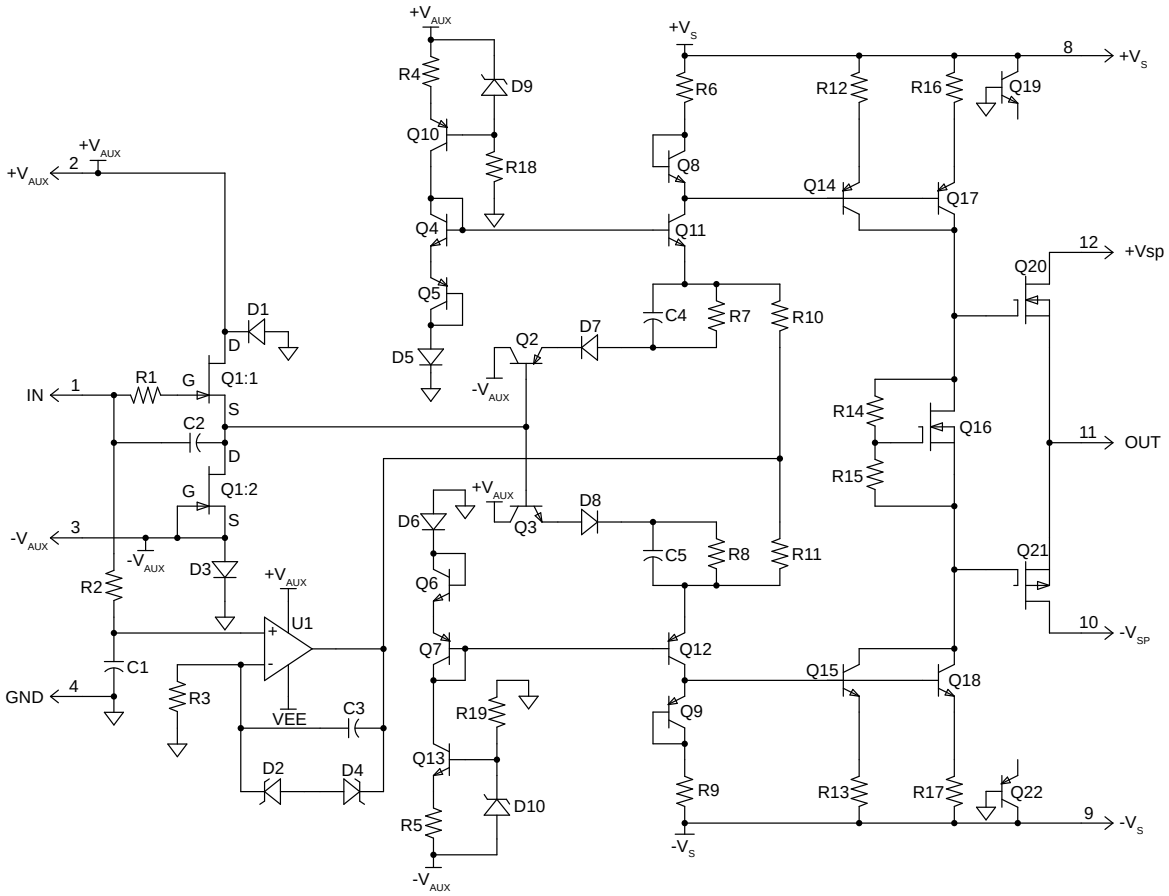
- Piezo Drive
- CRT Beam Intensity Control
- ATE Applications
- Line Driver

GENERAL DESCRIPTION

The PA107DP is a state of the art wideband high power operational amplifier designed to drive resistive, capacitive or inductive loads. For optimum linearity the output stage is biased for class A/B operation. Feed forward technology is used to obtain wide bandwidth and excellent DC performance, but constricts use to inverting mode only. External compensation allows the user to obtain both high gain and wide bandwidth. Use of a heatsink is required to realize the SOA.

This hybrid integrated circuit uses thick film resistors, ceramic capacitors, and semiconductors to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12 pin SIP package occupies only 2 square inches. The use of compressible insulation washers voids the warranty.

EQUIVALENT SCHEMATIC



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$		40	200	V
SUPPLY VOLTAGE, $-V_S$		-20	-100	V
SUPPLY VOLTAGE, $-V_{AUX}$ to $+V_{AUX}$		20	36	V
SUPPLY VOLTAGE, $-V_{AUX}$		-10	-18	V
OUTPUT CURRENT, Steady State, (Within SOA)			1.5	A
OUTPUT CURRENT, peak, (Within SOA)			5	A
POWER DISSIPATION, internal, DC			62.5	W
INPUT VOLTAGE		$-V_{AUX}$ + 2	$+V_{AUX}$ - 2	V
TEMPERATURE, pin solder, 10s			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		-40	+85	°C
OPERATING TEMPERATURE, case		-25	+85	°C

SPECIFICATIONS

Parameter	Test Conditions	Min	Typ	Max	Units
	V_S = 100V, $-V_S$ = -100V, V_{AUX} = 15V, $-V_{AUX}$ = -15V				
INPUT					
OFFSET VOLTAGE			5	10	mV
OFFSET VOLTAGE vs. temperature			10		µV/°C
BIAS CURRENT, initial (Note 3)			300		pA
INPUT RESISTANCE, DC		13			GΩ
INPUT CAPACITANCE			2		pF
INPUT VOLTAGE RANGE		$-V_{AUX}$ + 2		$+V_{AUX}$ - 2	V
NOISE, RTI	1k source, 500 kHz BW, A_{CL} 101		13		nV/√Hz
GAIN					
OPEN LOOP GAIN @ DC			140		dB
OPEN LOOP GAIN @ 1MHz			40		dB
POWER BANDWIDTH, 170Vp-p	Full temperature range	2			MHz
OUTPUT					
VOLTAGE SWING	10MΩ in parallel with 10 pf		187		V_{P-P}
VOLTAGE SWING	I_O = 1.5A	$\pm V_S$ ±10			V
CURRENT, peak				±5	A
CURRENT, Steady State (within SOA)				±1.5	A
SLEW RATE, 25% to 75%		2500	3000		V/µS
SETTLING TIME to 0.1%			12		µS

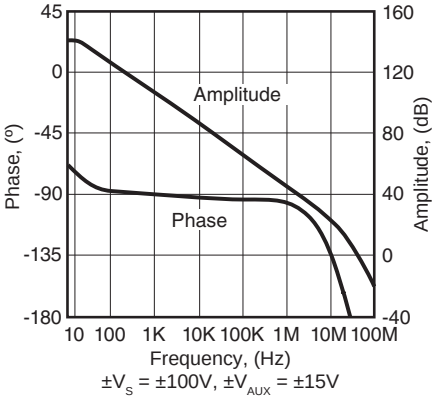
Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE, $+V_S$		20		100	V
VOLTAGE, $-V_S$		-100		-20	V
VOLTAGE, $+V_{AUX}$		10	15	18	V
VOLTAGE, $-V_{AUX}$		-18	-15	-10	V
CURRENT, QUIESCENT, $+V_S$		20	30	35	mA
CURRENT, QUIESCENT, $-V_S$		20	30	35	mA
CURRENT, QUIESCENT, $-V_{AUX}$		16	19	21	mA
CURRENT, QUIESCENT, $+V_{AUX}$		16	19	21	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 6)				1.5	°C/W
RESISTANCE, DC junction to case				2	°C/W
RESISTANCE, junction to air				30	°C/W
TEMPERATURE RANGE, case		-25		85	°C

NOTES:

1. All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10ºC of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stages.
5. $+V_{AUX}$ and $-V_{AUX}$ denote the positive and negative supply voltages to the input stages.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

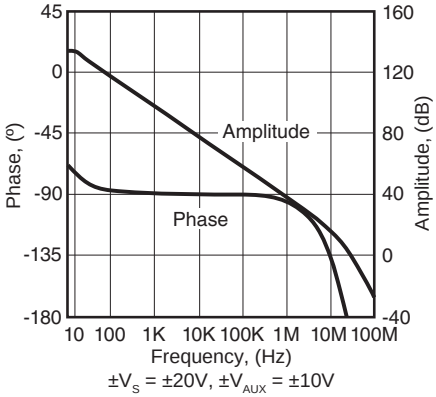
2. TYPICAL PERFORMANCE GRAPHS

HIGH VOLTAGE SMALL SIGNAL RESPONSE



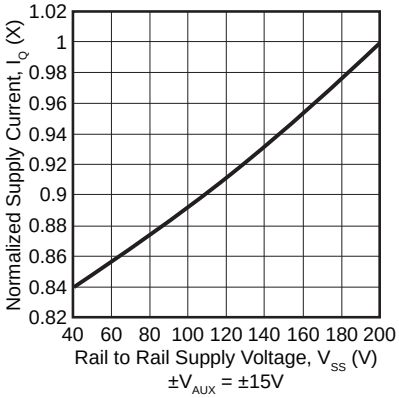
$\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

LOW VOLTAGE SMALL SIGNAL RESPONSE



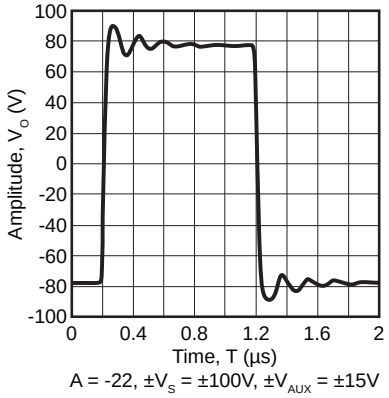
$\pm V_S$ = ±20V, $\pm V_{AUX}$ = ±10V

HIGH VOLTAGE SUPPLY CURRENT



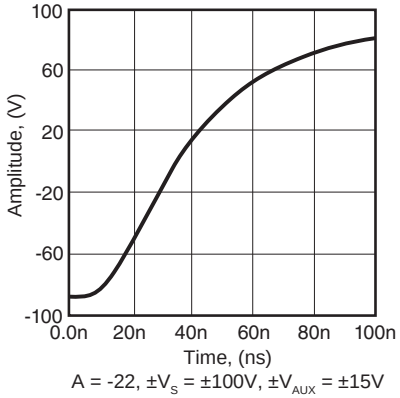
$\pm V_{AUX}$ = ±15V

RESPONSE to 500KHz SQUARE WAVE



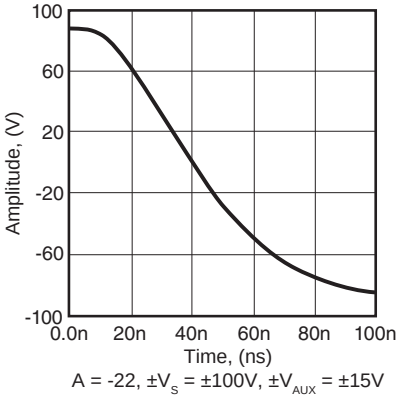
A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

POSITIVE SLEW



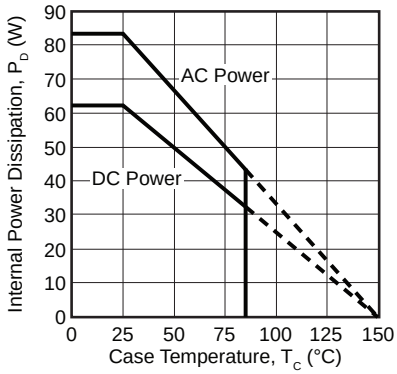
A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

NEGATIVE SLEW

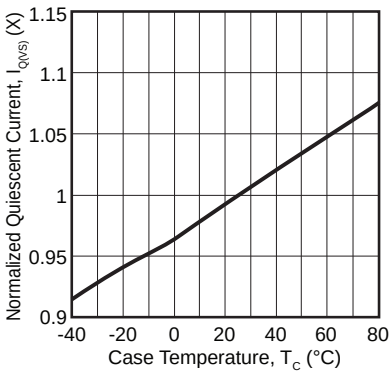


A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

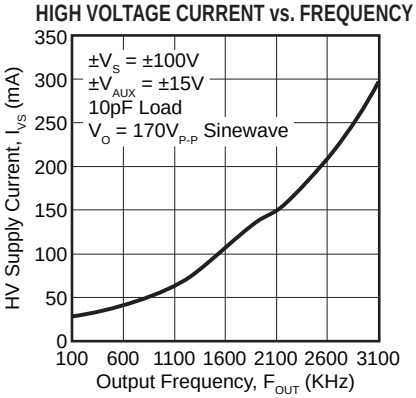
POWER DERATING



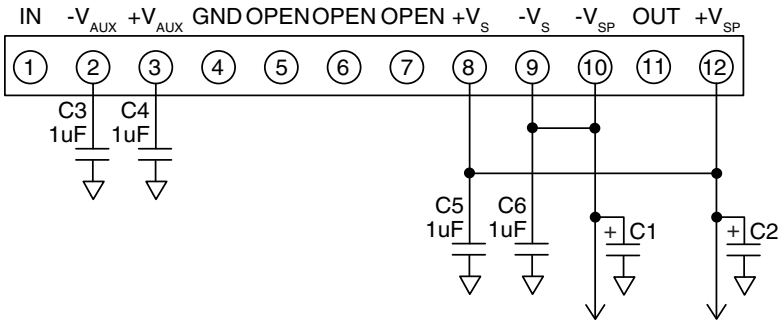
HIGH VOLTAGE CURRENT vs. TEMPERATURE



HIGH VOLTAGE CURRENT vs. FREQUENCY



EXTERNAL CONNECTIONS



C1-2 = 10uF/A out (peak), electrolytic/tantalum, low frequency bypass.
C3-4 = 1uF 25V X7R ceramic capacitor recomended.
C5-6 = 1uF 200V X7R ceramic capacitor recomended.

12-pin SIP
Package Style DP
Formed leads available
See Package Style EE

PIN DESCRIPTIONS

Pin #	Pin name	Description
1	IN	Summing Junction Input for Inverting Operational Amplifier
2	$+V_{AUX}$	+10V to +18V Supply for Input Circuits
3	$-V_{AUX}$	-10V to -18V Supply for Input Circuits
4	GND	Ground
5		Open Pin
6		Open Pin
7		Open Pin
8	$+V_S$	+20V to +100V Supply for Gain and Gate Driver Circuits
9	$-V_S$	-20V to -100V Supply for Gain and Gate Driver Circuits
10	$-V_{SP}$	-20V to -100V Supply for Output Source Follower
11	OUT	High Power Output of Amplifier
12	$+V_{SP}$	+20V to +100V Supply for Output Source Follower

3. GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

CAUTION

In order to achieve the highest speed with limited space short circuit protection and thermal protection were sacrificed. Do not short the output. Note that if current limiting at 1.5 A could be used, and the output was shorted, internal dissipation would be 150 W. This would still destroy the amplifier, albeit more slowly.

4. INTERNAL POWER DISSIPATION AND HEATSINK SELECTION

With the unique combination of high voltage and speed of the PA107, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of this amplifier. To more accurately predict operating temperatures use Power Design1 revision 10 or higher, or use the following procedure:
Find internal dissipation (PD) resulting from driving the load. Use Power Design or refer to Apex Applications Note 1, General Operating Considerations, paragraph 7. Find total quiescent power (PD_Q) by multiplying 0.035 A by V_{SS} (total supply voltage), plus 0.021 times the total V_{AUX} ($+V_{AUX} + |-V_{AUX}|$). Find output stage quiescent power (PD_{QOUT}) by multiplying 0.001 by V_{SS}.
Calculate a heatsink rating which will maintain the case at 85°C or lower.

$$R_{\emptyset SA} = \frac{T_C - T_A}{PD + PD_Q} \text{ -0.1°C/W}$$

Where:
T_C = maximum case temperature allowed
T_A = maximum ambient temperature encountered

$$R_{\emptyset SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) \bullet R_{\emptyset JC}}{PD + PD_Q} \text{ -0.1°C/W}$$

Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower.
Where:
T_J = maximum junction temperature allowed.
$R_{\emptyset JC}$ = AC or DC thermal resistance from the specification table.
Use the larger heatsink of these two calculations.
Power Design is an Excel spreadsheet available free from www.cirrus.com

5. REACTIVE LOADS

The PA107DP is stable at a gain of 20 or above when driving either inductive or capacitive loads. However an inductor is essentially a short circuit at DC, therefore there must be enough resistance in series to keep low frequency power within ratings.

When driving a 1nF capacitive load with a 180 V_{P-P} square wave, the current peak is 1 A. Driving the same capacitor with a 2.3 MHz sine wave, the power bandwidth frequency, results in 2.6 A_{P-P}. The power dissipated in the amplifier while driving a purely capacitive load is given by the formula:

$$P = 2V_{PK}V_S/\pi X_C$$
$$P = 2I_{PK}V_S/\pi$$

Where:

V_{PK} = Peak Voltage
V_S = Supply Voltage
X_C = Capacitive Reactance

Notice that the power increases as V_{PK} increases, such that the maximum internal dissipation occurs when V_{PK} is maximum. The power dissipated in the amplifier while driving 1 nF at 2.3 MHz would be 82.76 W. This would not be a good thing to do! But driving 1 nF at 1 MHz at 180V_{P-P} would result in 36.0 W, which could be within the AC power rating.

This formula is optimistic; it is derived for an ideal class B amplifier output stage.

6. FEEDBACK CONSIDERATIONS

The output voltage of an unloaded PA107DP can easily go as high as 95 V. All of this voltage can be applied across the feedback resistor, so the minimum value of a ½ W resistor in the feedback is 18050Ω. Practically, 20K is the minimum value for a un-derated ½ W feedback resistor.

In order to provide the maximum slew rate, power bandwidth, and useable gain bandwidth; the PA107DP is not designed to be unity gain stable. It is necessary to add external compensation for gains less than 20. Often lower performance op-amps may be stabilized with a capacitor in parallel with the feedback resistor. This is because there is effectively one additional pole affecting the response. In the case of the PA107DP, however there are multiple poles clustered near 30 MHz, therefore this approach does not work. A method of compensation that works is to choose a feedback capacitor such that the time constant of the feedback capacitor times the feedback resistor is greater than 33 n-seconds. Also install a capacitor from pin 1 to ground, the summing junction, greater than 20 times as large as the feedback capacitor. The feedback capacitor or summing junction capacitor without the other will degrade stability and often cause oscillation. With the compensation described the closed loop bandwidth will be the reciprocal of $2\pi\tau_{FB}$.

Alternatively, at the expense of noise and offset, the amplifier can be stabilized by a resistor across the summing junction such that the parallel combination of the input resistor and summing junction resistor is less than a twentieth of the value of the feedback resistor. Note that this will increase noise and offset by to 20 times the RTI values, but with 10 mV max offset and 13 nV/$(Hz)^{1/2}$ noise, performance will be acceptable for many applications.

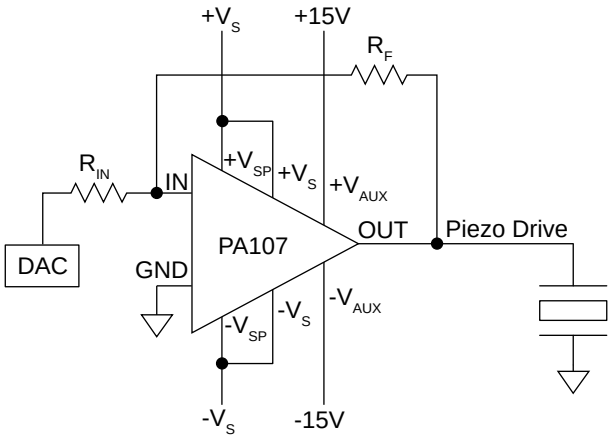
As seen by the very small values of capacitance used in compensation for low gain, stray feedback capacitance and/or summing junction capacitance can have a VERY large effect on performance. Therefore stray capacitance must be minimized in the layout. The summing junction lead must be as short as possible, and ground plane must be kept away from the summing junction lead.

7. SLEW RATE AND FULL POWER BANDWIDTH

In the PA107DP the slew rate is measured from the 25% point to the 75% point of a 180V_{P-P} square wave. Slew rate is measured with no load and with auxiliary supplies at a nominal ±15 V and V_S supplies at a maximum ±100V.

Power bandwidth is defined as the highest frequency at which an unloaded amplifier can have an undistorted sine wave at full power as its output. This frequency can be calculated as the slew rate divided by π times the peak to peak amplitude; which would be 4.7 MHz for the PA107DP. Unfortunately running full output at this frequency causes internal dissipation of up to 107 W, well over the power limits for the PA107DP. Cutting the frequency to 2 MHz reduces internal dissipation to 34 W, acceptable with a good heatsink.

TYPICAL APPLICATION



CONTACTING CIRRUS LOGIC SUPPORT

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For inquiries via email, please contact apex.support@cirrus.com.
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To find the one nearest to you, go to www.cirrus.com

PA119CE • PA119CEA

Video Power Operational Amplifier

FEATURES

- VERY FAST SLEW RATE — 900 V/µs
- POWER MOS TECHNOLOGY — 4A peak rating
- LOW INTERNAL LOSSES — 0.75V at 2A
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- WIDE SUPPLY RANGE — ±15V TO ±40V

APPLICATIONS

- VIDEO DISTRIBUTION AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS UP TO 5 MHz
- MODULATION OF RF POWER STAGES
- POWER LED OR LASER DIODE EXCITATION

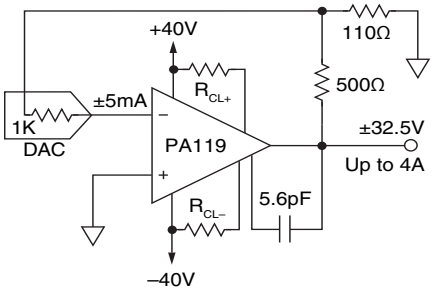
DESCRIPTION

The PA119 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA119 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary power MOS output stage. For optimum linearity, especially at low levels, the power MOS transistors are biased in a class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit of 0.5A can be increased with the addition of two external resistors. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. A heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

TYPICAL APPLICATION



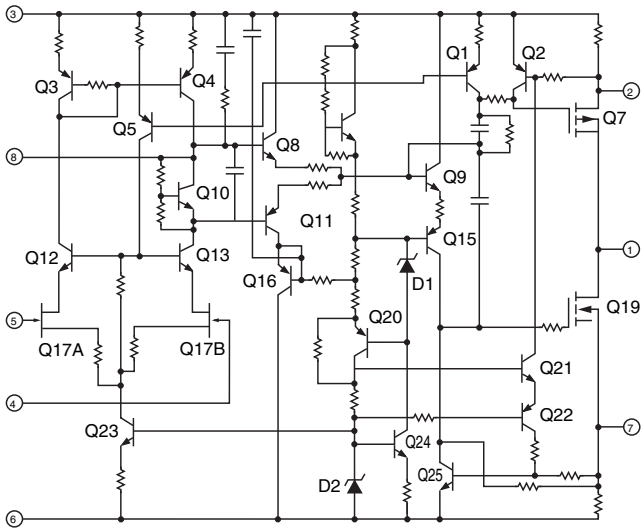
PA119 AS FAST POWER DRIVER

8-pin TO-3
PACKAGE STYLE CE

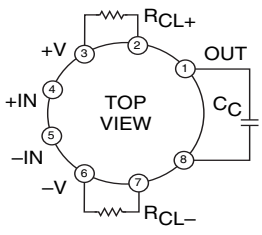
TYPICAL APPLICATION

This fast power driver utilizes the 900V/µs slew rate of the PA119 and provides a unique interface with a current output DAC. By using the DAC's internal 1KΩ feedback resistor, temperature drift errors are minimized, since the temperature drift coefficients of the internal current source and the internal feedback resistor of the DAC are closely matched. Gain of V_{OUT} to I_{IN} is –6.5/mA. The DAC's internal 1K resistor together with the external 500Ω and 110Ω form a "tee network" in the feedback path around the PA119. This effective resistance equals 6.5KΩ . Therefore the entire circuit can be modeled as 6.5KΩ feedback resistor from output to inverting input and a 5mA current source into the inverting input of the PA119. Now we see the familiar current to voltage conversion for a DAC where $V_{OUT} = -I_{IN} \times R_{FEEDBACK}$.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C
1	330pF
10	22pF
100	2.2pF
1000	none

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	75W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder — 10 sec	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to 150°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

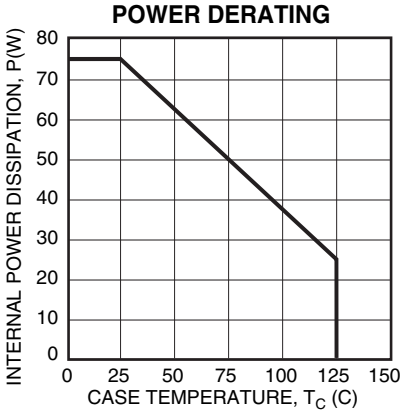
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA119 MIN	PA119 TYP	PA119 MAX	PA119A MIN	PA119A TYP	PA119A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±3		±.35	±.75	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25°C to +85°C		10	30		5	15	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		10	200		5	50	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		5	100		3	25	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = 25°C to +85°C	$\pm V_S$–15	$\pm V_S$–12		*	*		V
COMMON MODE REJECTION, DC	T_C = 25°C to +85°C, V_{CM} = ±20V	70	104		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1KΩ		111			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	74	88		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, C_C = 2.2pF		100			*		MHz
POWER BANDWIDTH, A_V = 100	T_C = 25°C, C_C = 2.2pF		3.5			*		MHz
POWER BANDWIDTH, A_V = 1	T_C = 25°C, C_C = 330pF		250			*		kHz
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 4A	$\pm V_S$–5	$\pm V_S$–1.5		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 2A	$\pm V_S$–3	$\pm V_S$–.75		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 78mA	$\pm V_S$–1	$\pm V_S$–.5		*	*		V
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, A_V = 100	T_C = 25°C, C_C = 2.2pF	600	900		750	*		V/µs
SLEW RATE, A_V = 10	T_C = 25°C, C_C = 22pF		650			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = 25°C to +85°C	±15	±35	±40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		100	120		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = 25°C to +85°C, F > 60Hz		1.46	1.64		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = 25°C to +85°C, F < 60Hz		1.84	2.0		*	*	°C/W
RESISTANCE, junction to air	T_C = 25°C to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

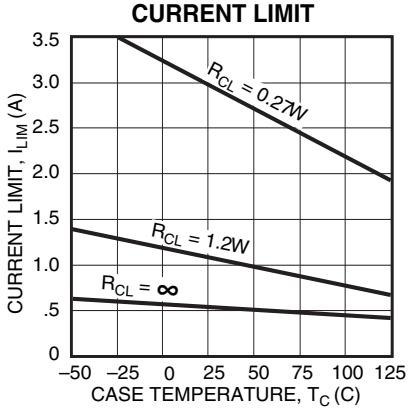
NOTES: * The specification of PA119A is identical to the specification for PA119 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

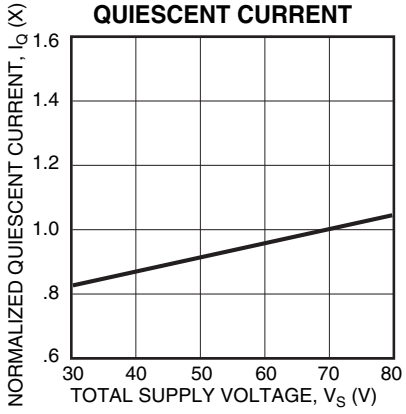
POWER DERATING



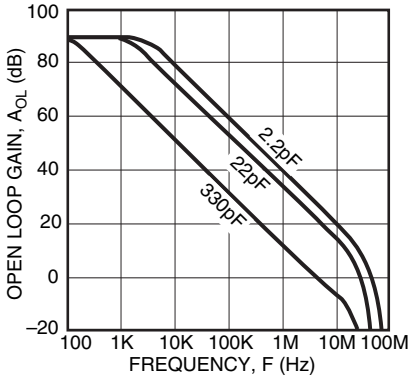
CURRENT LIMIT



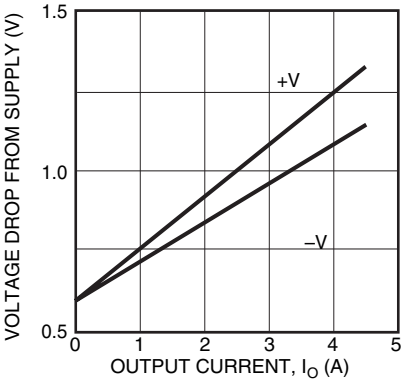
QUIESCENT CURRENT



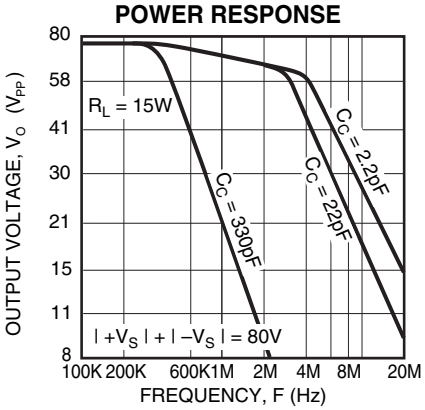
SMALL SIGNAL RESPONSE



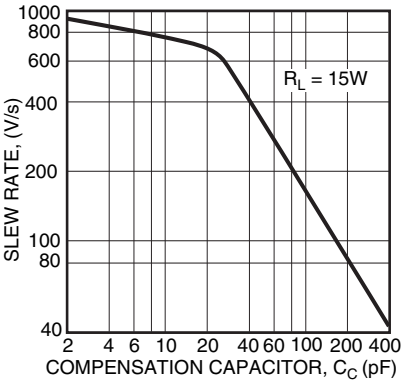
OUTPUT VOLTAGE SWING



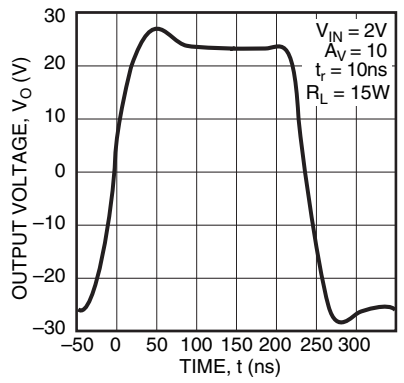
POWER RESPONSE



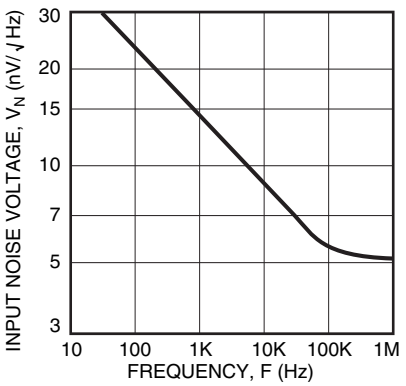
SLEW RATE VS. COMP.



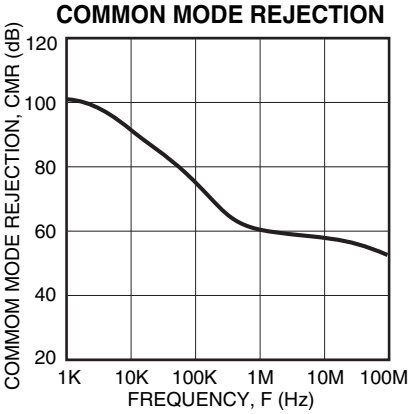
PULSE RESPONSE



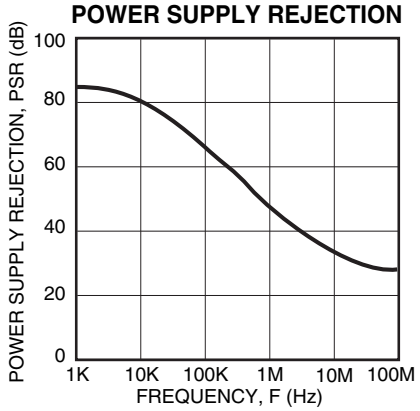
INPUT NOISE



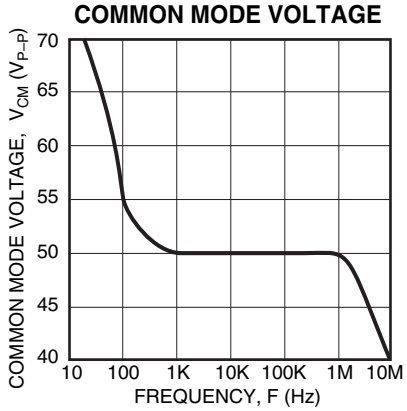
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

Q2 (and Q25) limit output current by turning on and removing gate drive when voltage on pin 2 (pin 7) exceeds .65V differential from the positive (negative) supply rail. With internal resistors equal to 1.2Ω, current limits are approximately 0.5A with no external current limit resistors. With the addition of external resistors current limit will be:

$$I_{LIM} = \frac{.65V}{R_{CL}} + .54A$$

To determine values of external current limit resistors:

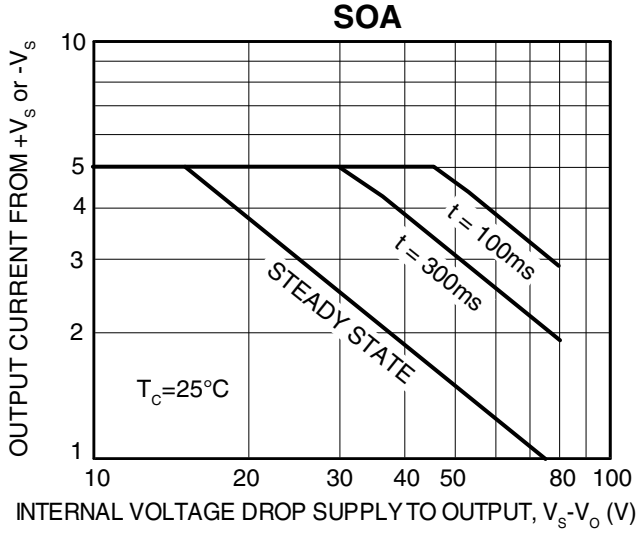
$$R_{CL} = \frac{.65V}{I_{CL} - .54A}$$

PHASE COMPENSATION

At low gain settings, an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered when determining gain settings. The capacitance values listed in the external connection diagram, along with good high frequency layout practice, will insure stability. Interpolate values for intermediate gain settings.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:



1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

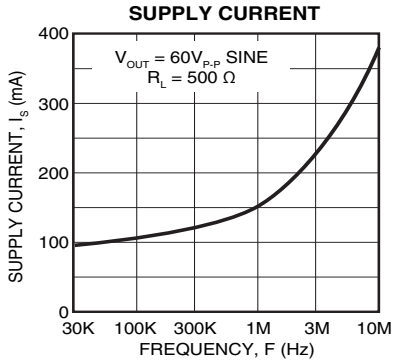
1. Capacitive and inductive loads up to the following maximums are safe:

±V_S	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1µF	11mH
30V	500µF	24mH
20V	2500µF	75mH
15V	∞	100mH

2. Safe short circuit combinations of voltage and current are limited to a power level of 100W.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SUPPLY CURRENT

The PA119 features a class A/B driver stage to charge and discharge gate capacitance of Q7 and Q19. As these currents approach 0.5A, the savings of quiescent current over that of a class A driver stage is considerable. However, supply current drawn by the PA119, even with no load, varies with slew rate of the output signal as shown below.



OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductances, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the steady state boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth, the PA119 is more likely to oscillate than lower bandwidth power operational amplifiers. To prevent oscillations a reasonable phrase margin must be maintained by:

1. Selection of the proper phase compensation capacitor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a larger capacitor at the expense of slew rate. Total physical length (pins of the PA119, capacitor leads plus printed circuit traces) should be limited to a maximum of 3.5 inches.
2. Keep the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or by bypassing the feedback resistor.
3. Connect the case to any AC ground potential.

CONTACTING CIRRUS LOGIC SUPPORT

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To find the one nearest to you, go to www.cirrus.com

Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- ♦ LOW COST
- ♦ WIDE BANDWIDTH - 1.1 Mhz
- ♦ HIGH OUTPUT CURRENT - 1.5A PER AMPLIFIER
- ♦ WIDE COMMON MODE RANGE Includes negative supply
- ♦ WIDE SUPPLY VOLTAGE RANGE Single supply: 5V to 40V Split supplies: ± 2.5V to ± 20V
- ♦ LOW QUIESCIENT CURRENT
- ♦ VERY LOW DISTORTION

APPLICATIONS

- ♦ HALF AND FULL BRIDGE MOTOR DRIVERS
- ♦ AUDIO POWER AMPLIFIER
  - Stereo - 11.3W RMS per amplifier
  - Bridge - 22.6W RMS per two amplifiers
  - Two Bridges - 45.2W RMS per package
- ♦ 3 PHASE MOTOR DRIVER
  - 3 Channels - 33.9W RMS per package
- ♦ IDEAL FOR SINGLE SUPPLY SYSTEMS
  - 5V - Peripherals
  - 12V - Automotive
  - 28V - Avionic
- ♦ PACKAGING OPTIONS
  - 20-Pin PSOP, JEDEC MO-166-AB (PA162DK)

DESCRIPTION

The amplifier design is a dual power op amp on a single monolithic die. The quad output PA162 combines two dual op amp die in a single PSOP package. This approach provides a cost-effective solution to applications where multiple amplifiers are required or a bridge configuration is needed. Four independent amplifiers coupled with low quiescent current and very low THD makes this an ideal low-distortion 4-channel audio amplifier for applications such as laptops and computer speakers.

The quad output PA162DK is available in a surface mount 20-pin PSOP, JEDEC MO-166-AB package. Built-in thermal shutdown allows the devices to self-protect against thermal overloads. Care must be exercised to observe the Safe Operating Area (SOA) curve and proper heatsinking will ensure maximum reliability.

The wide common mode input range includes the negative rail, facilitating single supply applications. This makes it possible to have a ground-based input driving a single supply amplifier with ground acting as the second or bottom supply of the amplifier.

E

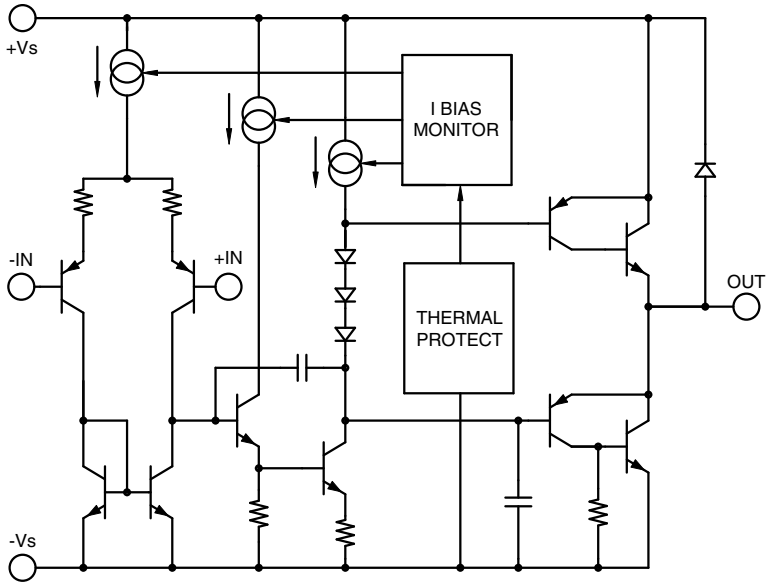


FIGURE 1. Equivalent schematic (one channel)

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, total		5	40	V
OUTPUT CURRENT		SOA		
POWER DISSIPATION, internal (1 amplifier)			15	W
POWER DISSIPATION, internal (2 amplifiers)[5]			24	W
POWER DISSIPATION, internal (3 amplifiers)[5]			36	W
POWER DISSIPATION, internal (4 amplifiers)[5]			45	W
INPUT VOLTAGE, differential		-Vs	+Vs	
INPUT VOLTAGE, common mode		+Vs	-Vs-.5V	
JUNCTION TEMPERATURE, max[2]			150	°C
TEMPERATURE, pin solder - 10 secs max.			220	°C
TEMP RANGE STORAGE		-55	150	°C
OPERATING TEMP RANGE, case[2]		-40	125	°C

SPECIFICATIONS (PER AMPLIFIER)

Parameter	Test Conditions[2,3]	Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			1	15	mV
OFFSET VOLTAGE, vs. temperature	Full temp range		20		µV/°C
BIAS CURRENT, initial			100	500	nA
COMMON MODE RANGE	Full temp range	-Vs		+Vs	V
COMMON MODE REJECTION, DC		60	90		dB
POWER SUPPLY REJECTION	Full temp range	60	90		dB
CHANNEL SEPARATION	I_{OUT} = 500mA, f = 1kHz	50	68		dB
INPUT NOISE VOLTAGE	R_S = 100Ω, f = 1 to 100kHz		22		nV/√Hz
GAIN					
OPEN LOOP GAIN	V_O = ±10V, R_L = 2.0KΩ	89	100		dB
GAIN BANDWIDTH PRODUCT	f = 100kHz, C_L = 100pF, R_L = 2.0KΩ		0.9	1.4	MHz
PHASE MARGIN	Full temp range		65		°C
POWER BANDWIDTH	V_O(P-P) = 28V		13.6		kHz
OUTPUT					
CURRENT, peak				1.5	A
CURRENT, continuous				1	A
SLEW RATE		1.0	1.4		V/µS
VOLTAGE SWING	Full temp range, I_O = 100mA	|Vs| -1.1	|Vs| -0.8		V
VOLTAGE SWING	Full temp range, I_O = 1A	|Vs| -1.8	|Vs| -1.4		V
HARMONIC DISTORTION	A_V = 1, R_L = 50Ω, V_O = .5VRMS, f = 1kHz		.02		%

Parameter	Test Conditions[2,3]	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE, Vss[4]		5	30	40	V
CURRENT, quiescent +Vs (A/B)			8	10	mA
CURRENT, quiescent +Vs (C/D)			8	10	mA
CURRENT, quiescent total			16	20	mA
THERMAL					
RESISTANCE, junction to case					
DC, 1 amplifier			7.16	7.87	°C/W
DC, 2 amplifiers[5]			4.69	5.16	°C/W
DC, 3 amplifiers[5]			3.08	3.39	°C/W
DC, 4 amplifiers[5]			2.51	2.77	°C/W
AC, 1 amplifier			5.37	5.90	°C/W
AC, 2 amplifiers[5]			3.52	3.87	°C/W
AC, 3 amplifiers[5]			2.31	2.54	°C/W
AC, 4 amplifiers[5]			1.89	2.07	°C/W
RESISTANCE, junction to air[7]			25		°C/W

NOTES:

1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Unless otherwise noted, the following conditions apply: $\pm V_S$ = ±15V, T_C =25°C.
4. $+V_S$ and $-V_S$ denote the positive and negative rail respectively. V_{SS} denotes total rail-to-rail supply.
5. Rating applies when power dissipation is equal in each of the amplifiers. Power and thermal ratings are based on two separate dual monolithic power op-amps on one integrated copper heatslug. Amplifiers A and B are combined on one monolithic die while amplifiers C and D are on the other.
6. If $-V_S$ is disconnected before $+V_S$, a diode between $-V_s$ and ground is recommended to avoid damage.
7. Rating applies when the heatslug of the DK package is soldered to a minimum of 1 square inch foil area of a printed circuit board.

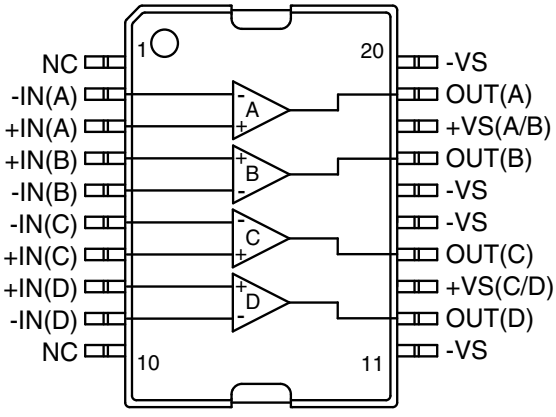
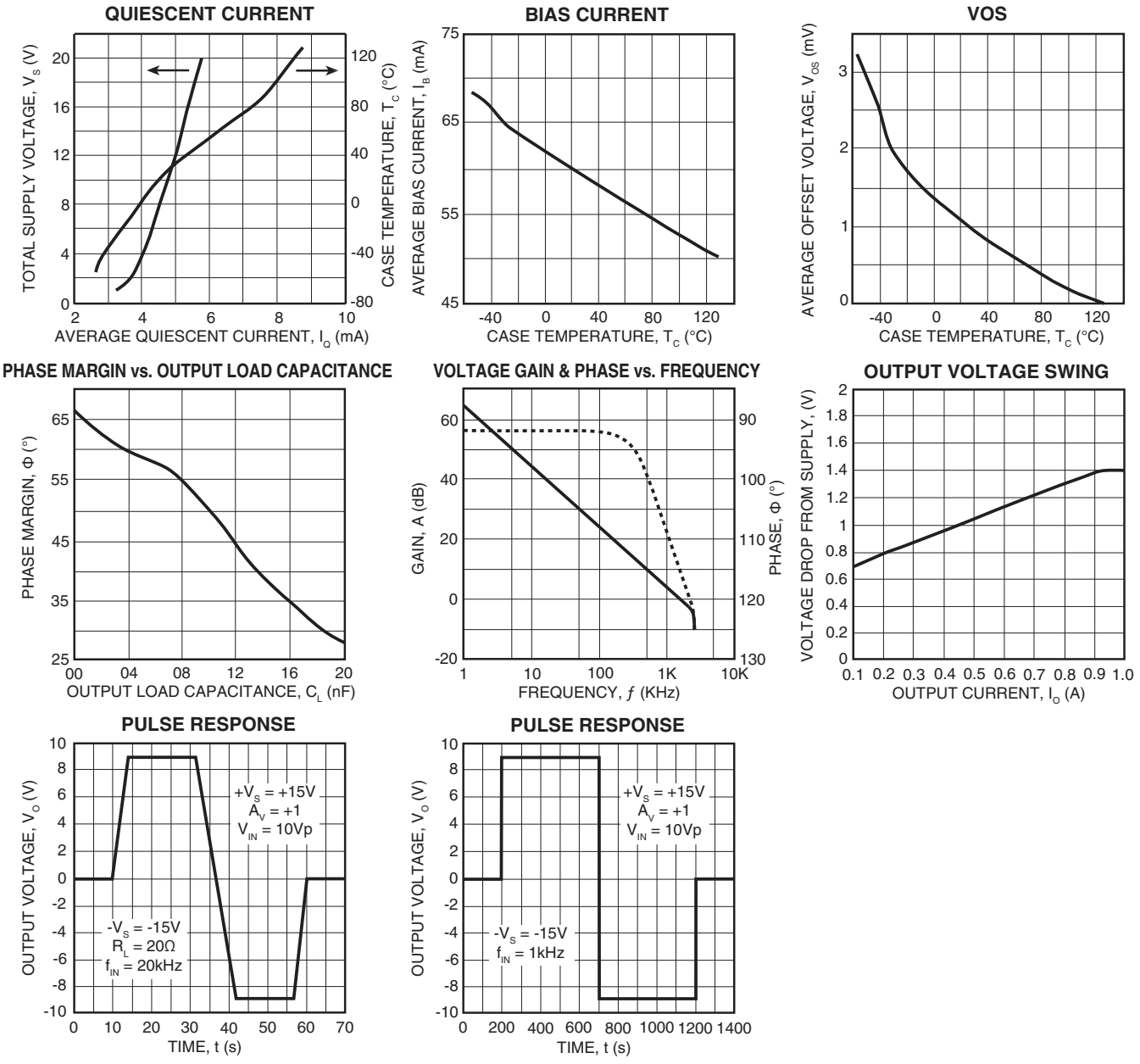


FIGURE 2. EXTERNAL CONNECTIONS.

20-pin PSOP
PACKAGE STYLE DK



TYPICAL APPLICATION

R1 and R2 set up Amplifier A as non-inverting. Amplifier B is set up as a unity gain inverter driven from the output of Amplifier A. Note that Amplifier B inverts the signals about the reference node, which is set at mid-supply by R5 and R6. When the command input is midrange, so is the output of Amplifier A. Since this is also equivalent to the reference node voltage, the output of Amplifier B is the same resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 3). Inputs less than 5V drive the motor in the opposite direction.

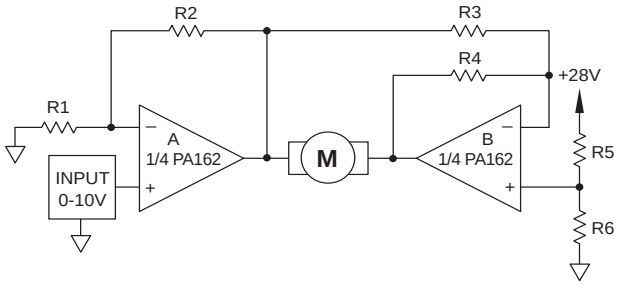


FIGURE 3. BI-DIRECTIONAL SPEED CONTROL FROM A SINGLE SUPPLY.

TYPICAL APPLICATION (CONT)

The amplifiers are especially well-suited for applications such as this. The extended common mode range allows command inputs as low as 0V. The output swing lets it drive within 2V of the supply at an output of 1A. This means that a command input that ranges from 0 to 10V will drive a 24V motor from full scale CCW to full scale CW at ±1A.

-Vs (pins 11, 15, 16 and 20) must be tied to the heatslug externally on the PCB. To ease metal routing on the PCB, run a direct trace from the -Vs pin to the center heat slug. The PA162 can be used in a three amplifier configuration for a three phase inverter or motor as shown in Figure 4.

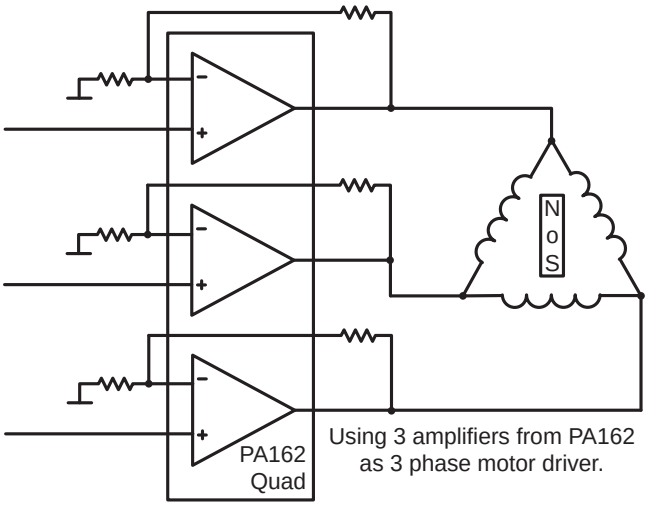


FIGURE 4. 3 Phase Inverter

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heatsinking, mounting, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, heatsink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions. For applications with load current exceeding 300mA, oscillation may appear. The oscillation may occur only with the output voltage swing at the negative or positive half cycle. Under most operating and load conditions acceptable stability can be achieved by providing a series RC snubber network connected from the output to ground (see Figure 5). The recommended component values of the of the network are, R_{SN} = 10Ω and C_{SN} = 0.01µF. Please refer to Application Note 1 for further details.

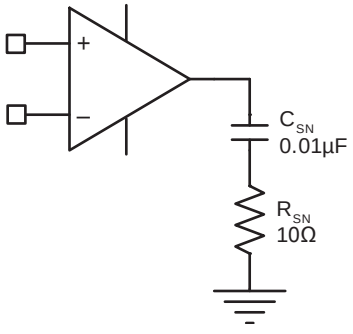
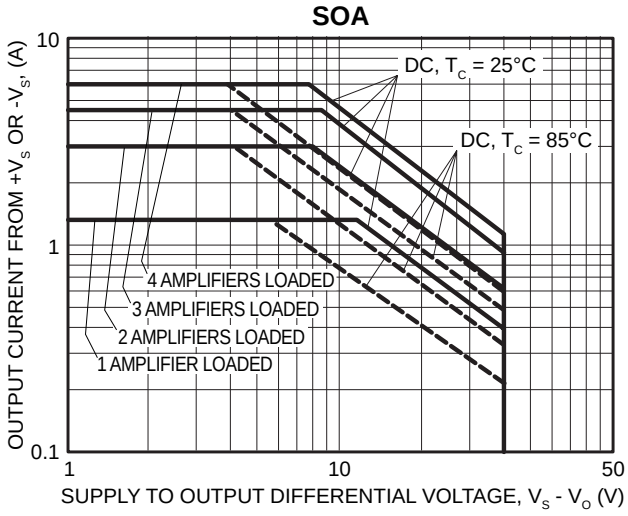


FIGURE 5. R-C Snubber

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.



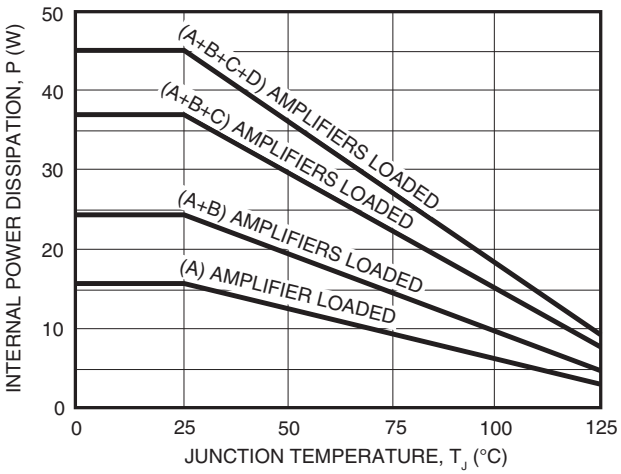
THERMAL CONSIDERATIONS

The PA162DK has a large exposed integrated copper heatslug to which the monolithic is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area of the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA162DK. Solder connection to an area of 1 to 2 square inches of foil is required for minimal power applications.

Where the PA162DK is used in higher power applications, it is necessary to use surface mount techniques of heatsinking. Surface mount techniques include the use of a surface mount fan in combination with a surface mount heatsink on the backside of the FR4/ PC board with through hole thermal vias. Other highly thermal conductive substrate board materials are available for maximum heat sinking.

The Power Derating graph assumes that the power dissipation is equal in each of the amplifiers. Power and thermal ratings are based on two separate dual monolithic power op amps on one integrated copper heat slug. Amps A and B are combined on one monolithic die while amps C and D are combined on the other. This multi chip configuration provides superior thermal performance by isolating each of the dual amplifiers. When loading either of the dual amplifiers it is possible to achieve better thermal performance by loading any combination of amplifiers (A or B) + (C or D).

POWER DERATING



MOUNTING PRECAUTIONS

1. Always use a heat sink. Even unloaded the PA162DK can dissipate up to .8 watts.
2. Avoid bending the leads. Such action can lead to internal damage.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

High Voltage Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- RoHS COMPLIANT
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT TYP.—2.2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK

APPLICATIONS

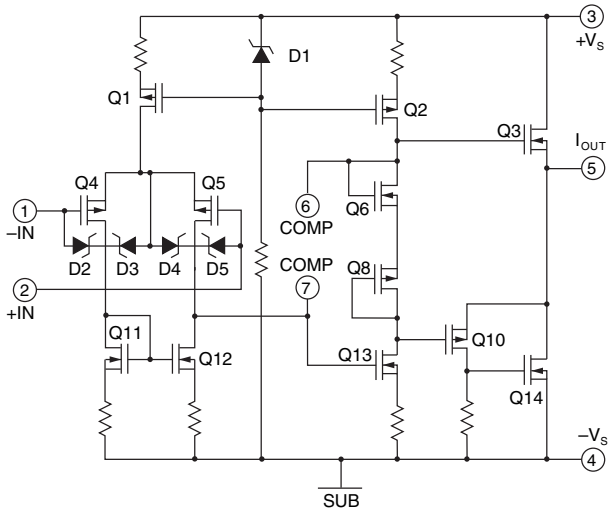
- TELEPHONE RING GENERATOR
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- PACKAGING OPTIONS
  7 TO-220 with staggered Lead Form (PA240CX)
  7 DDPAK Surface Mount Package (PA240CC)

DESCRIPTION

The PA240 is a high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA240 is packaged in two standard package designs. The surface mount version of the PA240, the PA240CC, is an industry standard non-hermetic plastic 7-pin DDPAK. The through hole version of the PA240, the PA240CX, is an industry standard non-hermetic plastic 7-pin TO-220 package. The PA240CX is a staggered lead formed option that offers industry standard 100 mil spacing. This allows for easier PC board layout. (Please refer to package drawings for outline dimensions.)

EQUIVALENT SCHEMATIC



DDPAK
PKG. STYLE CC

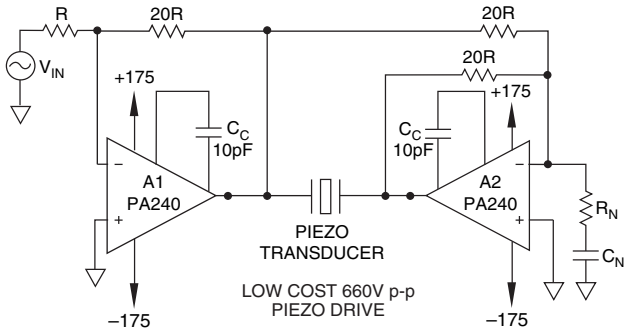
TO-220
STAGGERED LEADS
PKG. STYLE CX

High voltage considerations should be taken when designing board layouts for the PA240. The PA240 may require a derate in supply voltage depending on the spacing used for board layout. The 15-mil and 14-mil minimum spacing of the 7 TO-220 and 7 DDPAK respectively is adequate to standoff the 350V rating of the PA240. However, a supply voltage derate to 250V is required if the spacing of circuit board artwork is less than 11 mils. In cases where the PA240 is used to its maximum voltage rating, the PA240CX is recommended given that the staggered lead form allows for 100-mil standard spacing.

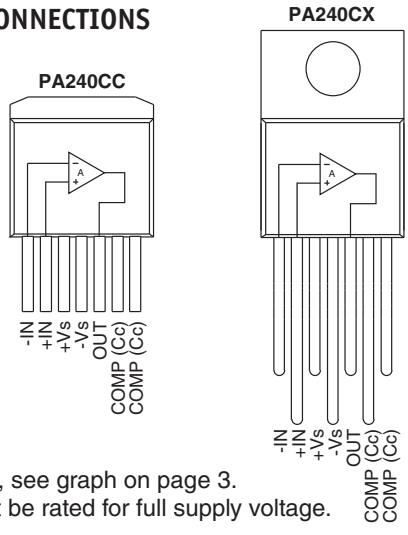
The metal tabs of both the PA240CC and PA240CX packages are directly tied to -Vs.

TYPICAL APPLICATION

Reference Application Notes 3, 20 and 25



EXTERNAL CONNECTIONS



For CC values, see graph on page 3.
Note: CC must be rated for full supply voltage.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak[3]	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	14W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

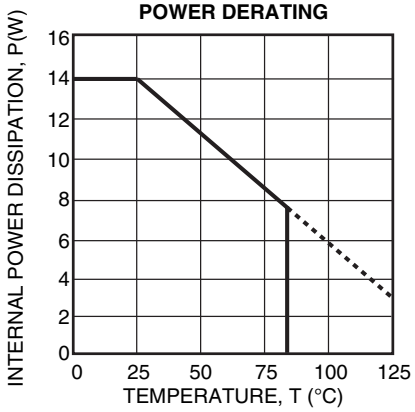
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA240 MIN	PA240 TYP	PA240 MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			25	40	mV
OFFSET VOLTAGE, vs. temperature[3]	25°C to 85°C		100	250	µV/°C
OFFSET VOLTAGE, vs. temperature[3]	-25°C to 25°C		270	500	µV/°C
OFFSET VOLTAGE, vs supply			3		µV/V
OFFSET VOLTAGE, vs time			70	130	µV/kh
BIAS CURRENT, initial			50	200	pA
BIAS CURRENT, vs supply			2		pA/V
OFFSET CURRENT, initial			50	200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			6		pF
COMMON MODE, voltage range		$+V_S$–14			V
COMMON MODE, voltage range		$-V_S$+12			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, R_S = 1K		50		µV RMS
NOISE, low frequency	1-10 Hz		125		µV p-p
GAIN					
OPEN LOOP at 15Hz	R_L = 5K	90	96		dB
BANDWIDTH, gain bandwidth product			3		MHz
POWER BANDWIDTH	280V p-p		30		kHz
OUTPUT					
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		V
CURRENT, peak[3]		120			mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	10V step, A_V = –10		2		µs
SLEW RATE	C_C = 3.3pF		30		V/µs
RESISTANCE[4], 1mA	R_{CL} = 0		150		Ω
RESISTANCE[4], 40 mA	R_{CL} = 0		5		Ω
POWER SUPPLY					
VOLTAGE		±50	±150	±175	V
CURRENT, quiescent			2.2	2.5	mA
THERMAL					
RESISTANCE, AC junction to case	F > 60Hz		5.9	6.85	°C/W
RESISTANCE, DC junction to case	F < 60Hz		7.7	8.9	°C/W
RESISTANCE, junction to air (CX)	Full temperature range		60		°C/W
RESISTANCE, junction to air (CC)[5]	Full temperature range		27		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	°C

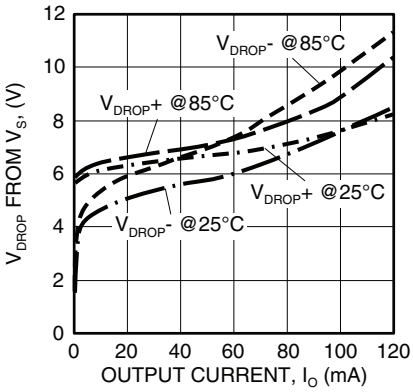
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Guaranteed but not tested.
4. Since the PA240 has no current limit, load impedance must be large enough to limit output current to 120mA.
5. Heat tab attached to 3/32" FR-4 board with 2oz. copper. Topside copper area (heat tab directly attached) = 1000 sq. mm, backside copper area = 2500 sq. mm, board area = 2500 sq. mm.

CAUTION The PA240 is constructed from MOSFET transistors. ESD handling procedures must be observed.

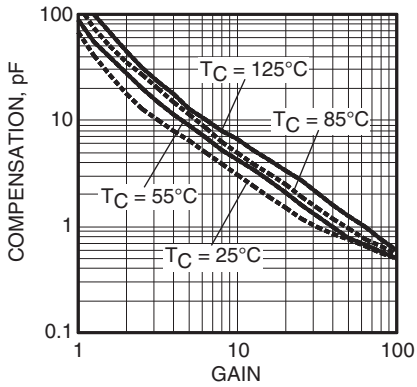
POWER DERATING



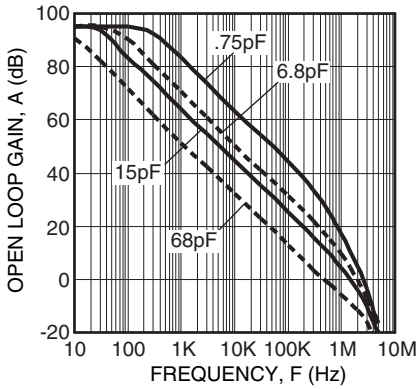
OUTPUT VOLTAGE SWING



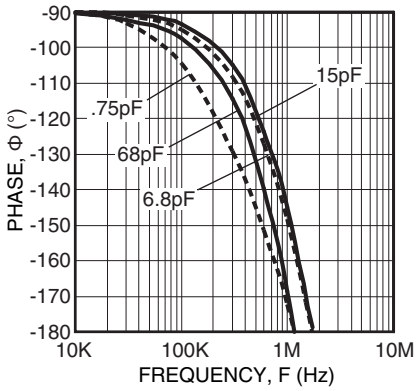
GAIN AND COMPENSATION



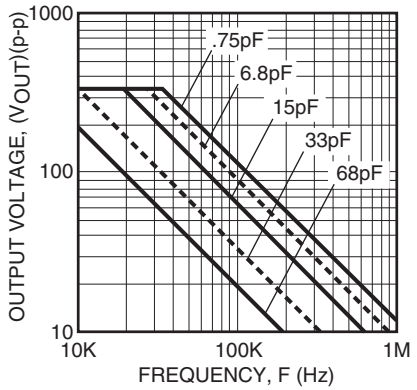
SMALL SIGNAL RESPONSE



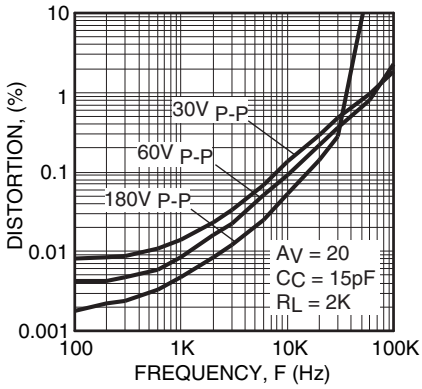
PHASE RESPONSE



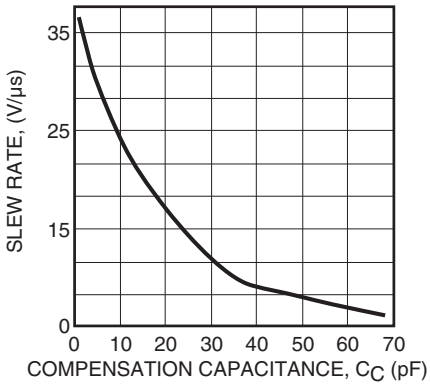
POWER RESPONSE



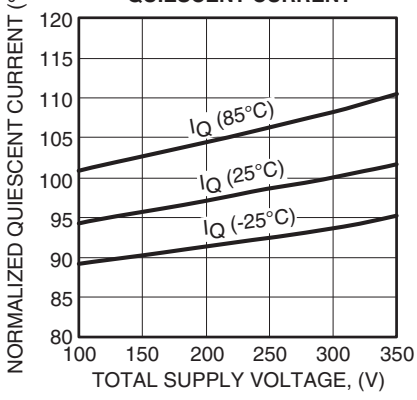
HARMONIC DISTORTION



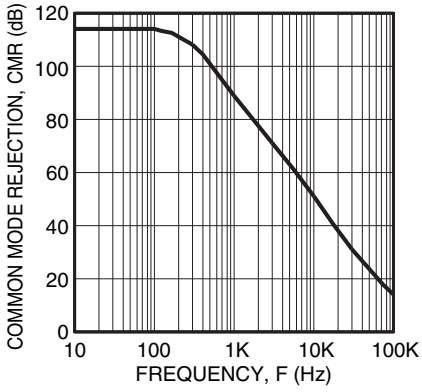
SLEW RATE



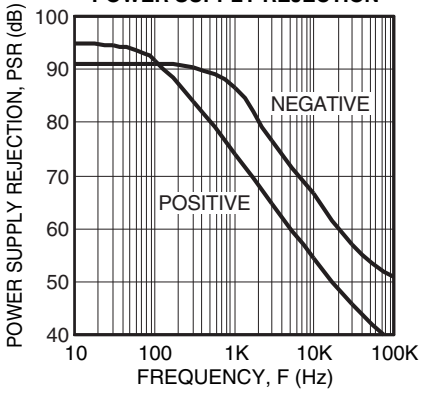
QUIESCENT CURRENT



COMMON MODE REJECTION



POWER SUPPLY REJECTION



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG.

OTHER STABILITY CONCERNS

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that while "gain" is the most commonly used term, β (the feedback factor) is really what counts when designing for stability.

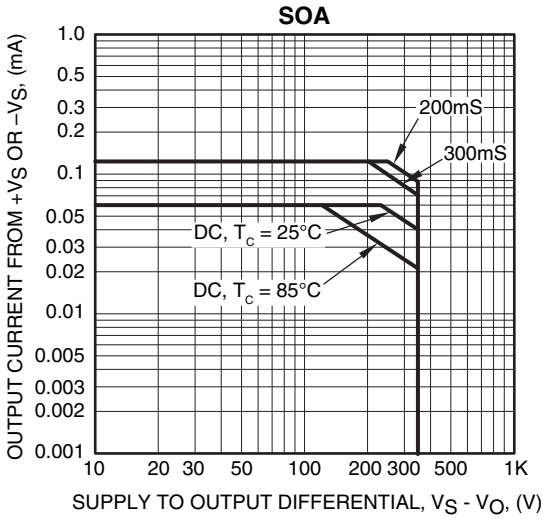
1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).
2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider Rin=4.7k, Rf=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47k rolls off the circuit at 103kHz, and at 2MHz has reduced gain from 11 to roughly 1.5 and the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input resistors) should be limited to 5k ohms or less. The amplifier input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or estimate the total sum point capacitance, multiply by Rin/Rf, and parallel Rf with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps β constant over a wide frequency range. Paragraph 6 of Application Note 19 details suitable stability tests for the finished circuit.

SAFE OPERATING AREA

The MOSFET output stage of the PA240 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metallization.
3. Temperature of the output MOSFETS.



These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

HEATSINKING

The PA240CC 7-pin DDPAK surface mountable package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The PA240CC requires surface mount techniques of heatsinking. A solder connection to a copper foil area as defined in Note 5 of Page 2 is recommended for circuit board layouts. This may be adequate heatsinking but the large number of variables suggests temperature measurements to be made on the top of the package. Do not allow the temperature to exceed 85°C.

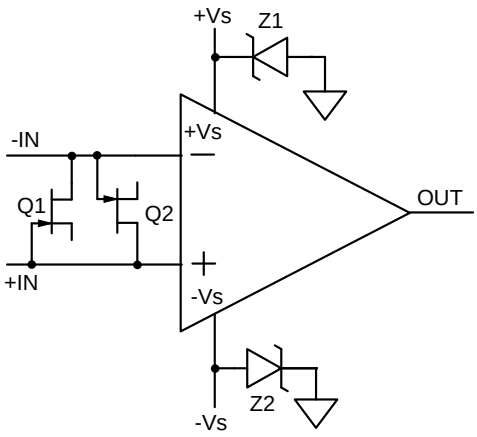


FIGURE 1

OVERVOLTAGE PROTECTION

Although the PA240 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

APPLICATION REFERENCES:

For additional technical information please refer to the following Application Notes:

AN01: General Operating Considerations
AN03: Bridge Circuit Drives
AN25: Driving Capacitive Loads
AN38: Loop Stability with Reactive Loads

E

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

High Voltage Power Operational Amplifier

FEATURES

- RoHS COMPLIANT
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT TYP.—2.2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120mA PEAK
- AVAILABLE IN DIE FORM—CPA241

APPLICATIONS

- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

8-PIN TO-3
PACKAGE STYLE CE

24-PIN PSOP
PACKAGE STYLE DF

10-PIN SIP
PACKAGE STYLE DW

DESCRIPTION

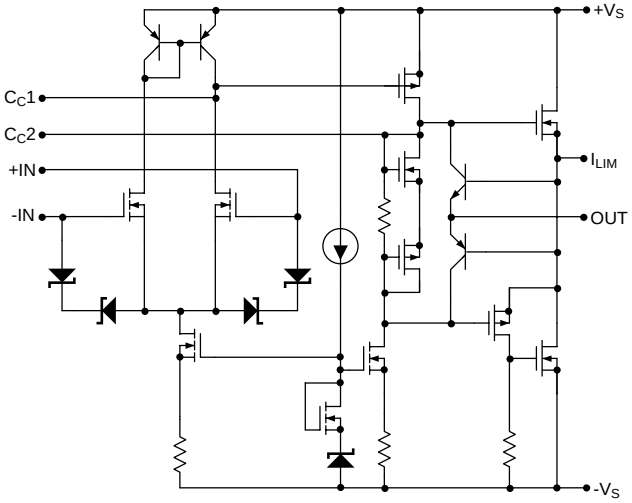
The PA241 is a high voltage monolithic MOSFET operational amplifier which achieves performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitation and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA241CE is packaged in a hermetically sealed 8-pin TO-3 package. The metal case of the PA241CE is isolated in excess of full supply voltage.

The PA241DF is packaged in a 24 pin PSOP (JEDEC MO-166) package. The metal heat slug of the PA241DF is isolated in excess of full supply voltage.

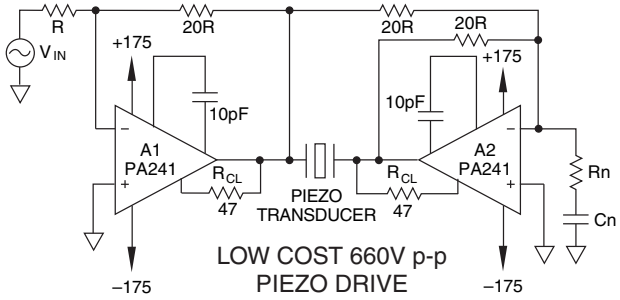
The PA241DW is packaged in Apex Precision Power's hermetic ceramic SIP package. The alumina ceramic isolates the die in excess of full supply voltage.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

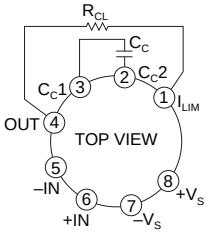
Ref: APPLICATION NOTE 20: "Bridge Mode Operation of Power Amplifiers"



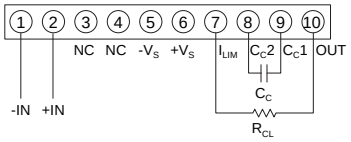
Two PA241 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

EXTERNAL CONNECTIONS

PA241CE

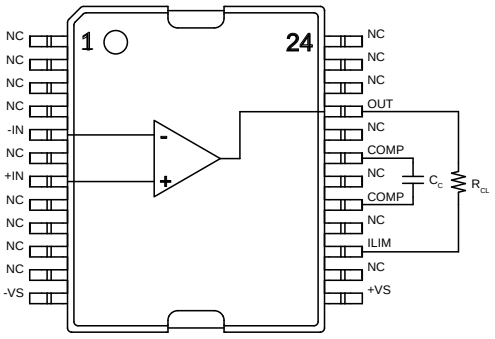


PA241DW



For CC values, see graph on page 4.
Note: CC must be rated for full supply voltage.

PA241DF



NOTE: PA241CE Recommended mounting torque is 4-7 in•lbs (.45 -.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

ABSOLUTE MAXIMUM RATINGS

	PA241CE PA241CEA	PA241DF PA241DFA
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V	350V
OUTPUT CURRENT, continuous within SOA	60 mA	60 mA
OUTPUT CURRENT, peak	120 mA	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W	12W
INPUT VOLTAGE, differential	±16 V	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C	220°C
TEMPERATURE, junction[2]	150°C	150°C
TEMPERATURE, storage	–65 to +150°C	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C	–40 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA241CE, PA241DF MIN	PA241CE, PA241DF TYP	PA241CE, PA241DF MAX	PA241CEA MIN	PA241CEA TYP	PA241CEA MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[3]	25° to 85°C		100	250		*	*	µV/°C
OFFSET VOLTAGE, vs. temperature[3]	-25° to 25°C		270	500		*	*	µV/°C
OFFSET VOLTAGE, vs supply			3			*		µV/V
OFFSET VOLTAGE, vs time			70	130		*	*	µV/kh
BIAS CURRENT, initial[6]			5/50	50/200		*	*	pA
BIAS CURRENT, vs supply			0.2/2			*		pA/V
OFFSET CURRENT, initial[6]			2.5/50	50/200		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		
INPUT CAPACITANCE			6			*		pF
COMMON MODE, voltage range		$+V_S$–14			*			V
COMMON MODE, voltage range		$-V_S$+12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, R_S = 1K		50			*		µV RMS
NOISE, low frequency	1-10 Hz		125			*		µV p-p
GAIN								
OPEN LOOP at 15Hz	R_L = 5K	90	96		*	*		dB
BANDWIDTH, gain bandwidth product			3			*		MHz
POWER BANDWIDTH	280V p-p		30			*		kHz
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		$\pm V_S$–10	$\pm V_S$–8.5		V
CURRENT, peak[4]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	10V step, A_V = –10		2			*		µs
SLEW RATE	C_C = 3.3pF		30			*		V/µs
RESISTANCE[5], 1mA	R_{CL} = 0		150			*		Ω
RESISTANCE[5], 40 mA	R_{CL} = 0		5			*		Ω
POWER SUPPLY								
VOLTAGE		±50	±150	±175	*	*	*	V
CURRENT, quiescent			2.2	2.5		*	2.3	mA
THERMAL								
PA241CE RESISTANCE, AC junction to case	F > 60Hz		5.4	6.5		*	*	°C/W
PA241DF RESISTANCE, AC junction to case	F > 60Hz		6	7		*	*	°C/W
PA241CE RESISTANCE, DC junction to case	F < 60Hz		9	10.4		*	*	°C/W
PA241DF RESISTANCE, DC junction to case	F < 60Hz		9	11		*	*	°C/W
PA241CE RESISTANCE, junction to air	Full temperature range		30			*		°C/W
PA241DF RESISTANCE, junction to air[7]	Full temperature range		25			*		°C/W
TEMPERATURE RANGE, case	Meets full range spec's	–25		+85	*		*	°C

NOTES: * "A" specification is the same as the non "A" specification.

1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Sample tested by wafer to 95%.
4. Guaranteed but not tested.
5. The selected value of R_{CL} must be added to the values given for total output resistance.
6. Specifications separated by / indicate values for the PA241CE and PA241DF respectively.
7. Rating applies with solder connection of heatslug to a minimum 1 square inch foil area of the printed circuit board.

CAUTION The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

ABSOLUTE MAXIMUM RATINGS

	PA241DW PA241DWA
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	9W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

SPECIFICATIONS

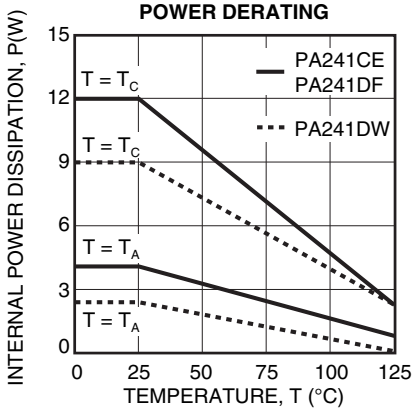
		PA241DW			PA241DWA			
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[3]	25° to 85°C		100	250		*	*	µV/°C
OFFSET VOLTAGE, vs. temperature[3]	-25° to 25°C		270	500		*	*	µV/°C
OFFSET VOLTAGE, vs supply			3			*		µV/V
OFFSET VOLTAGE, vs time			70	130		*		µV/kh
BIAS CURRENT, initial			100	2000		*	*	pA
BIAS CURRENT, vs supply			15	50		*	*	pA/V
OFFSET CURRENT, initial			100	400		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		
INPUT CAPACITANCE			6			*		pF
COMMON MODE, voltage range		$+V_S$–14			*			V
COMMON MODE, voltage range		$-V_S$+12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, R_S = 1K		50			*		µV RMS
NOISE, low frequency	1-10 Hz		125			*		µV p-p
GAIN								
OPEN LOOP at 15Hz	R_L = 5K	90	96		*	*		dB
BANDWIDTH, gain bandwidth product			3			*		MHz
POWER BANDWIDTH	280V p-p		30			*		kHz
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		$\pm V_S$–10	$\pm V_S$–8.5		V
CURRENT, peak[4]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	10V step, A_V = –10		2			*		µs
SLEW RATE	C_C = 3.3pF		30			*		V/µs
RESISTANCE[5], 1mA	R_{CL} = 0		150			*		Ω
RESISTANCE[5], 40 mA	R_{CL} = 0		5			*		Ω
POWER SUPPLY								
VOLTAGE		±50	±150	±175	*	*	*	V
CURRENT, quiescent			2.2	2.5		*	2.3	mA
THERMAL								
PA241DW RESISTANCE, AC junction to case	F > 60Hz		7	10		*	*	°C/W
PA241DW RESISTANCE, DC junction to case	F < 60Hz		12	14		*	*	°C/W
PA241DW RESISTANCE, junction to air	Full temperature range		55			*		°C/W
TEMPERATURE RANGE, case	Meets full range spec's	–25		+85	*		*	°C

NOTES: * "A" specification is the same as the non "A" specification.

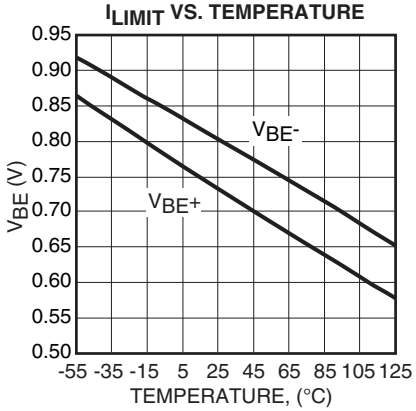
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Sample tested by wafer to 95%.
4. Guaranteed but not tested.
5. The selected value of R_{CL} must be added to the values given for total output resistance.

CAUTION The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

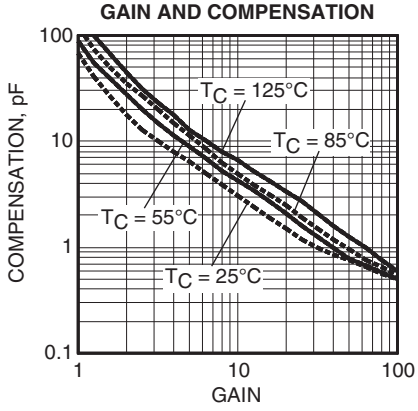
POWER DERATING



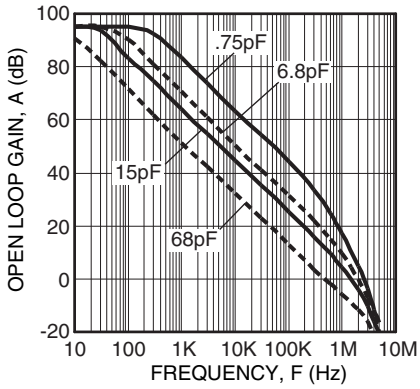
I_{LIMIT} VS. TEMPERATURE



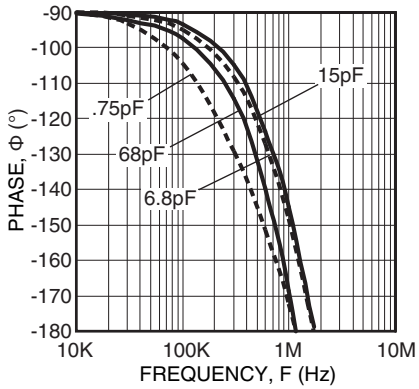
GAIN AND COMPENSATION



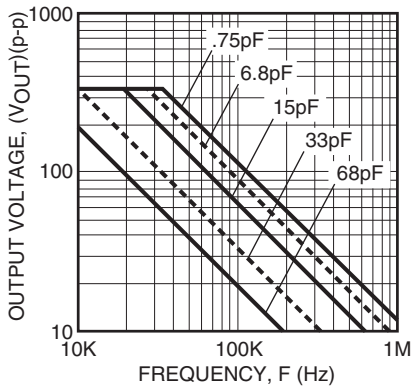
SMALL SIGNAL RESPONSE



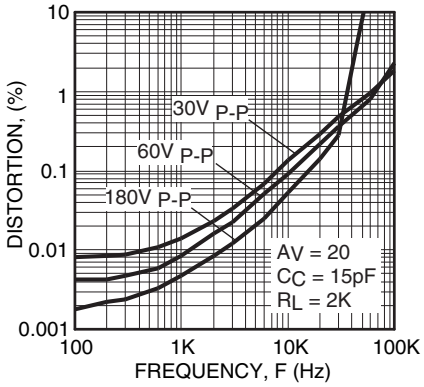
PHASE RESPONSE



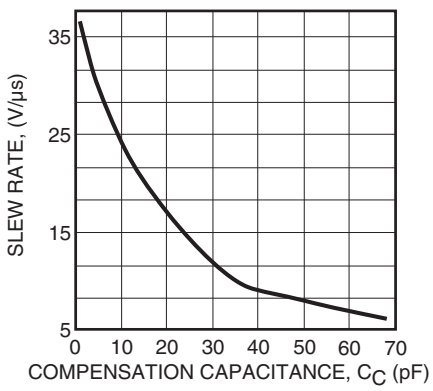
POWER RESPONSE



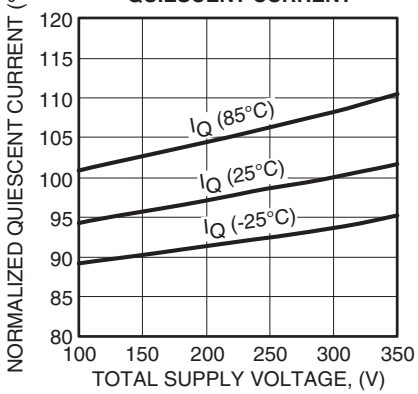
HARMONIC DISTORTION



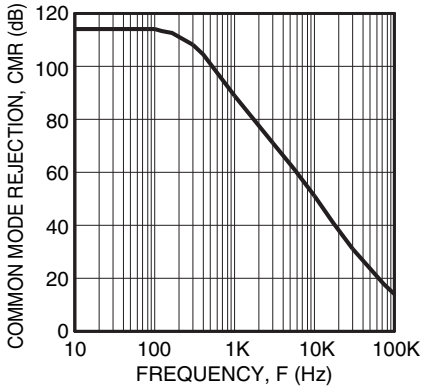
SLEW RATE



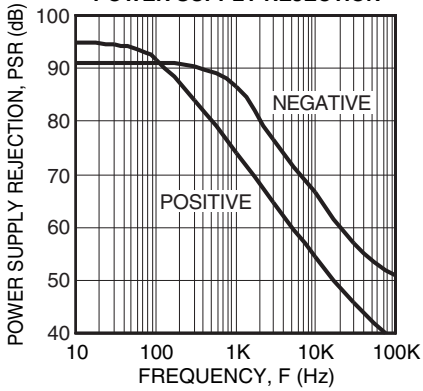
QUIESCENT CURRENT



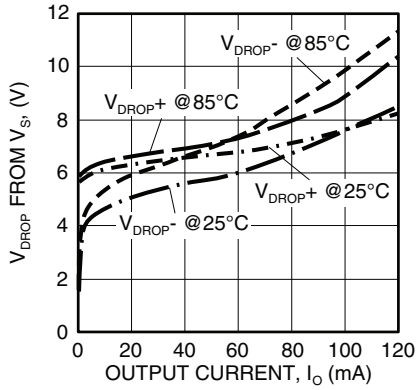
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG.

OTHER STABILITY CONCERNS

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that while "gain" is the most commonly used term, β (the feedback factor) is really what counts when designing for stability.

1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).
2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider Rin=4.7k, Rf=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47k rolls off the circuit at 103kHz, and at 2MHz has reduced gain from 11 to roughly 1.5 and the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input resistors) should be limited to 5k ohms or less. The amplifier input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or estimate the total sum point capacitance, multiply by Rin/Rf, and parallel Rf with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps β constant over a wide frequency range. Paragraph 6 of Application Note 19 details suitable stability tests for the finished circuit.

CURRENT LIMIT

For proper operation, the current limit resistor, Rcl, must be connected as shown in the external connection diagram. The minimum value is 3.9 ohms, however for optimum reliability, the resistor should be set as high as possible. The maximum practical value is 110 ohms. Current limit values can be predicted as follows:

$$Ilimit = \frac{Vbe}{Rcl}$$

Where Vbe is shown in the CURRENT LIMIT typical graph.

Note that +Vbe should be used to predict current through the +Vs pin, -Vbe for current through the -Vs pin, and that they vary with case temperature. Value of the current limit resistor at a case temperature of 25° can be estimated as follows:

$$Rcl = \frac{0.7}{Ilimit}$$

When the amplifier is current limiting, there may be spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, value of the current limit resistor, and the load. The oscillation will cease as the amplifier comes out of current limit.

SAFE OPERATING AREA

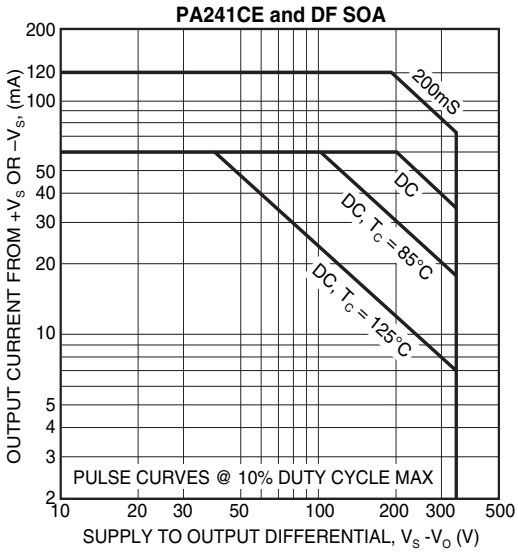
The MOSFET output stage of the PA241 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

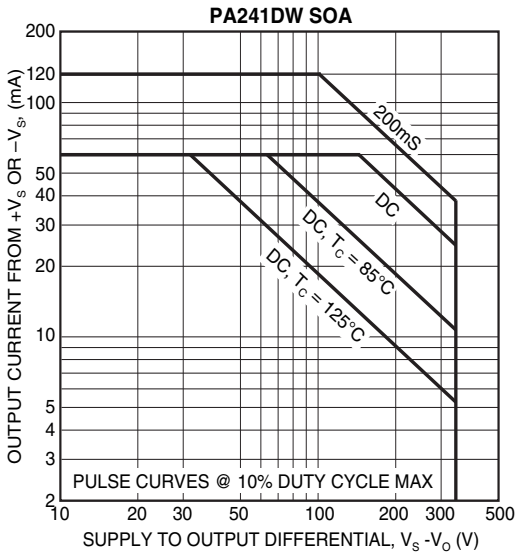
1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metalization.
3. Temperature of the output MOSFETS.

These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C and correspond to thermal resistances of 5.2°C/W for the PA241CE and DF and 10.4°C/W for the PA241DW respectively. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

HEATSINKING

The PA241DF package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area on the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA241DF. Solder connection to an area of 1 to 2 square inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.





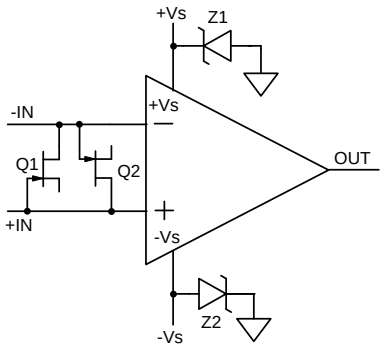


FIGURE 1

OVERVOLTAGE PROTECTION

Although the PA241 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

APPLICATION REFERENCES:

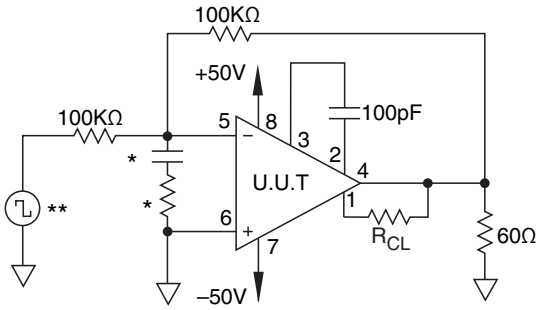
For additional technical information please refer to the following Application Notes:
AN1: General Operating Considerations
AN3: Bridge Circuit Drives
AN25: Driving Capacitive Loads
AN38: Loop Stability with Reactive Loads

Table 4 Group A Inspection

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		2.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		30	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	V_{IN} = 0, A_V = 100		30	mV
1	Input Offset Voltage	V_{OS}	25°C	±175V	V_{IN} = 0, A_V = 100		30	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$–I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–40°C	±150V	V_{IN} = 0, A_V = 100		2.5	mA
3	Input Offset Voltage	V_{OS}	–40°C	±150V	V_{IN} = 0, A_V = 100		60	mV
3	Input Offset Voltage	V_{OS}	–40°C	±50V	V_{IN} = 0, A_V = 100		60	mV
3	Input Bias Current, +IN	$+I_B$	–40°C	±150V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$–I_B$	–40°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–40°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		3	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		30	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	V_{IN} = 0, A_V = 100		30	mV
2	Input Offset Voltage	V_{OS}	125°C	±175V	V_{IN} = 0, A_V = 100		30	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		1	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±150V	V_{IN} = 0		1	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		1	nA
4	Output Voltage	V_O	25°C	±52V	R_L = 1K, I_O = 40mA	40		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	50	125	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF, C_C = 68pF		10	mVrms
4	Slew Rate	SR	25°C	±150V	R_L = 5K, C_C = 6.8pF	5		V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5K, F = 15Hz	90		dB
4	Common Mode Rejection	CMR	25°C	±102V	R_L = 5K, F = DC, V_{CM} = ±90V	84		dB
6	Output Voltage	V_O	–40°C	±52V	R_L = 1K, I_O = 40mA	40		V
6	Slew Rate	SR	–40°C	±150V	R_L = 5K, C_C = 6.8pF	5		V/µs
6	Open Loop Gain	A_{OL}	–40°C	±150V	R_L = 5K, F = 15Hz	90		dB
6	Common Mode Rejection	CMR	–40°C	±102V	R_L = 5K, F = DC, V_{CM} = ±90V	80		dB
5	Output Voltage	V_O	125°C	±50V	R_L = 1K, I_O = 30mA	30		V
5	Slew Rate	SR	125°C	±150V	R_L = 5K, C_C = 6.8pF	5		V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 15Hz	90		dB
5	Common Mode Rejection	CMR	125°C	±102V	R_L = 5K, F = DC, V_{CM} = ±90V	80		dB

The PA241M is available ONLY in the CE (8-pin TO-3) package style.

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Internal power dissipation of approximately 2.1W at case temperature = 125°C.

High Power Operational Amplifier

RoHS COMPLIANT

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous	60mA
INPUT VOLTAGE, differential	±16V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction	150°C

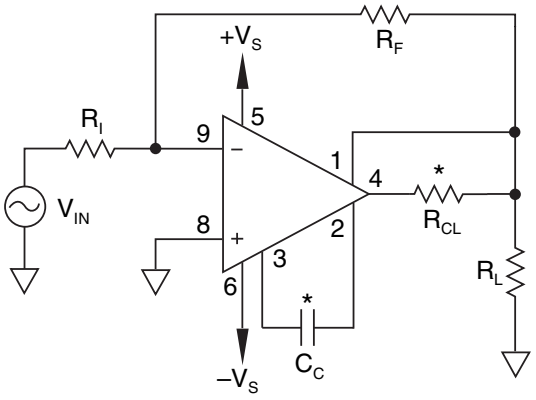
NOTE: Refer to parent product data sheet PA241 for typical AC electrical characteristics, precautions, applications and other test parameters.

DC WAFER PROBED SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE, initial	V_S = ±50V		15	40	mV
BIAS CURRENT, initial			56	200	pA
COMMON MODE REJECTION	V_{CM} = ±90 V DC	84	94		dB
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		V
SUPPLY CURRENT, quiescent	V_S = ±50 V	1.8	2.1	2.3	mA

NOTES: 1. Unless otherwise stated V_S = ±50 V, T_A = 25°C, DC input specification ± value given.
2. Sample tested by wafer to 95%.

TYPICAL EXTERNAL CONNECTIONS



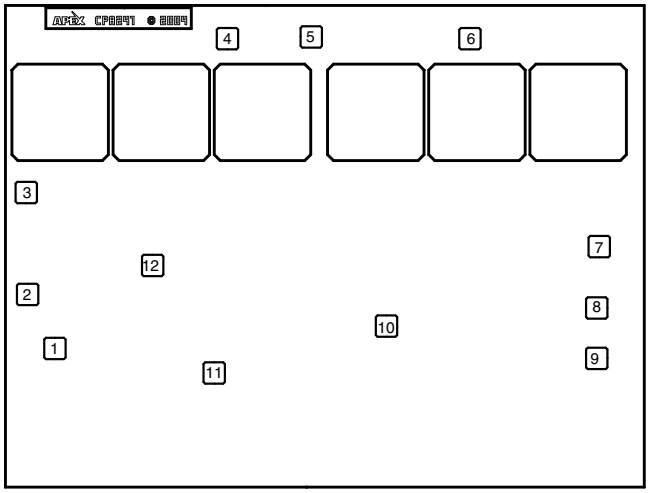
* Required component and value if given.
Optional balance components are recommended values.
C_C is NPO, rated for full supply voltage $-V_S$ to $+V_S$.

NOTE: Diagram for connection illustration only.
All op amp configurations are possible.

Pad	Function	Pad	Function
1	Output	5	+Vs
2	Compensation	6	-Vs
3	Compensation	8	+IN
4	Current Limit	9	-IN

CAUTION The CPA241 is a MOSFET amplifier. ESD handling procedures must be observed

DIE LAYOUT



Dimension: 154.5 x 117.5 ± 2.5 Mils.
Thickness: 15 Mil (380µ).
Backside Metal: None, Silicon.
Bond pad: 5 Mil sq (127µ) Al.
Make no connection to bond pads not listed by function.

Note: The backside of the CPA241 die is isolated up to 500V. The top side walls of the CPA241 die are isolated up to 300V.

Ordering Information:
Order #: CPA241DI80:
Die are only available in waffle packages with a total of 80 die per package.

PA243

High Voltage Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- RoHS COMPLIANT
- SURFACE MOUNT PACKAGE
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT TYP.—2.2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK

APPLICATIONS

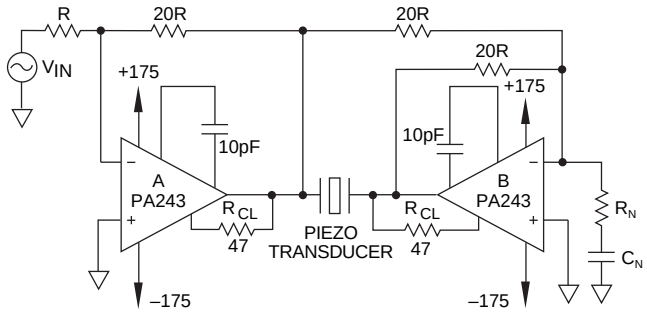
- TELEPHONE RING GENERATOR
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING

DESCRIPTION

The PA243 is a dual high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. This approach provides a cost-effective solution to applications where multiple amplifiers are required. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no secondary breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

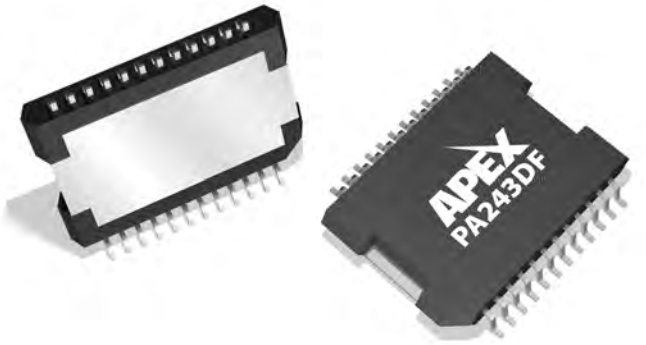
The PA243DF is packaged in a 24 pin PSOP (JEDEC MO-166) package. The heatslug of the PA243DF package is isolated in excess of full supply voltage.

TYPICAL APPLICATION



LOW COST 660V $_{P-P}$ PIEZO DRIVE

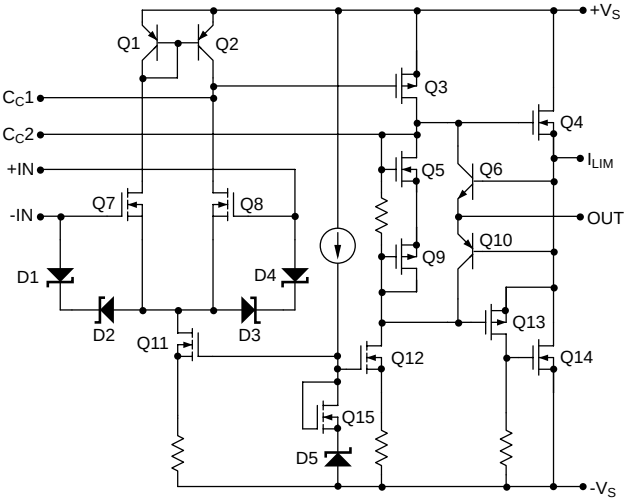
A single PA243 amplifier operates as a bridge driver for a piezo transducer providing a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths. See application note 20 for more details.



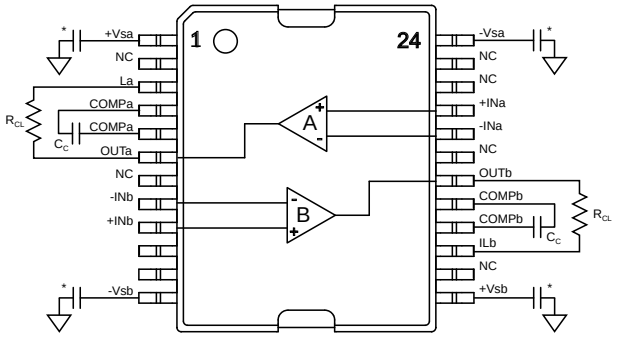
24-PIN PSOP

PACKAGE STYLE DF

EQUIVALENT SCHEMATIC (ONE OF TWO CHANNELS)



EXTERNAL CONNECTIONS



For C_C values, see graph on page 3.
Note: C_C must be rated for full supply voltage.
* Supply bypassing required. See general Operating Considerations.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

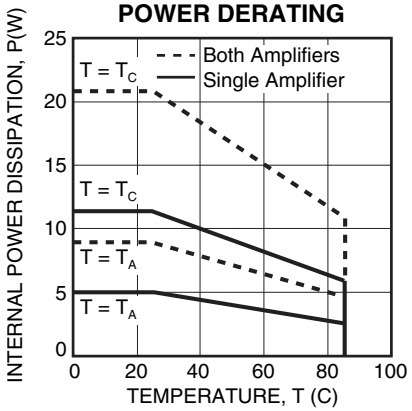
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			25	40	mV
OFFSET VOLTAGE, vs. temperature[3]	25°C to 85°C		100	250	µV/°C
OFFSET VOLTAGE, vs. temperature[3]	-25°C to25°C		270	500	µV/°C
OFFSET VOLTAGE, vs supply			3		µV/V
OFFSET VOLTAGE, vs time			70	130	µV/kh
BIAS CURRENT, initial			50	200	pA
BIAS CURRENT, vs supply			2		pA/V
OFFSET CURRENT, initial			50	200	pA
INPUT IMPEDANCE, DC			10^{11}		
INPUT CAPACITANCE			6		pF
COMMON MODE, voltage range		$+V_S$–14			V
COMMON MODE, voltage range		$-V_S$+12			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, R_S = 1K		50		µV RMS
NOISE, low frequency	1-10 Hz		125		µV p-p
GAIN					
OPEN LOOP at 15Hz	R_L = 5K	90	96		dB
BANDWIDTH, gain bandwidth product			3		MHz
POWER BANDWIDTH	280V p-p		30		kHz
OUTPUT					
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		V
CURRENT, peak[3]		120			mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	10V step, A_V = –10		2		µs
SLEW RATE	C_C = 3.3pF		30		V/µs
RESISTANCE[4], 1mA	R_{CL} = 0		150		Ω
RESISTANCE[4], 40 mA	R_{CL} = 0		5		Ω
POWER SUPPLY					
VOLTAGE		±50	±150	±175	V
CURRENT, quiescent			2.2	2.5	mA
THERMAL					
RESISTANCE, junction to case					
AC, single amplifier	F > 60Hz		6	7	°C/W
DC, single amplifier	F < 60Hz		9	11	°C/W
AC, both amplifiers[5]			3.3	4.0	°C/W
DC, both amplifiers[5]			5.0	6.0	°C/W
RESISTANCE, junction to air[6]	Full temperature range		25		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

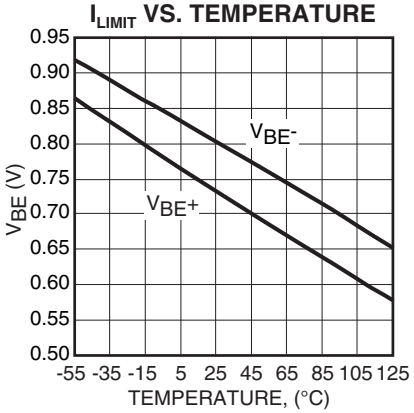
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Guaranteed but not tested.
4. The selected value of R_{CL} must be added to the values given for total output resistance.
5. Rating applies when power dissipation is equal in the two amplifiers.
6. Rating applies with solder connection of heatslug to a minimum 1in² foil area of the printed circuit board.

CAUTION The PA243 is constructed from MOSFET transistors. ESD handling procedures must be observed.

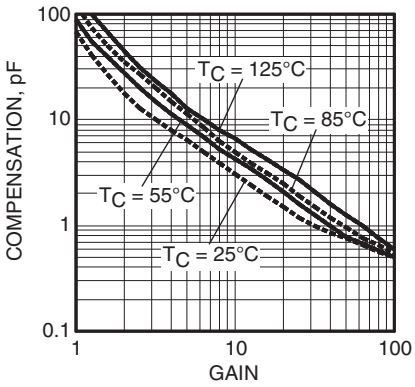
POWER DERATING



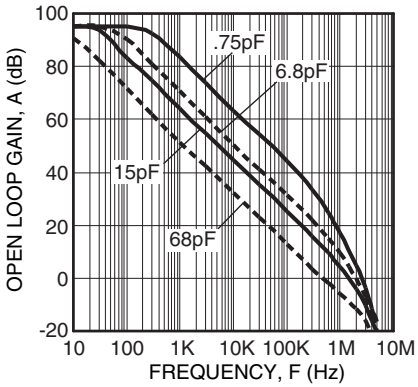
I_{LIMIT} VS. TEMPERATURE



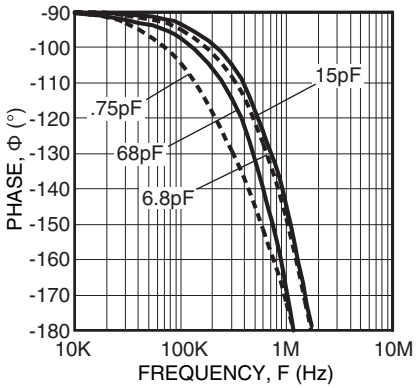
GAIN AND COMPENSATION



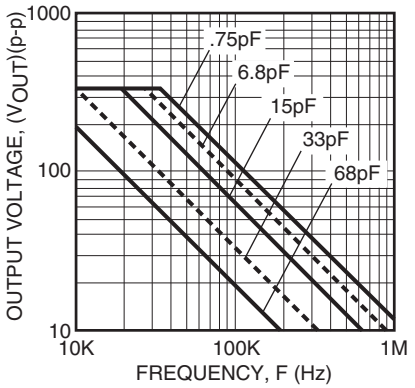
SMALL SIGNAL RESPONSE



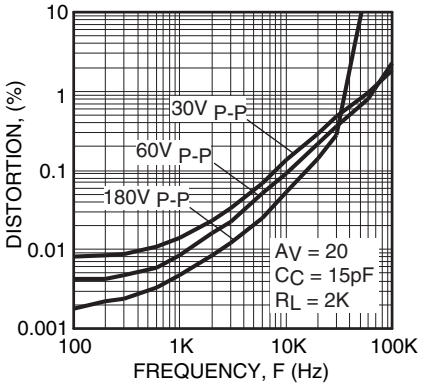
PHASE RESPONSE



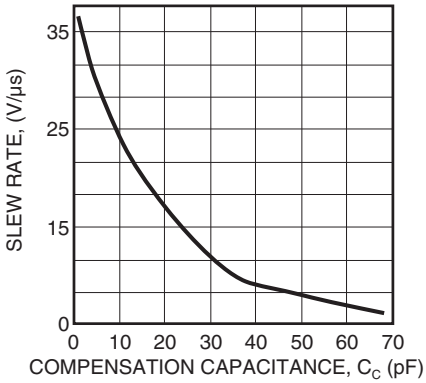
POWER RESPONSE



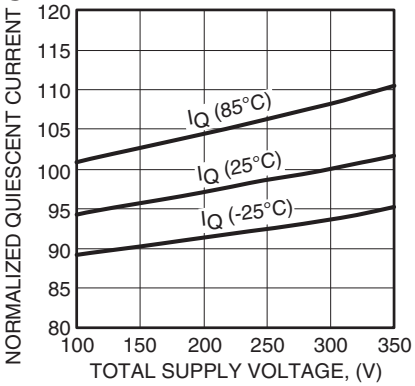
HARMONIC DISTORTION



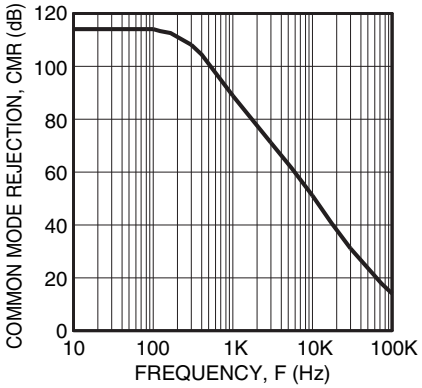
SLEW RATE



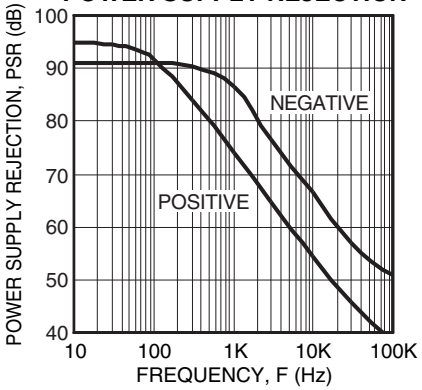
QUIESCENT CURRENT



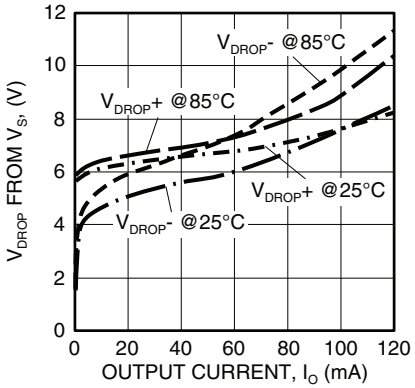
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG.

OTHER STABILITY CONCERNS

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that while "gain" is the most commonly used term, β (the feedback factor) is really what counts when designing for stability.

1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).
2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider Rin=4.7k, Rf=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47k rolls off the circuit at 103kHz, and at 2MHz has reduced gain from 11 to roughly 1.5 and the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input resistors) should be limited to 5k ohms or less. The amplifier input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or estimate the total sum point capacitance, multiply by Rin/Rf, and parallel Rf with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps β constant over a wide frequency range. Paragraph 6 of Application Note 19 details suitable stability tests for the finished circuit.

CURRENT LIMIT

For proper operation, the current limit resistor, Rcl, must be connected as shown in the external connection diagram. The minimum value is 3.9 ohms, however for optimum reliability, the resistor should be set as high as possible. The maximum practical value is 110 ohms. Current limit values can be predicted as follows:

$$Ilimit = \frac{Vbe}{Rcl}$$

Where Vbe is shown in the CURRENT LIMIT typical graph.

Note that +Vbe should be used to predict current through the +Vs pin, -Vbe for current through the -Vs pin, and that they vary with case temperature. Value of the current limit resistor at a case temperature of 25° can be estimated as follows:

$$Rcl = \frac{0.7}{Ilimit}$$

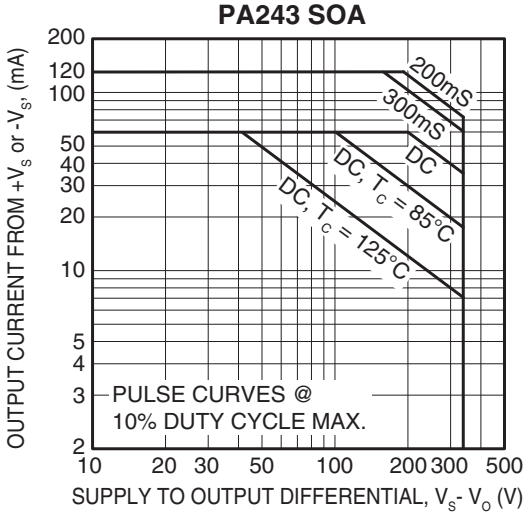
When the amplifier is current limiting, there may be spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, value of the current limit resistor, and the load. The oscillation will cease as the amplifier comes out of current limit.

SAFE OPERATING AREA

The MOSFET output stage of the PA243 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metalization.
3. Temperature of the output MOSFETS.

PA243 SOA

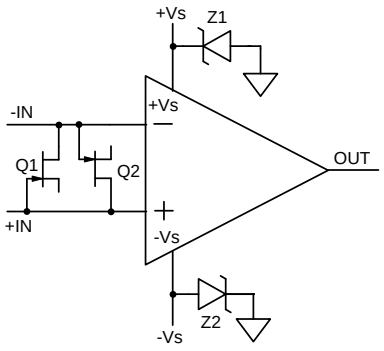


These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C and correspond to thermal resistances of 5.2°C/W for the PA243DF. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

HEATSINKING

The PA243DF package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area on the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA243DF. Solder connection to an area of 1 to 2 square inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.

FIGURE 1



OVERVOLTAGE PROTECTION

Although the PA241 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

APPLICATION REFERENCES:

For additional technical information please refer to the following Application Notes:

AN1: General Operating Considerations
AN3: Bridge Circuit Drives
AN25: Driving Capacitive Loads
AN38: Loop Stability with Reactive Loads

Power Booster Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±30V to ±100V
- HIGH OUTPUT CURRENT — Up to 2A Continuous
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW RATE — 50V/µs Minimum
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 160 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 180V p-p

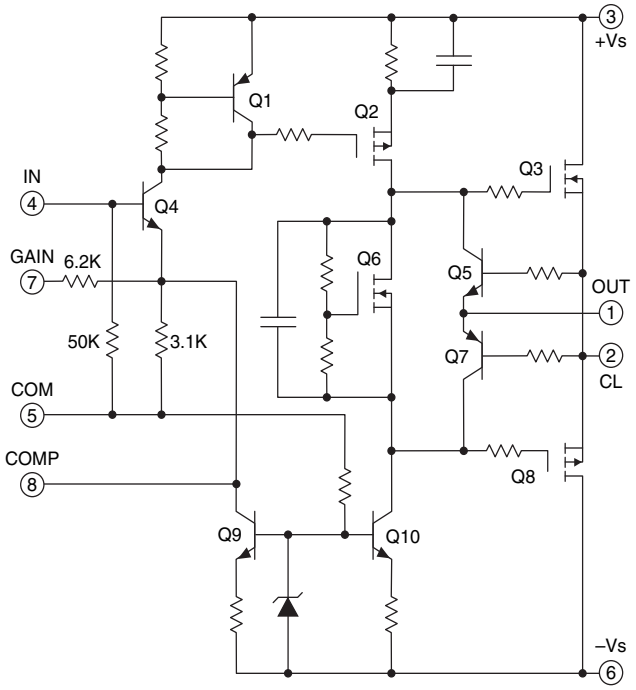
DESCRIPTION

The PB50 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB50 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Junction Transistors. Internal feedback and gainset resistors are provided for a pin-strappable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

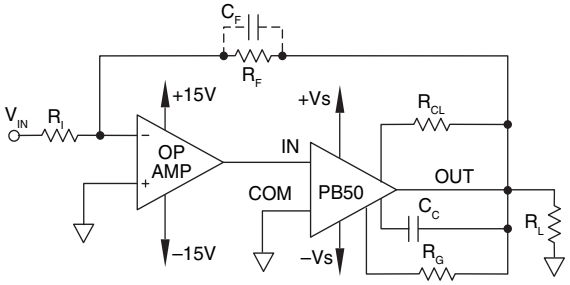
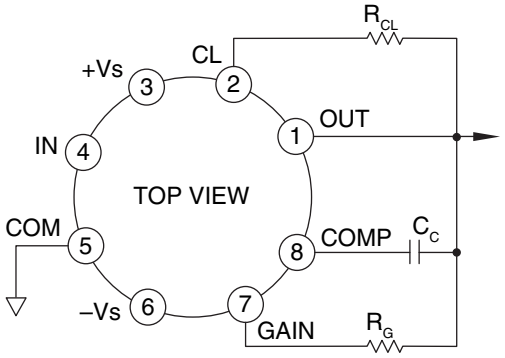


Figure 1. Inverting composite amplifier.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
OUTPUT CURRENT, within SOA	2A
POWER DISSIPATION, internal at T_C = 25°C[1]	35W
INPUT VOLTAGE, referred to common	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

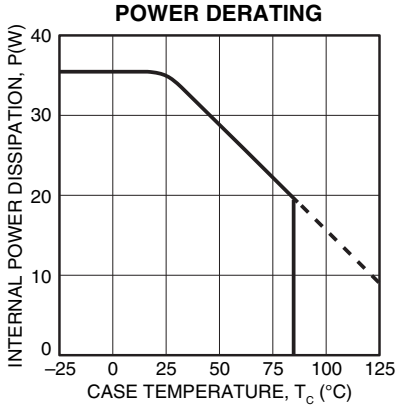
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			±.75	±1.75	V
OFFSET VOLTAGE, vs. temperature	Full temperature range		–4.5	–7	mV/°C
INPUT IMPEDANCE, DC		25	50		kΩ
INPUT CAPACITANCE			3		pF
CLOSED LOOP GAIN RANGE		3	10	25	V/V
GAIN ACCURACY, internal Rg, Rf	A_V = 3		±10	±15	%
GAIN ACCURACY, external Rf	A_V = 10		±15	±25	%
PHASE SHIFT	F = 10kHz, AV_{CL} = 10, C_C = 22pF		10		°
	F = 200kHz, AV_{CL} = 10, C_C = 22pF		60		°
OUTPUT					
VOLTAGE SWING	Io = 2A	V_S–11	V_S –9		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		V
CURRENT, continuous		2			A
SLEW RATE	Full temperature range	50	100		V/µs
CAPACITIVE LOAD	Full temperature range		2200		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2		µs
POWER BANDWIDTH	V_C = 100Vpp	160	320		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 25, Vcc = ±100		100		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 3, Vcc = ±30		1		MHz
POWER SUPPLY					
VOLTAGE, $\pm V_S$[3]	Full temperature range	±30[5]	±60	±100	V
CURRENT, quiescent	V_S = ±30		9	12	mA
	V_S = ±60		12	18	mA
	V_S = ±100		17	25	mA
THERMAL					
RESISTANCE, AC junction to case[4]	Full temp. range, F > 60Hz		1.8	2.0	°C/W
RESISTANCE, DC junction to case	Full temp. range, F < 60Hz		3.2	3.5	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	°C

NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. $+V_S$ must be at least 15V above COM, $-V_S$ must be at least 30V below COM.

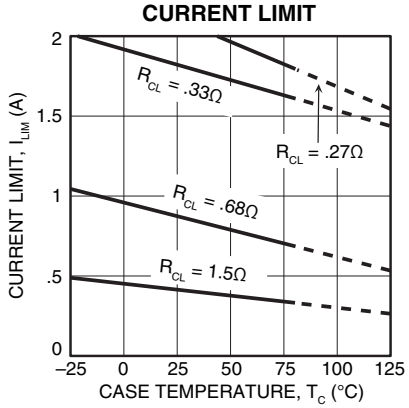
CAUTION The PB50 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

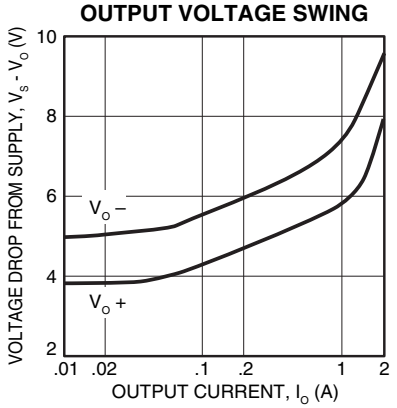
POWER DERATING



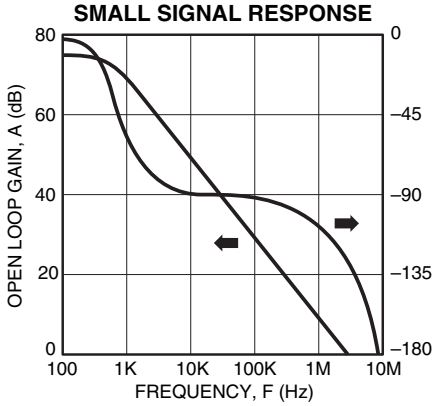
CURRENT LIMIT



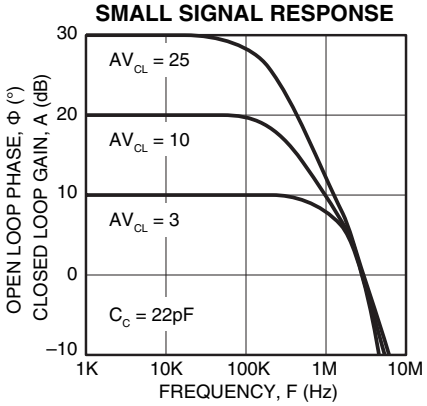
OUTPUT VOLTAGE SWING



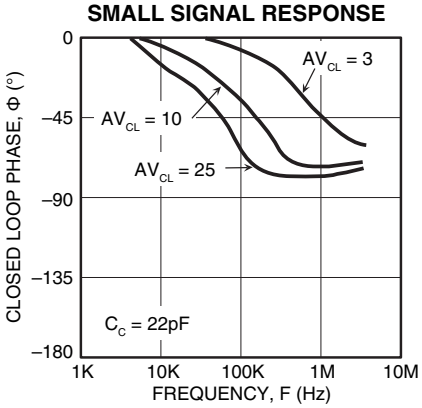
SMALL SIGNAL RESPONSE



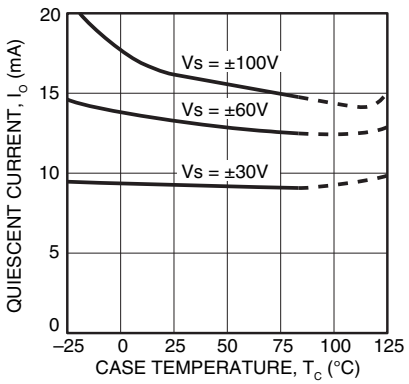
SMALL SIGNAL RESPONSE



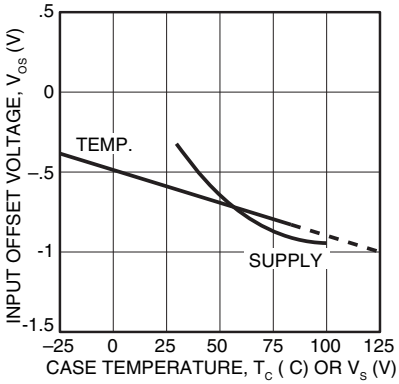
SMALL SIGNAL RESPONSE



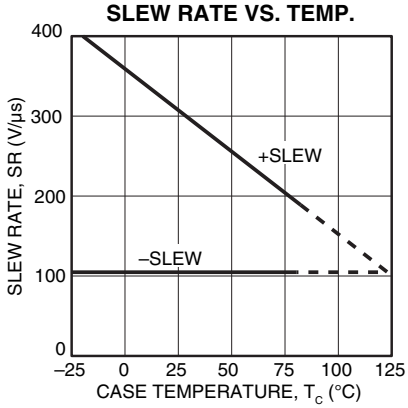
QUIESCENT CURRENT



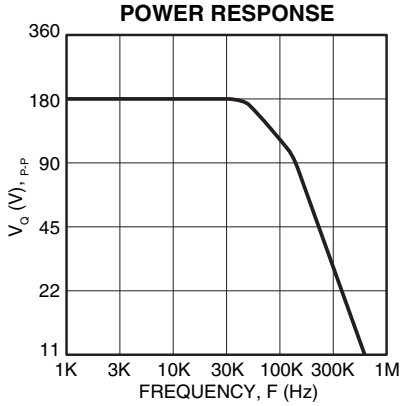
INPUT OFFSET VOLTAGE



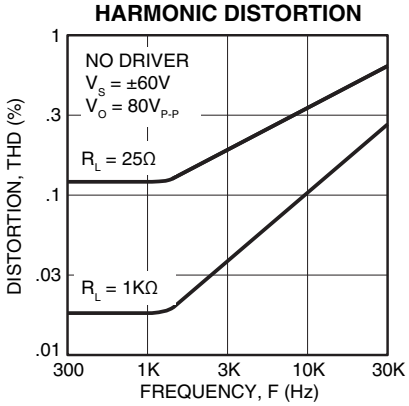
SLEW RATE VS. TEMP.



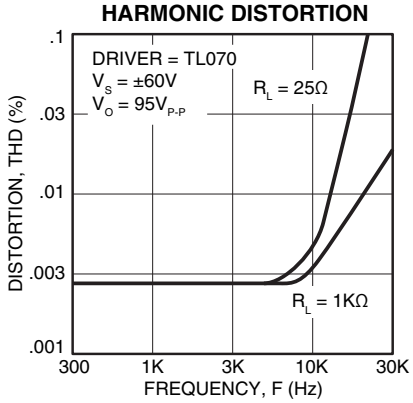
POWER RESPONSE



HARMONIC DISTORTION



HARMONIC DISTORTION



GENERAL

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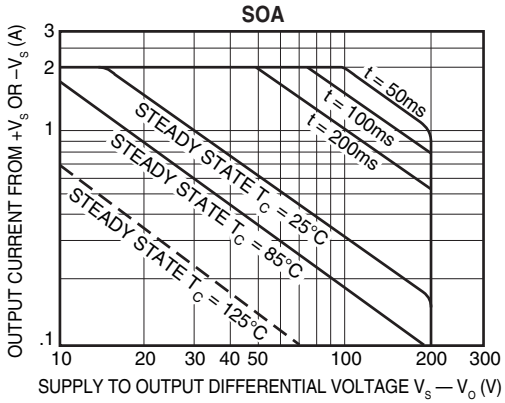
CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.27Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.



SAFE OPERATING AREA (SOA)

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av-1) \bullet 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.1K) + 1 = 3

Av (composite) = 60K/2K = - 30

Av (driver) = - 30/3 = -10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

Table 1:
Typical values for case where op amp effective gain = 1.

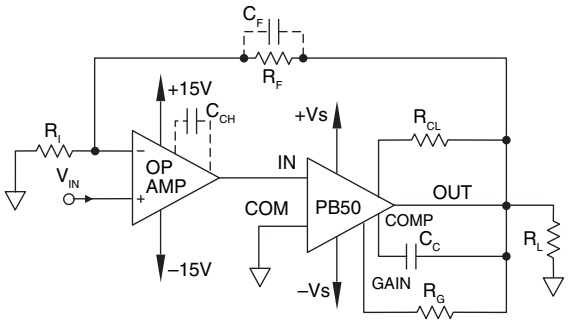


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

PB51 • PB51A

Power Booster Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT —
  1.5A Continuous (PB51), 2.0A Continuous (PB51A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Minimum (PB51)
  75V/µs Minimum (PB51A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical
- EVALUATION KIT — EK29

12-PIN SIP
PACKAGE STYLE DP

Formed leads available. See package styles ED & EE

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 280V P-P

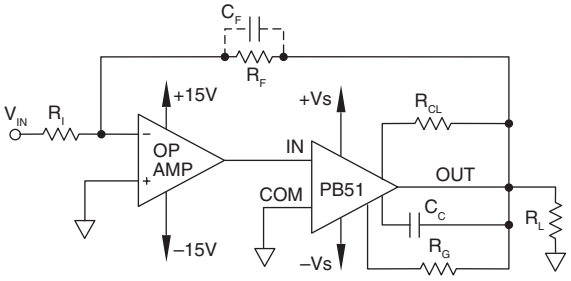
DESCRIPTION

The PB51 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB51 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

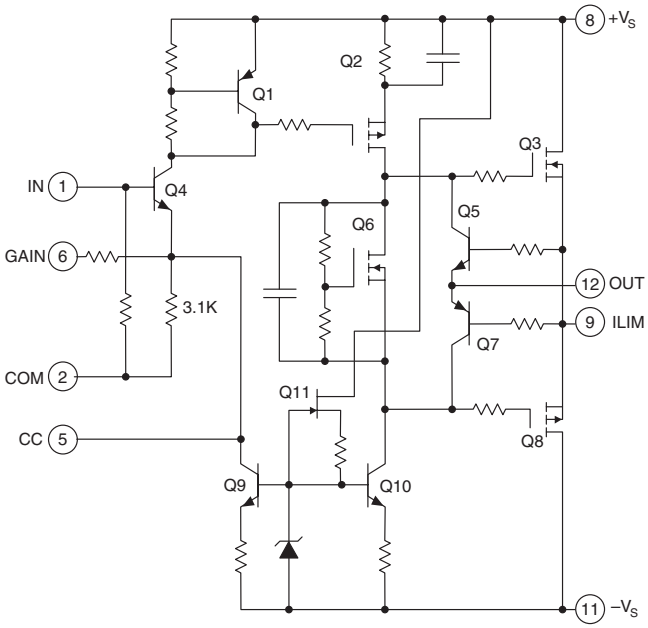
The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12-pin Power SIP package is electrically isolated.

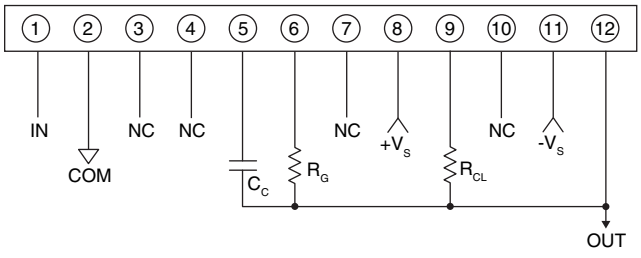
TYPICAL APPLICATION



EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at T_C = 25°C[1]	83W
INPUT VOLTAGE, referred to COM	±15V
TEMPERATURE, pin solder—10s max.	260°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–40 to +85°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

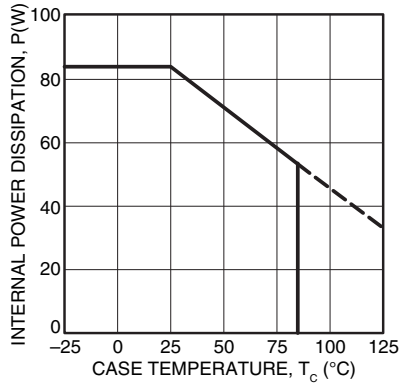
PARAMETER	TEST CONDITIONS[2]	PB51 MIN	PB51 TYP	PB51 MAX	PB51A MIN	PB51A TYP	PB51A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		k
INPUT CAPACITANCE			3			*		pF
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	AV = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	AV = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AVC_L = 10, CC = 22pF		10			*		°
	f = 200kHz, AVC_L = 10, CC = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	VS–11	VS–8		VS–15	VS–11		V
VOLTAGE SWING	Io = 1A	VS–10	VS–7		*	*		V
VOLTAGE SWING	Io = .1A	VS–8	VS–5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	RL = 100, 2V step		2			*		µs
POWER BANDWIDTH	VC = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	CC = 22pF, AV = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	CC = 22pF, AV = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, ±VS[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	VS = ±15		11			*		mA
	VS = ±60		12			*		mA
	VS = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case5	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES: * The specification of PB51A is identical to the specification for PB51 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $+V_S/-V_S$ must be at least 15V above/below COM.

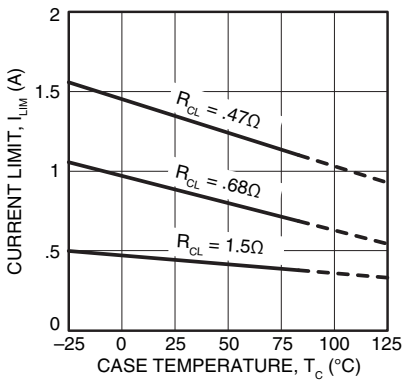
CAUTION The PB51 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

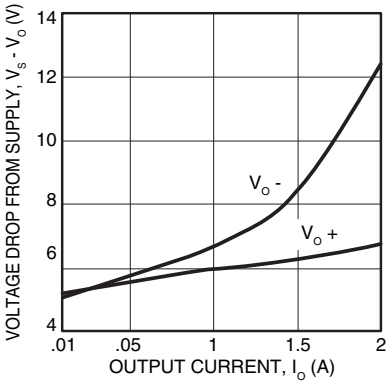
POWER DERATING



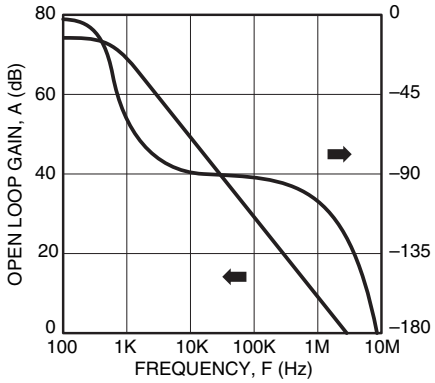
CURRENT LIMIT



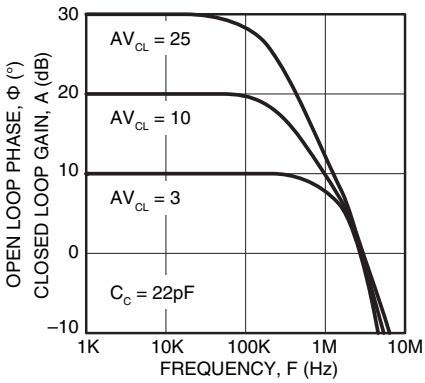
OUTPUT VOLTAGE SWING



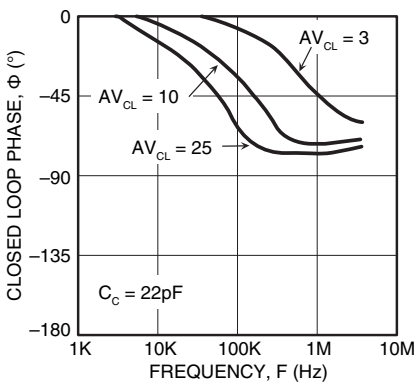
SMALL SIGNAL RESPONSE



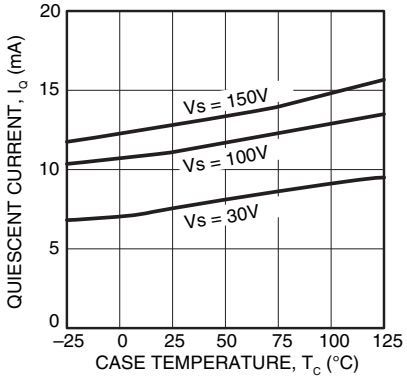
SMALL SIGNAL RESPONSE



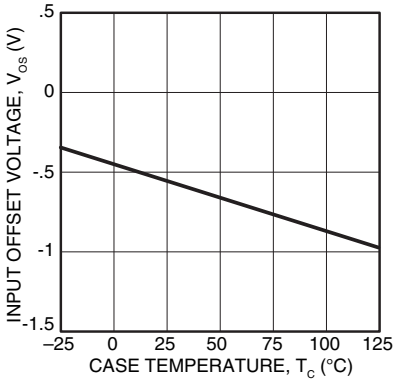
SMALL SIGNAL RESPONSE



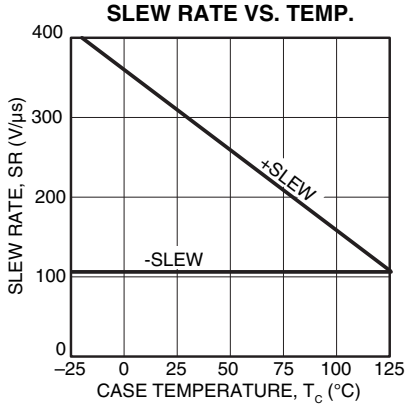
QUIESCENT CURRENT



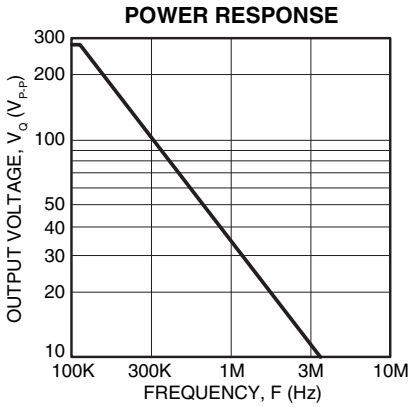
INPUT OFFSET VOLTAGE



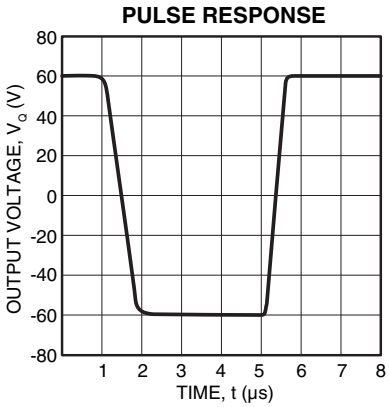
SLEW RATE VS. TEMP.



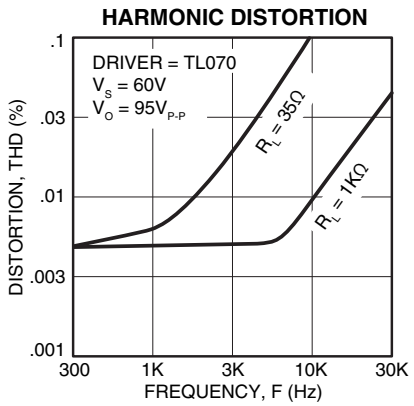
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION



GENERAL

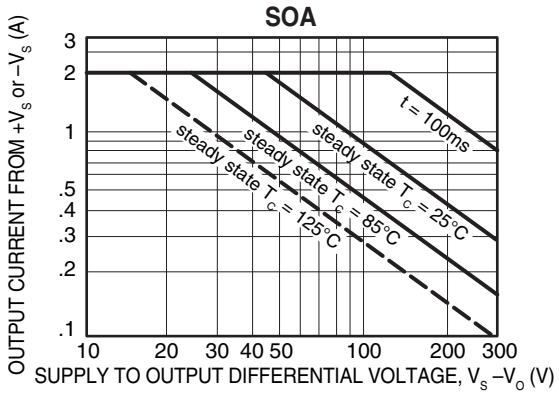
Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33 with a maximum practical value of 47. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows:

$+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av-1) \bullet 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.1K) + 1 = 3

Av (composite) = 60K/2K = – 30

Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

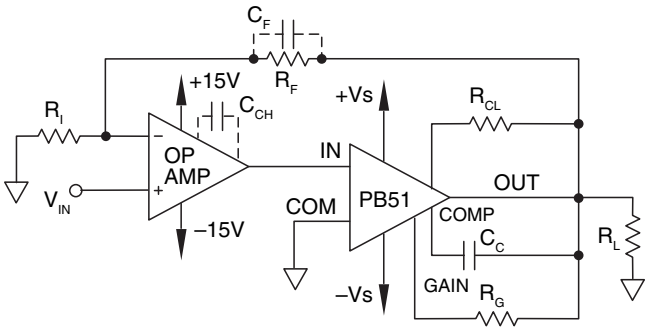
1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

TABLE 1. TYPICAL VALUES FOR CASE WHERE OP AMP EFFECTIVE GAIN = 1.



SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

Power Booster Amplifier

RoHS COMPLIANT

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT —
  - 1.5A Continuous (PB58)
  - 2.0A Continuous (PB58A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Minimum (PB58)
  - 75V/µs Minimum (PB58A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical
- EVALUATION KIT — See EK50

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 280V p-p

DESCRIPTION

The PB58 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB58 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers voids the warranty.

TYPICAL APPLICATION

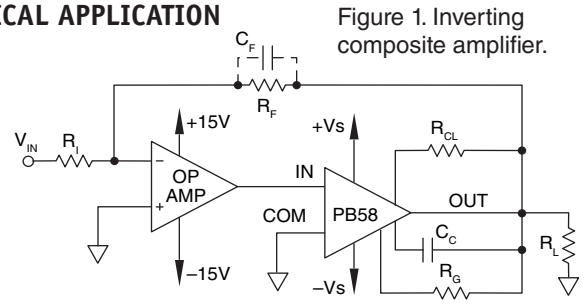
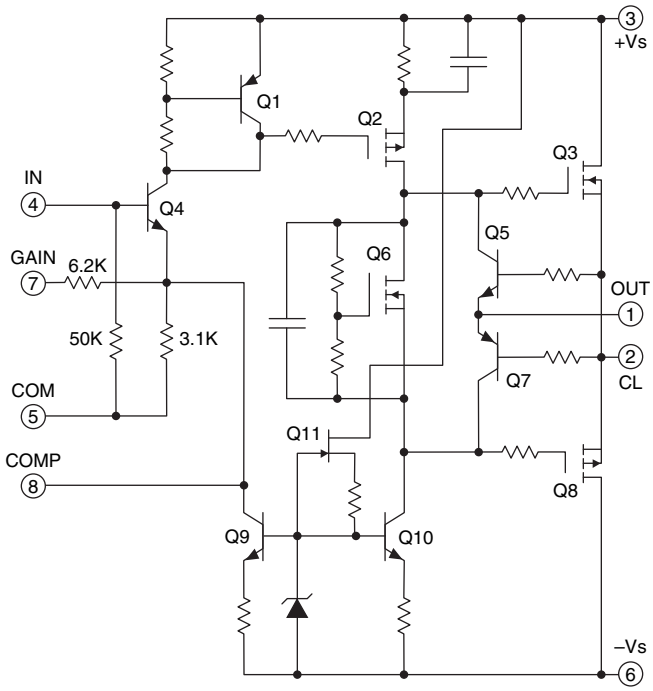


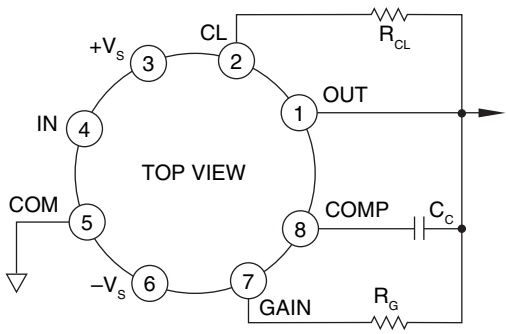
Figure 1. Inverting composite amplifier.

8-PIN TO-3
PACKAGE STYLE CE

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at T_C = 25°C[1]	83W
INPUT VOLTAGE, referred to COM	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

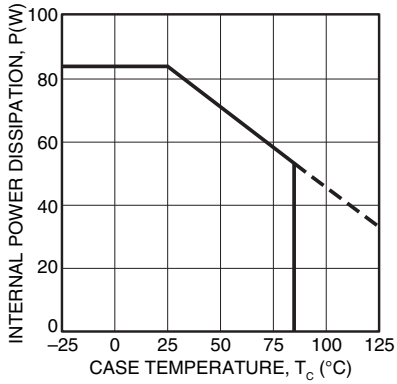
PARAMETER	TEST CONDITIONS[2]	PB58 MIN	PB58 TYP	PB58 MAX	PB58A MIN	PB58A TYP	PB58A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		kΩ
INPUT CAPACITANCE			3			*		pF
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	A_V = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	A_V = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AV_{CL} = 10, C_C = 22pF		10			*		°
	f = 200kHz, AV_{CL} = 10, C_C = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	V_S–11	V_S –8		V_S–15	V_S–11		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		*	*		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2			*		µs
POWER BANDWIDTH	V_C = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, $\pm V_S$[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	V_S = ±15		11			*		mA
	V_S = ±60		12			*		mA
	V_S = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES: * The specification of PB58A is identical to the specification for PB58 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $+V_S/-V_S$ must be at least 15V above/below COM.

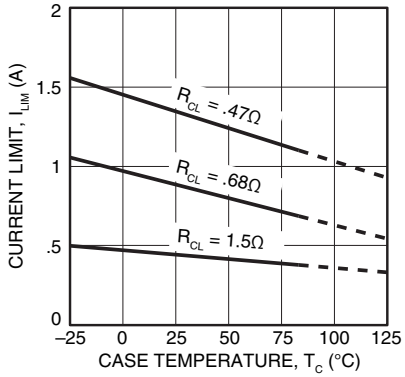
CAUTION The PB58 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

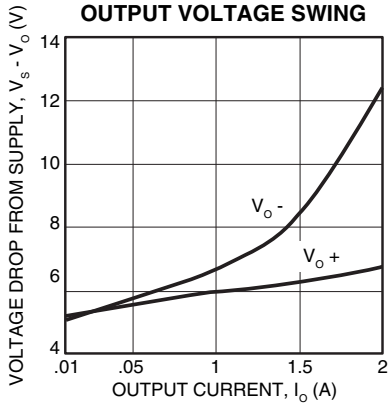
POWER DERATING



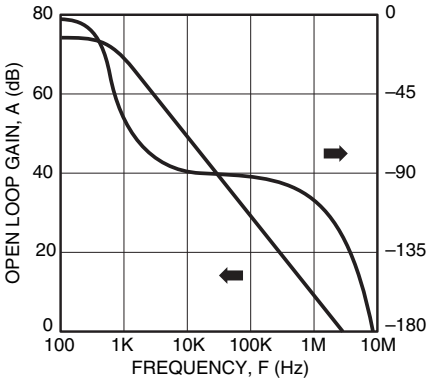
CURRENT LIMIT



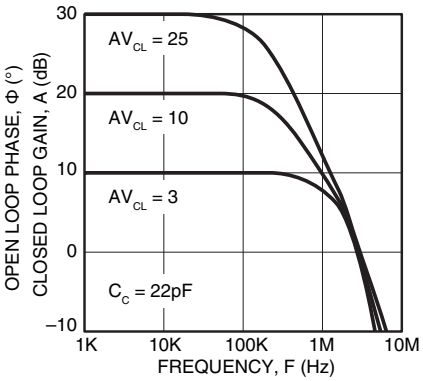
OUTPUT VOLTAGE SWING



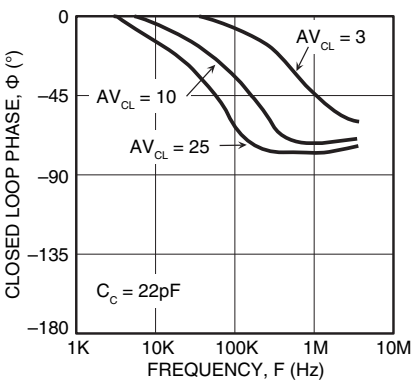
SMALL SIGNAL RESPONSE



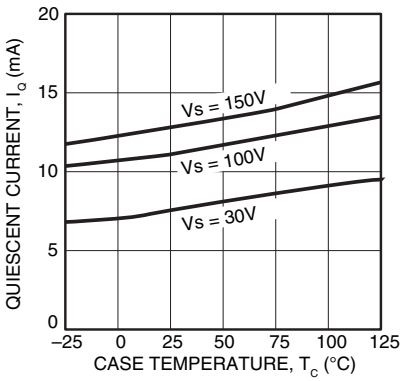
SMALL SIGNAL RESPONSE



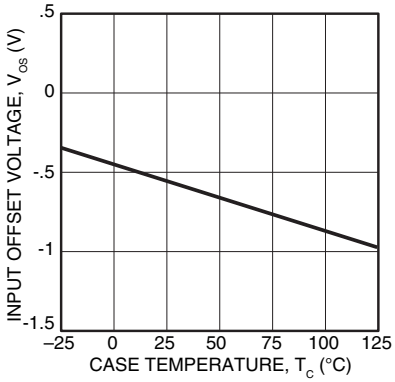
SMALL SIGNAL RESPONSE



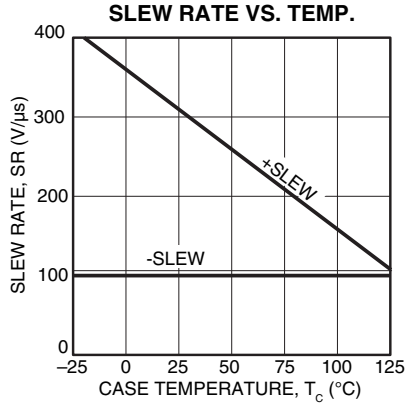
QUIESCENT CURRENT



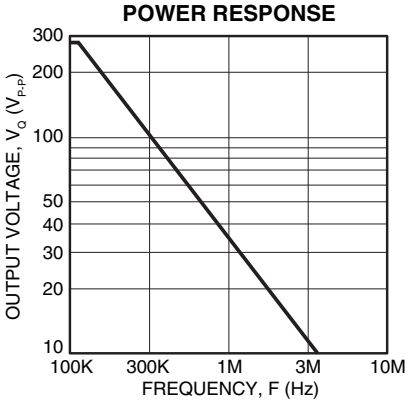
INPUT OFFSET VOLTAGE



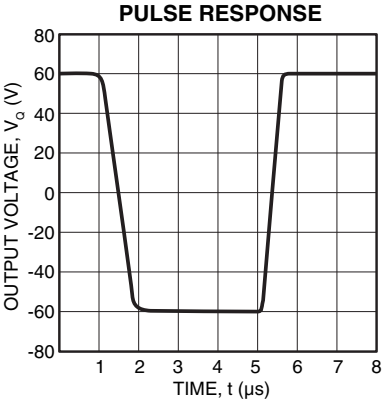
SLEW RATE VS. TEMP.



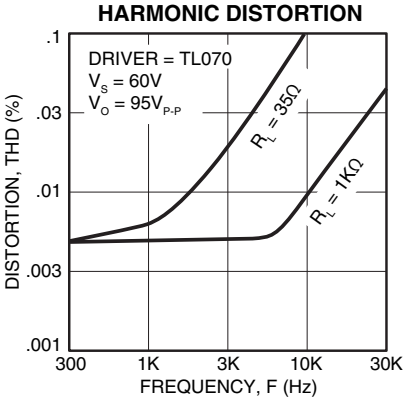
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION

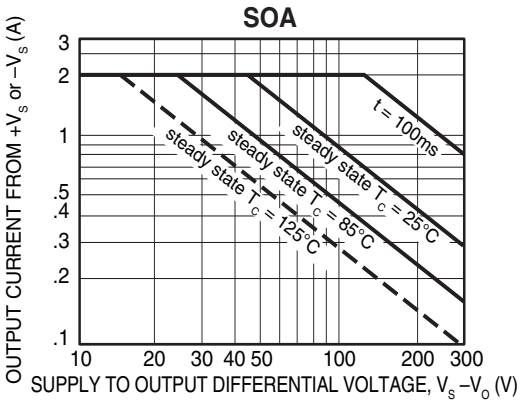


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.



SAFE OPERATING AREA

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av-1) \bullet 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.1K) + 1 = 3

Av (composite) = 60K/2K = – 30

Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

Table 1: Typical values for case where op amp effective gain = 1.

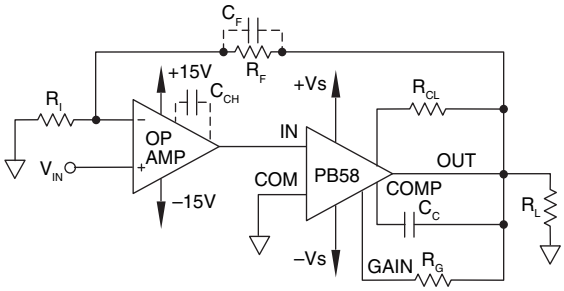


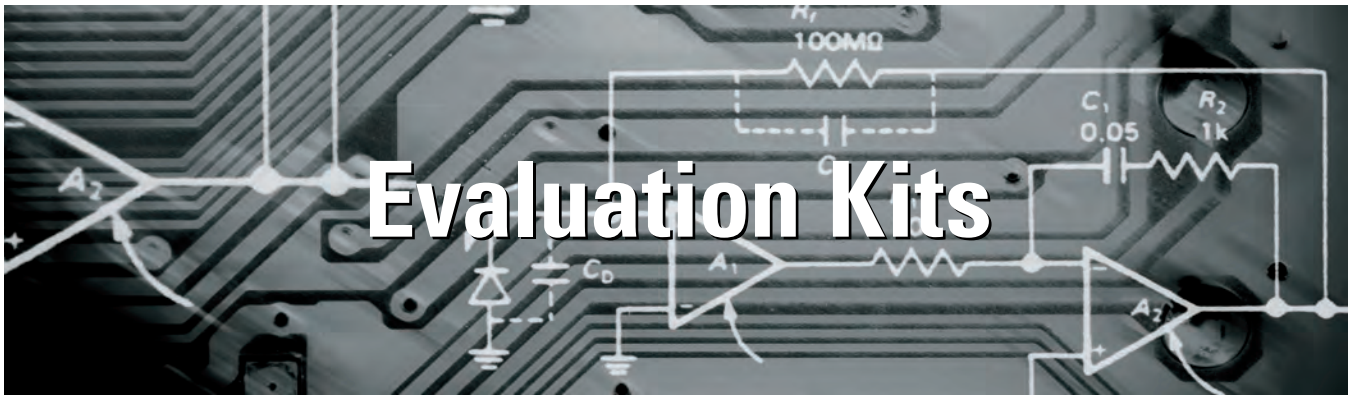
Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.



Evaluation Kits

F

CIRRUS LOGIC®

Evaluation Kit for SA01 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA01 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK01 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally. The PC board and the foot print of the heatsink measure 3" by 5".

PARTS LIST

Part #	Description	Quantity
HS16	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL07	PC Board	1
60SPG00001	Spacer Grommets	4
TW10	Thermal Washer	1 Box/10 each

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW10 thermal washer or a thin, even coat of thermal grease to the bottom of the SA01. If grease is from a tube make sure there is no sign separation of solids and liquids. If from a jar, stir it prior to application.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with thermal grease.
* Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M)
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

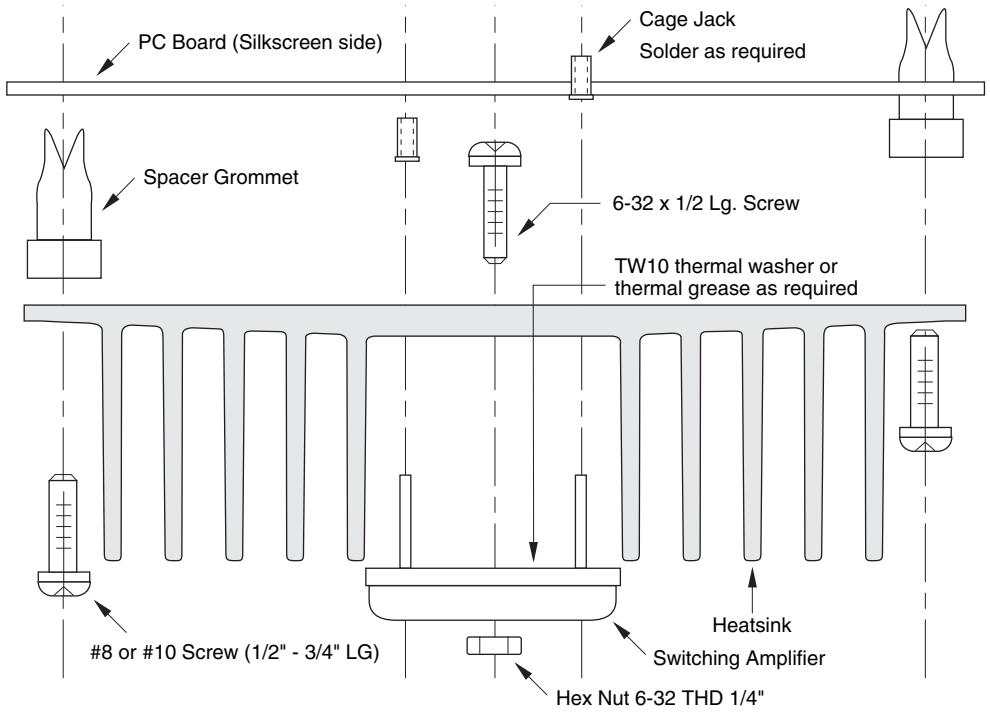
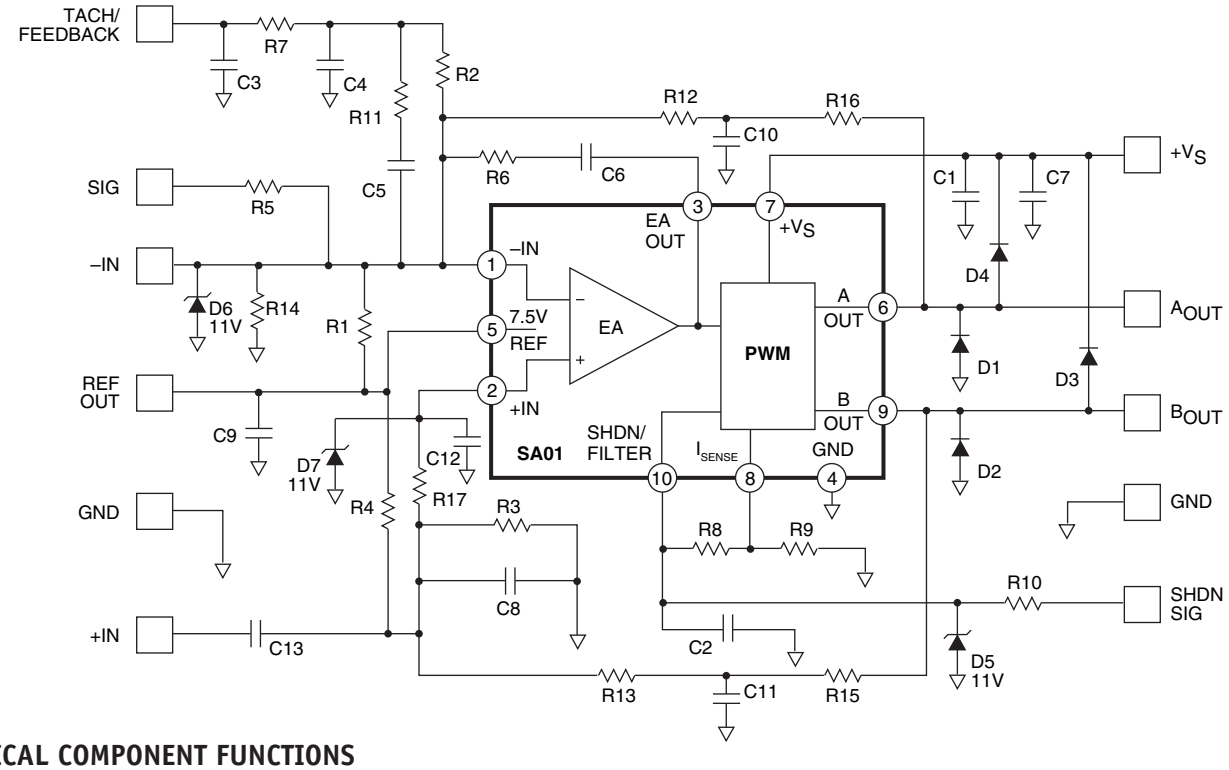


FIGURE 1.

FIGURE 2. PCB SCHEMATIC.

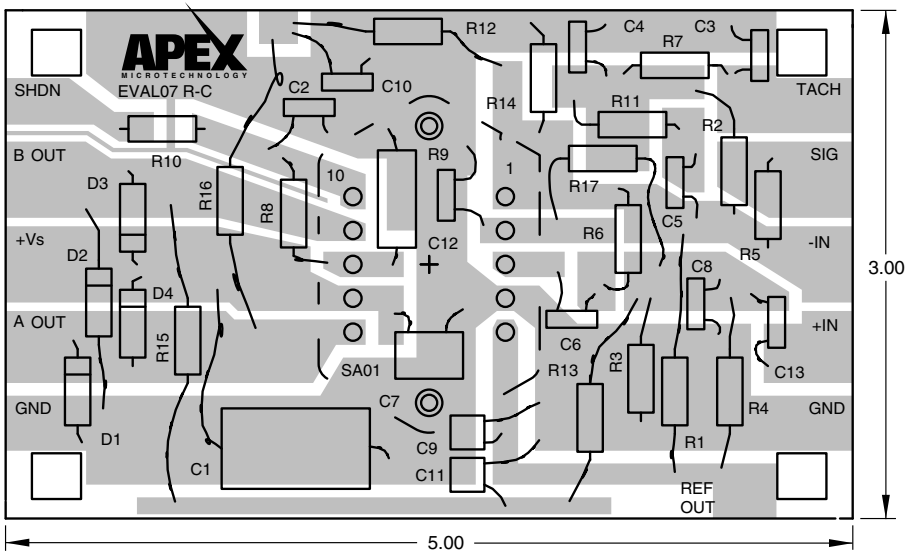


TYPICAL COMPONENT FUNCTIONS

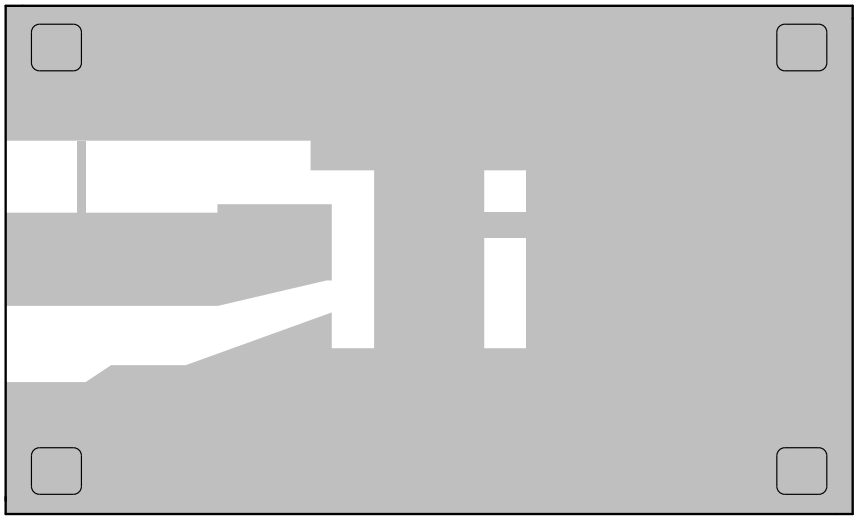
R1	Provides -IN bias from the Reference voltage.
R2	Sets DC scaling for external feedback such as tachometers, position sensors or current sensors.
R3	With R4 sets DC operating point of +IN, with R13 and R15 sets gain of voltage feedback circuit.
R4	With R3 sets DC operating point of +IN.
R5	Input scaling of the control signal.
R6	With C6 sets the corner frequency of the integrator.
R7	With C3 & C4 forms a low pass filter for the external feedback loop. Often used with tachometers.
R8	With C2 forms a low pass filter for the current limit circuit.
R9	Current sense. Often is a piece of resistance wire.
R10	With R8 divides shutdown signal voltage feeding SHDN/FILTER pin.
R11	With C5 sets corner frequency for external feedback loop.
R12, 13, 15, 16	Provides voltage feedback for a voltage controlled output.
R14	Helps set gain or scale input voltage levels.
R17	With C12 provides low pass filtering of +IN signal.
C1	Power supply bypass.
C2	With R8 form a low pass filter for the current limit circuit, also filters the SHDN signal.
C3, 4	With R7 forms a low pass filter for the external feed back loop. Often used with tachometers.
C5	With R11 sets corner frequency for external feedback loop.
C6	With R6 sets the corner frequency of the integrator.
C7	Power supply bypass, must have very low ESR in MHz range.
C8	Filters reference or feedback voltage at +IN.
C9	Bypass for the reference voltage.
C10, 11	With R15 and R16 provides low pass filtering of voltage feedback.
C12	With R17 provides low pass filtering of +IN signal.
C13	Provides AC coupling of +IN signal.
D1 – D4	Optional flyback diodes.
D5 – D7	Input protection zener diodes.

FIGURE 3. PCB

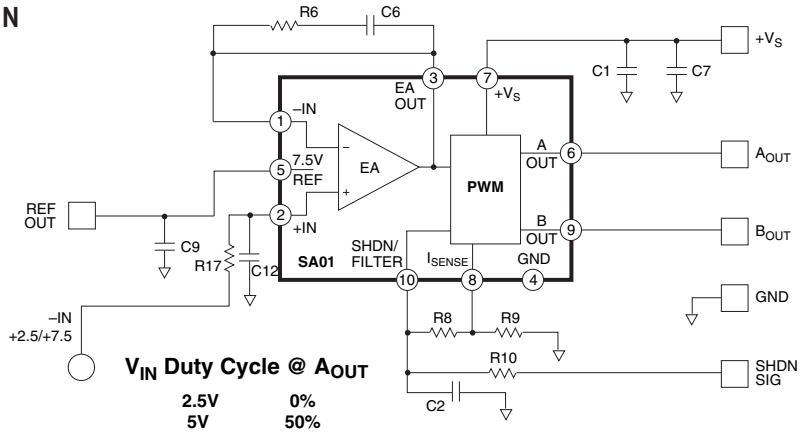
TOP SIDE



BOTTOM SIDE



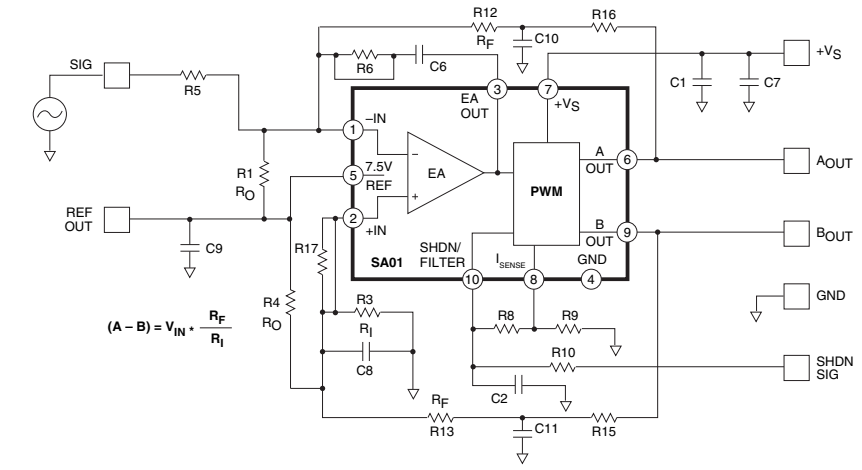
OPEN LOOP OPERATION



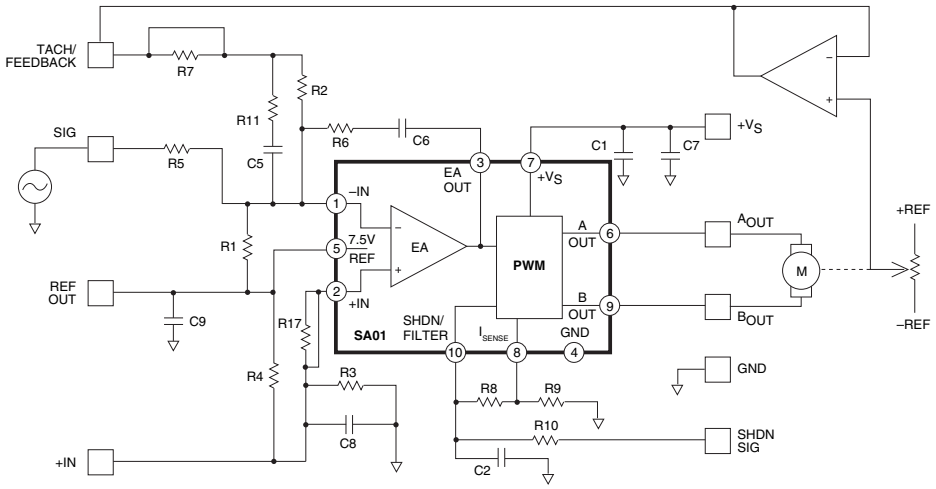
V_{IN}	Duty Cycle @ A_{OUT}
2.5V	0%
5V	50%
7.5V	100%

$$(A - B) = \frac{V_{IN} - 5}{2.5} * V_S - I_O * R_{DSON}$$

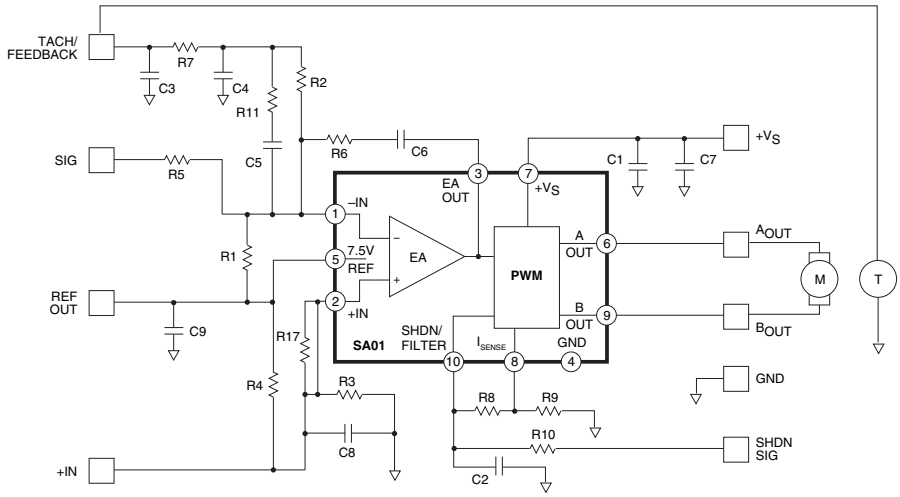
VOLTAGE CONTROL



POSITION CONTROL



SPEED CONTROL



Evaluation Kit for SA03 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA03 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK03 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL09	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	6

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW05 thermal washer to the bottom of the amplifier.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with TW05 washer.
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

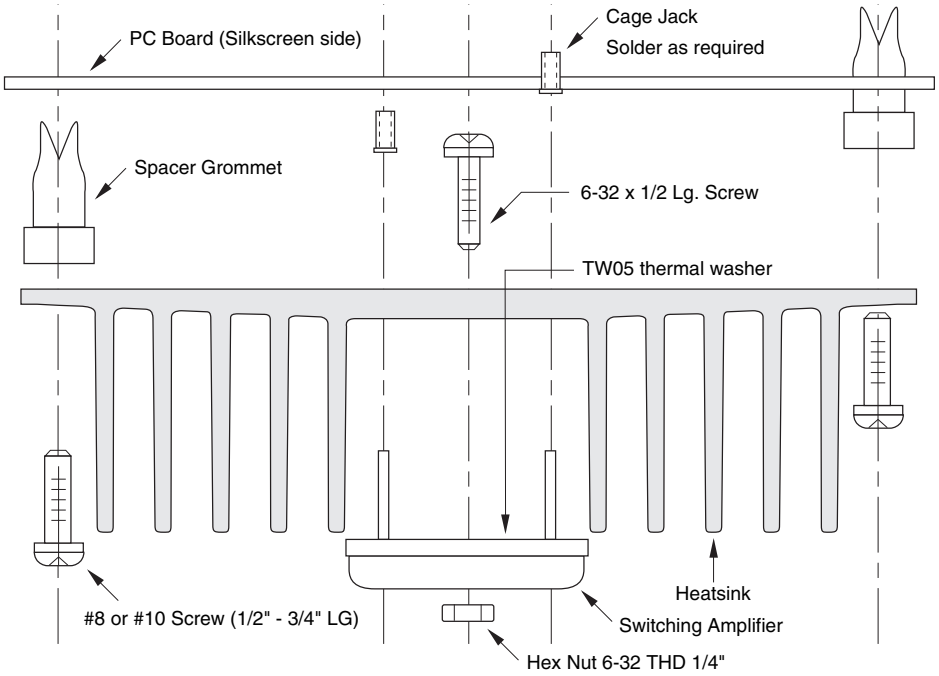
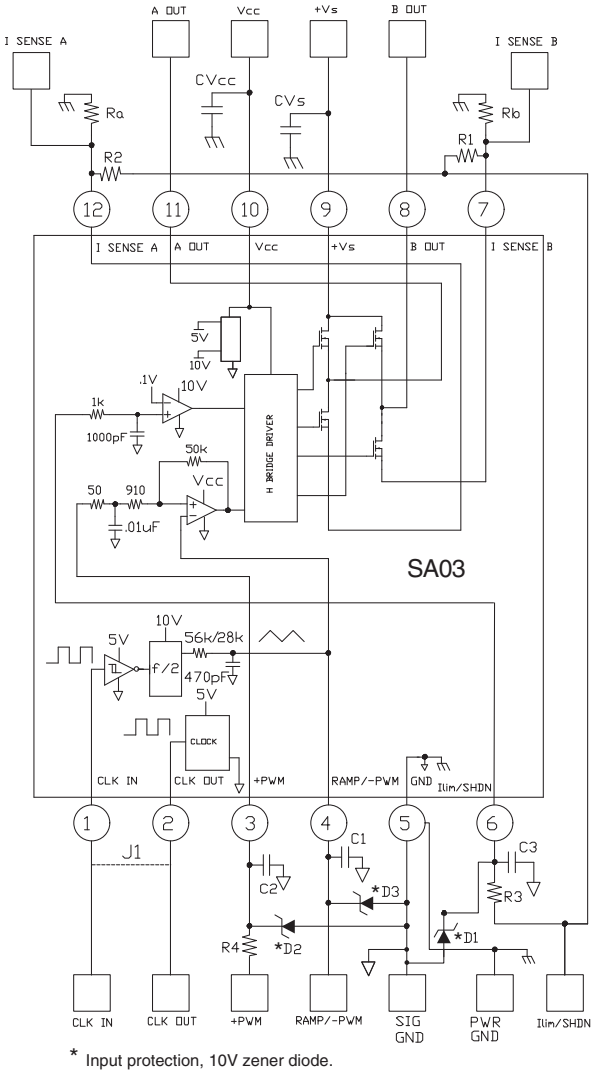


FIGURE 1.

A block diagram of the amplifier is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or banana jacks.

FIGURE 2. PCB SCHEMATIC.



* Input protection, 10V zener diode.

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

FIGURE 3. FUNCTIONAL TEST CIRCUIT

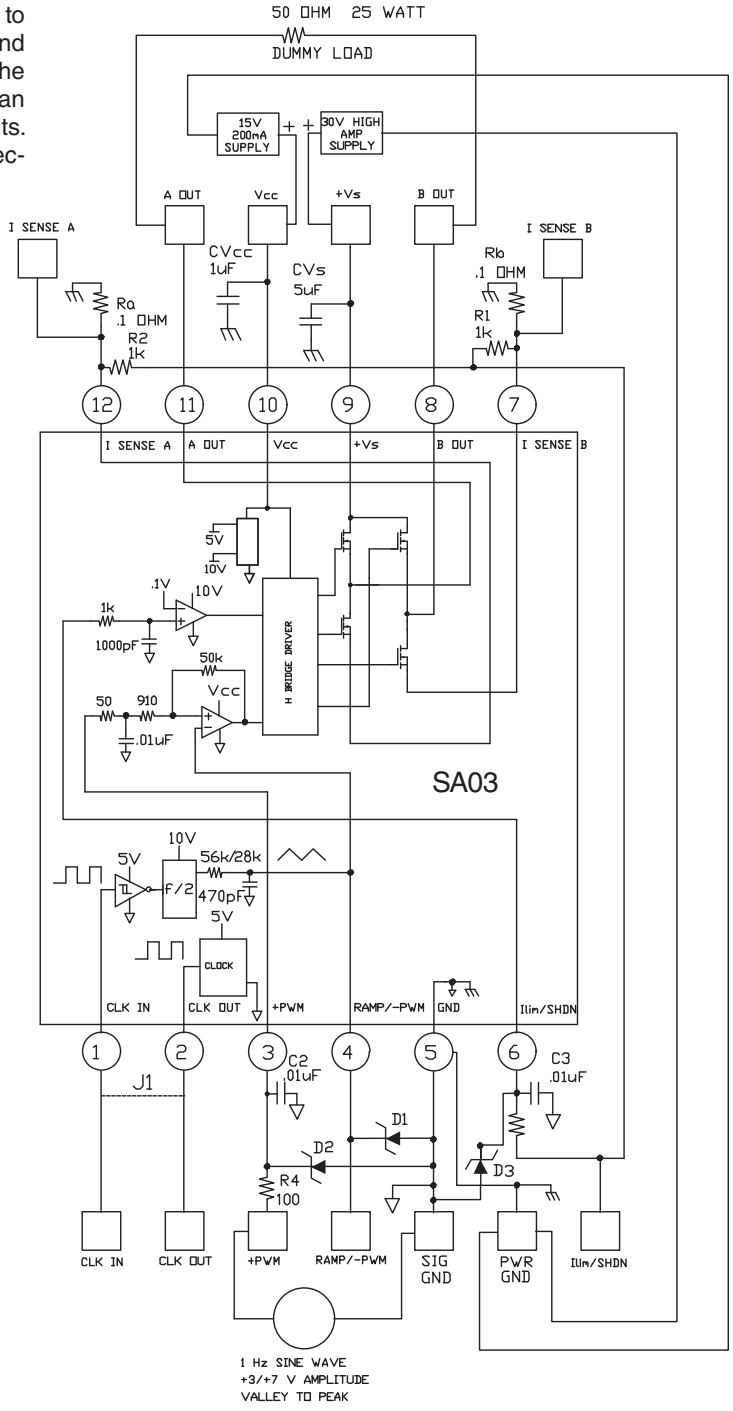
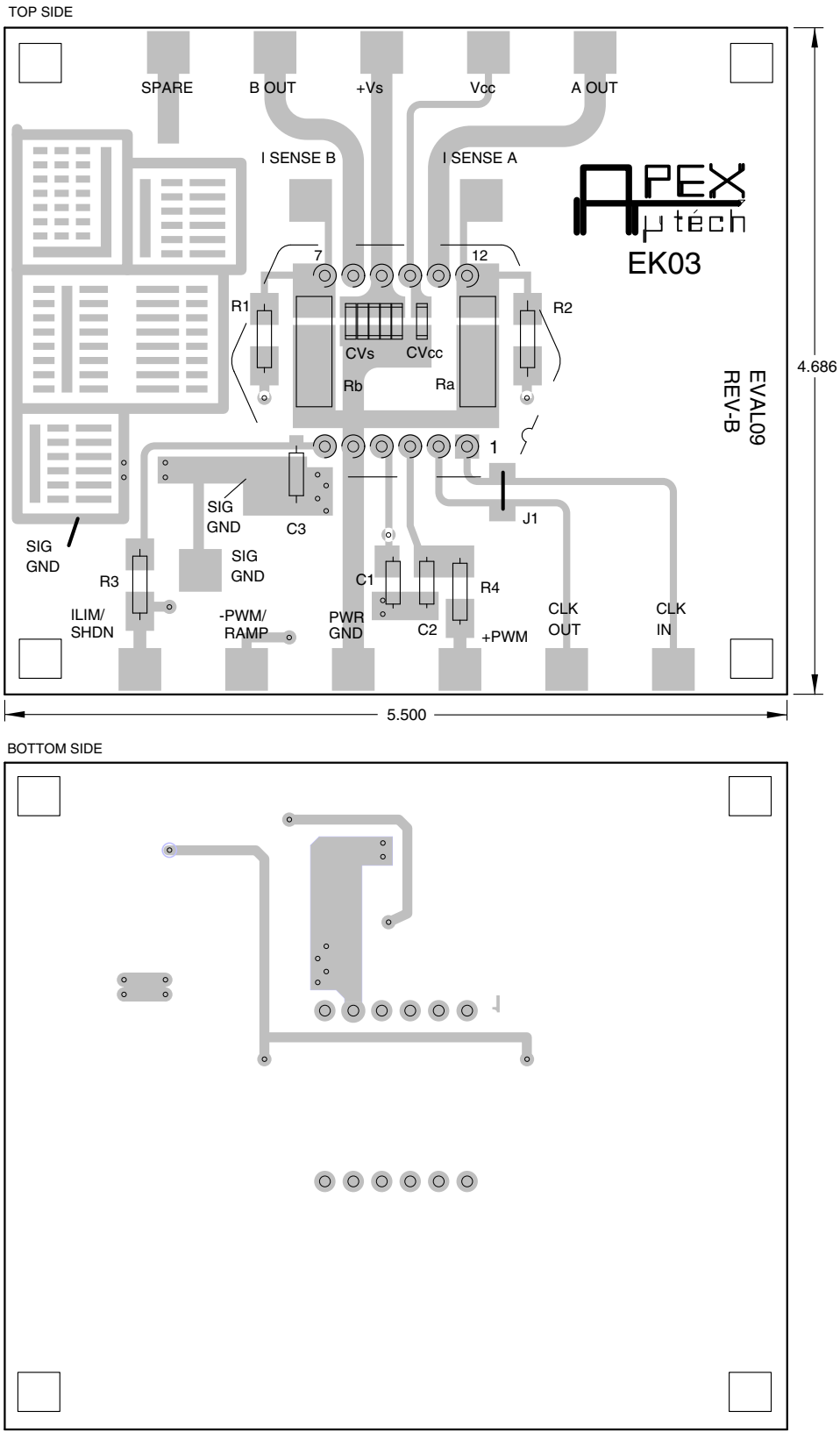


FIGURE 4. PCB


TOP SIDE
SPARE
B OUT
+Vs
Vcc
A OUT
I SENSE B
I SENSE A
EK03
7
12
R1
R2
CVs
CVcc
Rb
Ra
1
J1
SIG
GND
C3
SIG
GND
SIG
GND
R3
C1
R4
ILIM/
SHDN
-PWM/
RAMP
PWR
GND
C2
+PWM
CLK
OUT
CLK
IN
EVAL09
REV-B
4.686
5.500
BOTTOM SIDE

Evaluation Kit for SA60 Pin-Out

INTRODUCTION

Fast and easy breadborading of circuits using the SA60 are possible with the EK06 evaluation kit. The amplifier may be mounted vertically with the HS20 heat sink, or horizontally. Connections are provided for required power supply bypassing recommended protection components, as well as optional current sense resistors. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

CAUTION **Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.**

ASSEMBLY

1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1 – 12. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to include proper bypassing. See the SA60 data sheet for help in selecting these components. 1uF capacitors and a .10Ω resistor have been included with the EK06 kit but may be replaced with other components as necessary. C1, not provided, should be selected for the voltage required by the application. See Apex Precision Power Application Note 30 for guidelines in selecting this bypass capacitor. If current sense resistors are not used, the I SENSE traces on the EVAL11 board must be shorted to power ground in place of the resistors.
3. Place the TW07 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20). Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M). Do not over torque.
5. Install leads of the DUT into the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heat sink as shown in the assembly diagram (Figure 1).

PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL11	PC Board	1
MS06	Mating Socket	1
OX7R105KWN	1µF Ceramic Capacitor	2
CSR07	.1 Ω 1% Resistor	2
TWO7	Thermal Washer	1 package
HS22	Heatsink	2

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Power ground and signal ground must be separated to avoid switching noise in the DUT.

FIGURE 1.

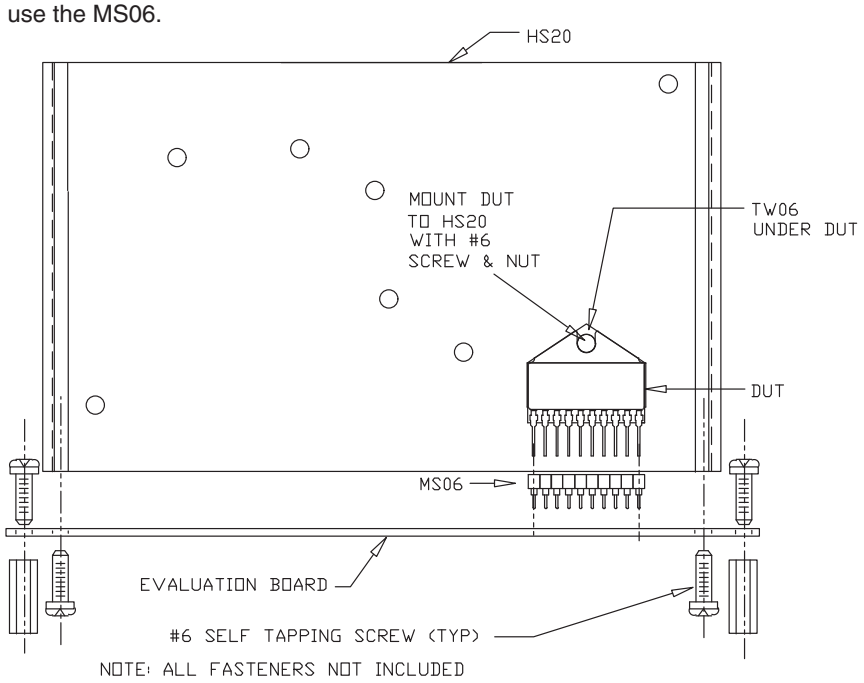
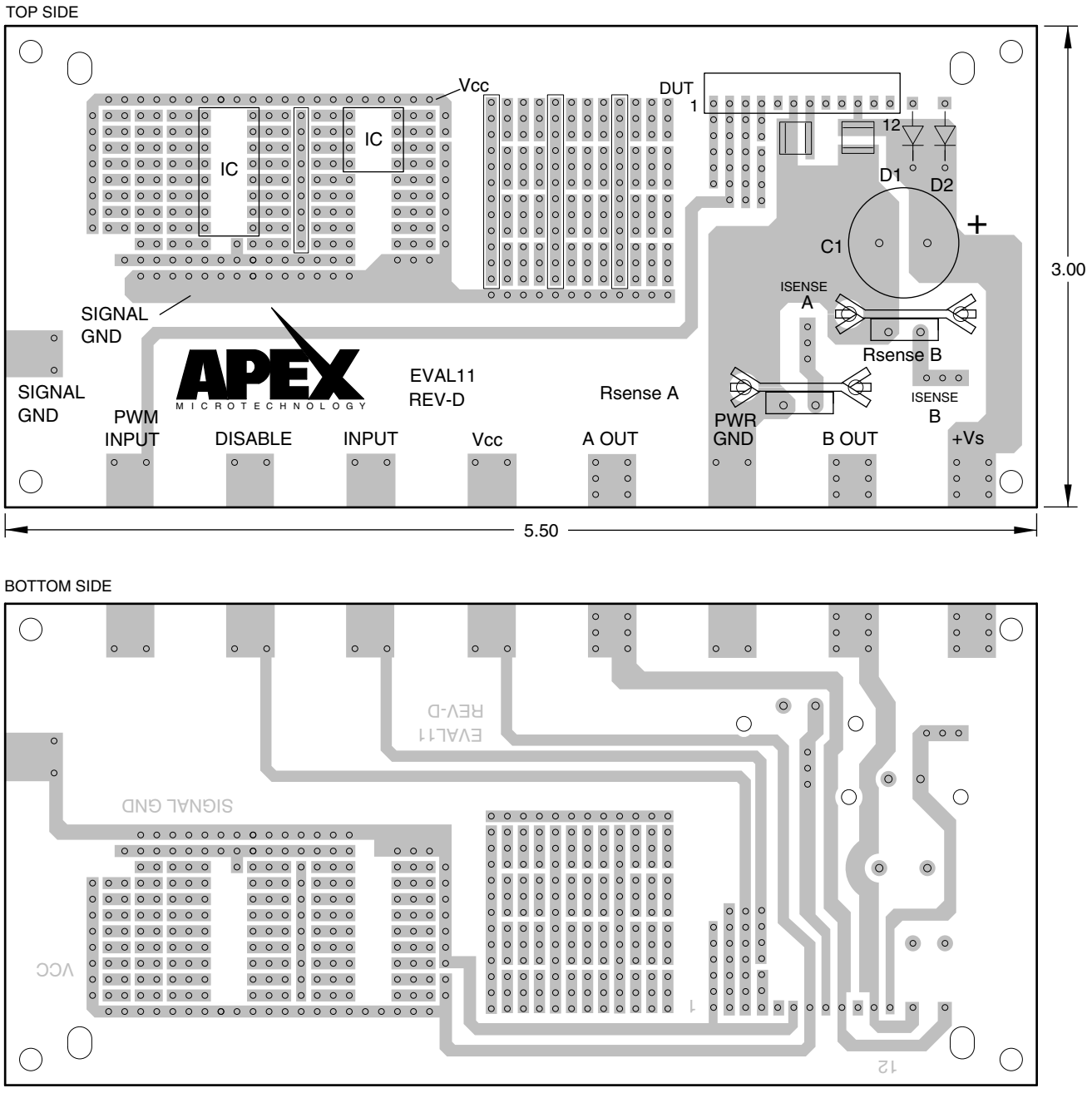


FIGURE 2.


TOP SIDE
Vcc
DUT
1
12
IC
IC
D1
D2
C1
+
3.00
ISENSE
A
SIGNAL
GND
Rsense B
APEX
MICROTECHNOLOGY
EVAL11
REV-D
SIGNAL
GND
Rsense A
ISENSE
B
PWR
GND
PWM
INPUT
DISABLE
INPUT
Vcc
A OUT
B OUT
+Vs
5.50
BOTTOM SIDE

Evaluation Kit for SA07 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifier circuits using the SA07 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 1.

ASSEMBLY

See Figure 3.

1. Solder the surface mount ceramic capacitors to the DUT side of the circuit board at CVs and CVcc.
2. Select a current limiting resistor from the two values provided. See the product data sheet for information on how to select a value. Apply a thin coating of thermal grease to the back of the resistors. Press the resistor body onto the circuit board foil at positions Ra and Rb and solder the leads.
3. Assemble the amplifier, thermal washer and heat sink to the circuit board as illustrated in Figure 1. As a last step push the clip through the heat sink and circuit board until it locks. Solder the amplifier pins to the circuit side of the circuit board.
4. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
5. Add other components as necessary to complete your application circuit.

BEFORE YOU GET STARTED

* All APEX amplifiers should be handled using proper ESD precautions.
* Always use thermal grease between the amplifier and heatsink.
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.

PARTS LIST

Part #	Description, Vendor	Quantity
CLAMP02	Mounting clip, Apex	1
HS21	Heat sink, Apex	1
EVAL18	PC Board, Apex	1
TWO9	Thermal washer, Apex	1 Box/10 each
OX7R105KWN	Capacitor, Novacap 1825B105K201N	2
CRS01	Resistor, Caddock MP725-0.10-1%	2
CRS02	Resistor, Caddock MP725-0.05-1%	2

Figure 1 shows the schematic of the evaluation kit's pre-wired connections Components supplied with the kit are marked with an asterisk (*). All other connections are made via the breadboarding areas of the circuit board.

FIGURE 1.

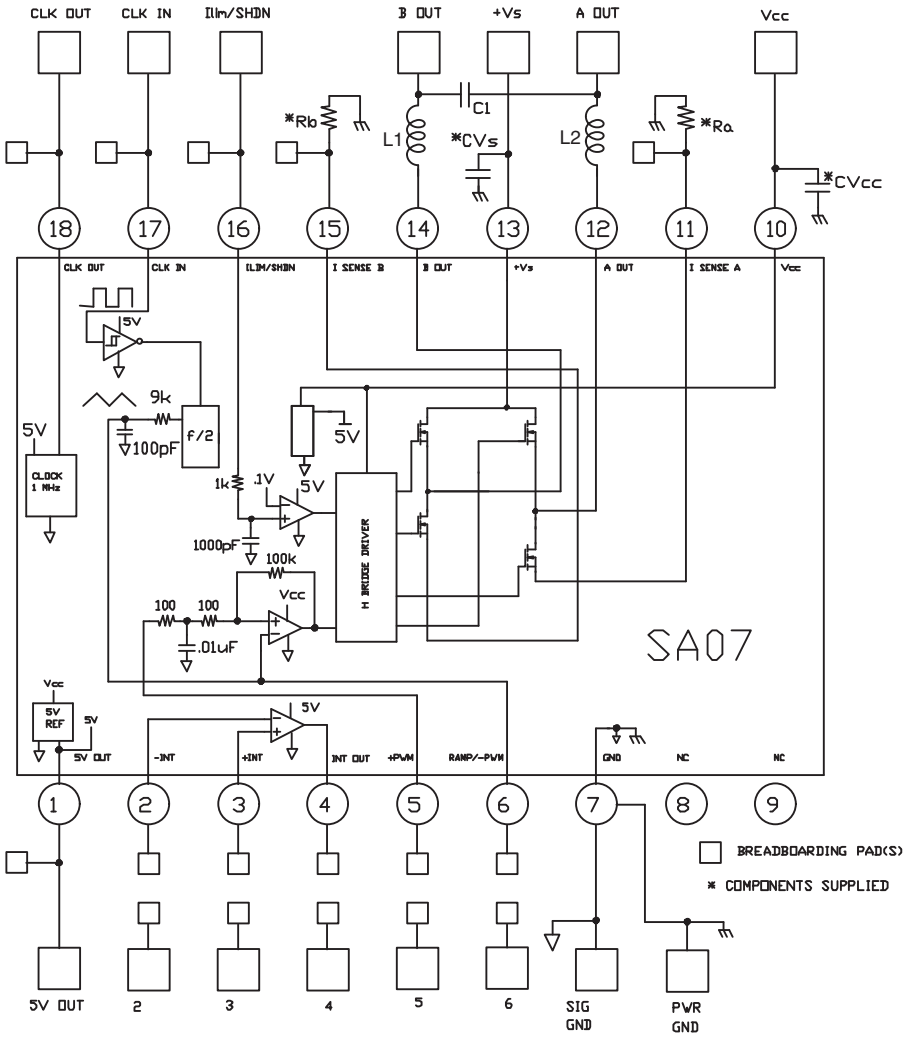


Figure 2 shows a suggested simple test circuit that you can build to gain a familiarity with the evaluation kit as well as the amplifier. At the A OUT or B OUT pads relative to power ground you should observe a square wave with a frequency of approximately 500kHz, 30V p-p which is being modulated from approximately 0 to 100 % duty cycle at a rate of 1 Hz.

FIGURE 2.

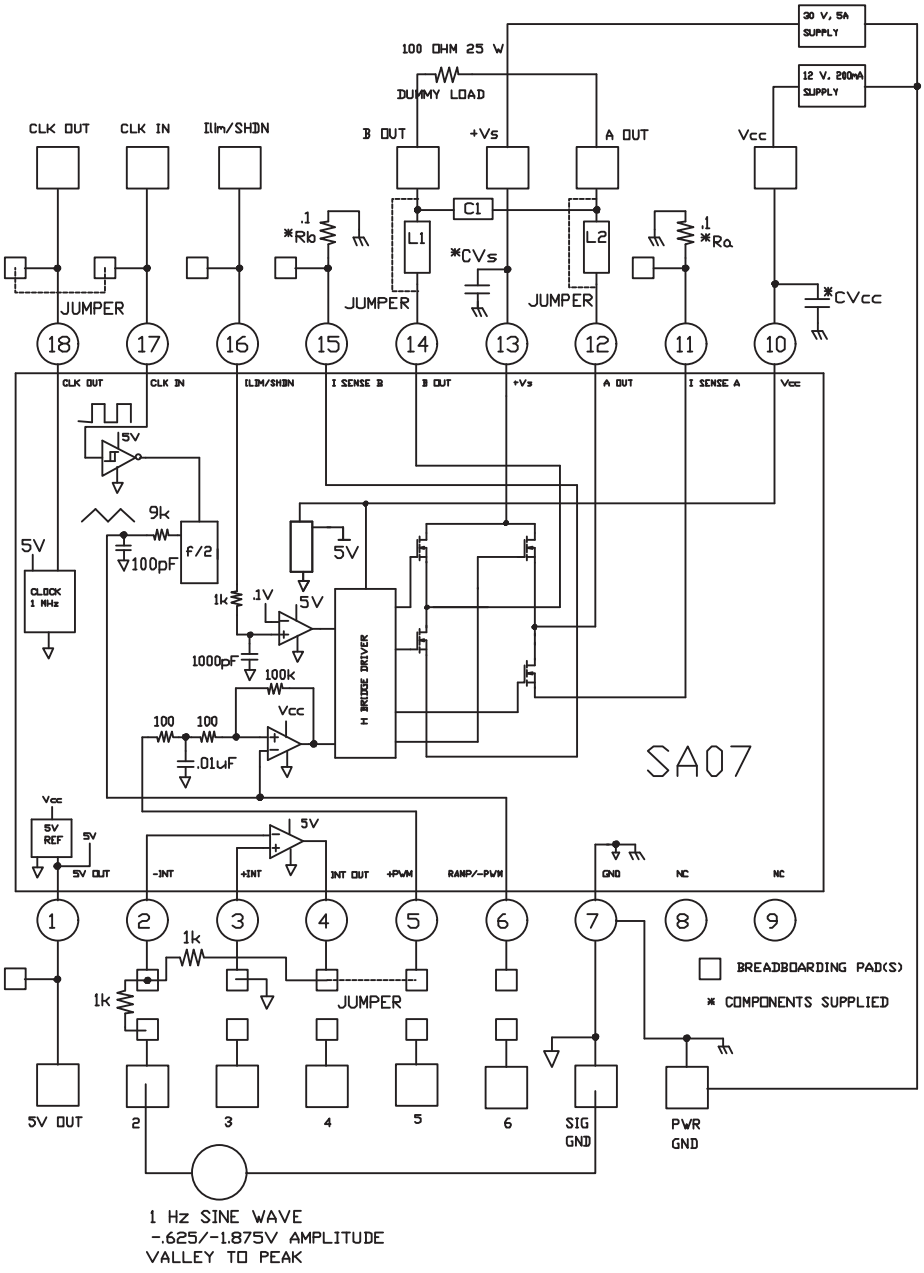
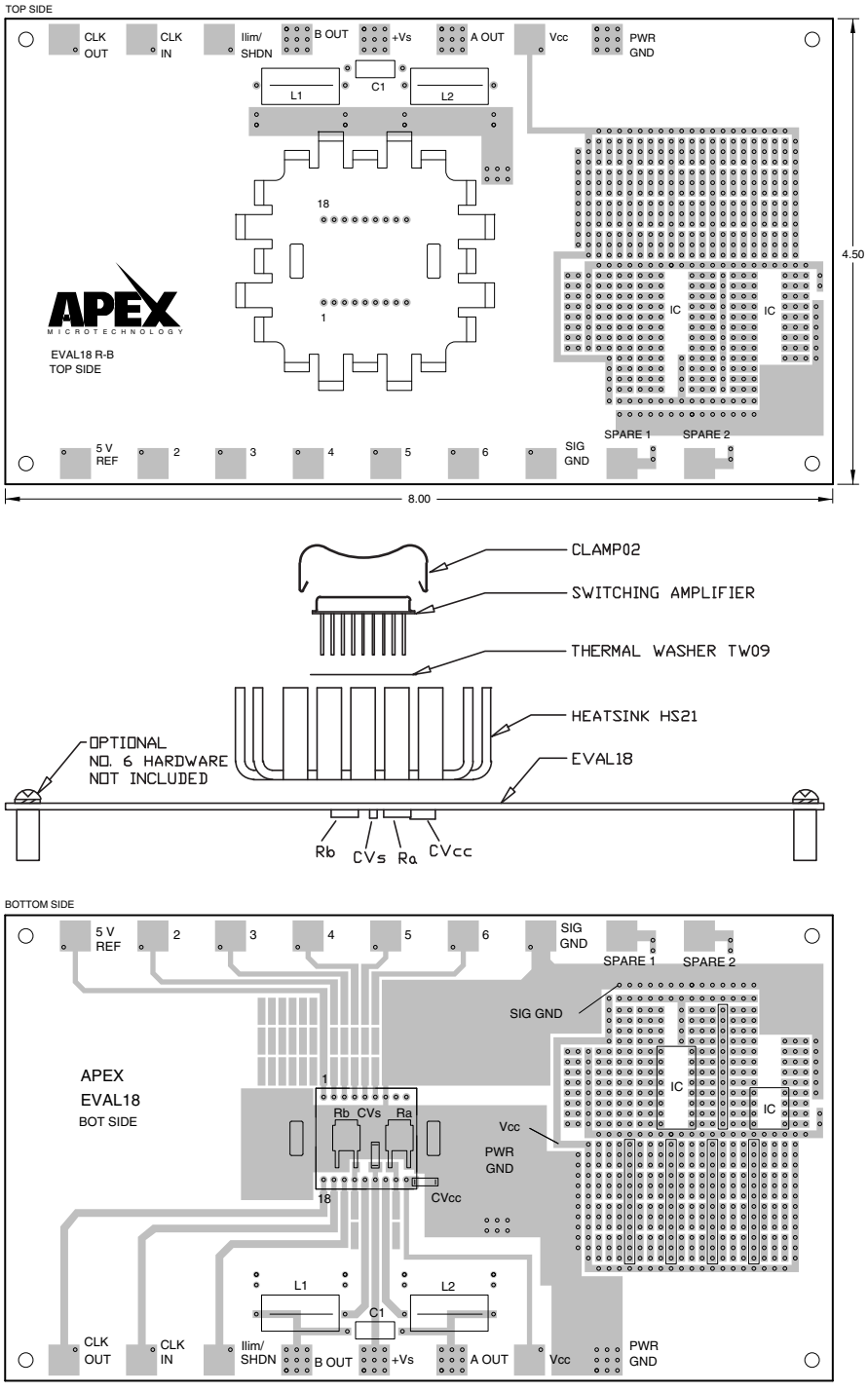


FIGURE 3. PCB


TOP SIDE
CLK OUT
CLK IN
Ilim/ SHDN
B OUT
+Vs
A OUT
Vcc
PWR GND
L1
C1
L2
18
1
APEX
MICROTECHNOLOGY
EVAL18 R-B
TOP SIDE
IC
IC
SPARE 1
SPARE 2
5 V REF
2
3
4
5
6
SIG GND
4.50
8.00
CLAMP02
SWITCHING AMPLIFIER
THERMAL WASHER TW09
HEATSINK HS21
EVAL18
OPTIONAL
NO. 6 HARDWARE
NOT INCLUDED
Rb
CVs
Ra
CVcc
BOTTOM SIDE
APEX
EVAL18
BOT SIDE
Rb CVs Ra
CVcc
Vcc
PWR GND
SIG GND

Evaluation Kit for TO-3 and MO-127 Packages

INTRODUCTION

This kit provides a solid mechanical platform with good shielding and grounding to breadboard eight pin TO-3 packages or the MO-127 package with 0.060" pins. This kit is not intended as an alternate for kits dedicated to specific amplifiers. See www.Cirrus.com for availability of dedicated kits.

Construction will involve surface mounting and 3D techniques. Holes are provided to mount standard banana and BNC connectors for I/O. See the Apex Precision Power Accessories Information data sheet for a selection of flat-back heatsinks and thermal washers for these packages.

Note that HS11 is compatible with EK09 and all three sockets can be used if desired. If the EK09 is to be used as an MO-127 platform only, HS18 rated at 1° C/W is a cost effective alternative to HS11 if internal power dissipation permits. Lower cost alternatives for two package TO-3 applications are HS02, HS01, and HS09. For single package TO-3 applications the HS13 is also suitable. The six chip capacitors provided can be used as the critical first step in power supply bypass for dual supplies for all three sockets. These capacitors are rated at 200V.

PARTS LIST

Part #	Description	Quantity
PB99-P2	top	1
PB99- P6	side	2
PB99-P7	side	2
MS02	cage jacks for one TO-3 socket	2
MS04	cage jacks for one MO-127 socket	1
OX7R105KWN	1µF Cap 1825B105K201N,Novacap	6

BEFORE YOU GET STARTED

- Attempt to visualize the finished circuit mechanically and in terms of where the high currents flow.
- Use proper ESD precautions.
- Verify heatsink is adequate
- Use thermal grease or Apex Precision Power thermal washer.
- Do not make or break any connection on a hot circuit.
- Start with lowest rated voltages.
- Checking for oscillations with an oscilloscope is a must.

ASSEMBLY

Let us define the side of the top board with solder pads for each pin (roughly triangular on the TO-3 sockets) as the component side, where all the support components will determine circuit function and will be inside the finished box. The other side of this board is hereby dubbed the amplifier side.

Insert cage jacks from the amplifier side and solder. Consider one of these techniques: 1) Place cage jacks in holes, cover with one of the 6" copper sides, flip over and solder, or 2) place cage jacks on pins of the amplifier, insert and solder. If done carefully, technique 2 can be used for the MO-127 package with 0.040" leads.

Starting with one short and one long side, locate a vertical square corner in your work area (a large heatsink standing on end works fine) and solder the two together. Repeat for the other two sides, and finally solder the two pairs together. With the component side up , place rectangle of sides on top and tack two opposite corners. When satisfied with alignment, solder the box together then add connectors and components as desired.

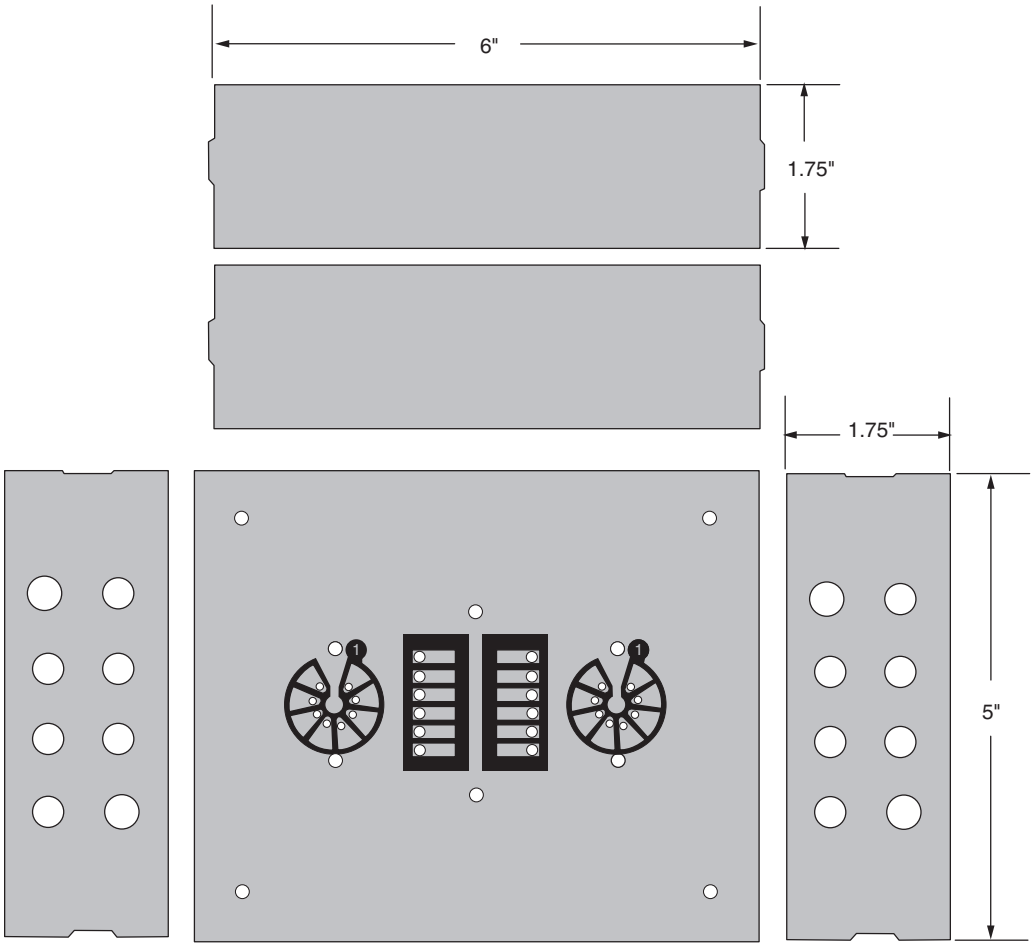
Note that copper on the inside and on the top of the box will all be tied to ground. Copper on the four outer sides of the box will be floating unless you tie them down.

Soldering a stranded #10 to #16 ground wire from the immediate area of the socket(s) to the ground connector of the power supply(ies) is good construction practice. If the circuit is not a bridge, run this same size wire from the socket area to the output return connector. This will avoid high currents in the ground plane which may destroy signal integrity or even an amplifier. This is a good time to think about star grounding where each ground connection has a dedicated path to the center of the star such that currents in any path are not capable of inducing voltage in any other path.

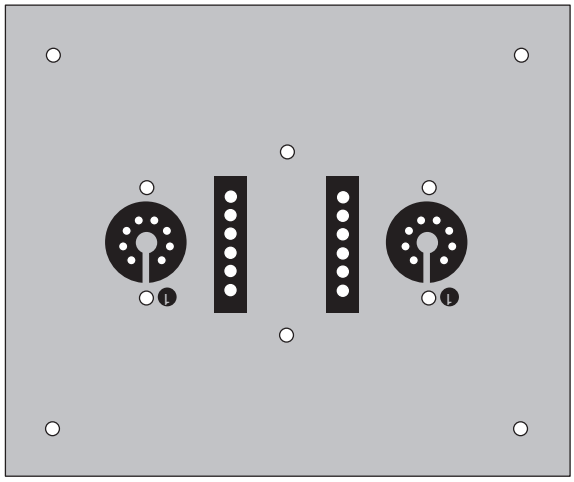
Note that the layout makes it easy to locate the star center nearly coincident with the socket center.

Auxiliary circuits may be mounted inside the box in 3-D fashion supported on ground connections or on daughter boards as convenient. Other style connectors, switches or indicators can easily be added by simply drilling the appropriate holes and mounting them.

FIGURE 1. COMPONENTS INCLUDED IN EK09.



Component side



Amplifier side

- 2 MS02,16 CAGE JACKS FOR TWO TO-3 SOCKETS
- MS04,12 CAGE JACKS FOR ONE MO-127 SOCKET
- OX7R105KWN, 6 CAPACITORS, 1µF, 200V

Figure 2.
External with heatsink (heatsink, amplifier, connectors and switches not supplied).

Figure 3.
Inside of assembled box. Holes for components on long side were user drilled.

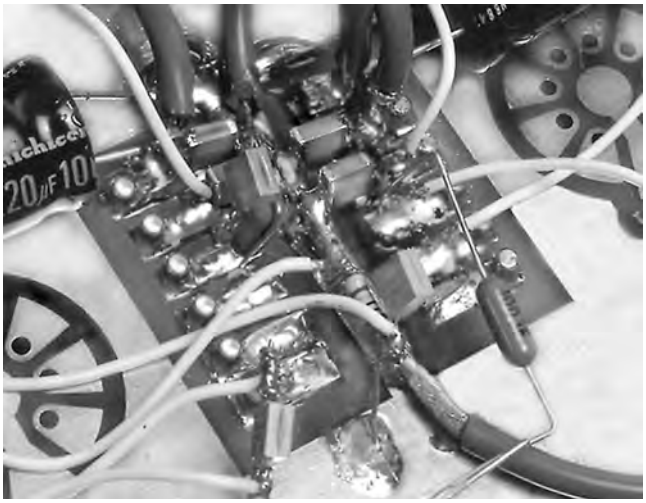


Figure 4.
Socket detail shows the center of the star ground system is right in the center of the socket.

Evaluation Kit for PA90, PA91, PA98

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA91 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 1.

PARTS LIST

Part #	Description, Vendor	Quantity
HS27	Heatsink, Apex Precision Power	1
EVAL24	PC Board, Apex Precision Power	1
TW07	Thermal Washer, Apex Precision Power	1 box, 10 ea.
P6KE250A	Transient Zener, Microsemi (250V)	2
CDC01	Capacitor .01µF 1kV, Sprague 5GAS10	2

ASSEMBLY

1. See Figure 2. Insert and solder the transient zener diodes at D3 and D4 (250V).
2. Insert and solder the disc bypass capacitors at C1 and C2.
3. Insert the HS27 heatsink and solder the solderable studs from the opposite side of the PCB.
4. Add banana jacks as necessary to complete connections to external circuits and power supplies.
5. Insert the amplifier into the PCB mounting holes located in the space between the heatsink fins. So not solder the pins at this time.
6. Hang the TW07 thermal washer near the end of a 6-32 X 3/8" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heatsink. Use a 6-32 nut to secure the screw from the opposite side of the heatsink. It is important that the entire back surface of the amplifiers mounting tab be in contact with the heatsink. Adjust the amplifiers position and tighten the mounting screw as necessary for this to be so.
7. Solder the amplifiers pins to the PCB.
8. Add other passive components as necessary to complete your circuit.
9. Most common configurations will ground the non-inverting pin of the amplifier. J1 is a convenient way to do this if necessary for your application circuit.
10. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
11. R1-R3 are multiple feedback resistors in series. Commonly available resistors do not have a breakdown voltage sufficient to stand off the output voltage of the amplifier. Using multiple resistors will divide down the voltage that each resistor must withstand.

FIGURE 1.

Figure 1 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). See the amplifier's data sheet for full application information.

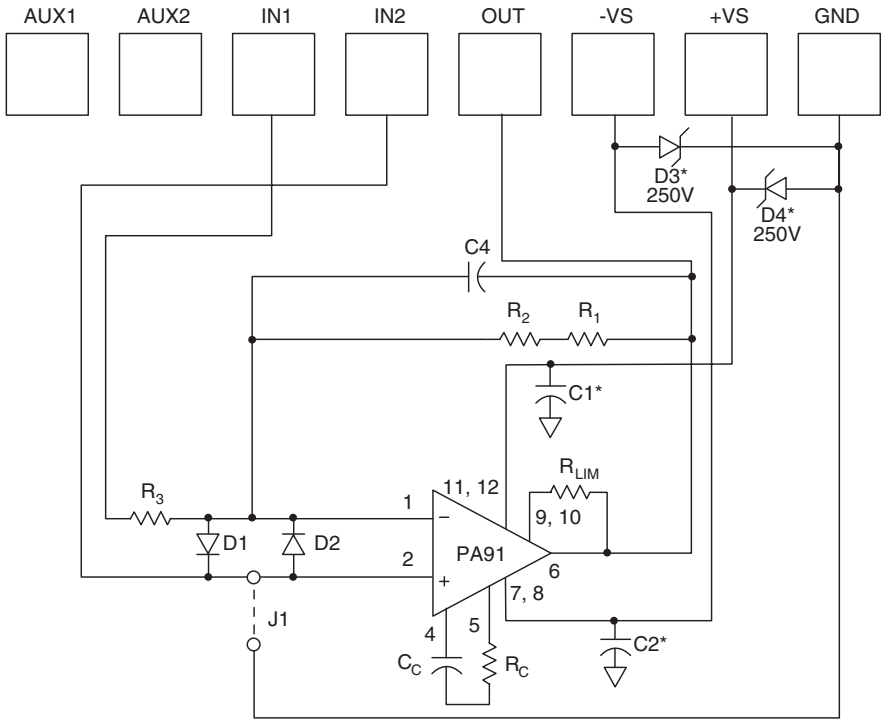
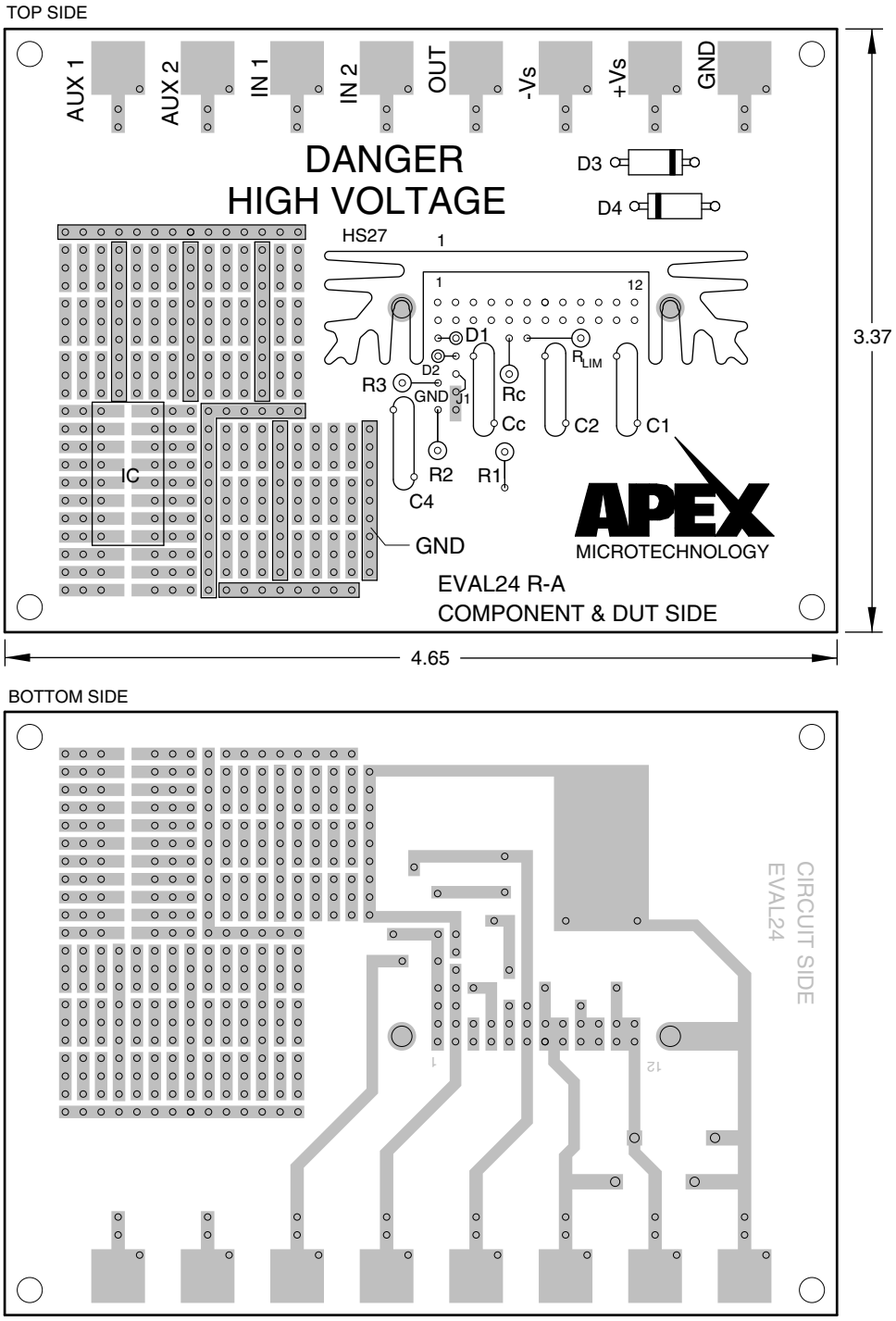


FIGURE 2. PCB


TOP SIDE
AUX 1
AUX 2
IN 1
IN 2
OUT
-Vs
+Vs
GND
DANGER
HIGH VOLTAGE
D3
D4
HS27
1
1
12
D1
D2
R3
GND
J1
Rc
Cc
C2
C1
R2
R1
C4
IC
GND
APEX
MICROTECHNOLOGY
EVAL24 R-A
COMPONENT & DUT SIDE
3.37
4.65
BOTTOM SIDE
CIRCUIT SIDE
EVAL24

Evaluation Kit for PA241DF

INTRODUCTION

Fast and easy breadboarding of circuits using the PA241DF IS possible with the EK13 evaluation kit. The amplifier may be surface mounted directly to the PC board. The PA241DF is soldered to a 2-square inch area of foil on the PC board for heat sinking. This foil heat sink is connected to–Vs. Connections are provided for required power supply bypassing, phase compensation components, and a current limit resistor. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

PARTS LIST

Part #	Description	Quantity
EVAL15	PC Board	1
OX7R105KWN	1µF Ceramic Capacitor	1
HS24	Heatsink	1

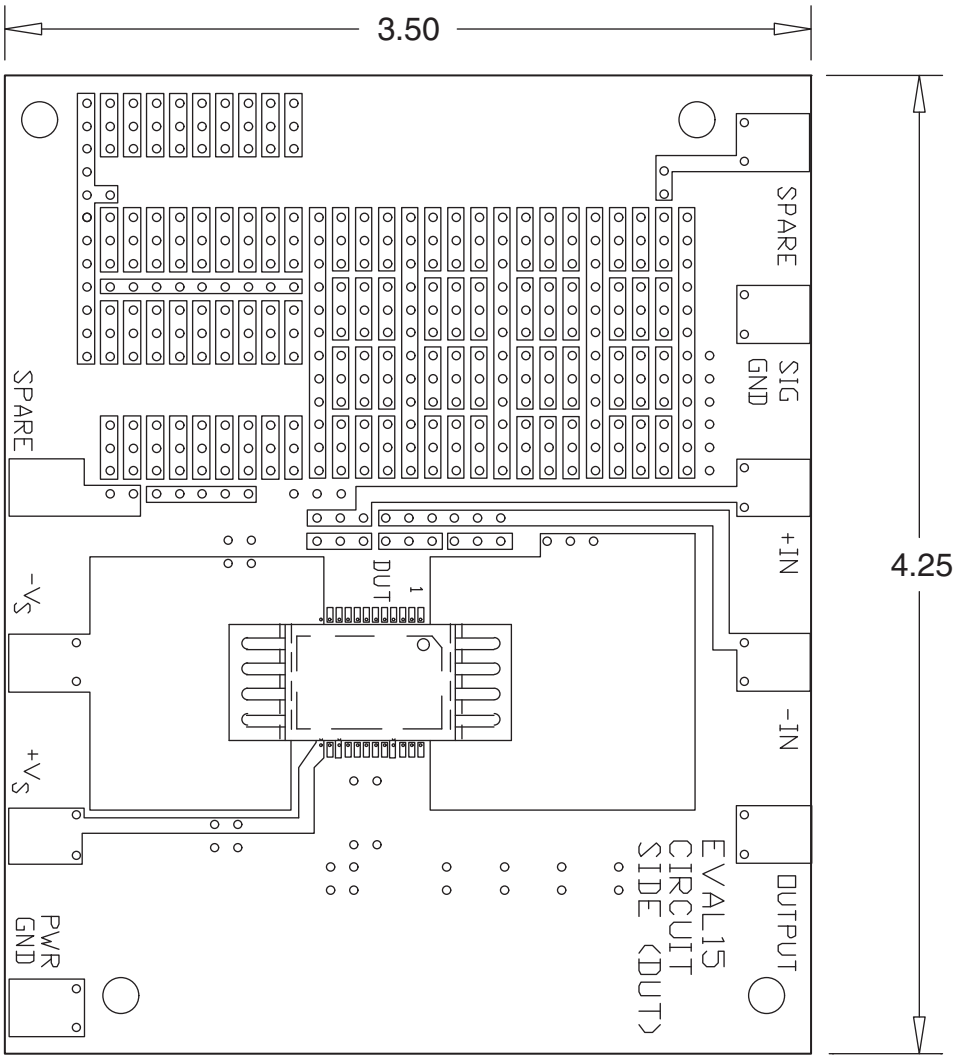
ASSEMBLY

The PA241DF is a surface mount device and should be assembled to the EVAL15 PC board using surface mount processes. Solder paste may be dispensed or screen-printed on the DUT pads. The heat tab on the back of the PA241DF provides maximum heat dissipation capabilities when soldered to the PCB metalization that runs under the DUT on the DUT side of the board. Solder should be applied here also. For prototype purposes, the tab can be thermally connected to the PCB metalization using thermal grease.

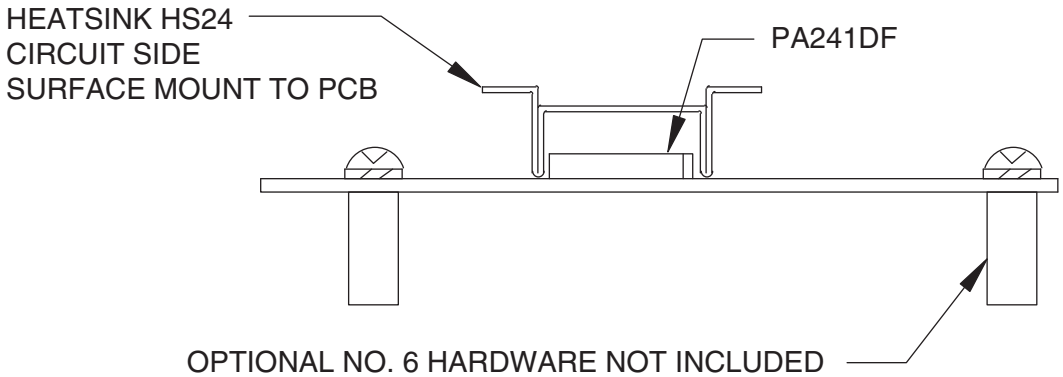
The PA241DF and HS24 should be reflowed to the PCB using a solder reflow furnace. If this is not available, a heat plate capable of solder reflow temperatures may be used. or, though time consuming, the leads may be soldered individually to the PCB with a soldering iron. In this case the use of thermal grease under the heat tab is recommended instead of solder for the thermal connection.

CAUTION High voltages will be present. Use caution in handling and probing when power is applied.

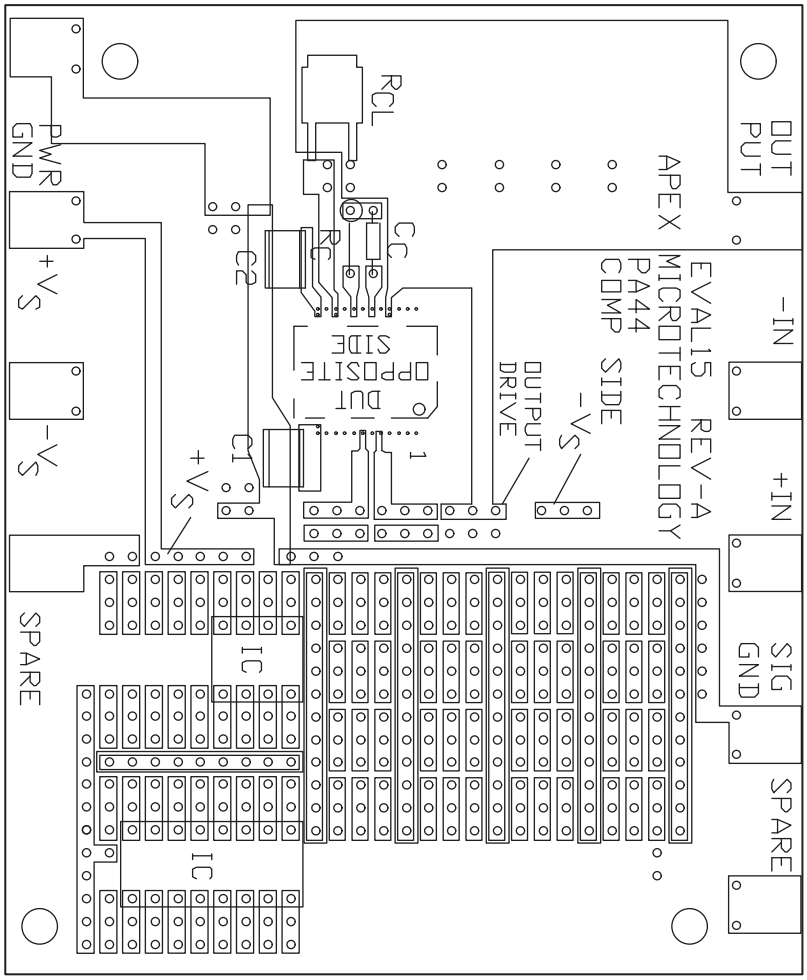
BOTTOM
DUT SIDE



F



TOP
COMP. SIDE



Evaluation Kit for DP Package Op Amps

INTRODUCTION

The EK14 evaluation kit provides a convenient way to breadboard circuits using Apex Precision Power power op amps packaged in the 12-pin SIP03 package. The amplifier may be mounted vertically with the HS20 heat sink, or horizontally. Connections are provided for required power supply bypassing, external compensation components, as well as current limit resistors. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

CAUTION **Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.**

PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL16	PC Board	1
MS06	Mating Socket	1
OX7R105KWN	1µF Ceramic Capacitor	2
CSR10	.15 Ω Resistor	2
TWO7	Thermal Washer	1 package

BEFORE YOU GET STARTED

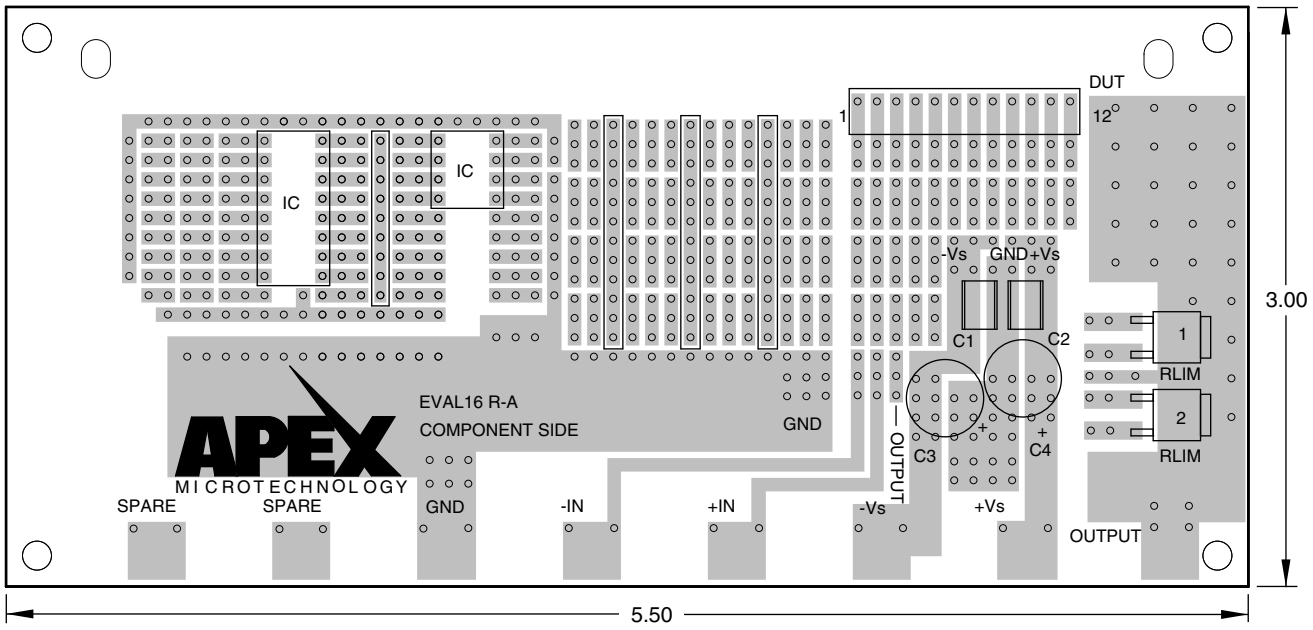
- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

ASSEMBLY

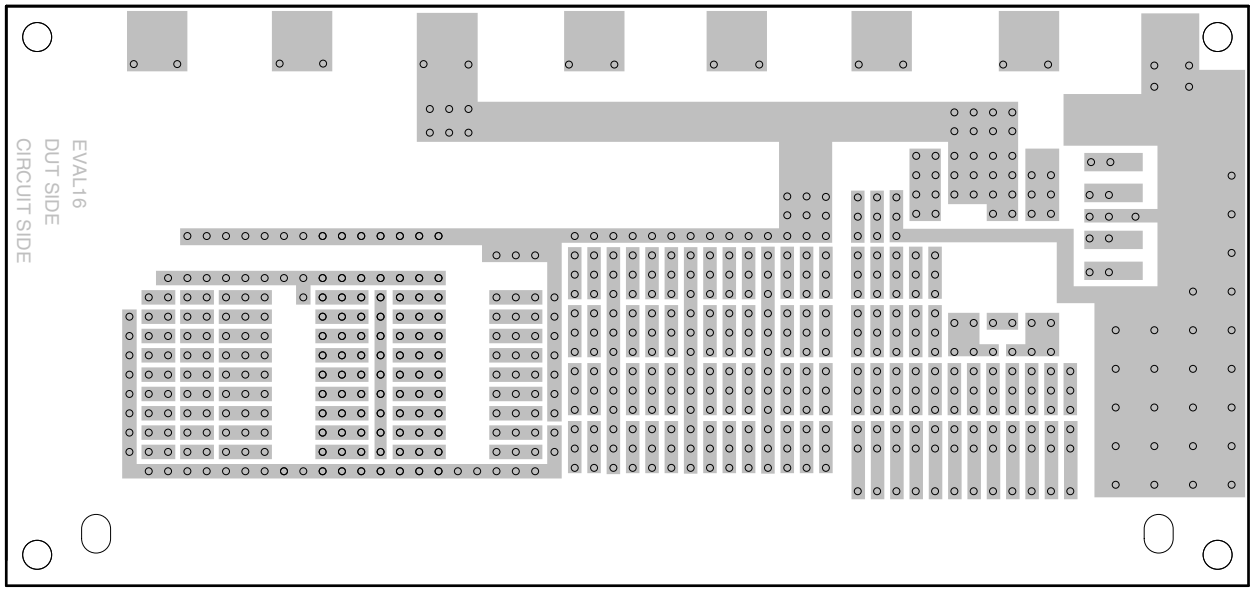
1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1 – 12. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to include proper bypassing, required compensation components and current limit resistors. See the op amp data sheet for help in selecting these components. 1uF capacitors and a .15 Ω resistor have been included with the EK12 kit but may be replaced with other components as necessary.
3. Place the TW07 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20. Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M). Do not over torque.
5. Install leads of the DUT into the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heat sink as shown in the assembly diagram (Figure 1).

FIGURE 1. PCB

TOP SIDE



BOTTOM SIDE



Evaluation Kit for SA08 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA08 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic is shown in Figure 3. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK15 are provided in this kit. Hardware similar to that shown in Figure 1 must be obtained locally.

BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with TW05 washer.
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL19	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
ZX7R105KTL	1µF Cap ST2225B105K501LLXW Novacap	2
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	1
TS01	Terminal Strip 66505 Beau Interconnect	1
EC01	470 µf Cap United Chemi-Con 82DA471M500MG2D	1
HS22	Heatsink Thermolly 6025B	2
CSR03	0.010 ohm resistor Caddock MP916-0.010 - 5%	2
CSR04	0.020 ohm resistor Caddock MP930-0.020 - 5%	2

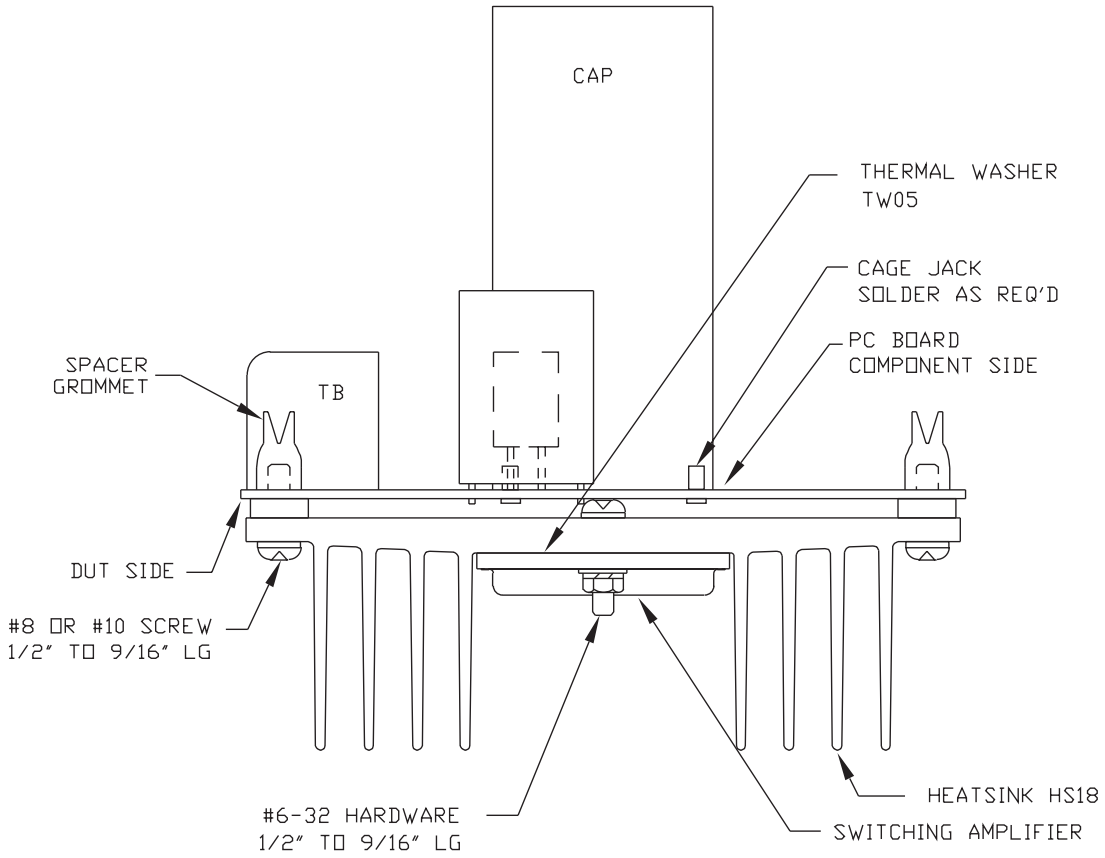


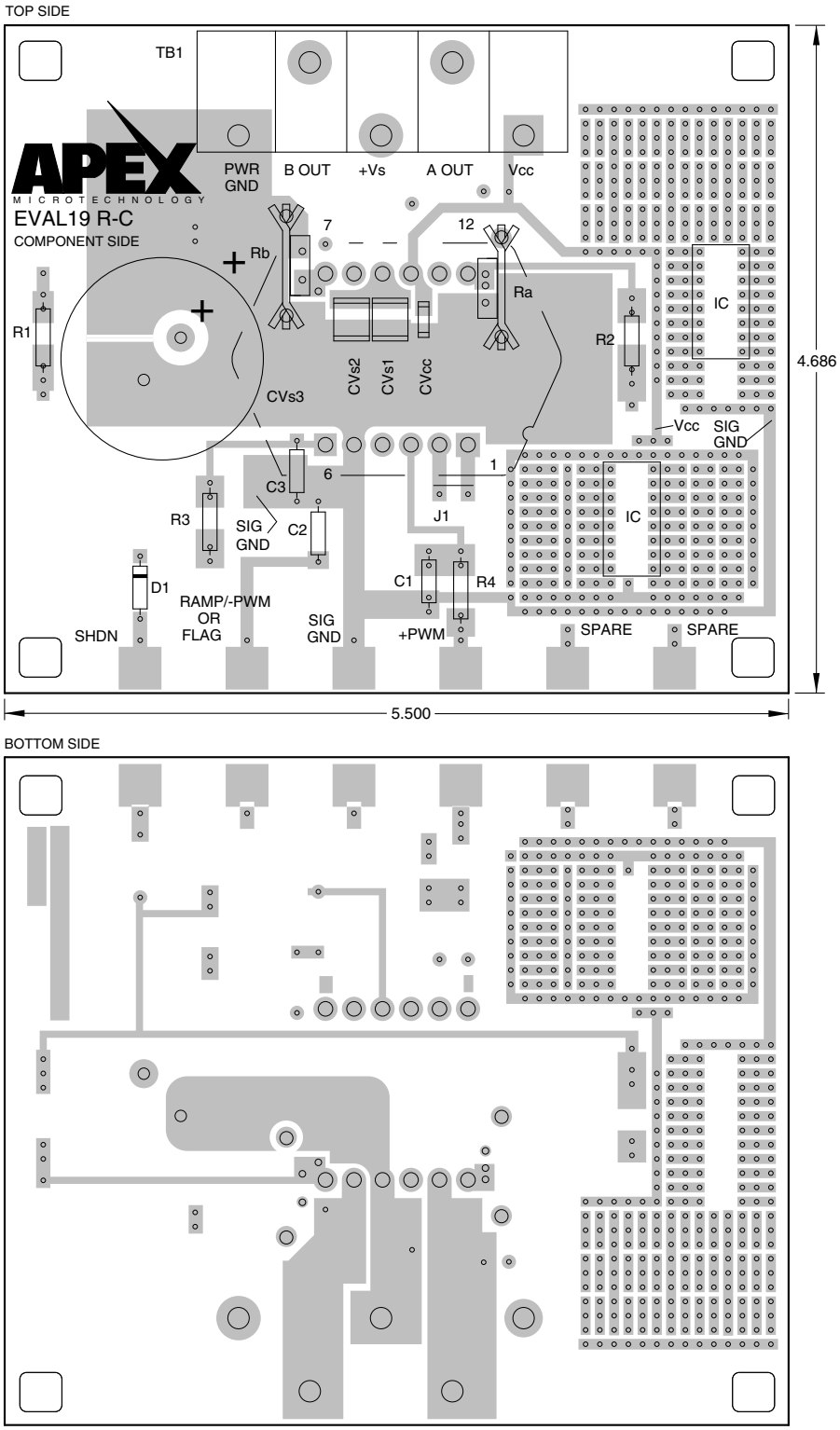
FIGURE 1.

ASSEMBLY

During assembly refer to Figure 1 and Figure 2.

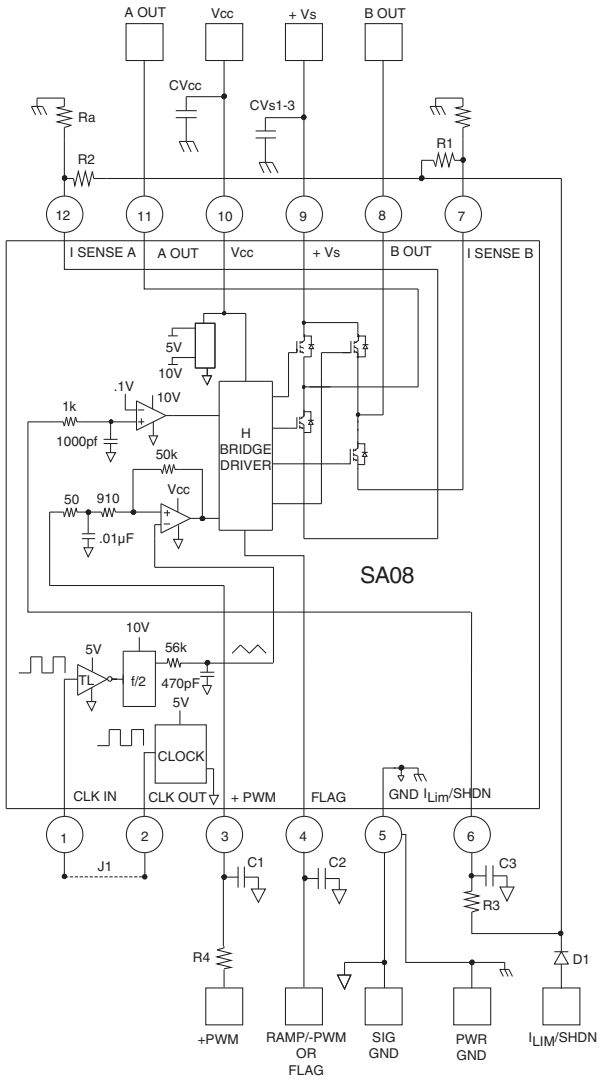
1. From the DUT of the PCB insert and solder the 12 cage jacks. Also solder the cage jacks from the circuit side as well, making sure the cage jack remains flush with the component side of the PCB.
2. Solder the 3 surface mount ceramic capacitors to the component side of the PCB.
3. From the component side of the PCB insert the terminal strip. Solder from the circuit side of the PCB. Be sure that the GND terminal hole in the PCB is fully filled with solder.
4. Two values of current limiting power resistors are supplied. Select one value (see the amplifier data sheet to learn how to calculate which resistor will suit your need). Coat the backside of the power resistor with heat sink compound (not supplied). Using 4-40 screws and nuts (not supplied) mount the resistors to the two small heat sinks supplied. Solder the resistor/heat sink assembly to the component side of the PCB.
5. Insert the electrolytic capacitor into the PCB from the component side and solder from the circuit side making sure to fill the mounting holes with solder.
6. From the circuit side, push spacer grommets into PCB until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
7. Apply TW05 thermal washer to the bottom of the amplifier.
8. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
9. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
10. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to the large pads at the edge of the PCB.
11. Insert amplifier pins into cage jacks and fasten PCB to heatsink.

FIGURE 2. PCB



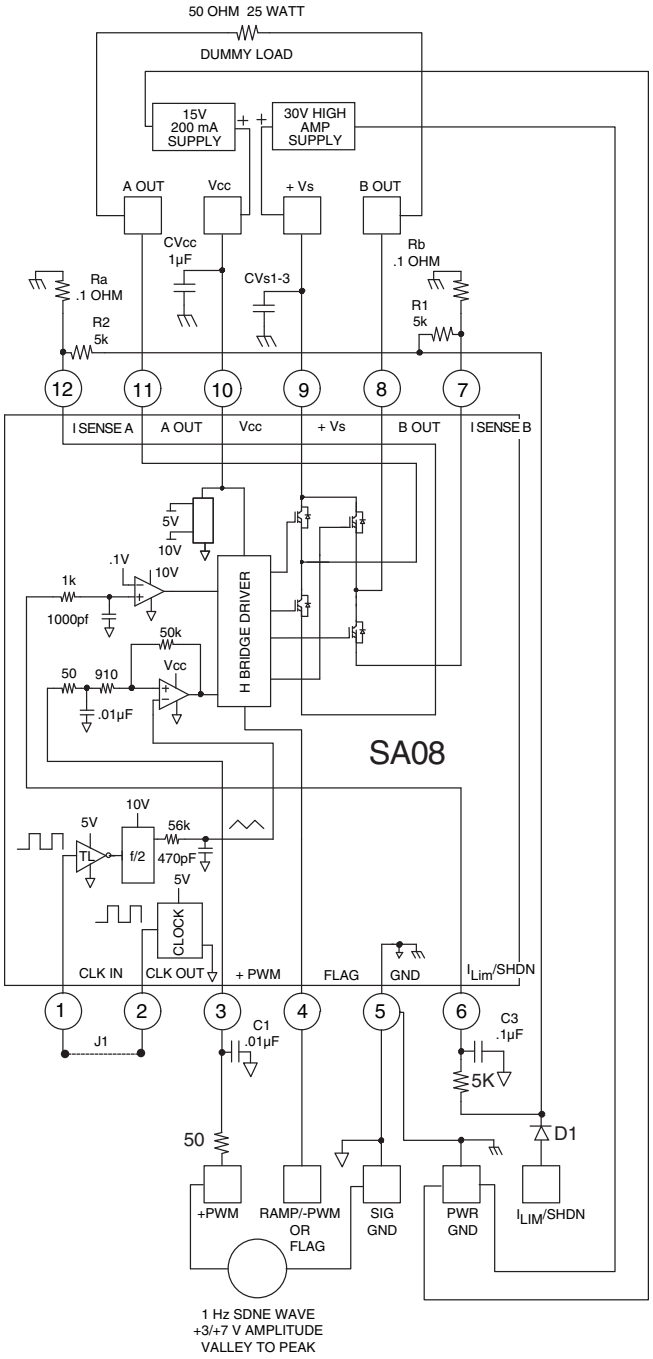
A block diagram of the SA08 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition, a large electrolytic capacitor is included. This capacitor was selected expressly for this evaluation kit and may not be (and likely won't be) suitable for your end application. You will need to select an electrolytic capacitor based on your analysis of the capacitor's ripple current, ripple current tolerance, operating temperature, operating voltage, acceptable service life and acceptable supply ripple. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. PCB SCHEMATIC.



The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

FIGURE 3. FUNCTIONAL TEST CIRCUIT



Evaluation Kit for PA90/PA91/PA92/PA93/PA98 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA90/PA91/PA92/PA93/PA98 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 2.

PARTS LIST

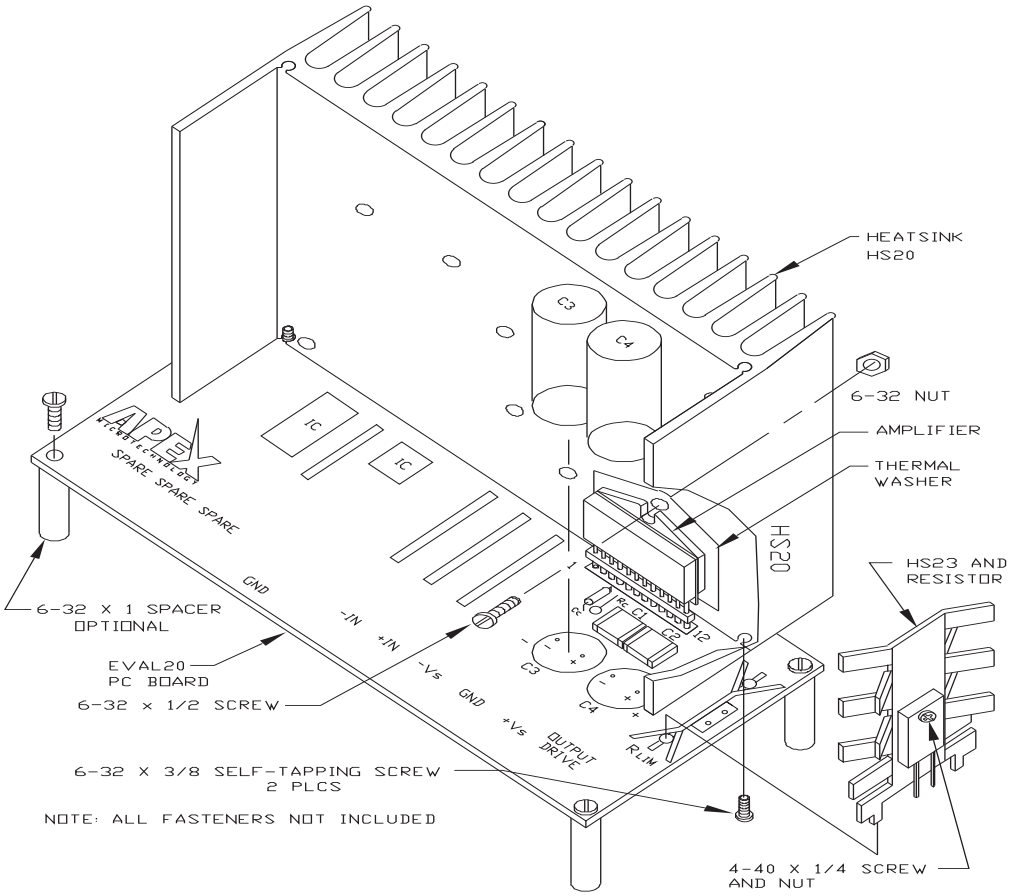
Part #	Description, Vendor	Quantity
HS23	Heatsink, Wakefield 232-200AB	1
HS20	Heatsink, Apex Precision Power	1
MS06	Mating Socket Strip, Apex Precision Power	1 bag, 2 ea.
EVAL20	PC Board, Apex Precision Power	1
TW07	Thermal Washer, Apex Precision Power	1 box, 10 ea.
ZX7R105KTL	Capacitor, NOVACAP ST2225K501LLXW	2
EC02	Capacitor, United Chemicon KME400VB33RM16X31LL	2
CSR05	Resistor, Caddock MP930-0.30 1%	1
CSR06	Resistor, Caddock MP930-0.20 1%	1
CSR07	Resistor, Caddock MP930-0.10 1%	1

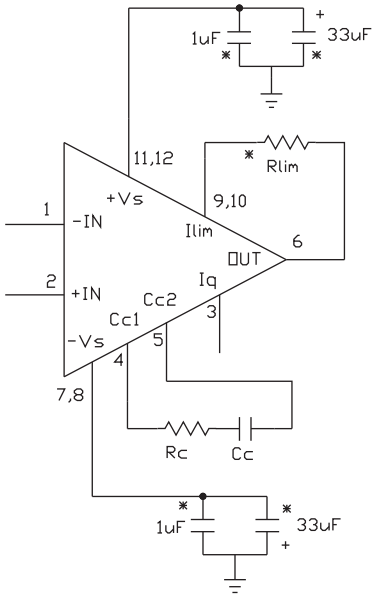
ASSEMBLY

1. See Figure 1. Solder the surface mount ceramic capacitors to the DUT side of the circuit board at C1 and C2.
2. Solder the electrolytic capacitors to the circuit board at C3 and C4. Match the polarity markings on the circuit board with those on the capacitor body.
3. Select a current limiting resistor from the three values provided. See the product data sheet for information on how to select a value. Apply a thin coating of thermal grease to the back of the resistor. Using a 4-40 X 1/4" screw and 4-40 nut, mount the resistor to the lower of the two holes in the small heat sink provided. Solder this assembly to the circuit board at R_{LIM}. After soldering the resistor leads the tabs on the heat sink may be bent with pliers to secure it to the circuit board.
4. Examine the large heat sink. Notice that there are several holes in the face of the heat sink. These are for mounting various Apex Precision Power amplifier models. The circuit board aligns the amplifier with the correct mounting hole once the heat sink is attached to the circuit board. The heat sink can be mounted in either of two positions. One position is used for mounting the amplifier to the heat sink **without** the mating socket strip (the mounting hole of the amplifier is closer to the circuit board). Rotating the heat sink 180 degrees allows mounting the amplifier **with** the mating socket strip (the mounting hole of the amplifier is further from the circuit board).
5. While developing your application circuit you will probably want to use the mating socket strip. Clip off the strip after the 12th position. Insert the strip into the circuit board from the DUT side and solder one pin on the reverse side. Check that the mating socket strip is fully seated against the circuit board then solder the remaining pins. Insert the amplifier fully into the mating socket strip, noting the pin 1 locations on the amplifier and the circuit board.
6. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired. The remaining two slotted holes are for mounting the large heat sink to the DUT side of the circuit board. Temporarily mount the heat sink with 2 #6 X 1/2" self tapping screws from the opposite side of the circuit board. Do not fully tighten the screws at this time. Check for alignment of the slot in the mounting tab of the amplifier with a hole in the heat sink. Dismount and rotate the heat sink if necessary to achieve an alignment with a hole in the heat sink. Position the heat sink so that the back of the amplifier mounting tab is flush with the heat sink then tighten the heat sink mounting screws.

7. Hang the thermal washer near the end of a 6-32 X 1/2" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heat sink. Secure the screw from the opposite side of the heat sink using a nut holder.
8. Add other components as necessary to complete your application circuit.

FIGURE 1.

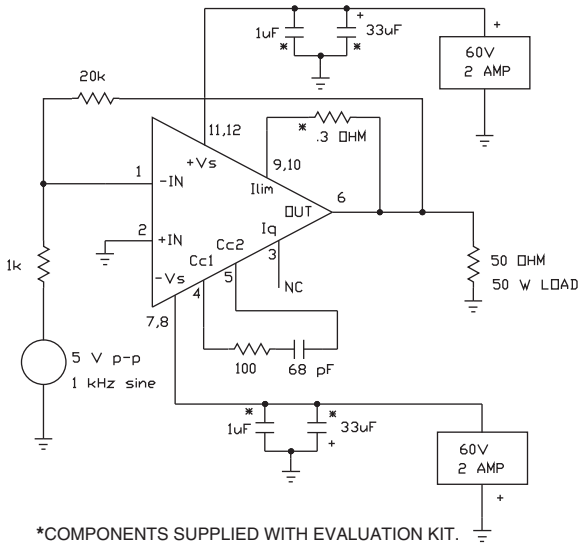




* COMPONENTS SUPPLIED WITH EVALUATION KIT.

FIGURE 2.

Figure 2 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). All other connections are made via the bread-boarding areas of the circuit board.



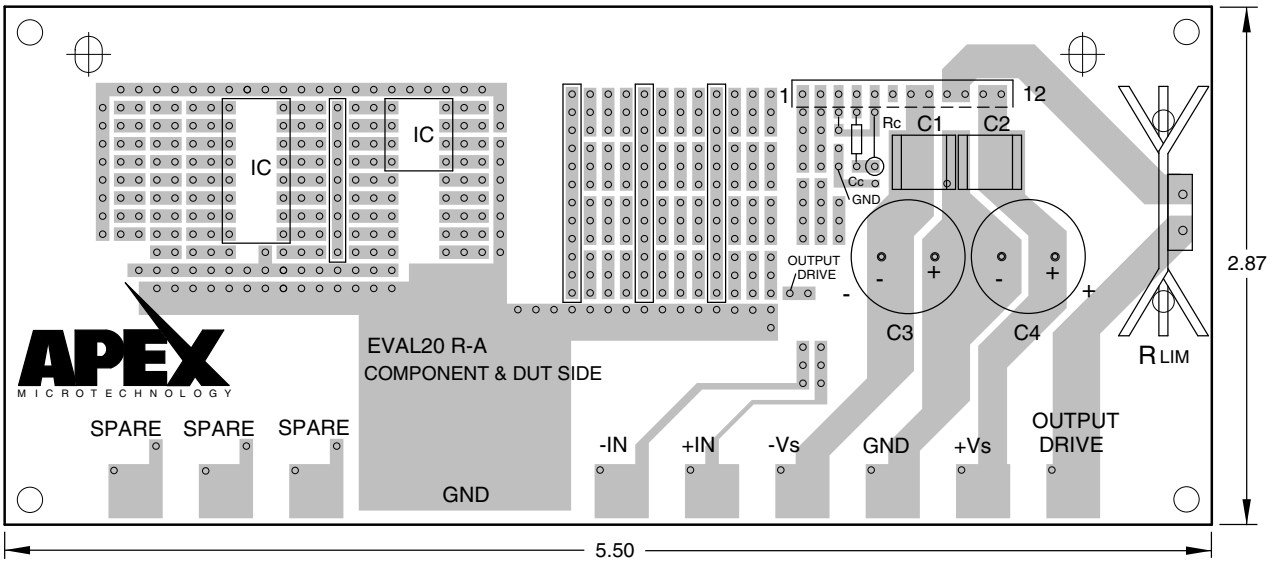
*COMPONENTS SUPPLIED WITH EVALUATION KIT.

FIGURE 3.

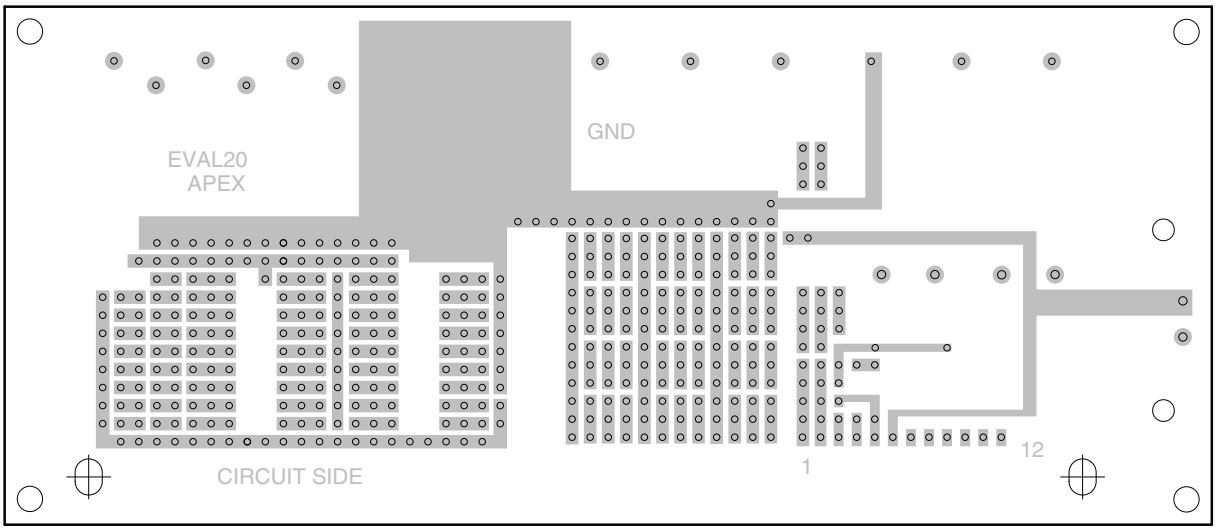
Figure 3 shows a suggested simple test circuit that you can build to gain a familiarity with the evaluation kit as well as the amplifier. At the output (pin 6) you should observe a 100 V p-p sine wave.

FIGURE 4. PCB

TOP SIDE



BOTTOM SIDE



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Evaluation Kit for SA12 PWM Amplifier

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA12 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic is shown in Figure 3. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK17 are provided in this kit. Hardware similar to that shown in Figure 1 must be obtained locally.

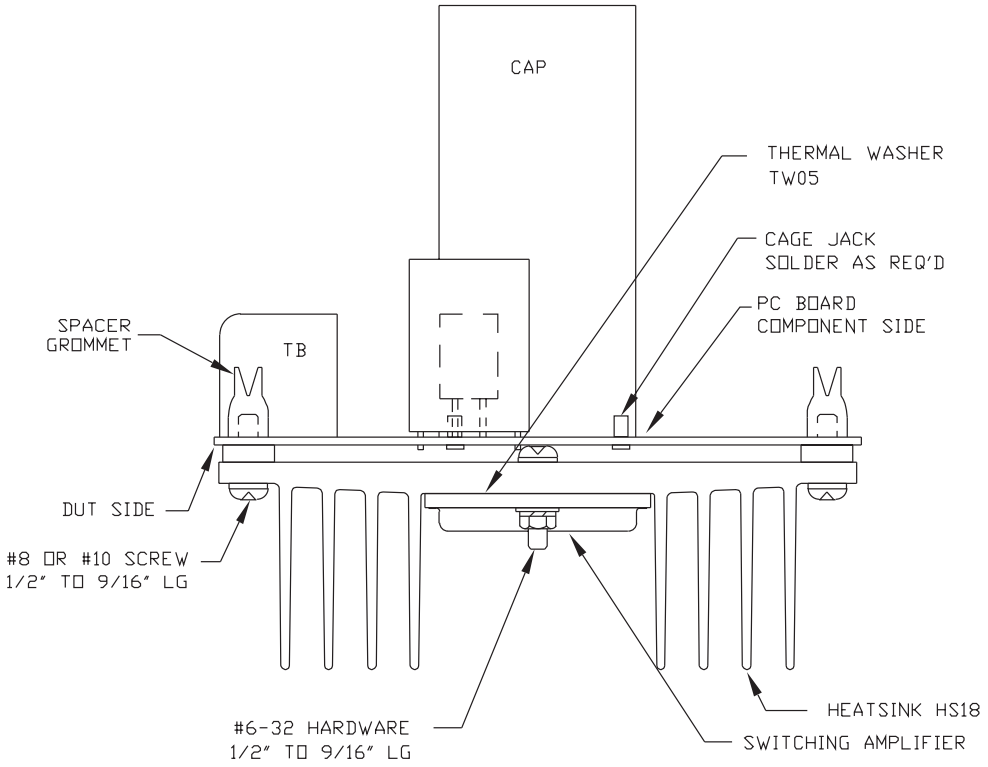
BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with TW05 washer.
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating allowed in the device data sheet.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL19	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	3
TS01	Terminal Strip 66505 Beau Interconnect	1
EC03	680 µf Cap United Chemi-Con KMH200VN68IM25X40T2	1
HS22	Heatsink Thermolly 6025B	2
CSR03	0.01 ohm resistor Caddock MP916-0.010 - 5%	2
CSR04	0.020 ohm resistor Caddock MP930-0.020 - 5%	2

FIGURE 1.

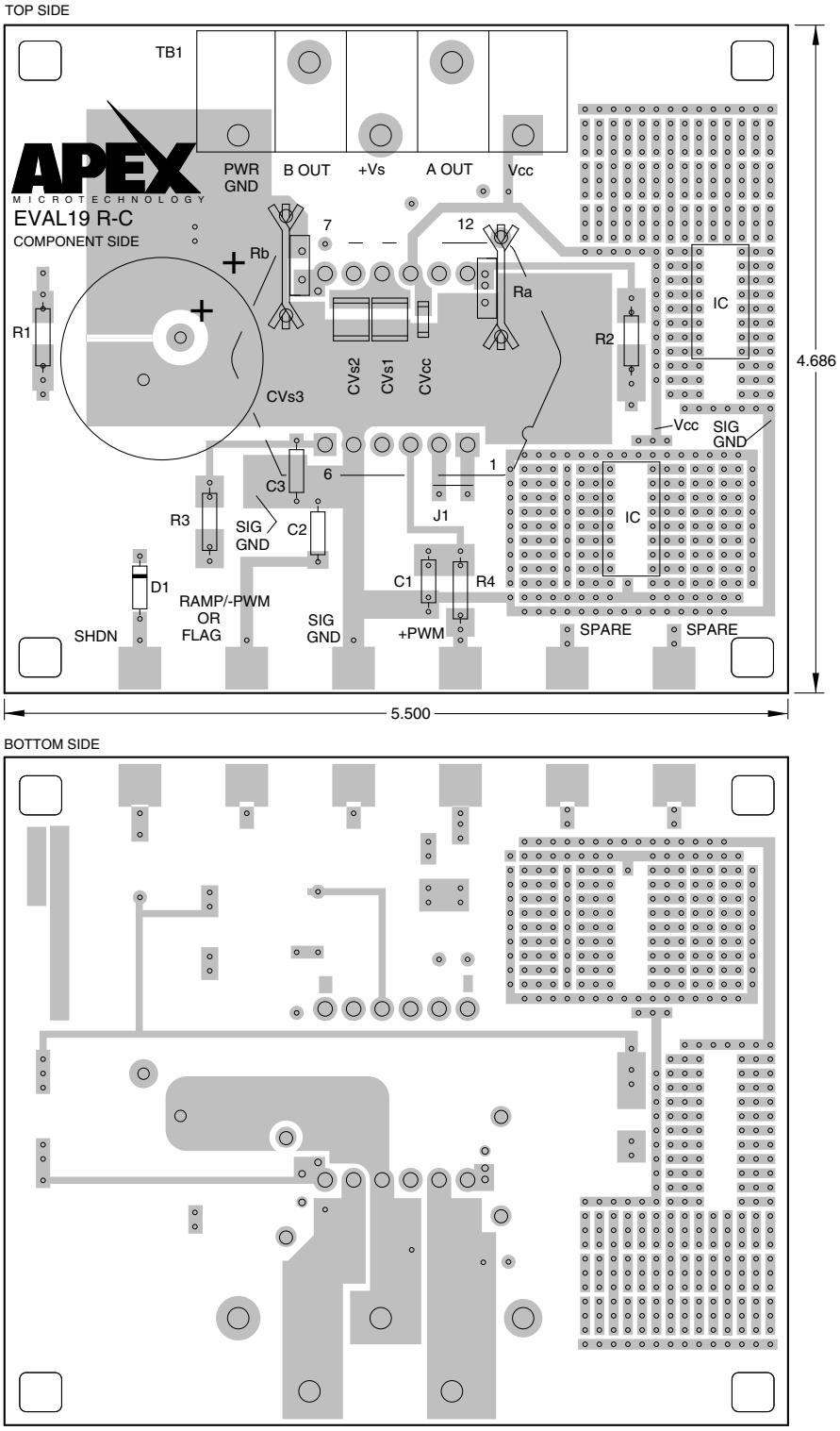


ASSEMBLY

During assembly refer to Figures 1 & 2

1. From the DUT of the PCB insert and solder the 12 cage jacks. Also solder the cage jacks from the circuit side as well, making sure the cage jack remains flush with the component side of the PCB.
2. Solder the 3 surface mount ceramic capacitors to the component side of the PCB.
3. From the component side of the PCB insert the terminal strip. Solder from the circuit side of the PCB. Be sure that the GND terminal hole in the PCB is fully filled with solder.
4. Two values of current limiting power resistors are supplied. Select one value (see the amplifier data sheet to learn how to calculate which resistor will suit your need). Coat the backside of the power resistor with heat sink compound (not supplied). Using 4-40 screws and nuts (not supplied) mount the resistors to the two small heat sinks supplied. Solder the resistor/heat sink assembly to the component side of the PCB.
5. Insert the electrolytic capacitor into the PCB from the component side and solder from the circuit side making sure to fill the mounting holes with solder.
6. From the circuit side, push spacer grommets into PCB until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
7. Apply TW05 thermal washer to the bottom of the amplifier.
8. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
9. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
10. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to the large pads at the edge of the PCB.
11. Insert amplifier pins into cage jacks and fasten PCB to heatsink.

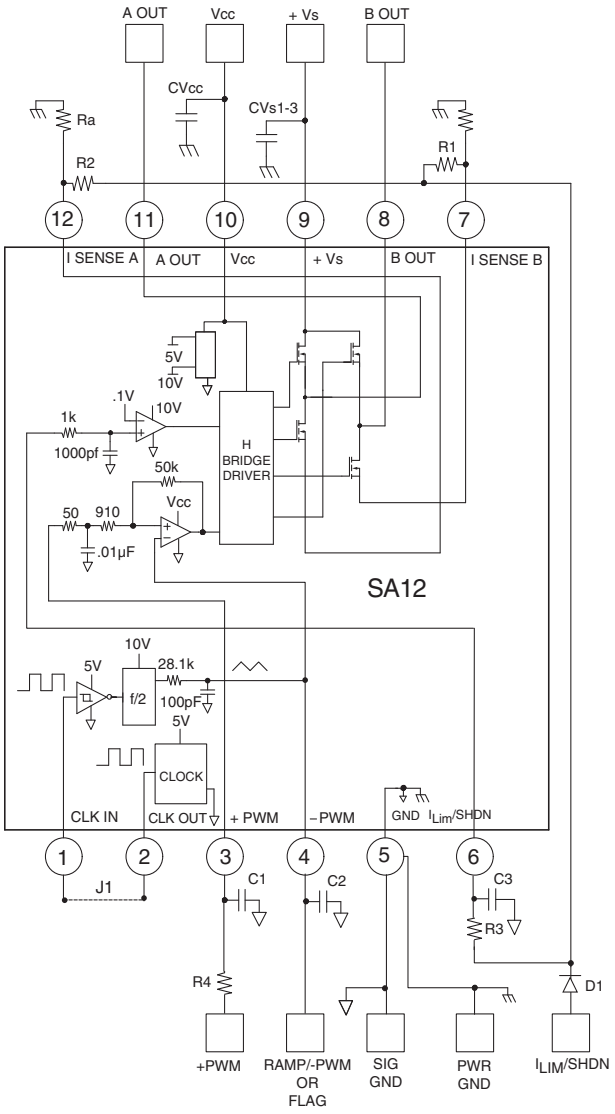
FIGURE 2. PCB



F

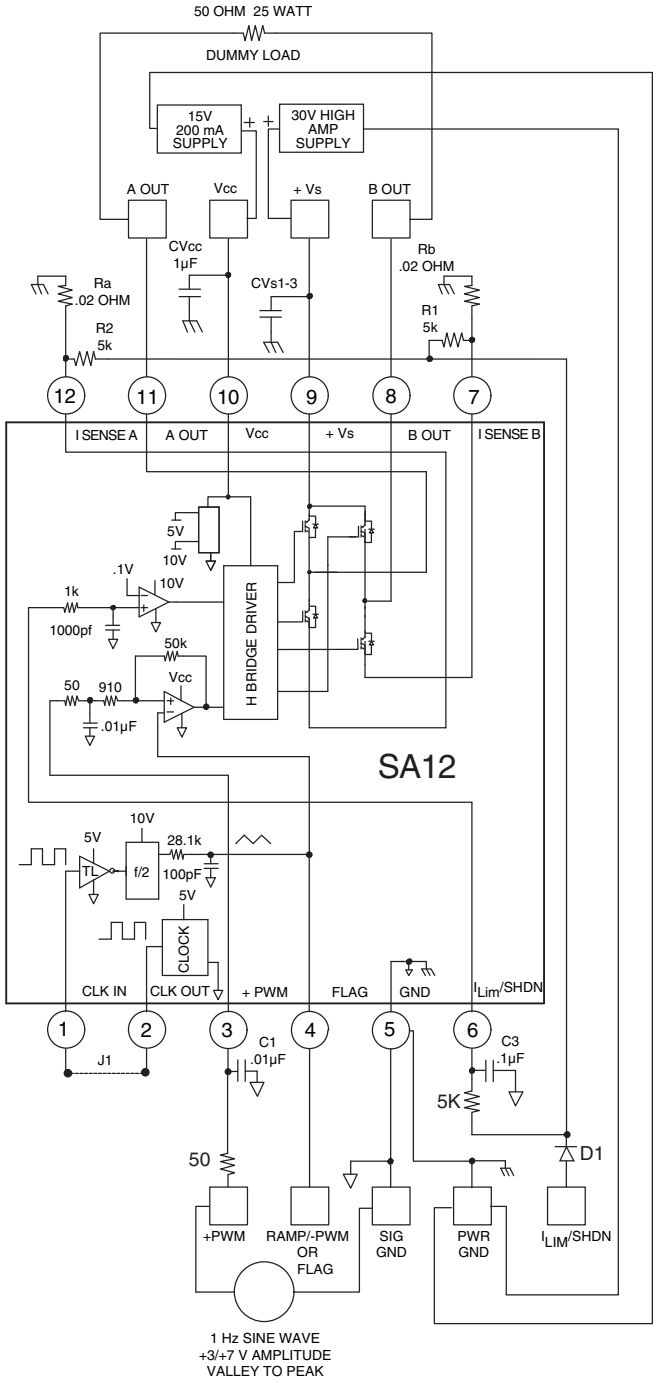
A block diagram of the SA12 is shown in Figure 3 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition, a large electrolytic capacitor is included. This capacitor was selected expressly for this evaluation kit and may not be (and likely won't be) suitable for your end application. You will need to select an electrolytic capacitor based on your analysis of the capacitor's ripple current, ripple current tolerance, operating temperature, operating voltage, acceptable service life and acceptable supply ripple. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. PCB SCHEMATIC.



The schematic of Figure 4 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 10 amps.

FIGURE 4. FUNCTIONAL TEST CIRCUIT



Evaluation Kit for PA94, PA95

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA94/PA95 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 1.

PARTS LIST

Part #	Description, Vendor	Quantity
HS27	Heatsink, Apex Precision Power	1
EVAL23	PC Board, Apex Precision Power	1
TW13	Thermal Washer, Apex Precision Power	1 box, 10 ea.
P6KE440A	TransZorb, General Semiconductor (440V)	2
CDC01	Capacitor .01µF 1kV, Sprague 5GAS10	2

ASSEMBLY

1. See Figures 2 & 3. Insert and solder the TransZorb diodes at D3 and D4 (440V).
2. Insert and solder the disc bypass capacitors at C1 and C2.
3. Insert the HS27 heatsink and solder the solderable studs from the opposite side of the PCB.
4. Add banana jacks as necessary to complete connections to external circuits and power supplies.
5. Insert the amplifier into the PCB mounting holes located in the space between the heatsink fins. So not solder the pins at this time.
6. Hang the TW13 thermal washer near the end of a 6-32 X 3/8" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heatsink. Use a 6-32 nut to secure the screw from the opposite side of the heatsink. It is important that the entire back surface of the amplifiers mounting tab be in contact with the heatsink. Adjust the amplifiers position and tighten the mounting screw as necessary for this to be so.
7. Solder the amplifiers pins to the PCB.
8. Add other passive components as necessary to complete your circuit.
9. Most common configurations will ground the non-inverting pin of the amplifier. J1 is a convenient way to do this if necessary for your application circuit.
10. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
11. R1-R5 are multiple feedback resistors in series. Commonly available resistors do not have a breakdown voltage sufficient to stand off the output voltage of the amplifier. Using multiple resistors will divide down the voltage that each resistor must withstand.

FIGURE 1.

Figure 1 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). See the amplifiers data sheet for full application information.

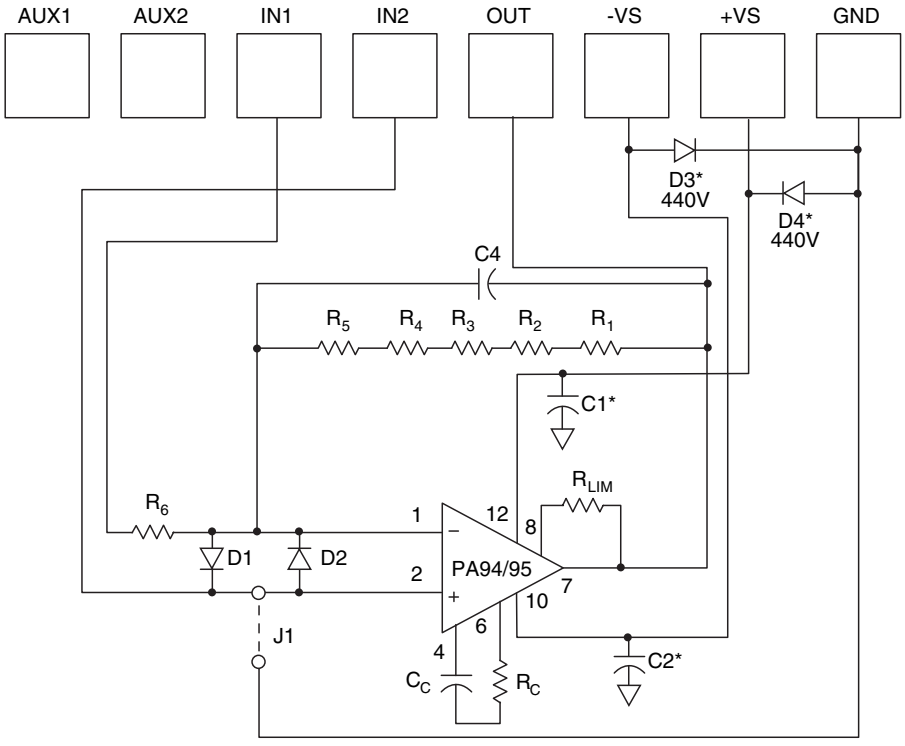
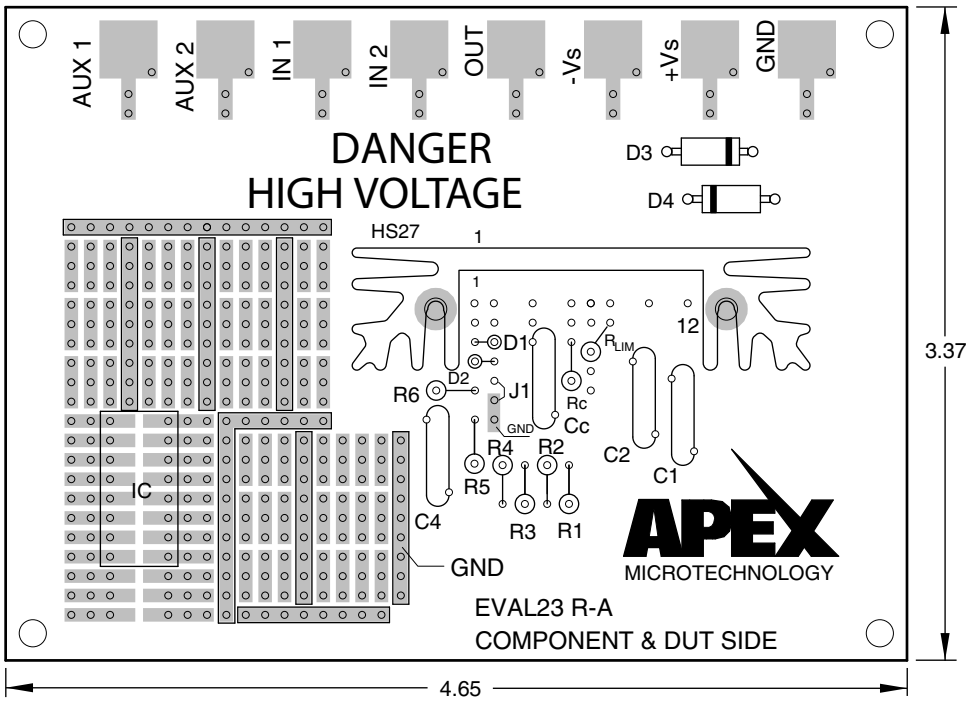
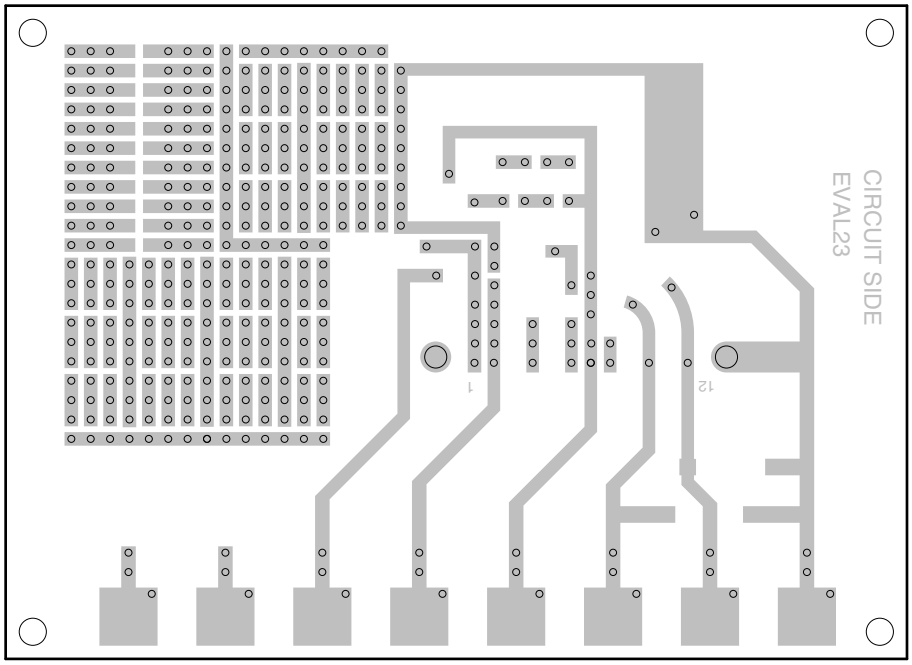


FIGURE 2. PCB

TOP SIDE



BOTTOM SIDE



Evaluation Kit for PA74 Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of power op amps that use the PA74 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations. In addition, it is flexible enough to do most standard amplifier test configurations.

The schematic for 1/2 of the PC board is shown in Figure 2. The schematic for the other half is identical except part reference designators are primed (i.e. R1 = R1'). Note that all of the components shown on the schematic will probably not be used for any single circuit. The component locations on the PC board (See Figure 3) provide maximum flexibility for a variety of configurations. Also included are loops for current probes as well as connection pads on the edge of the PC board for easy interconnects.

The hardware required to mount the PC board and the device under evaluation to the heatsink are included in the kit. Because of the limitless combination of configurations and component values that can be used, no other parts are included in this kit. However, generic formulas and guidelines are included in the Apex Precision Power DATABOOK and this evaluation kit documentation.

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions!
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Always use the heatsink included in this kit with thermal grease or a TW03 and torque the part to the specified 4-7 in-lbs (.45-.79 N•M).
- Do not change connections while the circuit is under power.
- Never exceed any of the absolute maximums listed in the device data sheet.
- Always use adequate power supply bypassing.
- Remember that internal power does not equal load power.
- Do not count on internal diodes to protect the output against sustained, high frequency, high energy kickback pulses.

PARTS LIST

Part #	Description	Quantity
HS11	Heatsink	1
EVAL02	PC Board	1
MS03	Mating Socket	2
HWRE01	Hardware Kit	1
TW03	Thermal Washer	1 Box/10

HWRE01 contains the following:

4	#8 Panhead Screw	4	#6 x 1.25" Panhead Screw
4	#8 .375" Hex Spacer	4	#6 x 5/16" Hex Nut
4	#8 1.00" Hex Standoff	2	#6 x 1/4" Hex Nut

ASSEMBLY HINTS

The mating sockets included with this kit have recessed nut sockets for mounting the device under evaluation. This allows assembly from one side of the heatsink, making it easy to swap devices under evaluation. The sizes of the stand-offs were selected to allow proper spacing of the board-to-heatsink and allow enough height for components when the assembly is inverted.

ASSEMBLY

1. Insert a #6 x 5/16" hex nut in each of the nut socket recesses located on the bottom of the mating socket.
2. Insert the socket into the pc board until it is firmly pressed against the ground plane side of the pc board.
3. Solder the socket in place (see Figure 1). Be sure the nuts are in the recesses prior to soldering.
4. Mount the PC board assembly to the heatsink using the stand-offs and spacers included.
5. Apply thermal grease or a TW03 to the bottom of the device under evaluation. Insert into the mating socket through the heatsink.
6. Use the #6 x 1.25" panhead screws to mount the amplifier to the heat sink. Do not overtorque. Recommended mounting torque is 4-7 in-lbs (.45-.79 N•M).

Mounting precautions, general operating considerations, and heatsinking information may be found in the Apex Precision Power DATA BOOK.

NOTE: Refer to HS11 Heatsink in Accessories section

Figure 1

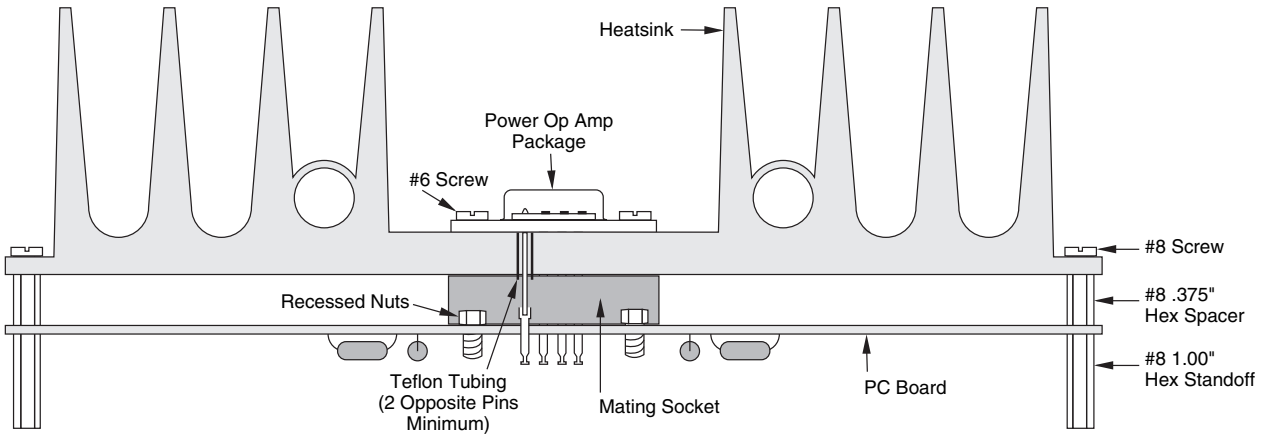
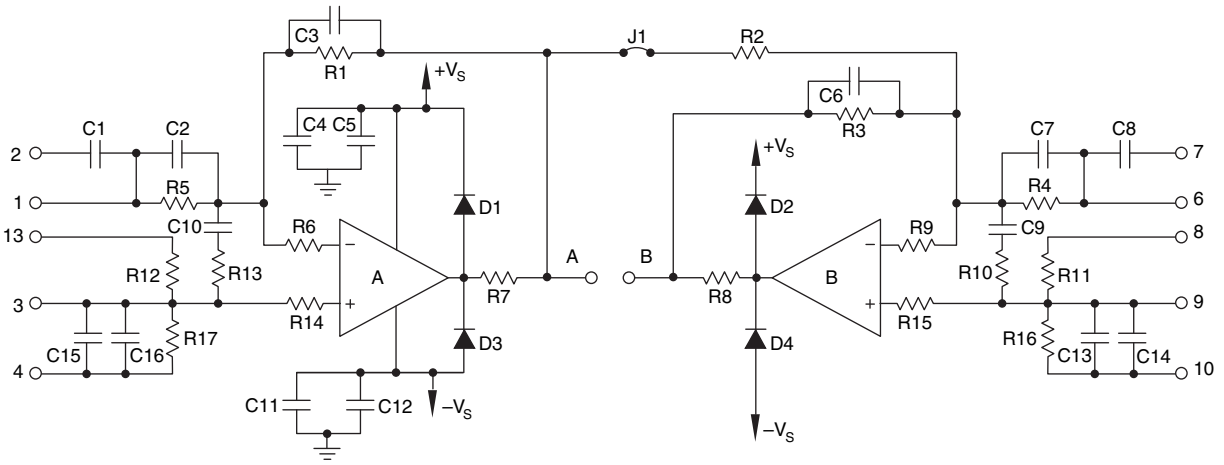


Figure 2

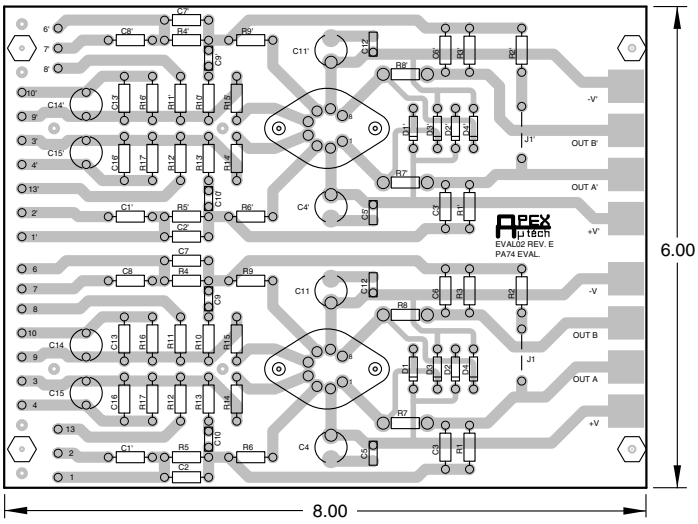


TYPICAL COMPONENT FUNCTIONS

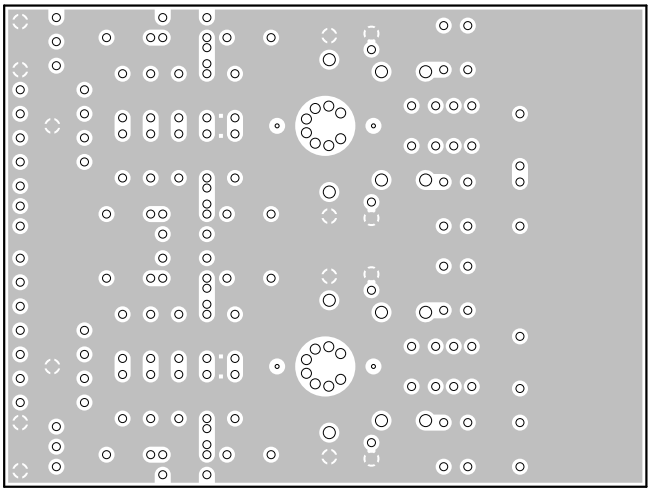
COMPONENT	FUNCTION
R1	Feedback resistor, A side
R2	Input resistor, B side, bridge mode
R3	Feedback resistor, B side
R4	Input resistor, B side
R5	Input resistor, A side
R6	Input bias current measurement (Note 4)
R7	Output current sense resistor or loop for current probe
R8	Output current sense resistor or loop for current probe
R9	Input bias current measurement (Note 4)
R10	Noise gain compensation (Note 1)
R11	Resistor divider network for single supply bias (Note 2)
R12	Resistor divider network for single supply bias (Note 2)
R13	Noise gain compensation (Note 1)
R14	Input bias current measurement
R15	Input bias current measurement
R16	Resistor divider network for single supply bias (Note 2)
R17	Resistor divider network for single supply bias (Note 2)
C1	Input coupling
C2	AC gain set
C3	AC gain or stability (Note 1)
C4	Power supply bypass
C5	Power supply bypass
C6	AC gain or stability (Note 1)
C7	AC gain set
C8	Input coupling
C9	Noise gain compensation (Note 1)
C10	Noise gain compensation (Note 1)
C11	Power supply bypass (Note 3)
C12	Power supply bypass (Note 3)
D1,2,3,4	Flyback protection (Note 5)
C13-16	Bias node noise bypass (Note 2)

Figure 3.

TOP SIDE



BOTTOM SIDE



BRIDGE MODE OPERATION

There are two types of bridge mode operation that will be covered in this section; dual (or split) supply and single supply. The PA74 is well suited for both types of bridge mode operation. If another vendor's pin compatible part is to be compared to the PA74, a close look at output swing and input common mode range is in order. The features that make the PA74 an excellent choice for bridge operation are not included in most other amplifiers. A lack of common mode range may cause permanent damage to other pin compatible parts and the inability of other amplifiers to swing close to the supply rails may cause a lack of available output voltage at the load as well as increase internal dissipation.

The circuit shown in Figure 4 is a dual supply bridge using the "master-slave" configuration. Resistors R 6,7,8,9,14,15 and J1 should be shorts. The available output voltage swing is Vss–(2*Vsat). If operating a PA74A at 3 Amps and 30 Volts total supply this translates to:

$$V_{AB}(max) = 30–(2*3.5) = 23$$

Of course this 23 volts may be applied in either direction across the load. To set the gain of the circuit you must determine the desired voltage across the load at Vin = full scale. Inserting these values into the following equation will yield the ratio of R1 to R5.

$$(V_{AB}/(2*Vin)) = R1/R5$$

The values of R 1,2,3, and 5 should be chosen such that input bias current will not cause an error voltage that is unacceptable. Set R2 equal to R3 to configure the slave amplifier as a unity gain inverter.

Figure 5 shows a typical single supply bridge circuit for an AC coupled input signal. DC coupled inputs may require a different topology to accommodate proper gain and offset terms for a desired transfer function.

The gain and output voltage capability for the single supply bridge are determined the same way as the dual supply bridge (see AN#2). The difference is the bias requirement for the slave amplifier. The noninverting input of the slave amplifier should be biased at mid supply, and must be bypassed.

Figure 4
Dual Supply Bridge

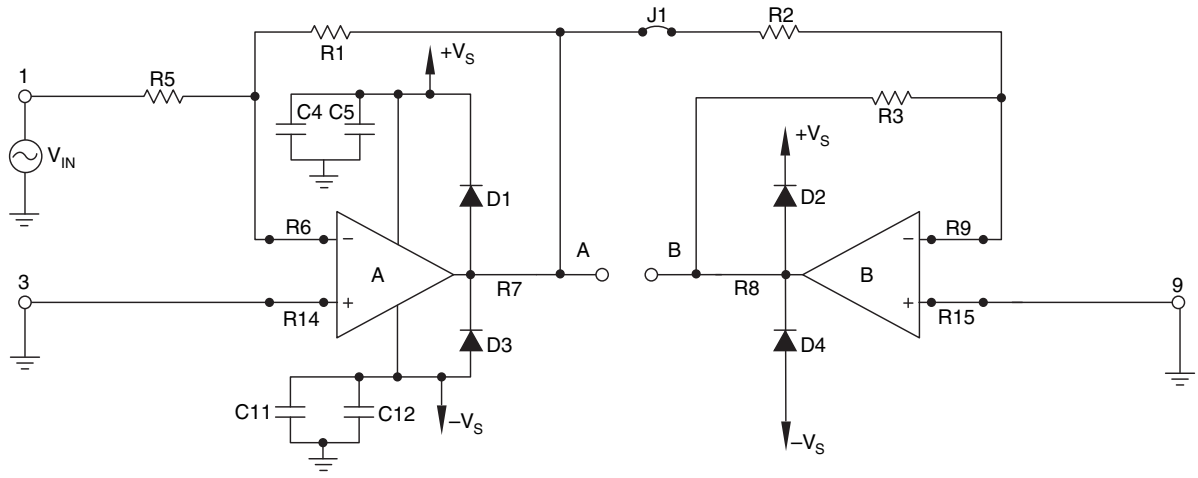
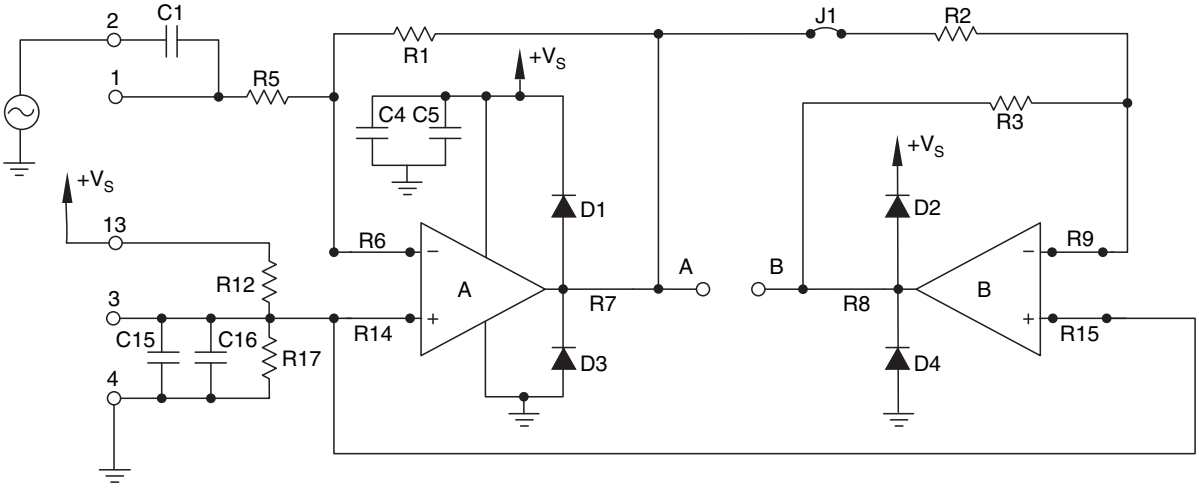


Figure 5
Single Supply Bridge



HS11 HEATSINK NOTE

The HS11 Heatsink is provided in this evaluation kit to **guarantee** adequate **thermal** design through heat removal from the part under evaluation. Once maximum power dissipation for the application is determined (refer to “General Operating Considerations” and Application Note 11 in the Apex Precision Power DATA BOOK), the final mechanical design will probably require substantially less heatsinking.

Apex Precision Power makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

NOTES: Refer to the following sections of the Apex Precision Power DATA BOOK as noted.

1. See Stability section of “General Operating Considerations.”
2. See “Gen. Operating Considerations,” and AN3 “Bridge Circuit Drives.”
3. See Power Supplies section of “General Operating Considerations.”
4. See “Parameter Definitions and Test Methods.”
5. See Amplifier Protection section of “Gen. Operating Considerations.”

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Evaluation Kit for PA60EU Pin-Out

INTRODUCTION

Fast, easy breadboarding of circuits using the PA60EU are possible with the PB80 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. The amplifier may be mounted horizontally or vertically. Components are labeled on both sides of the board for ease in probing.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually be necessary:

C5,C8 Power supply bypasses **MUST** be used. Usually ceramic types of 0.01 to 1.0µF.
C2, C9 Power supply bypass. Suggest 10µF per ampere of output current.
R1 Feedback resistor.
R3 Input resistor.
R8, C10 Snubber network.
R4, C7 Noise gain compensation. Necessary only occasionally, see Application Notes 19 and 25.

The following locations should be jumpered unless used (their most common anticipated function is listed).

R2, R10 Input protection.
CR1 V_{BOOST}.
R5, R6, R9 Output current sense.

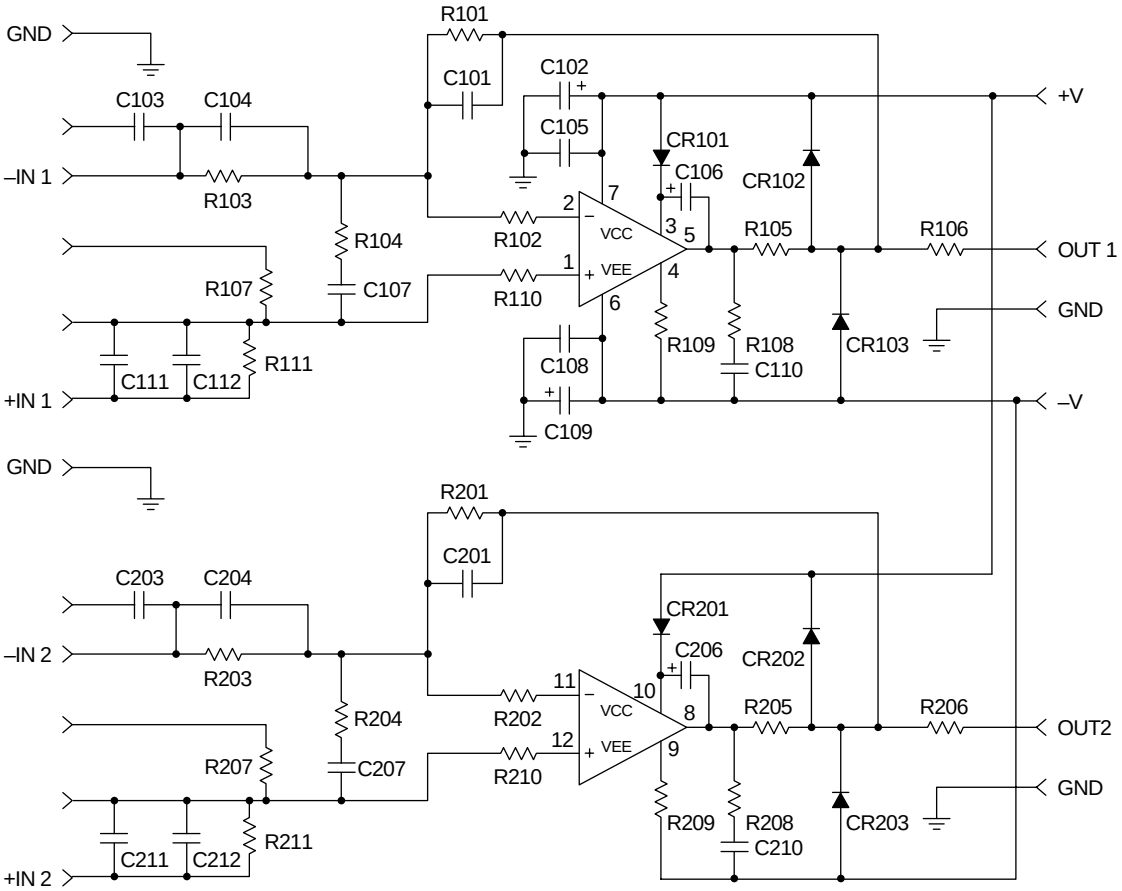
The function of any other components is up to the designer's needs and imagination.

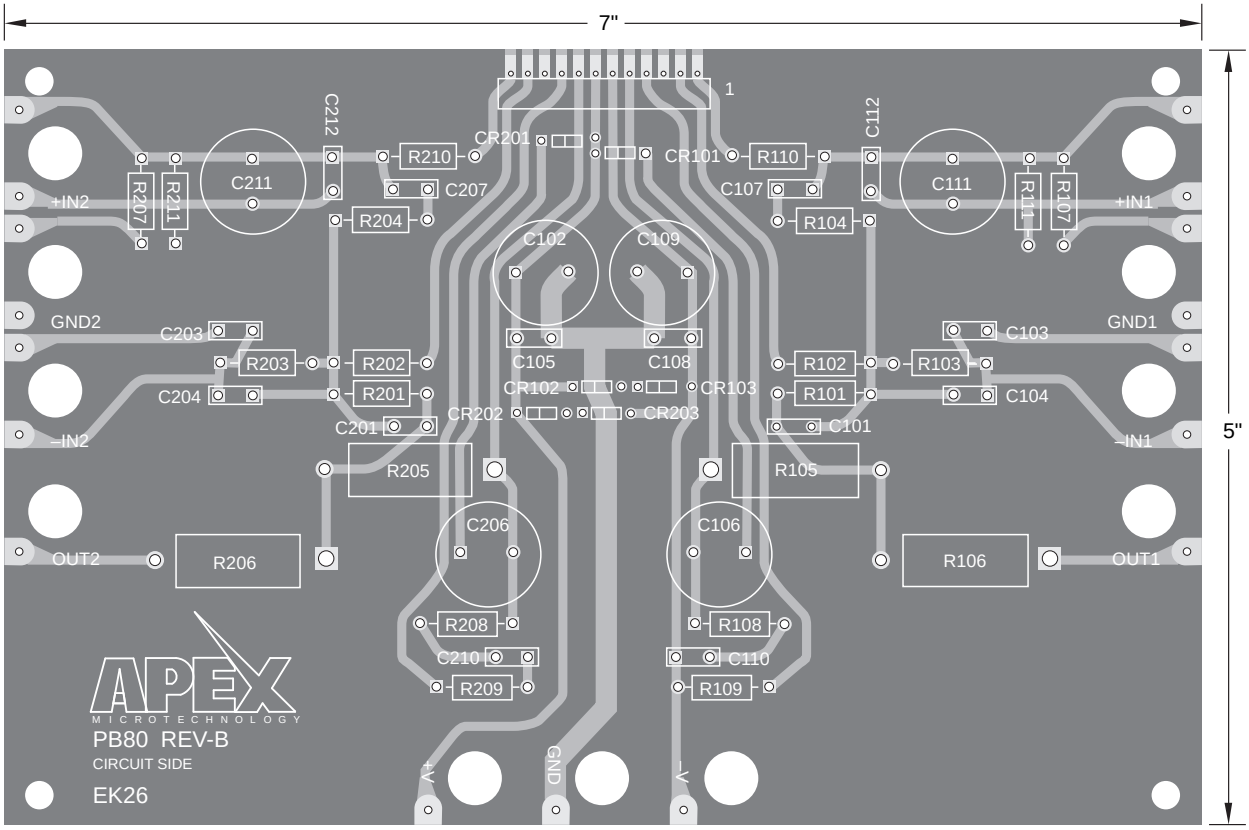
PA60EU CONSIDERATIONS:

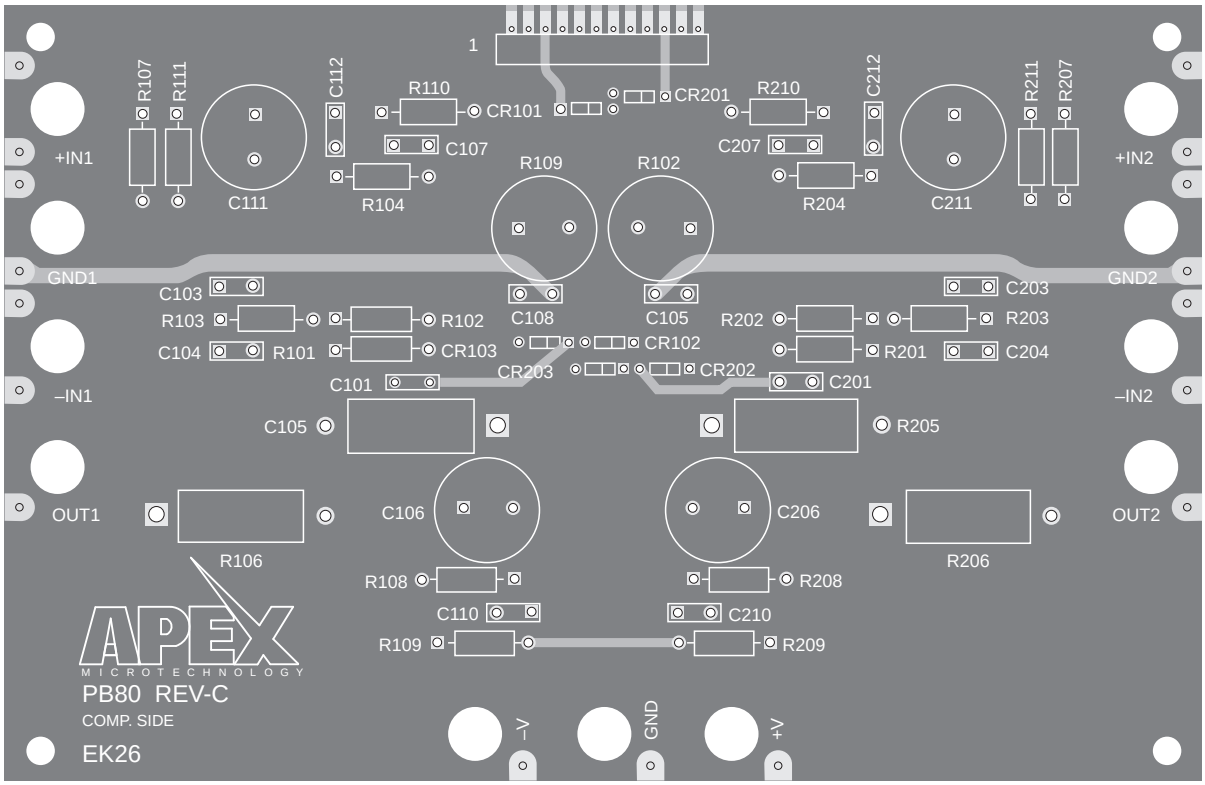
When using the EK26 for the PA60EU the following components on the schematic below must be left either shorted or open:

Short: R109, R209
Open: CR101, C106, CR201, C206

EQUIVALENT SCHEMATIC







NOTE: Illustration only, not to scale.

Evaluation Kit for PA50, PA52 Power Op Amps

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA50/PA52 pin out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal block and terminal pads at the edges of the circuit board. The terminal pads are suitable for soldering standard banana jacks or direct soldering of wires. The schematic is shown in Figure 2.

BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL29	PC Board	1
60SPG00001	Spacer Grommets	4
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	6
TS02	Terminal Strip Beau Interconnect 66507	1
TWO5	Thermal Washer	1 Box/12 each
EC05	2200 µf Cap 100V United Chemi-Con 82DA222M100KC2D	2
EC03	680µF 200V United Chemi-Con KMH200VN681M25X40T2	2

ASSEMBLY

During assembly refer to Figure 1

1. Note that each circuit board side is identified. From the circuit side of the circuit board (not the component side) insert and solder cage jack MS04 at pins 1-12. Be sure that the cage jack sits flush with the surface of the circuit board.
2. Solder the surface mount ceramic capacitors to the component of the circuit board at C3-C7.
3. Mount the electrolytic capacitors at C1 and C2 from the component side of the circuit board and solder from the circuit side of the circuit board. Note polarity and be sure to fill the holes with solder. Use correct voltage capacitor for your application.
4. Mount the terminal strip TS02 to the component side of the circuit board. Make sure the terminal strip sits flat against the circuit board and be sure to fill the holes with solder.
5. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
6. Add other components to complete your circuit design. Note that the solder terminals labeled 2 and 3 are left for you to connect to the amplifier via the components that you will add for your particular design.
7. Push the four nylon spacers into the circuit board from the circuit side of the circuit board at the four corner locations.
8. Apply TW05 thermal washer to the bottom of the PA50. Mount the amplifier to the HS18 heat sink provided and loosely attach with #6 screw and nut.
9. Place the assembled circuit board over the pins of the amplifier making sure that the pin 1 location on the circuit board matches up with pin 1 of the amplifier. Insert the pins of the amplifier into the circuit board mating cage jacks.
10. Mount the circuit board assembly to the heat sink with #6 self tapping or sheet metal screws at the four corners of the heat sink.
11. Tighten the screws that mount the amplifier to the heat sink via the access holes in the circuit board.

F

FIGURE 1.

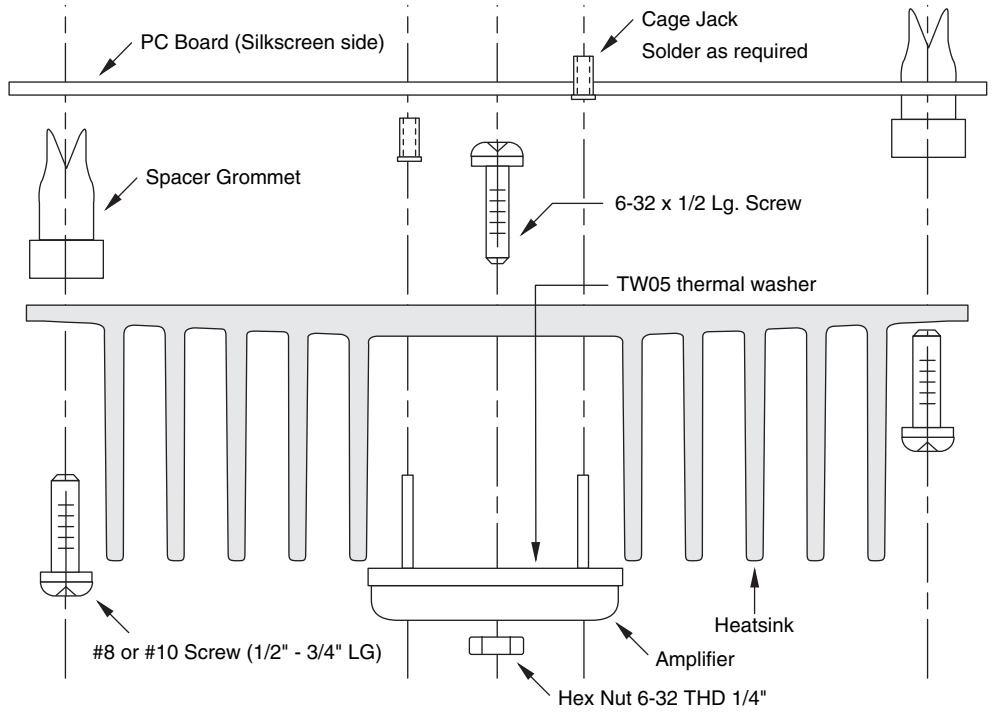


FIGURE 2. PCB SCHEMATIC.

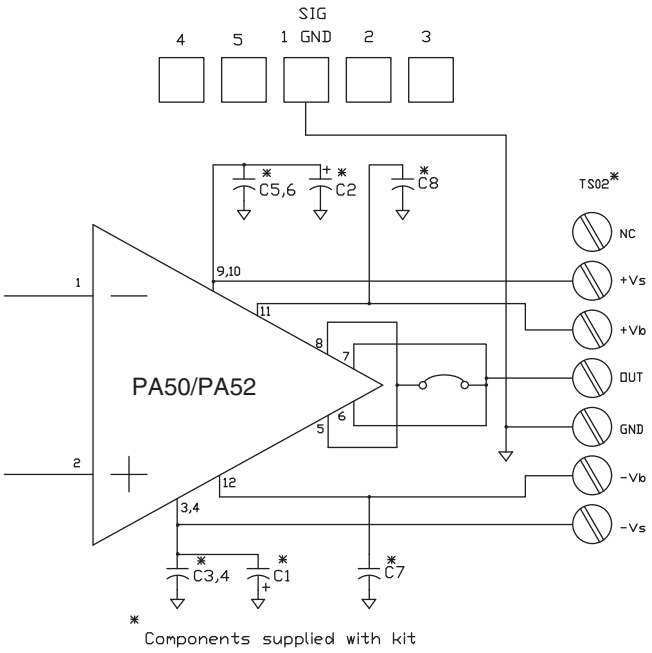
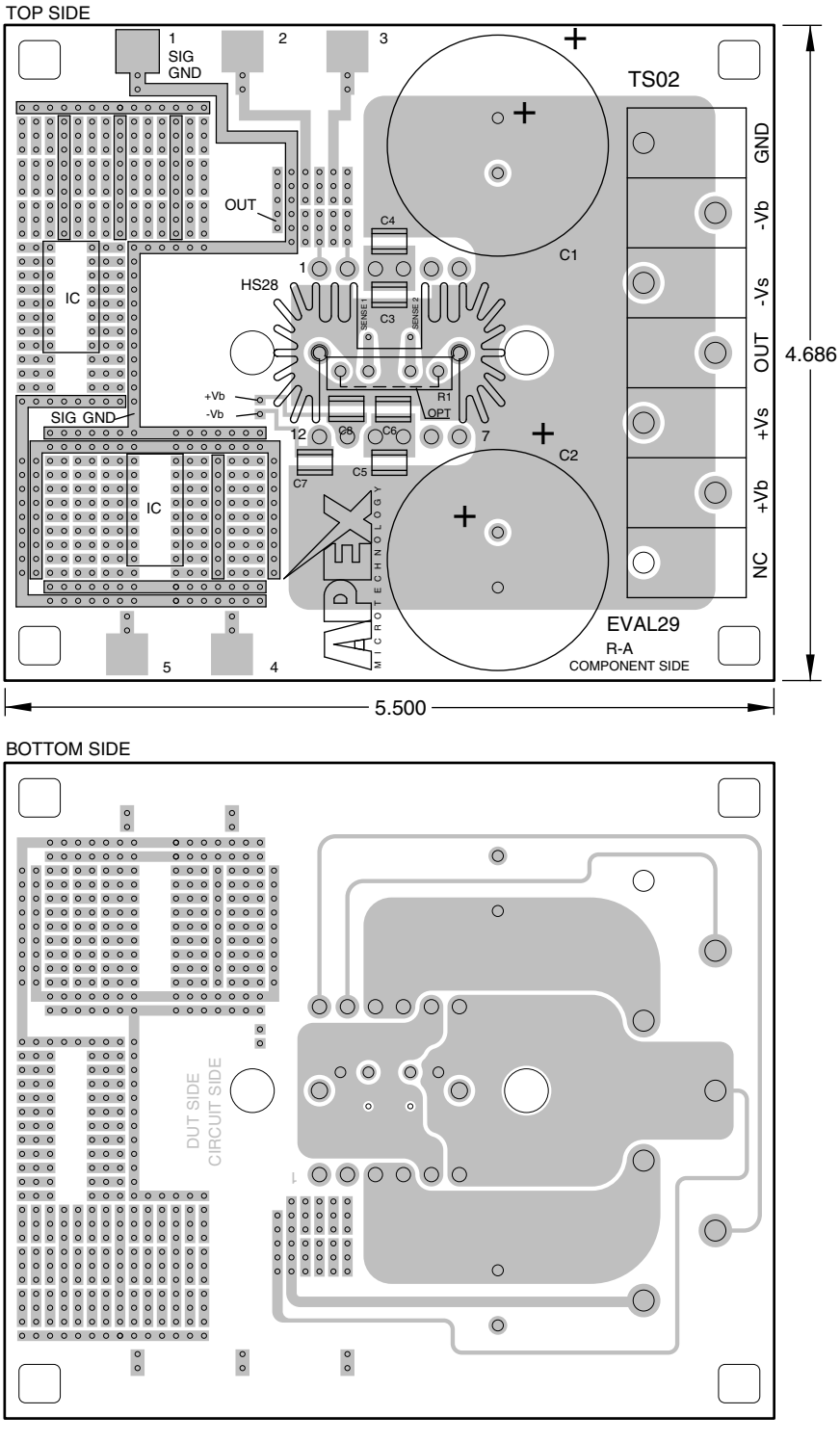


Figure 2 shows the schematic of the pre-wired connections of the EK27. Components which are supplied with the kit are marked *

FIGURE 3. PCB


TOP SIDE
1
SIG
GND
2
3
TS02
GND
-Vb
-Vs
OUT
+Vs
+Vb
NC
OUT
C4
C1
HS28
IC
C3
SENSE 1
SENSE 2
+Vb
-Vb
R1
OPT
SIG GND
12
C8
C6
7
C2
C7
C5
IC
4.686
EVAL29
R-A
COMPONENT SIDE
5
4
5.500
BOTTOM SIDE
DUT SIDE
CIRCUIT SIDE

Evaluation Kit for PA97

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA97 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 1.

PARTS LIST

Part #	Description, Vendor	Quantity
EVAL23	PC Board, Apex Precision Power	1
P6KE440A	TransZorb, General Semiconductor (440V)	2
CDC01	Capacitor .01µF 1kV, Sprague 5GAS10	2

ASSEMBLY

1. See Figure 1. Insert and solder the TransZorb diodes at D3 and D4 (440V).
2. Insert and solder the disc bypass capacitors at C1 and C2.
3. Jumper R_{LIM} and R_C Note that heatsink HS28 is not used.
4. Add banana jacks as necessary to complete connections to external circuits and power supplies.
5. Insert the amplifier into the PCB mounting holes located in the space between the heatsink fins (not used) and solder pins.
6. Add other passive components as necessary to complete your circuit.
7. Most common configurations will ground the non-inverting pin of the amplifier. J1 is a convenient way to do this if necessary for your application circuit.
8. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
9. R1-R5 are multiple feedback resistors in series. Commonly available resistors do not have a breakdown voltage sufficient to stand off the output voltage of the amplifier. Using multiple resistors will divide down the voltage that each resistor must withstand.

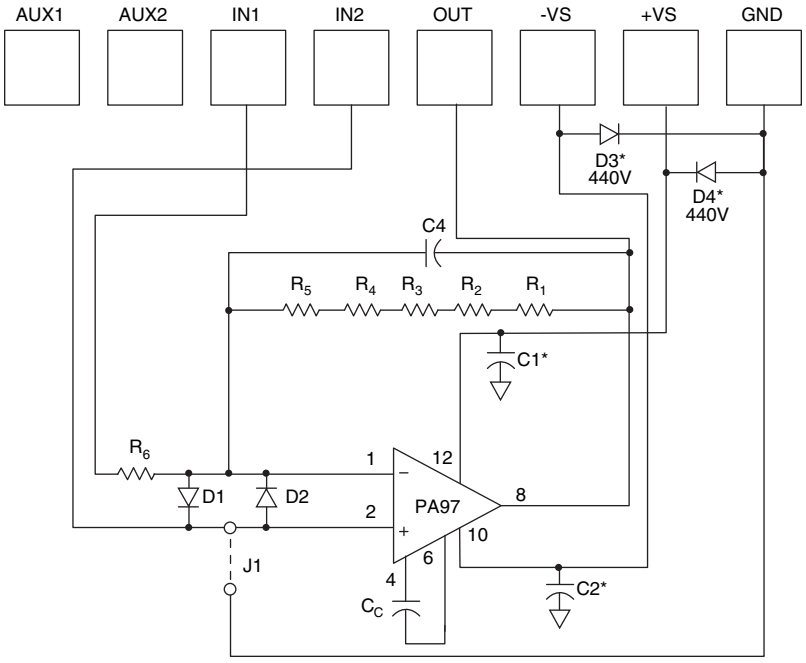
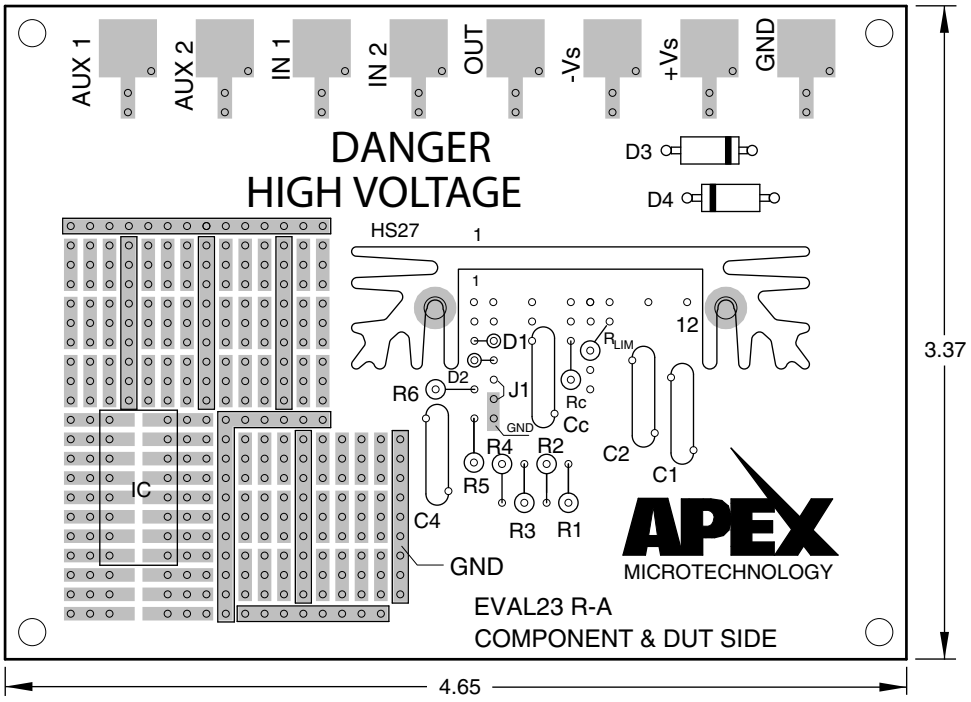


FIGURE 1.

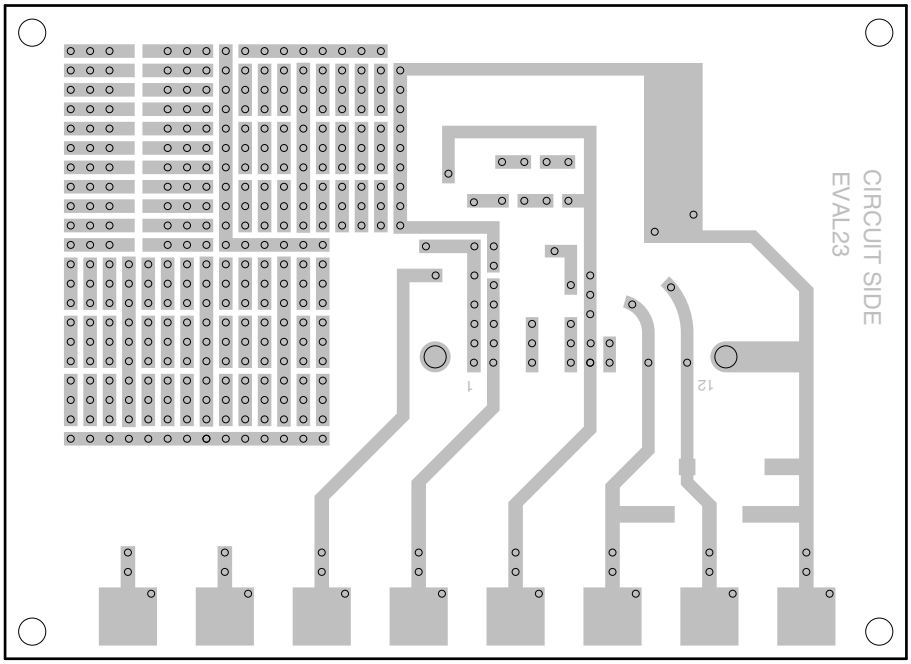
Figure 1 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). See the amplifier's data sheet for full application information.

FIGURE 2. PCB

TOP SIDE



BOTTOM SIDE



F

Power Booster Evaluation Kit

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of the PB51 high voltage power boosters. The PB51 is designed most commonly in combination with a small signal, general purpose op amp. However, they can also be used without a driver amplifier. This kit can be used to analyze a multitude of standard or proprietary circuit configurations.

CAUTION Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.

PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL30	PC Board	1
MS06	Mating Socket	1
TW07	Thermal Washer	1 package

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

ASSEMBLY

1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1-12. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to incude proper bypassing, required compensaton components and current limit resistors. See the op amp data sheet for help in selecting these components.
3. Place the TW07 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20. Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M) do not over torque.
5. Install leads of the DUT into the the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heatsink as shown in the assembly diagram (Figure1).

EQUIVALENT SCHEMATIC

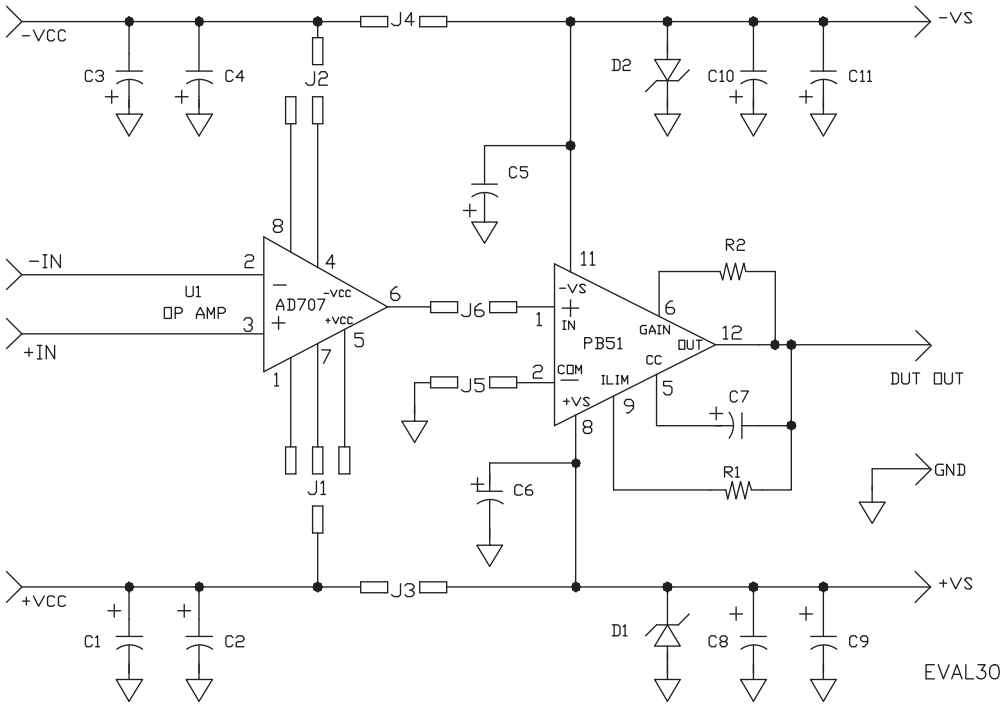
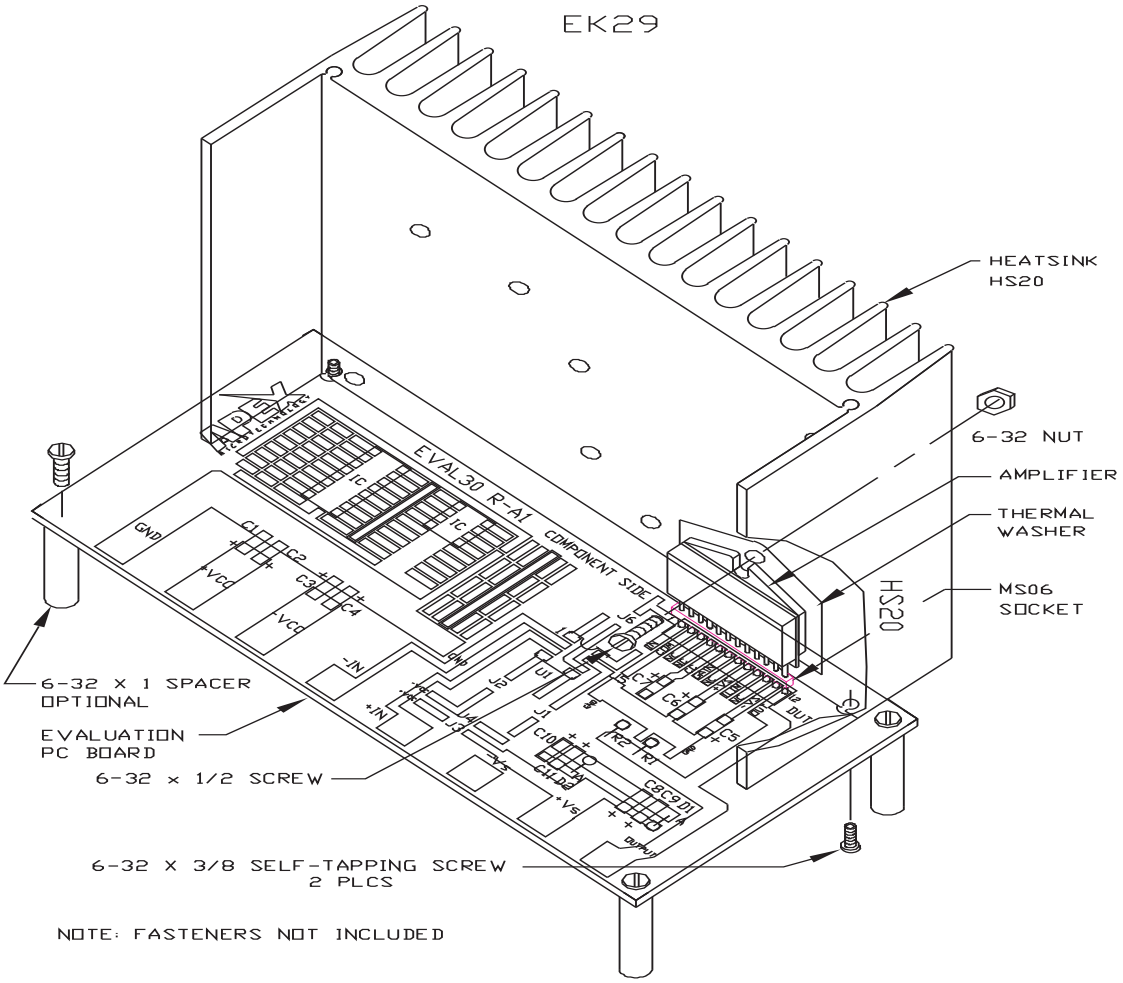


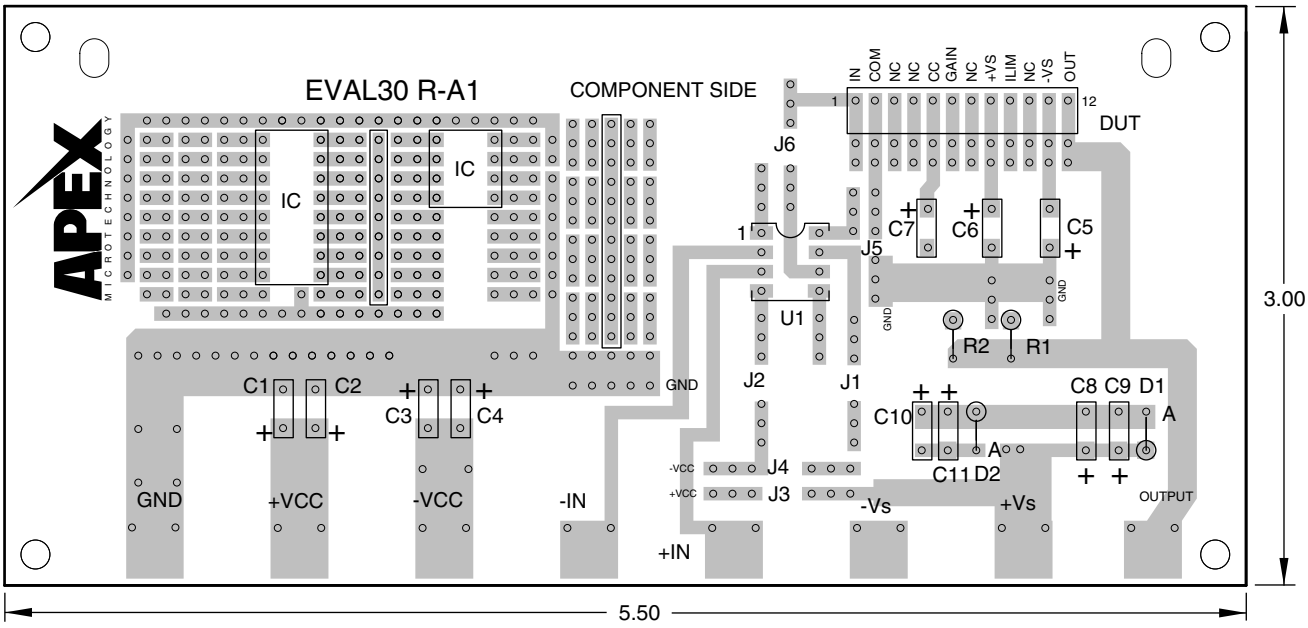
FIGURE 1.


EK29
HEATSINK
HS20
6-32 NUT
AMPLIFIER
THERMAL
WASHER
MS06
SOCKET
HS20
EVAL30 R-A1 COMPONENT SIDE
6-32 X 1 SPACER
OPTIONAL
EVALUATION
PC BOARD
6-32 x 1/2 SCREW
6-32 X 3/8 SELF-TAPPING SCREW
2 PLCS
NOTE: FASTENERS NOT INCLUDED

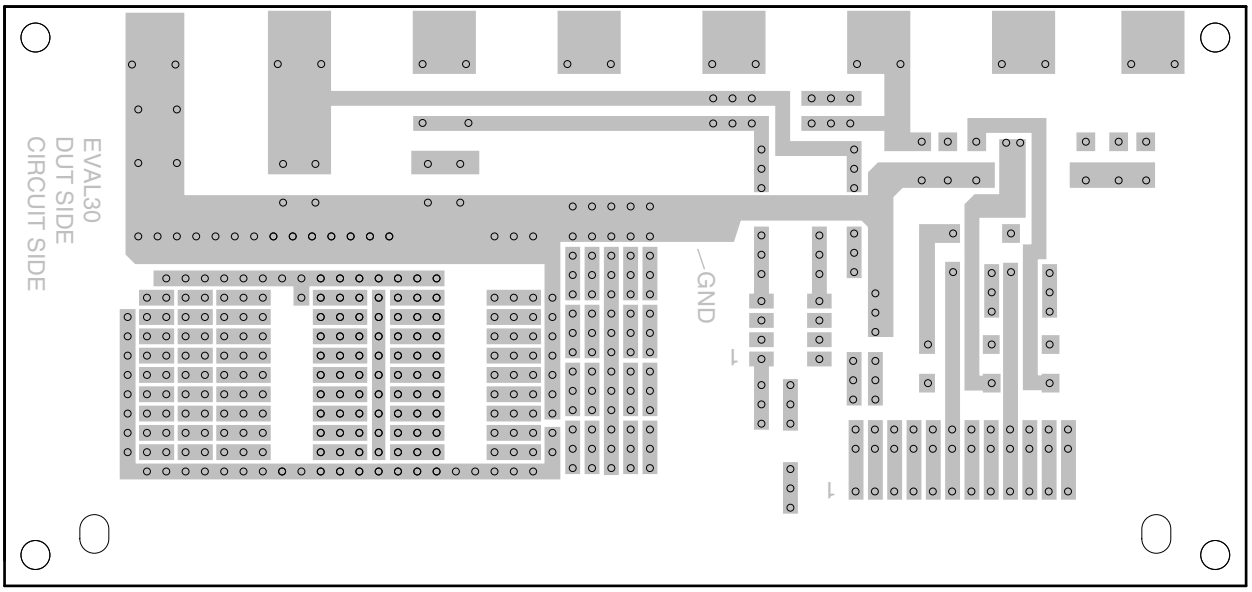
F

FIGURE 3. PCB

TOP SIDE



BOTTOM SIDE



Evaluation Kit for PA75CX or PA35CX Pin Out

INTRODUCTION

Fast, easy breadboarding of circuits using the PA75CX or PA35CX are possible with the EK33 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. Components are labeled on both sides of the board for ease in probing. This kit is not suitable for PA75CC, PA75CD, PA35CC or PA35CD.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually be necessary:

PARTS LIST

Part #	Description	Quantity
Eval33	Evaluation Board	1
Clamp04	Clamp for HS29	2
MS11	Pin Receptacle, 30 pin strip	1
TW14	Thermal Washer TO-220 10/Pack	1
HS29	Heat Sink, 2.7 DEG/W	1

TYPICAL COMPONENT FUNCTIONS

COMPONENT	FUNCTION
C1, C5, C7, C9	Power Supply bypasses MUST be used for each amplifier. Usually ceramic types of .01µF to 1.0µF and 10µF of capacitance per ampere of output current.
C2, C6	
R11, R5	Feedback resistors

The following locations should be jumpered unless used otherwise (their most common function is listed).

J3, J9	Output amp a to input amp b
J2, J8	-Vs
J4, J6	Connects paralleling output a to output b
J5, J10	Connects feedback for amp a

The following locations should be left open unless used otherwise (their most common anticipated function is listed).

J1, J7	Connects -Vs to ground reference

The function of all other components is up to the designer's circuit needs.

EQUIVALENT SCHEMATIC

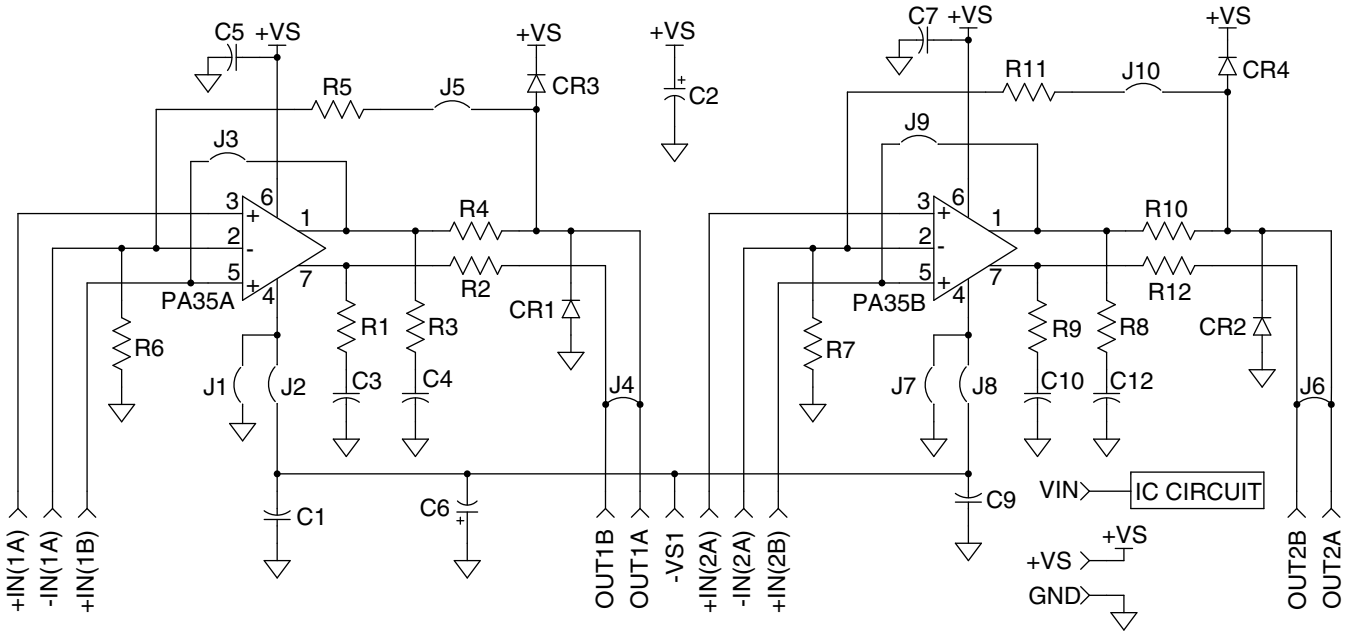
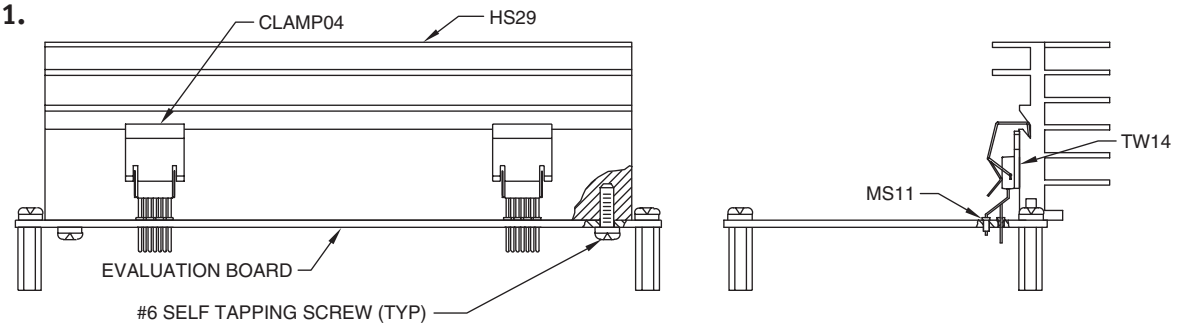
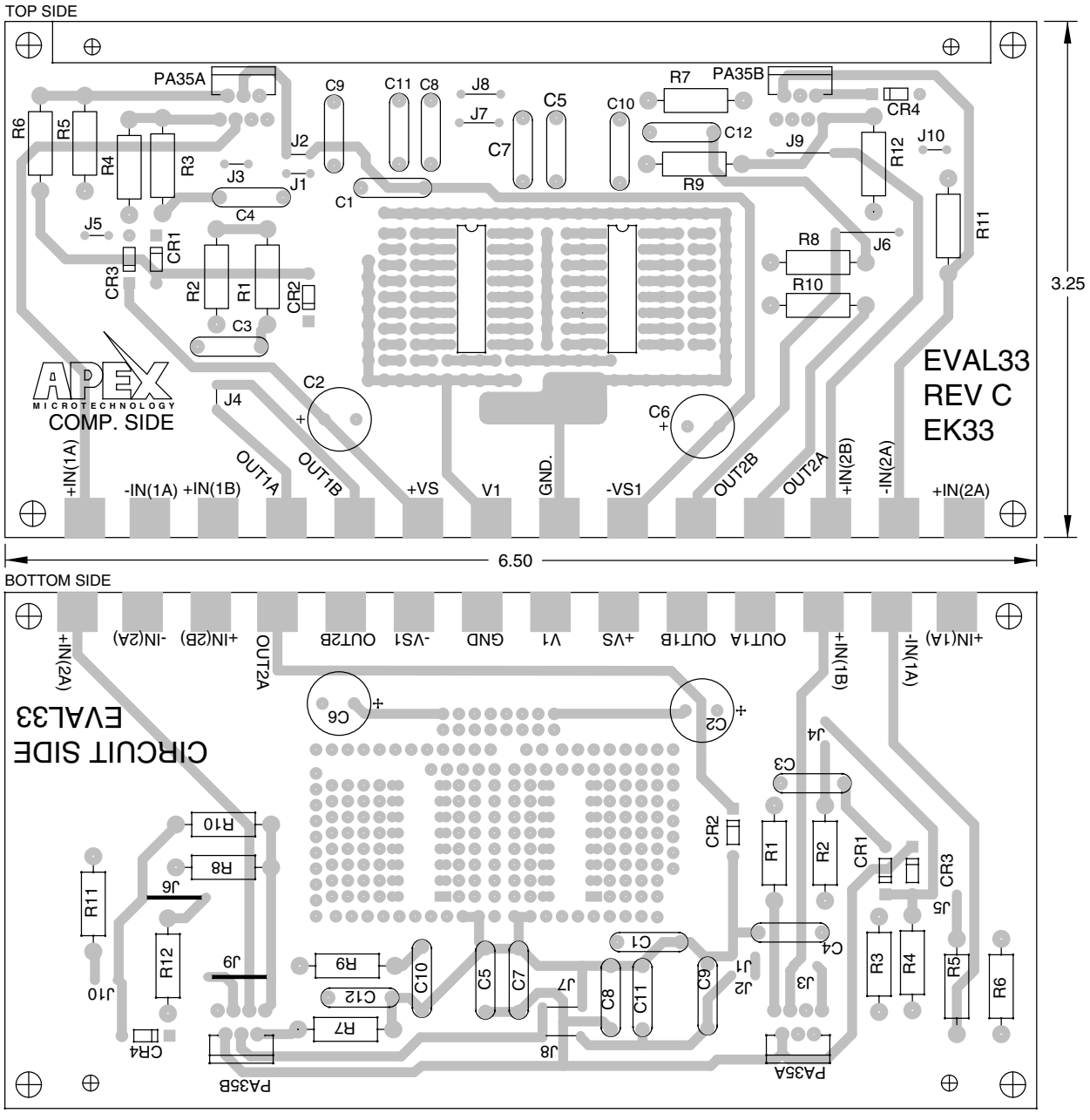


FIGURE 1.


CLAMP04
HS29
TW14
MS11
EVALUATION BOARD
#6 SELF TAPPING SCREW (TYP)


TOP SIDE
PA35A
PA35B
C9
C11
C8
J8
J7
C5
C7
C10
R7
C12
R9
CR4
J9
R12
J10
R11
J2
J1
J3
C4
C1
J5
CR1
CR3
R2
R1
CR2
C3
R8
J6
R10
C2
J4
C6
COMP. SIDE
EVAL33
REV C
EK33
3.25
6.50
+IN(1A)
-IN(1A)
+IN(1B)
OUT1A
OUT1B
+VS
V1
GND.
-VS1
OUT2B
OUT2A
+IN(2B)
-IN(2A)
+IN(2A)
BOTTOM SIDE
CIRCUIT SIDE
EVAL33

Evaluation Kit for PA240CX

INTRODUCTION

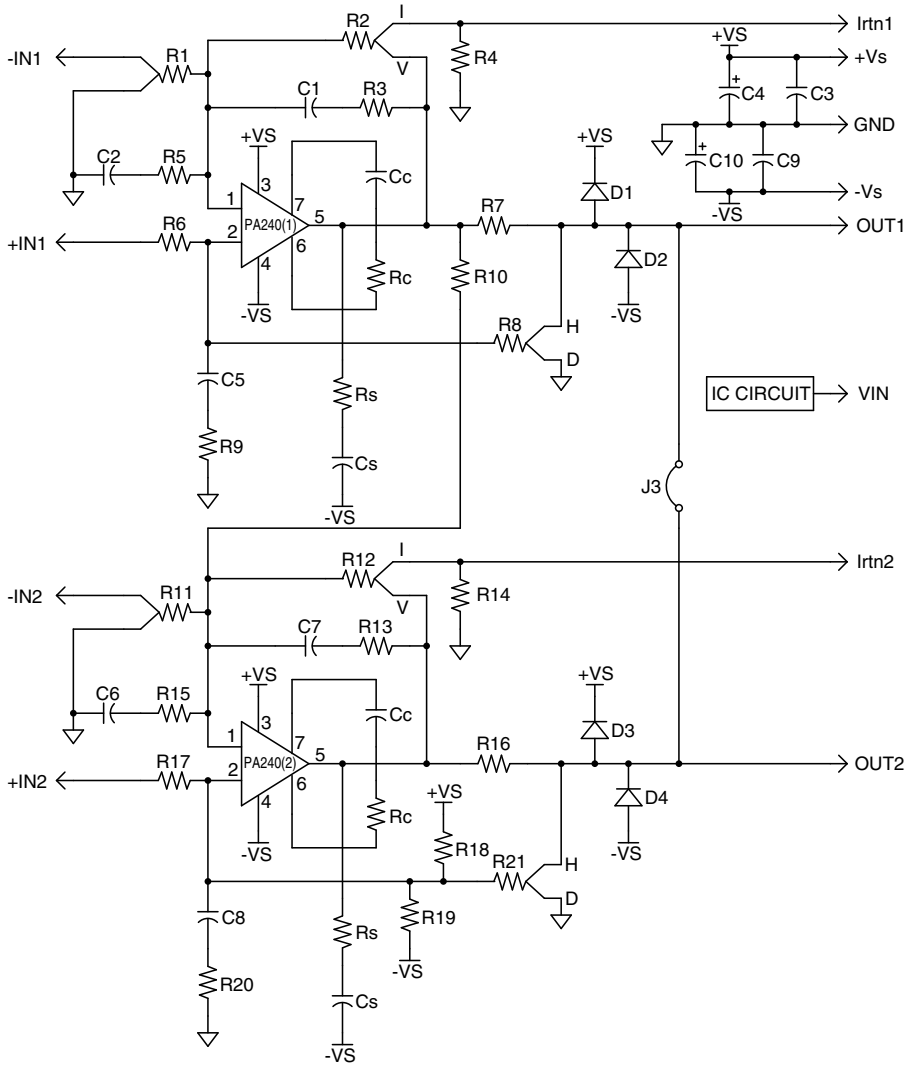
Fast, easy breadboarding of circuits using the PA240CX are possible with the EK34 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. The amplifier may be mounted horizontally or vertically. Components are labeled on both sides of the board for ease in probing.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually be necessary. This kit is not suitable for use with PA240CC.

PARTS LIST

Part #	Description	Quantity
Eval 34	Evaluation Board PA40/140CX	1
Clamp04	Clamp for HS29	2
MS11	Pin Receptacle, 30 pin strip	1
TW14	Thermal Washer TO220 10/Pack	1
HS29	Heat Sink, 2.7 DEG/W	1

EQUIVALENT SCHEMATIC

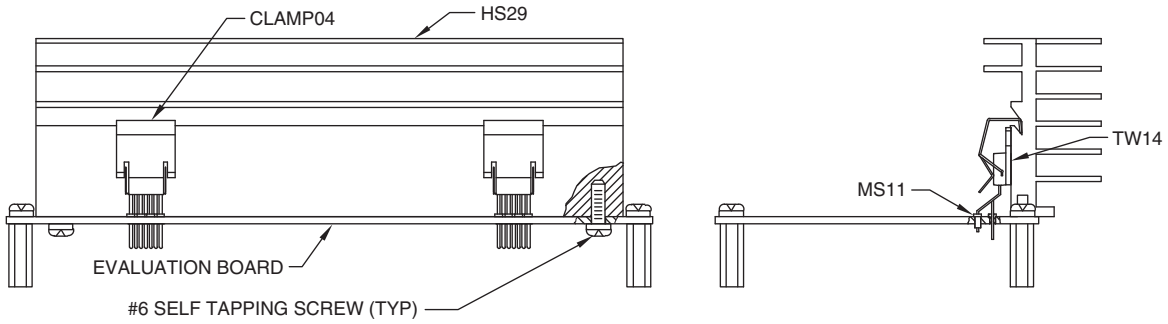


TYPICAL COMPONENT FUNCTIONS

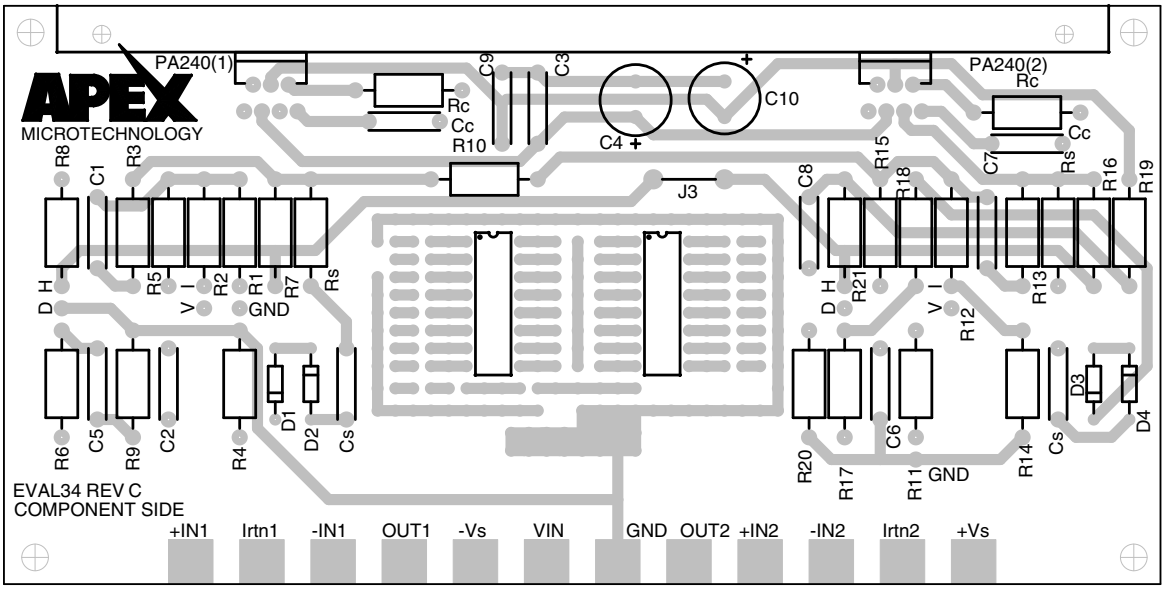
COMPONENT	FUNCTION
C1,7	Alone is a roll off, with R3, 13 is a current out stability network (ref. AN19)
C2,6	With R6, 15 forms noise gain compensation network (ref. AN25)
C3,4	Supply bypass, .22 to 1µF ceramic
C5,8	With R9, 20 forms a Howland stability network, can jumper both to ground +IN
Cc	Sets compensation to match desired gain
Cs	Normally not used.
D1-4	Flyback protection diodes
R1,11	Inverting inputs, install to input line or to ground
R2,12	Negative feedback, install to V for voltage out or to I for current output (ref. AN19)
R3,13	With C1, 7 forms a stability network for current output (ref. AN19)
R4,14	Current sense for current outputs (ref. AN13)
R5,15	With C2, 6 forms noise gain compensation network (ref. AN25)
R6,17	Input R for Howland current pump or differential, usually shorted for non-inverting
R7,19	Current sense for Howland current pump. Could also be used to isolate large Cloads (ref. AN25)
R8,21	Positive feedback, install to H for a Howland current pump, to D for a differential circuit
R9,20	With C5, 8 forms a Howland stability net work, can jumper both to ground +IN
R10	With an equal value R12 provides gain = -1 for a bridge slave (ref. AN3,20)
R18,19	Can provide mid-supply reference for single supply bridge (ref. AN3, 20)
Rc	Normally shorted.
Rs	Normally not used.

F

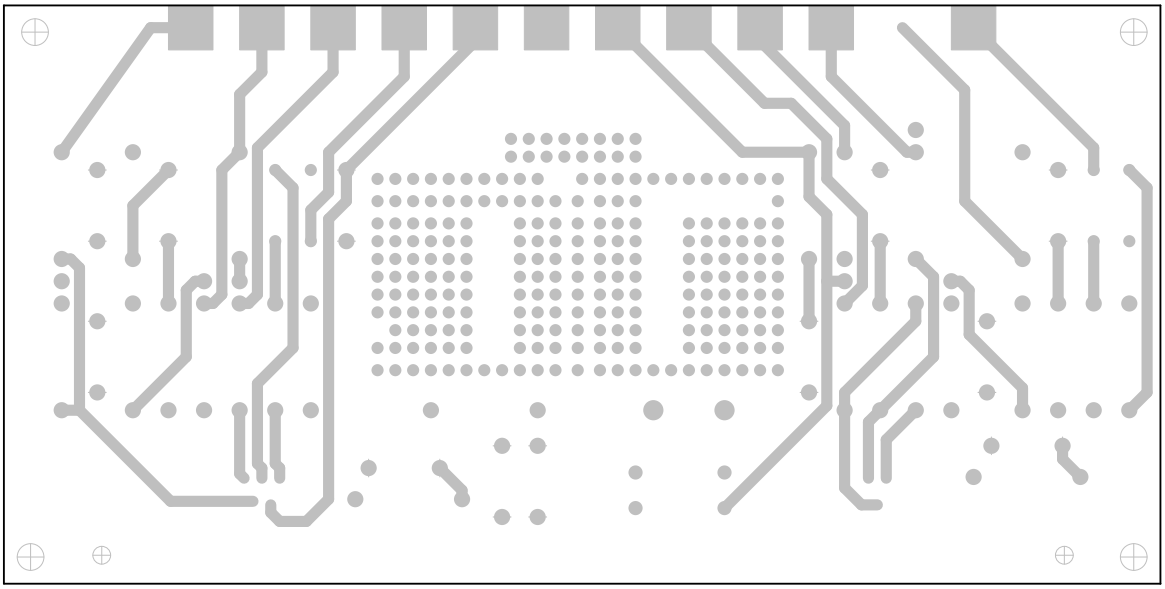
FIGURE 1.



EVAL34
TOP



EVAL34
BOTTOM



Evaluation Kit for PA15 and PA241DW Pin-Outs

INTRODUCTION

Fast, easy breadboarding of circuits using the PA241DW and the PA15 are possible with the EK42 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. The amplifier may be mounted horizontally or vertically. Components are labeled on both sides of the board for ease in probing.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually always be necessary:

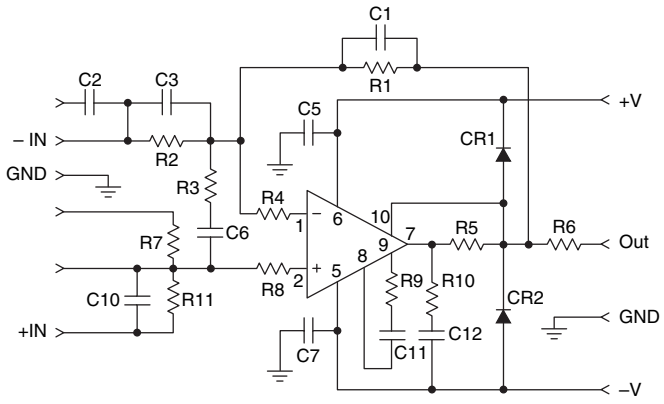
C5,C7	Power supply bypasses MUST be used. Usually ceramic types of 0.01 to 0.1µF.
R1	Feedback resistor.
R2	Input resistor.
R9, C11	Compensation (see amplifier data sheet).
R5	Current limit (see amplifier data sheet).
R7	Most often used as input bias current return for +input in non-inverting circuits.
R3, C6	Noise gain compensation. Necessary only occasionally, see Application Notes 19 and 25.

The following locations should be jumpered unless used (their most common anticipated function is listed).

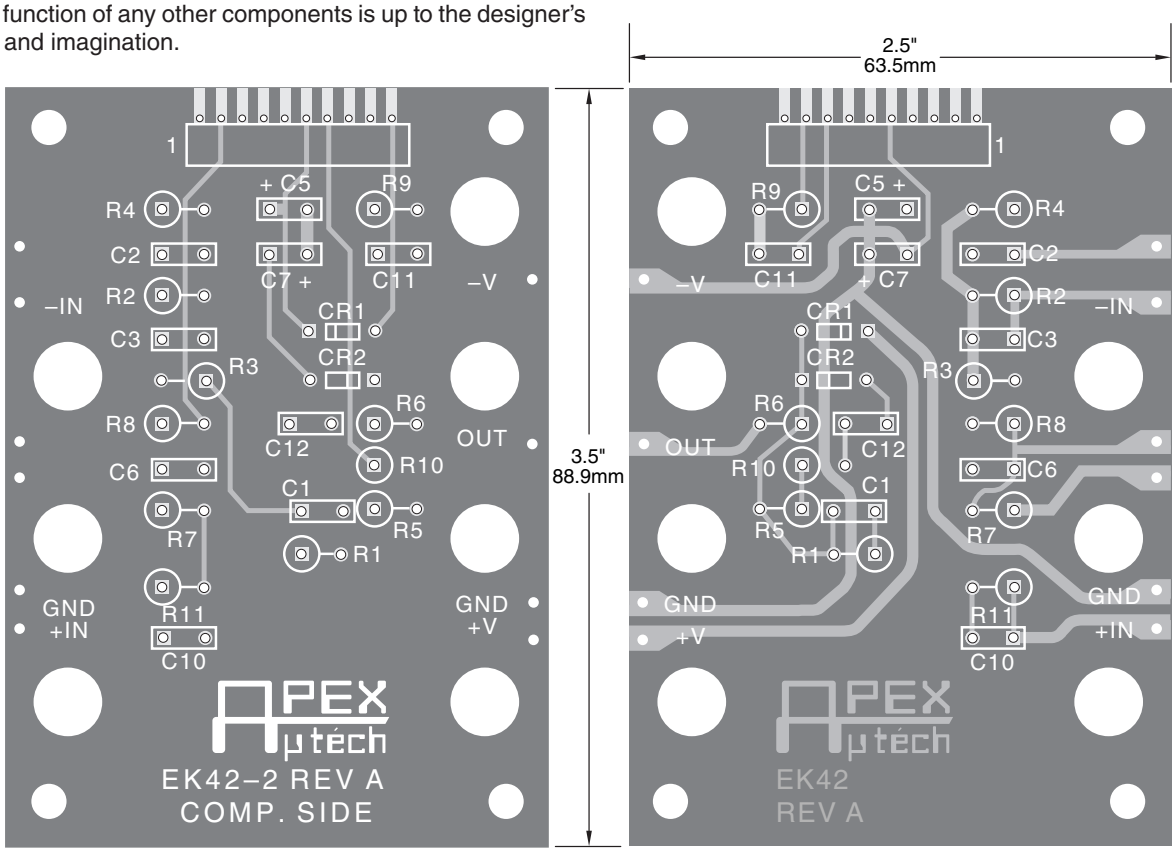
R4, R8	Input protection.
R11	General purpose.
R6	Output current sense.

The function of any other components is up to the designer's needs and imagination.

EQUIVALENT SCHEMATIC



CAUTION **High voltages will be present. Use caution in handling and probing when power is applied.**

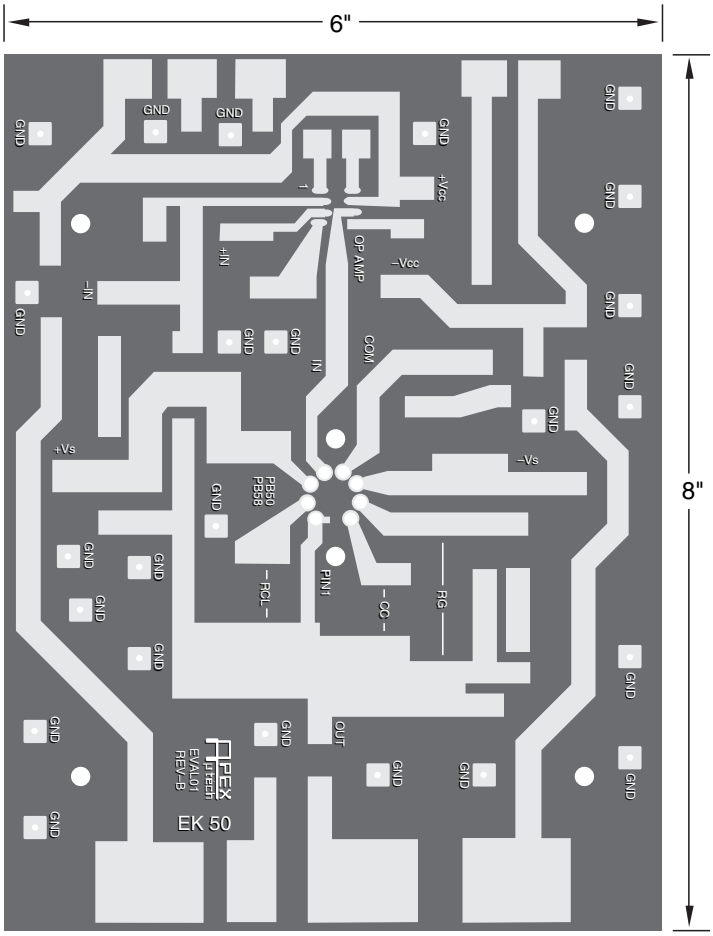


NOTE: Illustration only, not to exact scale.

Evaluation Kit for PB50, PB58 Power Boosters

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of the PB50 and PB58 high voltage power boosters. The PB50 and PB58 are designed most commonly in combination with a small signal, general purpose op amp. However, they can also be used without a driver amplifier. This kit can be used to analyze a multitude of standard or proprietary circuit configurations.



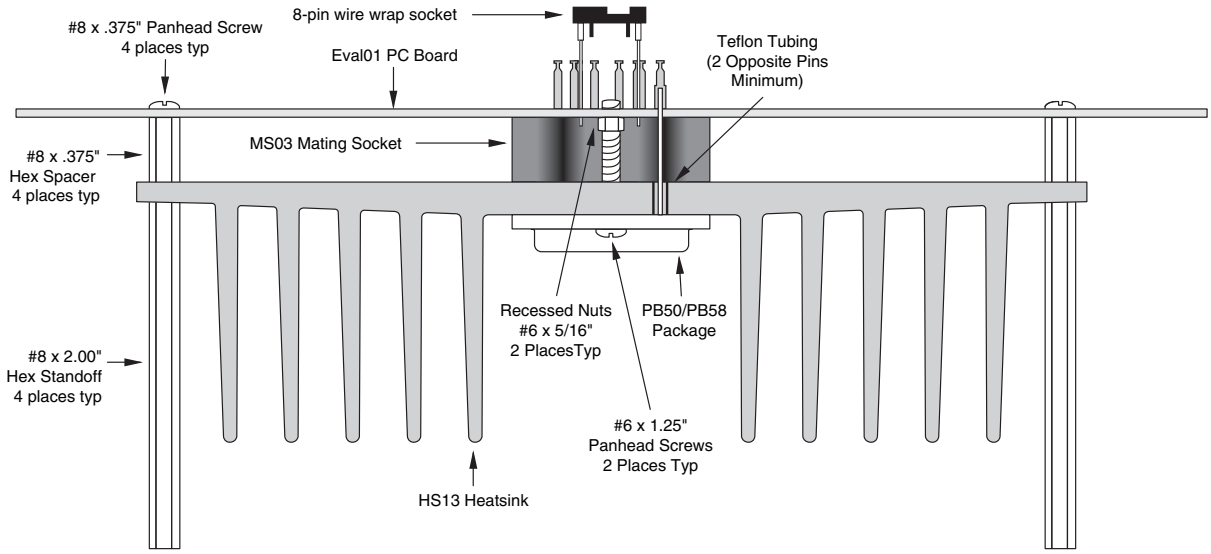
PARTS LIST

Part #	Description	Quantity
HS13	Heatsink	1
EVAL01	PC Board	1
MS03	Mating Socket	1
HWRE02	Hardware Kit	1
HWRE05	8-Pin Wire Wrap Socket	1
TW0 3	Thermal Washer	1 Box/10

HWRE02 contains the following:

- 4 #8 x .375" Panhead Screws
- 4 #8 x .375" Hex Spacers
- 4 #8 x 2.00" Hex Stand Offs
- 2 #6 x 1.25" Panhead Screws
- 2 #6 x 5/16" Hex Nuts

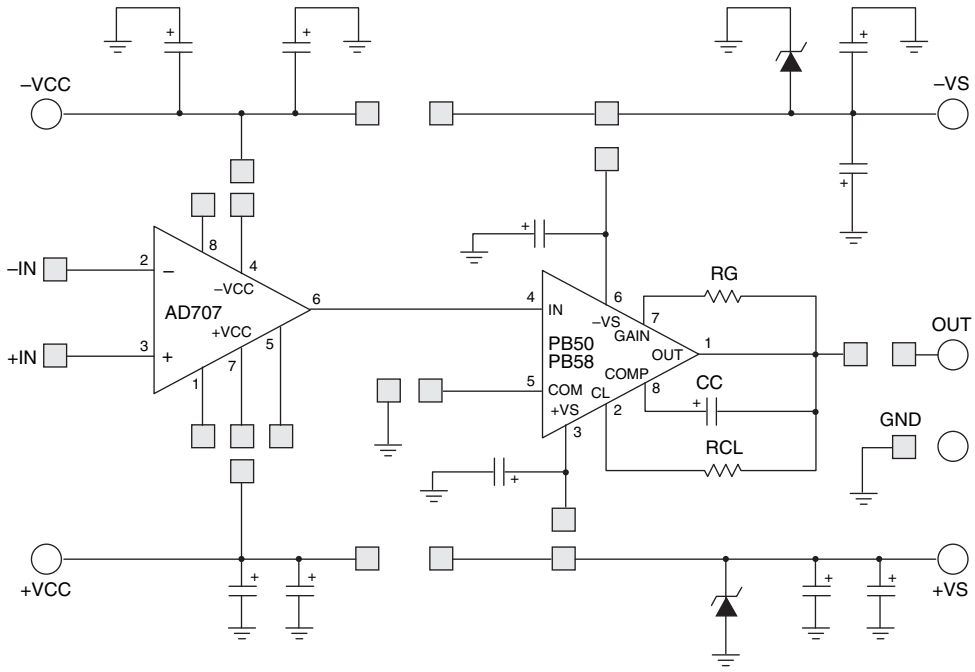
ASSEMBLY



CAUTION

1. Use thermal grease or Apex Precision Power Thermal Washer TW03 between power booster and heatsink.
2. Use 18 gauge teflon sleeve on at least two opposite pins
3. Mounting torque greater than 7 in•lbs on power booster mounting bolts will void warranty!

EQUIVALENT SCHEMATIC



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CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Evaluation Kit for DF (24-pin PSOP)

INTRODUCTION

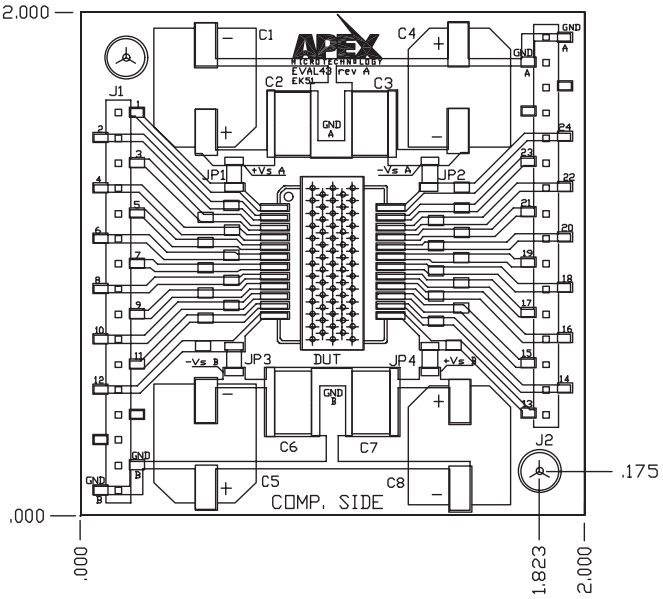
The EK51 evaluation kit provides a fast and easy breadboard solution for all devices in Apex Precision Power's PSOP1 package (24 PIN PSOP). The EK51 includes the EVAL43 board shown in Figure 1, as well as the universal EVAL36 board. The combination of the two boards provides a large area for breadboard circuit space while also providing an effective method of thermal management of the surface mount package. The device under evaluation is surface mounted directly to the EVAL43 PC board which provides a foil footprint area the size of the heat slug. This foil heat slug connection area consists of plated through thermal vias. The thermal vias offer a cost-effective way to decrease the thermal resistance between one side of the PC board which allows for the direct mounting of a heat sink or heat sink surface mount fan on the back side of the PC board.

PARTS LIST

Part#	Description	Qty
EVAL36	Universal PC Board, Apex Precision Power	1
EVAL43	PC Board, PSOP1, Apex Precision Power	1
TSM-116-01-T-SV	Terminal Strip, 16pin, Samtec	2
SSW-116-01-T-S	Socket Strip, 16pin, Samtec	2
OX7R105KWN	Cap, 200V, 1µF, Ceramic	4
*ERJ-6GEYOR00V	Res, 0.0Ω, 0805SMD, Panasonic	4
*AVS336M2AG24T	Cap, 100V, 33µF, CDE	4
*031606	Heat Sink w/ Fan, 3.4°C/W, AAVID	1
	or	
*031613	Heat Sink, 11.0°C/W, AAVID	1

* Parts not supplied. Parts are application dependent. Suggested part numbers are provided.

Figure 1: EVAL 43



ASSEMBLY

The PSOP1 should be assembled to the EVAL43 PC board using surface mount processes. Solder paste may be dispensed or screen-printed on the DUT pads as well as the foil heat slug pad. The heat slug on the bottom surface of the PSOP1 provides maximum heat dissipation capabilities when soldered to the PCB foil footprint area. However, for prototype purposes, the tab can be thermally connected to the PCB foil area using thermal grease.

If soldering the heat slug, ideally the PSOP1 should be soldered to the PCB using a solder reflow furnace. If a reflow furnace is not available, a heat plate capable of solder reflow temperatures may be used. Otherwise, the leads may be carefully soldered individually to the PCB with a thin tip soldering iron. However, in this case, the use of thermal grease under the heat tab is recommended instead of solder for thermal connection through the thermal vias.

The kit comes with ceramic bypass capacitors, which should be soldered on the space provided on the EVAL43 board. Also, space is provided for the appropriate electrolytic by-pass capacitors. Although these capacitors are not provided in the kit, a recommended capacitor is listed for 100V applications. For higher voltage applications, a larger electrolytic capacitor can be mounted on the EVAL36 board.

The EVAL43 is a generic evaluation board for the PSOP1. Jumpers are required to make appropriate connection to +Vs, -Vs and ground. When applicable, surface mount 0805 0Ω resistors can be used in the locations provided.

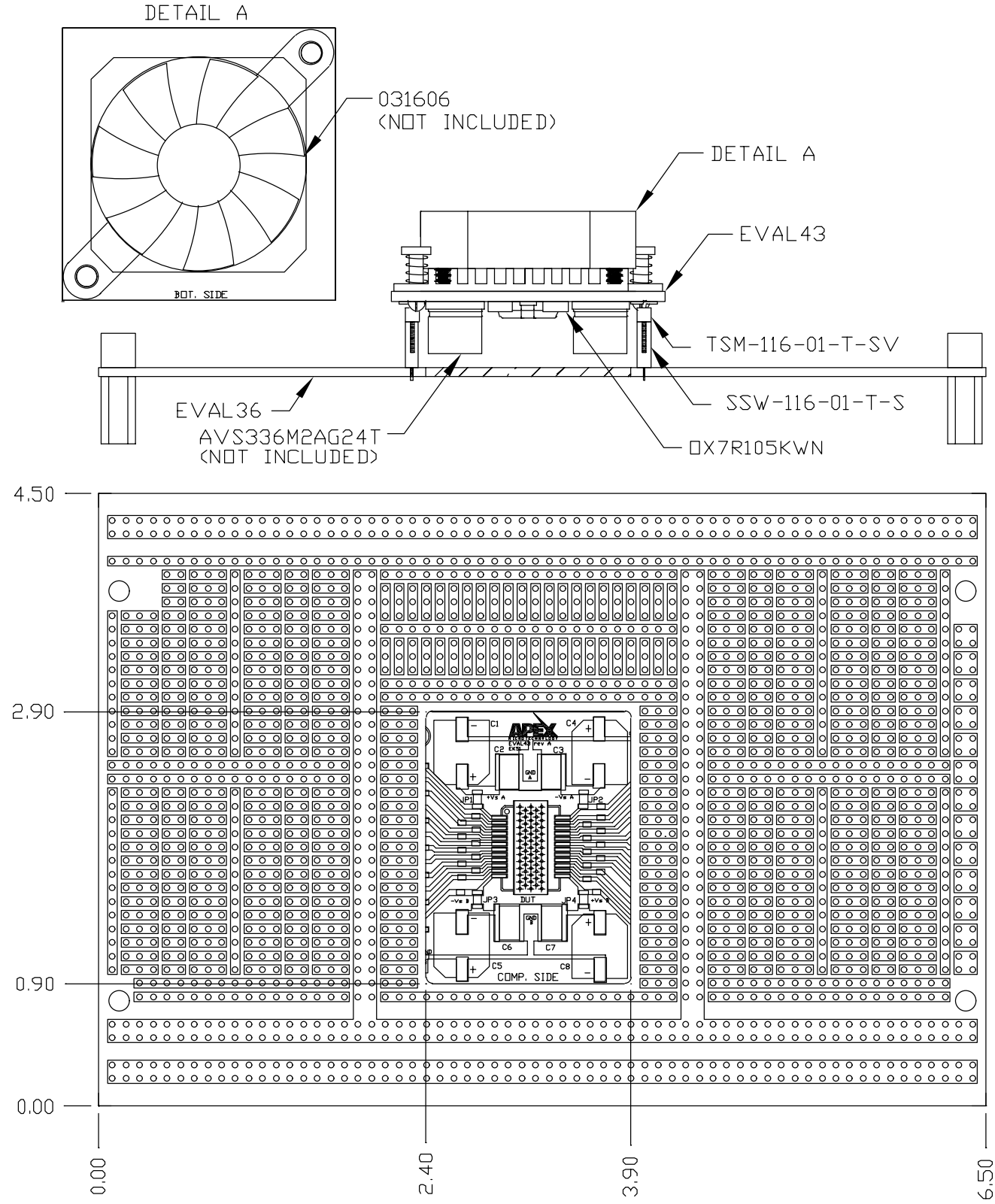
Once all the surface mount components are installed, the heat sink can then be mounted to the back of the PC board. High thermal conductive grease should be used when mounting the heat sink to the PC board. Note: A heat sink is not supplied with the kit, but several options are listed which are produced by AAVID Thermal Product, Inc.

Review Figure 2 on the next page for all other assemblies needed to construct this evaluation kit.

BEFORE YOU GET STARTED

* All Apex Precision Power amplifiers should be handled using proper ESD precautions.
* Always provide the appropriate heat sinking.
* Always use adequate power supply bypass capacitors.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

Figure 2: EVAL36



Evaluation Kit for MP230FC, MP240FC Pin-Out

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the MP230FC/MP240FC pin out. With ample bread boarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal block and the banana jacks at the edges of the circuit board. Additionally, an optional BNC connector can be inserted into the hole at the edge of the board and wired to the number 5 terminal pad.

BEFORE YOU GET STARTED

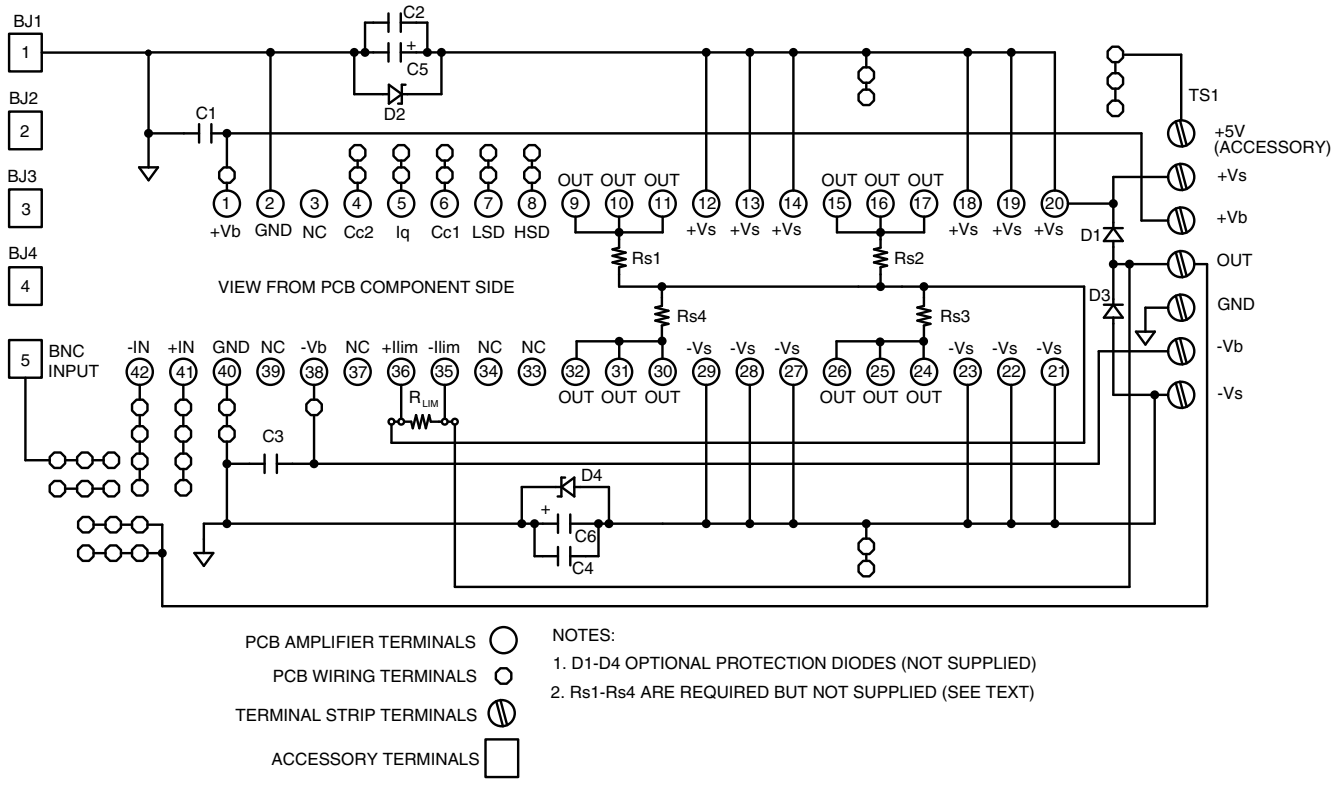
- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.

PARTS LIST

Ref	Apex Part #	Descrip/Vendor	Qty
NA	HS28	Heat Sink	1
NA	HS26	Heat Sink	1
NA	MS11	Cage jack strip	2
BJ1-4	BJ1	Banana Jack/ Deltron 164-6218	4
NA	EVAL45	PC Board	1
NA	60SPG00004	Spacer Grommets/ Micro Plastics	4
C1-4	OX7R105KWN	1uF Cap/ Novacap 1825B105K201N	4
TS1	TS02	Terminal Strip	1
C5,6*	EC05	2200uF 100V/ United Chemi-Con 82DA222M100KC2D	2
C5,6*	EC03	680uF 200V/ United Chemi-Con KMH200VN681M25MX40T2	2
RLIM*	CSR17	0.025 Ohm Resistor/ Isotek PBV-R025-1	1
RLIM*	CSR18	0.050 Ohm Resistor/ Isotek PBV-R050-1	1
RLIM*	CSR19	0.100 Ohm Resistor/ Isotek PBV-R100-1	1
Rs1-Rs4	NA	Separate purchase required See text.	4

*Chosen per directions

FIGURE 1. EVAL45 Schematic



ASSEMBLY

During assembly refer to Figure 3 and the data sheet for the product you are using, either the MP230FC or MP240FC.

1 Note that four balancing resistors, Rs1-Rs4, are required for this evaluation kit and that these resistors are not supplied. Each application will require different values and so these resistors must be purchased by the user before construction of the kit begins. See the recommendation in the product data sheet as to the type of resistor needed and a convenient source for purchasing the resistors. Do not be tempted to operate the amplifier without these resistors.

2. Note that each side of the circuit board is identified as either the "Component Side" or "DUT Side."
3. Locate the two pre-loaded 30-position cage jack carrier strips. Use wire cutters to cut off and discard 10 positions from one of the carrier strips. From the "DUT Side " of the PCB insert this carrier strip into the mounting holes for pins 1-20 of the amplifier and solder from the "Component Side" of the PCB. Be sure that the cage jacks are fully seated before soldering. Be careful that solder does not flow into the cage jack.
4. In a similar manner to step 3 cut off 8 positions from the remaining carrier strip, insert and solder into the mounting holes for amplifier pins 21-42.
5. Pull out and discard each of the carriers.
6. Solder the surface mount capacitors at C1, C2, C3, and C4 on the "Component Side" of the PCB.
7. Solder the surface mount balancing resistors that you purchased separately at Rs1-Rs4 on the "Component Side" of the PCB.
8. Mount the four horizontal banana jacks at locations BJ1-4 and a BNC connector, if desired (not supplied), to the PCB pad at location 5. Solder from the "DUT Side" of the PCB.
9. Mount the terminal strip to the "Component Side" of the PCB. Make sure the terminal strip is fully seated and solder the pins from the "DUT Side" of the PCB. Be sure to fill the mounting holes with solder.
10. Mount the electrolytic capacitors at C5 and C6 from the "Component Side" of the PCB. Match the polarity markings on the capacitor with the polarity markings on the PCB. Use the correct voltage capacitors for the product you are using: 100V capacitors for the MP230 and 200V capacitors for the MP240. Be sure the capacitors have snapped into the PCB and solder from the "DUT Side" of the PCB. Be sure to fill the holes with solder.
11. Several low ohm value resistors are provided with this evaluation kit: 0.025 ohm, 0.050 ohm and 0.100 ohm. These are used to implement current limiting in the output circuit. Select the value most appropriate for your application. Refer to the product data sheet to determine which resistor value you should use.
12. Mount the HS28 heat sink to the PCB and solder the mounting tabs of the heat sink.
13. Apply a thin layer of thermal grease on the back of the chosen current limiting sense resistor, insert the resistor into the PCB and mount the resistor to the HS28 heat sink using #4 screw and nut hardware (not supplied). Solder the leads of the current limiting resistor from the "DUT Side" of the board. Be sure to fill the mounting holes with solder.
14. Mount other components and wiring as needed to complete your application circuit using the pads and holes provided.
15. From the "DUT side" of the PCB snap the spacer- grommets into the holes at the four corners of the PCB. Notice that the holes are slightly rectangular and match the spacer-grommet's long and short sides to the holes in the PCB.
16. Apply a thin layer of thermal grease to the amplifier base. Position the amplifier over the mounting holes in the HS26 heat sink. Firmly push the amplifier onto the heat sink while slightly rotating the amplifier back and forth, ending with the mounting holes of the amplifier over the mounting holes in the heat sink.
17. Attach the amplifier to the heat sink with 4 4-40 X ½" male-female hex spacers (not supplied). These spacers serve as alignment pins and aide in the assembly of the PCB to the heat sink. Alternately, use 4-40 X ¼" machine screws to mount the amplifier to the heat sink. Do not over-tighten the spacers or screws as this provides no thermal benefit and may break the hardware.
18. Place the PCB assembly onto the HS26 heat sink so that the four hex spacers come through the aligning holes near the four corners of the amplifier position in the PCB. Carefully lower the PCB assembly until the pins of the amplifier engage the cage jacks. Alternately, sight through the aligning holes in the PCB and match-up the PCB to the screws used to mount the amplifier. In either case be sure the pins of the amplifier are engaged with the cage jacks and then continue pushing the PCB assembly in the area between the amplifier's pins until the 4 spacer grommets at the four corners of the PCB touch the HS26 heat sink. At this point you may need to push the PCB down slightly in the area of the amplifier if the PCB is bowed.
19. Use #8 X 1" sheet metal screws (not provided) to mount the PCB to the heat sink at the four spacer-grommets.
20. Hook up power and signals as necessary. The amplifier is now ready for testing.

FIGURE 2.

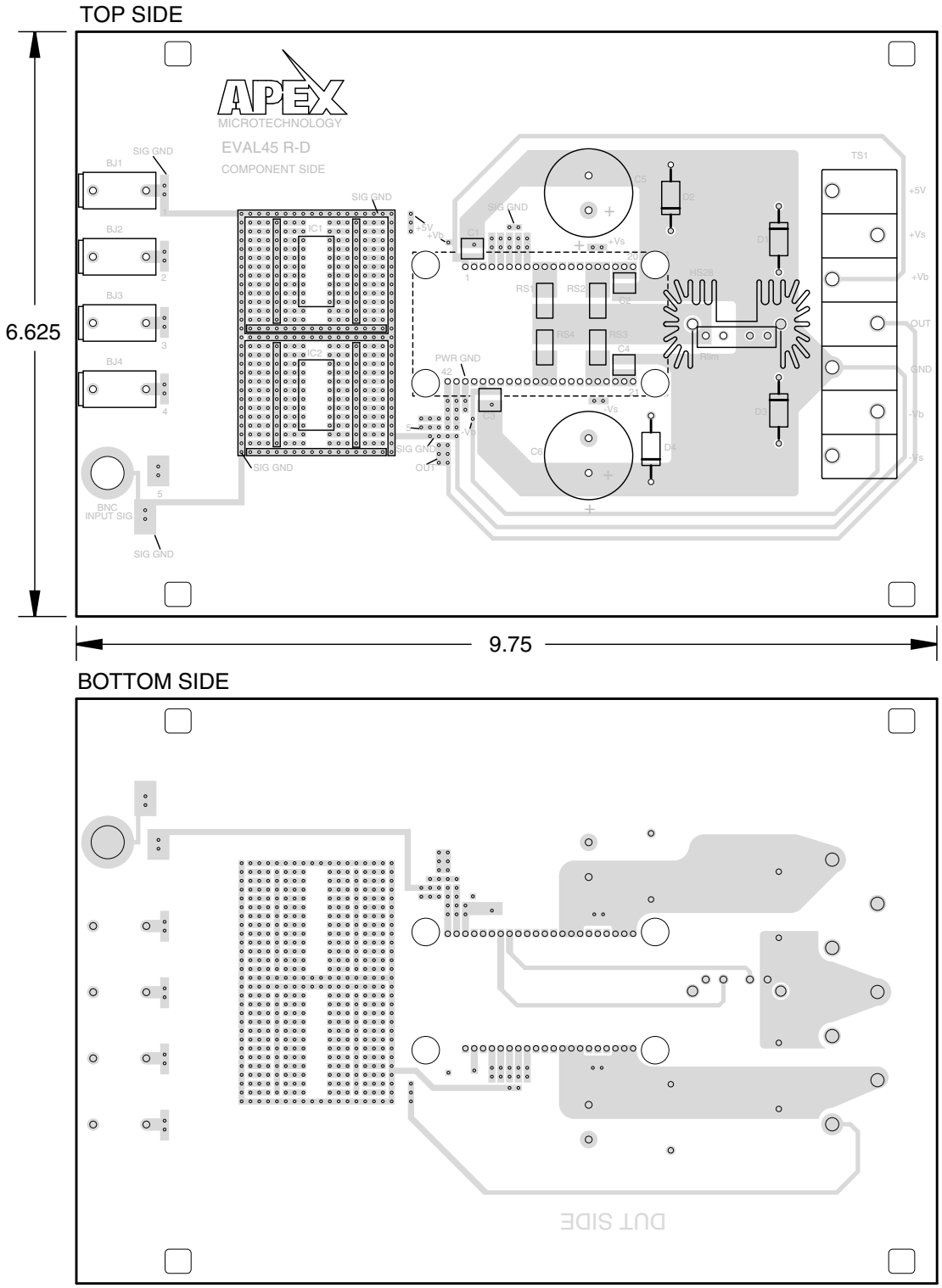
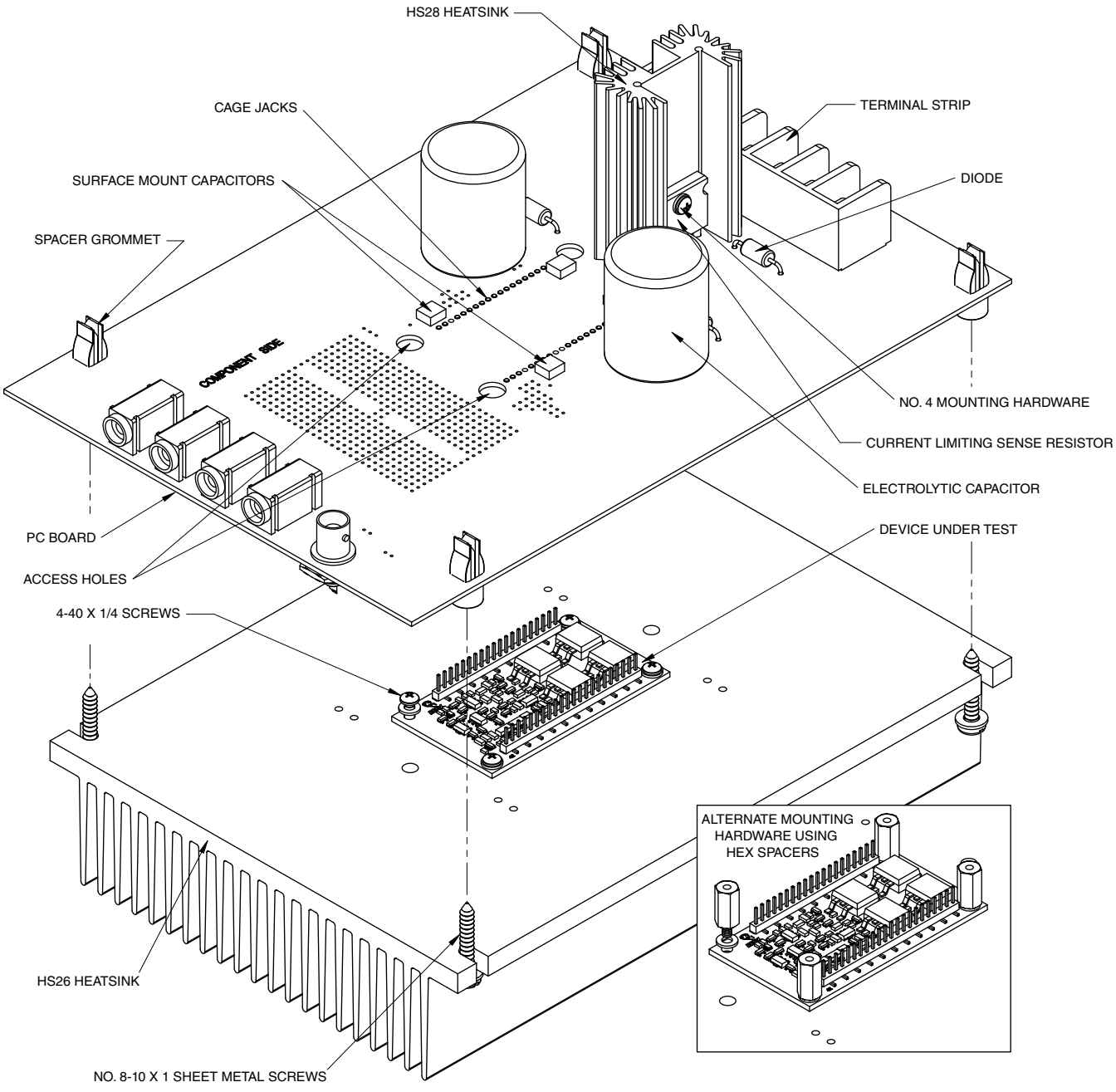

TOP SIDE
APEX
MICROTECHNOLOGY
EVAL45 R-D
COMPONENT SIDE
6.625
9.75
BOTTOM SIDE
DUT SIDE

FIGURE 3.


HS28 HEATSINK
CAGE JACKS
TERMINAL STRIP
SURFACE MOUNT CAPACITORS
DIODE
SPACER GROMMET
COMPONENT SIDE
NO. 4 MOUNTING HARDWARE
CURRENT LIMITING SENSE RESISTOR
ELECTROLYTIC CAPACITOR
DEVICE UNDER TEST
PC BOARD
ACCESS HOLES
4-40 X 1/4 SCREWS
ALTERNATE MOUNTING HARDWARE USING HEX SPACERS
HS26 HEATSINK
NO. 8-10 X 1 SHEET METAL SCREWS

F

Evaluation Kit for MSA240KC and MSA260KC

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM circuits using the MSA240KC/260KC pin out. With ample bread boarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal block and banana jacks at the edges of the circuit board.

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.

PARTS LIST

Ref	Apex Part No.	Description/Vendor	Qty
NA	HS28	Heat Sink, Apex Precision Power	2
NA	HS26	Heat Sink, Apex Precision Power	1
NA	MS11	30-pin socket carrier strip	2
NA	EVAL56	PC Board	1
NA	60SPG00004	Spacer Grommets/ Micro Plastics	4
BJ1-4	BJ1	Banana Jack/ Deltron 164-6218	4
C1,3	ZX7R105KTL	1uf 500V Cap/ Novacap ST2225B105K501LLXW	2
For identification note this capacitor has "legs".			
C2*	EC05	2200uF 100V/ United Chemi-Con 82DA222M100KC2D	1
C2*	EC06	470uF 450V/ United Chemi-Con KMH450VN471M35X50T2	1
TS1	TS02	Terminal Strip	1
R1,2*	CSR22	0.020Ω Resistor/ Isotek PBV-R020-1	2
R1,2*	CSR20	0.010Ω Resistor/ Isotek PBV-R010-1	2
R1,2*	CSR21	0.015Ω Resistor/2 Isotek PBV-R015-1	

*Chosen per directions

ASSEMBLY

During assembly refer to Figure 1 and the data sheet for the product you are using, either the MSA240KC or MSA260KC.

1. Note that each side of the circuit board is identified as either the component side or "DUT side".
2. Two 30-pin socket strips have been supplied with this kit that have been loaded with cage jacks. Using wire cutters trim the carrier to remove two sockets from one of the strips. Insert the socket strips from the "DUT side" of the board and solder the jacks from the "component side" of the board, making sure that each socket strip is fully seated before soldering. After soldering the jacks remove and discard the plastic carrier.
3. Solder the surface mount capacitors at C1 and C3 on the "component side" of the board.
4. From the "component side" mount banana jacks at BJ1-4 and solder from the "DUT Side" of the circuit board. Cut off excess lead lengths. Note that BJ1 is connected to SIG GND.
5. Several low ohm value resistors are provided with this evaluation kit: 0.020Ω, 0.015Ω and 0.010Ω. These are used to implement current limiting in the output circuit. Select the value most appropriate for your application. Refer to the product data sheet to determine which resistor value you should use.
6. From the "component side" of the PCB mount the HS28 heat sink closest to C2 (to be added later) and solder the mounting tabs of the heat sink from the "DUT side" with a high capacity soldering iron.
7. Apply a thin layer of thermal grease on the back of the chosen current limiting sense resistor R2 and insert the resistor into the PCB. Mount the resistor to the HS28 heat sink using #4 screw and nut hardware (not supplied). Place the screw into the mounting hole from the narrow-channel side of the heat sink and place the nut on the screw from the wide-channel side of the heat sink. Do not over tighten the screw. Finally, solder the resistor terminals to the PCB and **cut off the excess lead length**.
8. Mount the remaining HS28 heat sink similarly to step 6.
9. Repeat step 7 for R1 and the second HS28 heat sink.
10. Mount the electrolytic capacitor at C2 from the "component side" of the PCB. Match the polarity markings on the capacitor with the polarity markings on the PCB. Use the correct voltage capacitors for the product you are using: A 100V capacitor for the MSA240KC, or a 450V capacitor for the MSA260KC. Be sure the capacitors have snapped into the PCB and solder from the "DUT side" of the PCB. Be sure to fill the holes with solder.
11. Mount the terminal strip to the "component side" of the PCB. Make sure the terminal strip is fully seated and solder the pins from the "DUT side" of the PCB. Be sure to fill the mounting holes with solder.
12. Mount a BNC connector (not supplied) to the PCB at location 5 (near the banana jacks) if desired. The body of the BNC connector is tied to SIG GND.
13. Mount other components to complete your application circuit using the pads and holes provided. Refer to the data sheet for your model and note on page 4 that:

$$R_{RAMP} = 2 \times R_{OSC}$$

It is therefore convenient to use 3 resistors of equal value and make up R_{RAMP} from two of those resistors. Note on the PCB locations for R_{RAMP1} and R_{RAMP2} to do this.

ASSEMBLY CONT.

14. From the "DUT side" of the PCB snap the spacer- grommets into the holes at the four corners of the PCB. Notice that the holes are slightly rectangular and match the spacer-grommet's long and short sides to the holes in the PCB.
15. Apply a thin, uniform layer of thermal grease to the amplifier; a straight edge may be useful here. Position the amplifier over the mounting holes in the heatsink. Firmly push the amplifier onto the heatsink while slightly rotating the amplifier back and forth, ending with the mounting holes of the amplifier over the mounting holes in the heatsink.
16. Attach the amplifier to the heatsink with 4-40x½' male-female hex spacers (not supplied). These spacers serve as alignment pins and aide in the assembly of the PCB to the heatsink. Alternatively, use 4-40x¼' machine screws to mount the amplifier to the heatsink. Do not over-tighten the spacers or screws as this provides no thermal benefit and may break the hardware.
17. Place the PCB assembly on the heatsink/amplifier assembly so that the hex spacers come through the aligning holes near the corners of the amplifier location in the PCB. Carefully lower the PCB assembly until the pins of the amplifier engage the cage jacks. Alternately, sight through the aligning holes in the PCB and match-up the PCB to the screws used to mount the amplifier. In either case be sure the pins of the amplifier are engaged with the cage jacks and then continue pushing the PCB assembly in the area between the amplifier's pins until the four spacer grommets at the four corners of the PCB touch the heatsink. At this point the PCB should not be bowed.
18. Using #8 X 1" sheet metal screws (not provided) mount the PCB to the heat sink at the four spacer-grommets.
19. Hook up power and signals as necessary. The amplifier is now ready for testing.

FIGURE 1: SCHEMATIC DIAGRAM

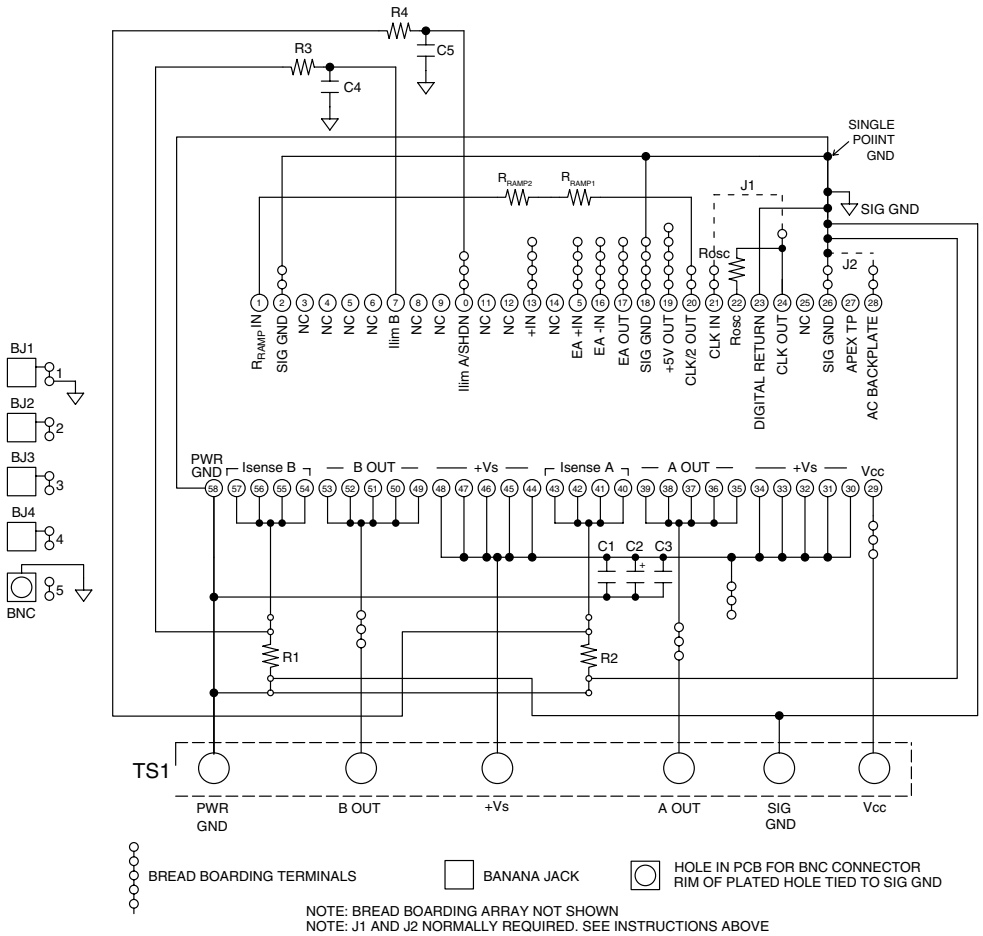
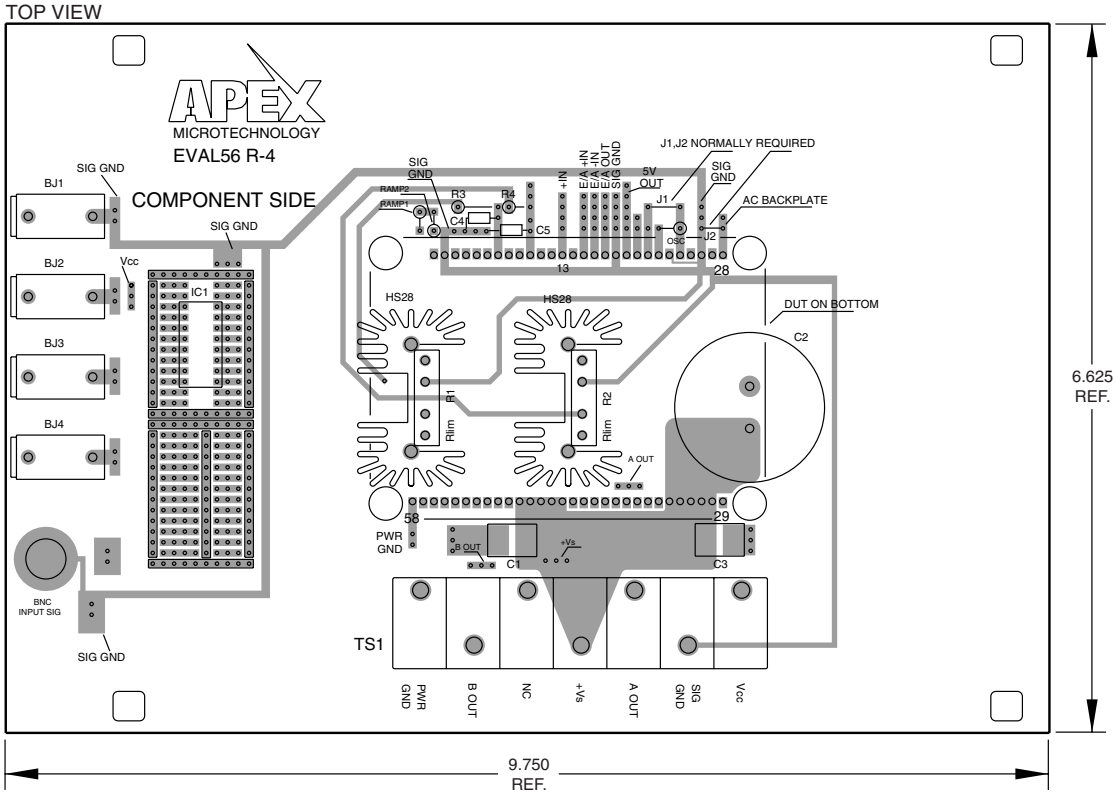


FIGURE 2:

TOP VIEW



BOTTOM VIEW

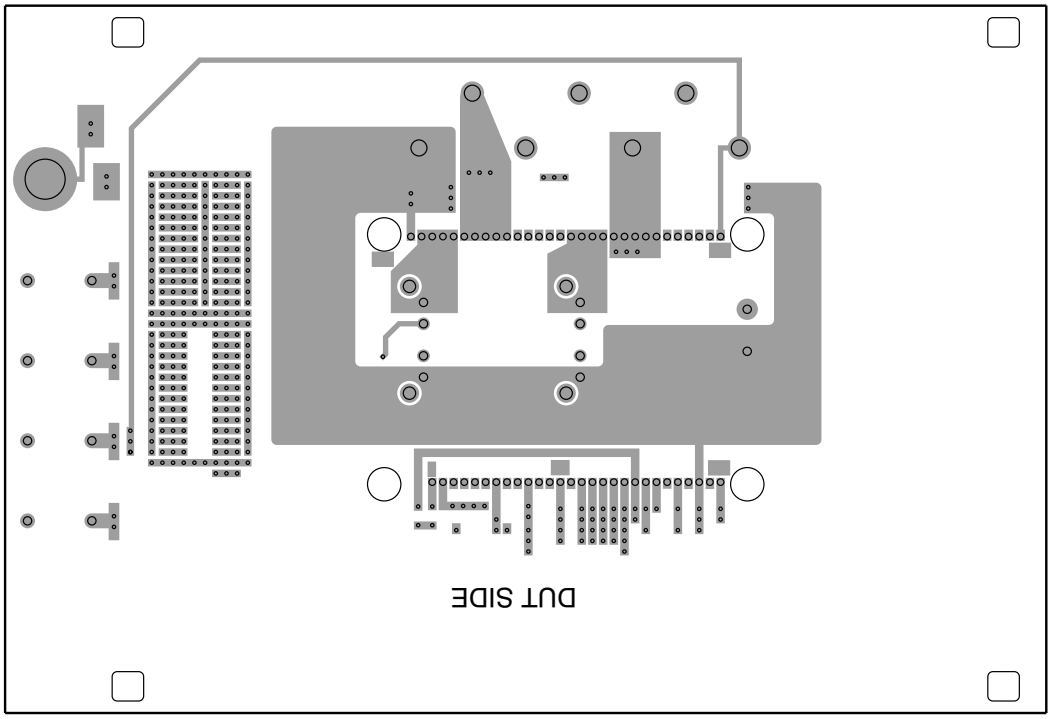
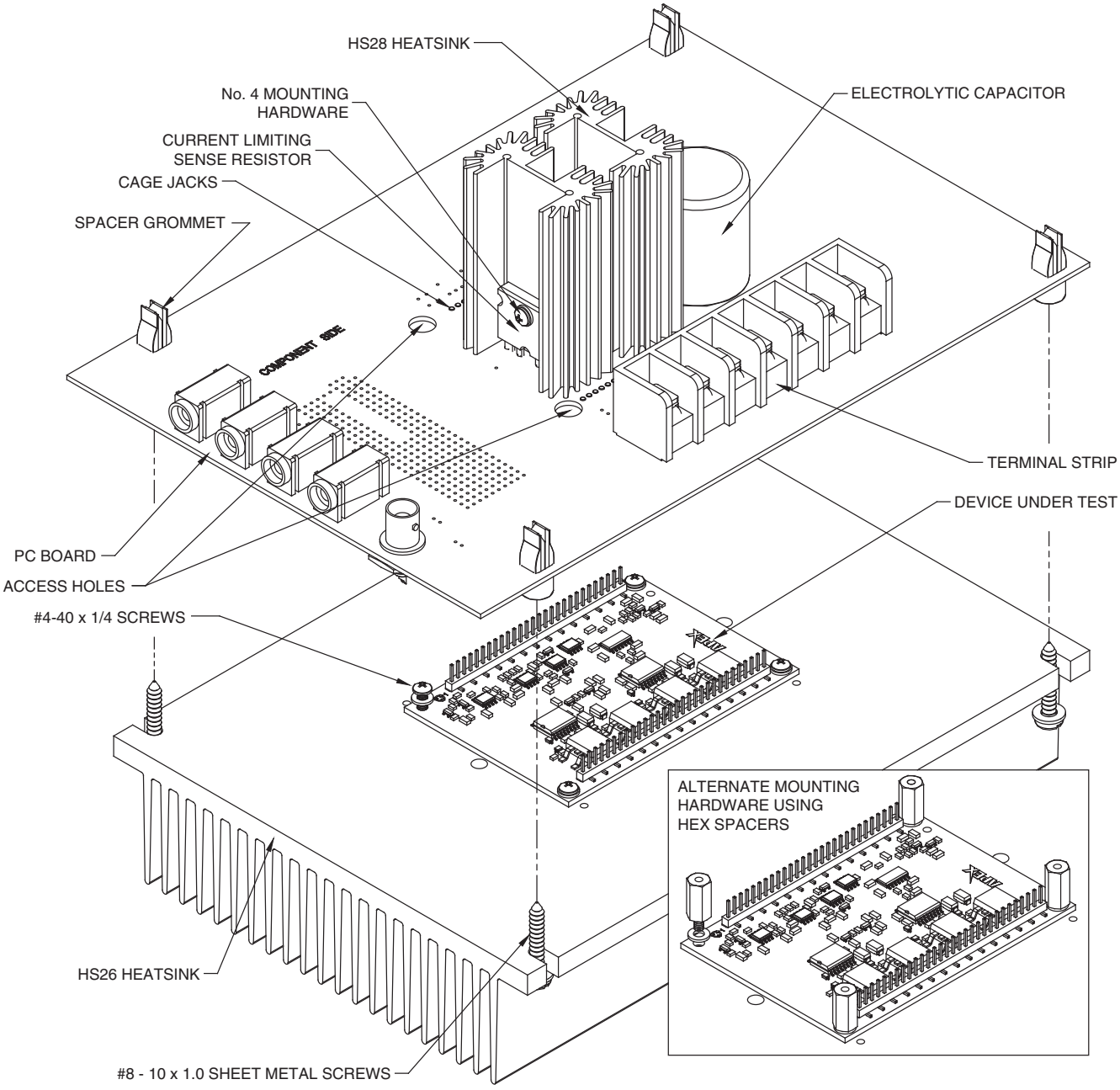


FIGURE 3:


HS28 HEATSINK
No. 4 MOUNTING HARDWARE
CURRENT LIMITING SENSE RESISTOR
CAGE JACKS
SPACER GROMMET
ELECTROLYTIC CAPACITOR
TERMINAL STRIP
DEVICE UNDER TEST
PC BOARD
ACCESS HOLES
#4-40 x 1/4 SCREWS
HS26 HEATSINK
#8 - 10 x 1.0 SHEET METAL SCREWS
ALTERNATE MOUNTING HARDWARE USING HEX SPACERS

Evaluation Kit for MP108FD and MP111FD

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the MP108FD & MP111FD pin out. With ample bread boarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal block and terminal pads at the edges of the circuit board. The terminal pads are suitable for soldering standard banana jacks or direct wiring of wires. Additionally, banana jacks and a BNC connector can be inserted into the holes at the edge of the board and wired to the numbered terminal pads.

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.

PARTS LIST

Ref	Apex Part #	Description/Vendor	Qty
NA	HS28	Heat Sink	1
NA	HS31	Heat Sink	1
NA	MS11	Strip of 30 cage jacks	2
NA	EVAL57	PC Board	1
NA	60SPG00004	Spacer Grommets/ Micro Plastics	4
C1,4,5,6	OX7R105KWN	1uF Cap/ Novacap 1825B105K201N	4
TS1	TS02	Terminal Strip	1
C2,3	EC03	680uF 200V/ United Chemi-Con KMH200VN681M25MX40T2	2
RLIM*	CSR18	0.050 Ohm Resistor/ Isotek PBV-R050-1	1
RLIM*	CSR19	0.100 Ohm Resistor/ Isotek PBV-R100-1	1

ASSEMBLY

During assembly refer to Figure 2 and the data sheet for the MP108FD & MP111FD.

1. Note that each side of the circuit board is identified as either the "component side" or "DUT side".
2. Cut the MS11 into groups of 16 and 18 cage jacks and insert from the "DUT side" of the board. On the "component side" of the board, solder all cage jacks having solder pads (7, 9, 10, 23, 24, 26, 29, and 31 have no solder pads). Make sure the cage jacks are fully seated before soldering. Be careful that solder does not flow into the cage jacks. Remove the unsoldered cage jacks with the carrier strip segments.
3. Solder the surface mount capacitors at C1, C4, C5, and C6 on the "component side" of the board.
4. Low ohm value resistors are provided with this evaluation kit: 0.050 ohm and 0.100 ohm. These are used to implement current limiting in the output circuit. Select the value most appropriate for your application. Refer to the product data sheet to determine which resistor value you should use.
5. Mount the HS28 heat sink to the PCB and solder the mounting tabs of the heat sink.
6. Apply a thin layer of thermal grease on the back of the chosen current limiting sense resistor, insert the resistor into the PCB and mount the resistor to the HS28 heat sink using #4 screw and nut hardware (not supplied). Be sure to cut off the excess resistor lead lengths.
7. Mount the electrolytic capacitors at C2 and C3 from the "component side" of the PCB. Match the polarity markings on the capacitor with the polarity markings on the PCB. Be sure the capacitors have snapped into the PCB and solder from the "DUT side" of the PCB. Be sure to fill the holes with solder.
8. Mount the terminal strip to the "component side" of the PCB. Make sure the terminal strip is fully seated and solder the pins from the "DUT side" of the PCB. Be sure to fill the mounting holes with solder.
9. Mount and wire the banana jacks and BNC connector (neither supplied) to the PCB pads at locations 1-5 as needed or desired.
10. Mount other components to complete your application circuit using the pads and holes provided.
11. From the "DUT side" of the PCB snap the spacer- grommets into the holes at the four corners of the PCB. Notice that the holes are slightly rectangular and match the spacer-grommet's long and short sides to the holes in the PCB.
12. Apply a thin, uniform layer of thermal grease to the amplifier; a straight edge may be useful here. Position the amplifier over the mounting holes in the heatsink. Firmly push the amplifier onto the heatsink while slightly rotating the amplifier back and forth, ending with the mounting holes of the amplifier over the mounting holes in the heatsink.
13. Attach the amplifier to the heatsink with 4-40x½' male-female hex spacers (not supplied). These spacers serve as alignment pins and aide in the assembly of the PCB to the heatsink. Alternatively, use 4-40x¼' machine screws to mount the amplifier to the heatsink. Do not over-tighten the spacers or screws as this provides no thermal benefit and may break the hardware.
14. Place the PCB assembly on the heatsink/amplifier assembly so that the hex spacers come through the aligning holes near the corners of the amplifier location in the PCB. Carefully lower the PCB assembly until the pins of the amplifier engage the cage jacks. Alternately, sight through the aligning holes in the PCB and match-up the PCB to the screws used to mount the amplifier. In either case be sure the pins of the amplifier are engaged with the cage jacks and then continue pushing the PCB assembly in the area between

ASSEMBLY CONT.

the amplifier's pins until the four spacer grommets at the four corners of the PCB touch the heatsink. At this point the PCB should not be bowed.

15. Use #8 X 1" sheet metal screws (not provided) to mount the PCB to the heat sink at the four spacer-grommets.
16. Inspect the assembly from the side and check that the PCB is not bowed toward the heat sink. If the PCB is bowed use a small tool to carefully pry the PCB away from the heat sink until the PCB is flat.
17. Hook up power and signals as necessary. The amplifier is now ready for testing.

FIGURE 1: SCHEMATIC DIAGRAM

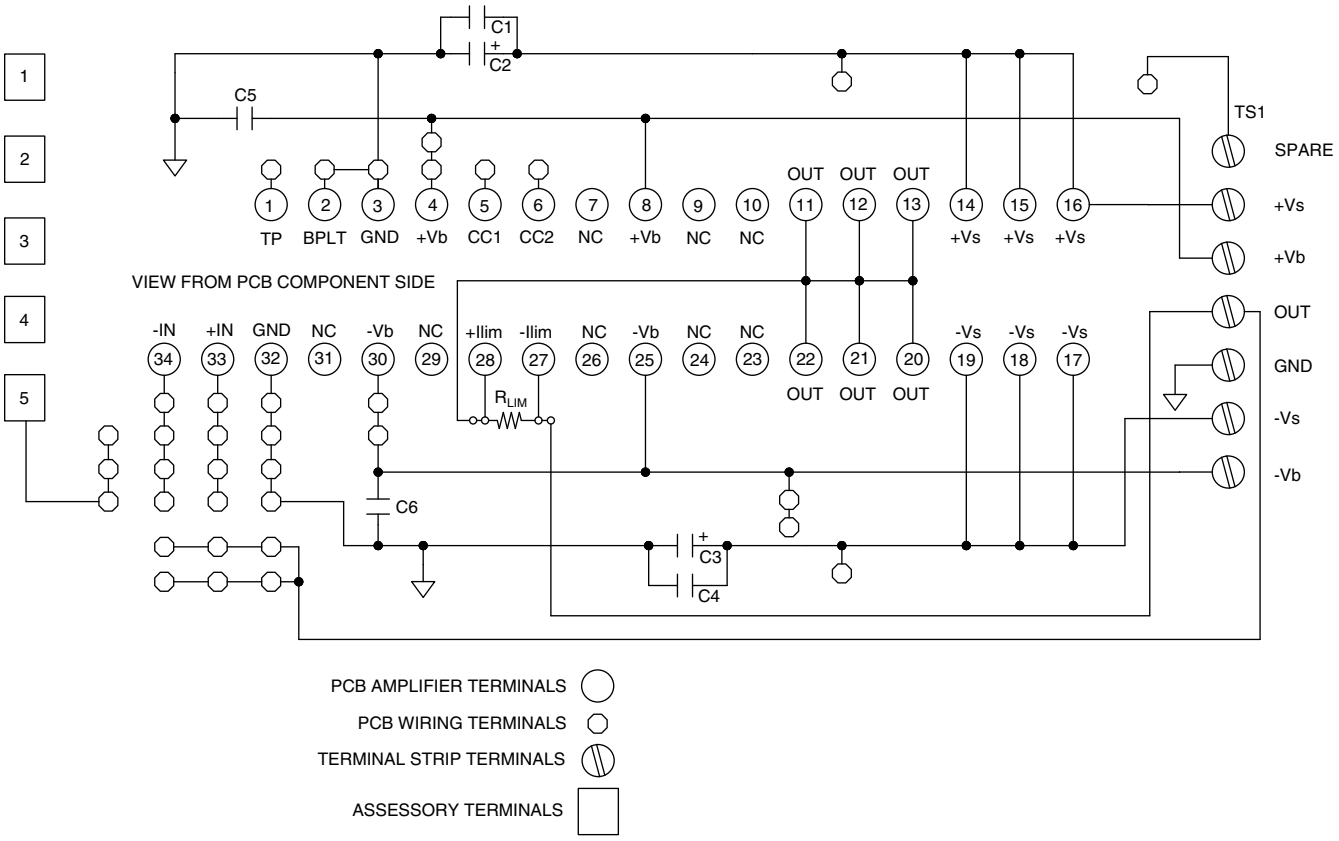
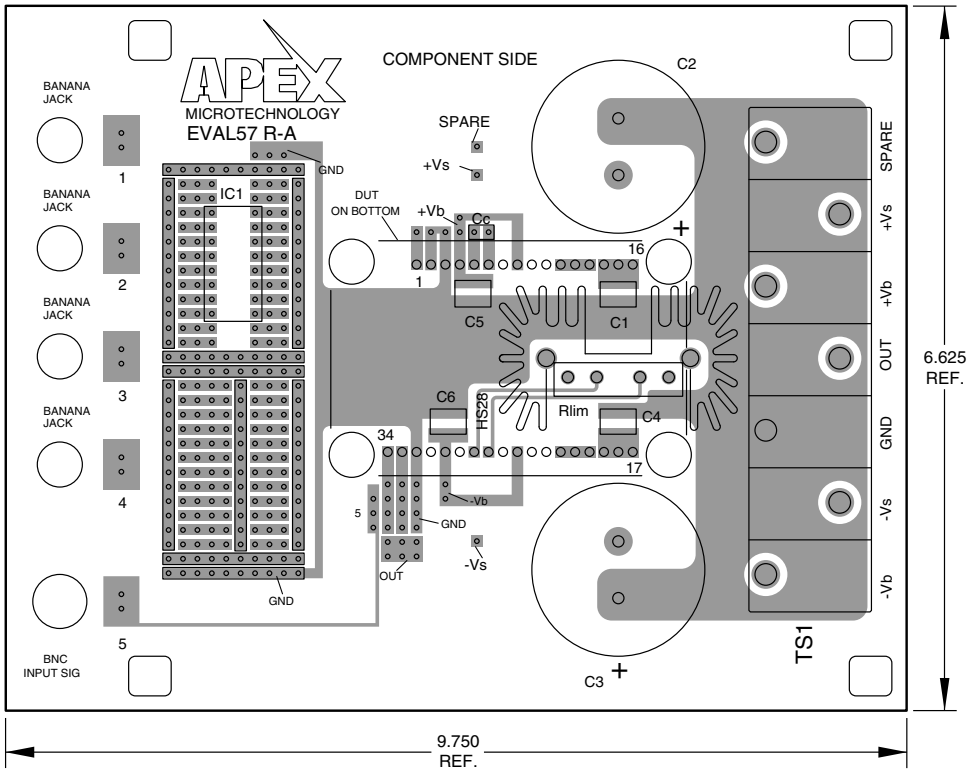


FIGURE 2:

TOP VIEW



BOTTOM VIEW

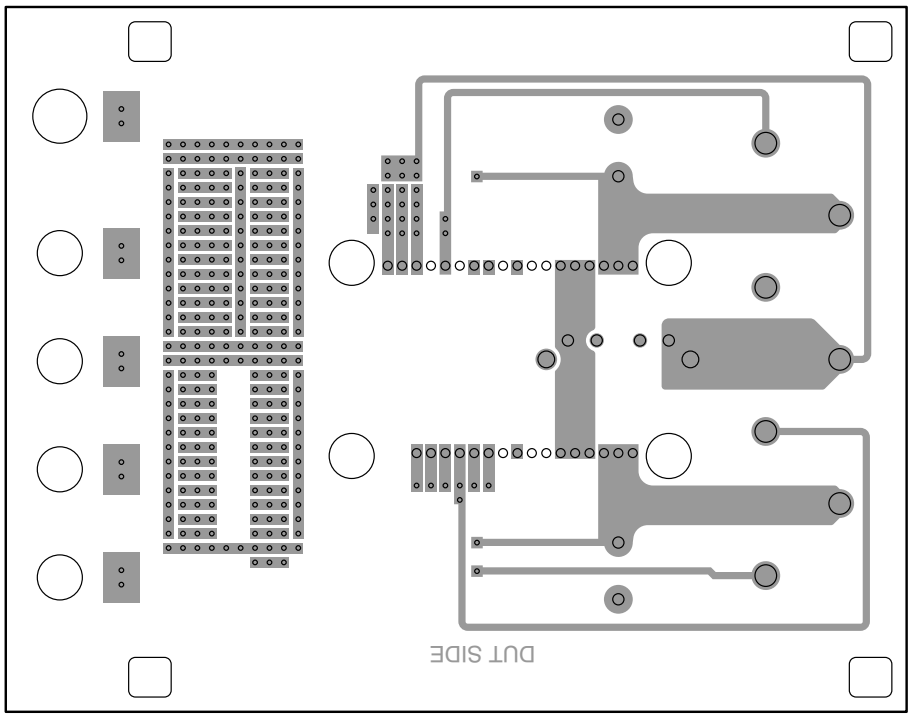
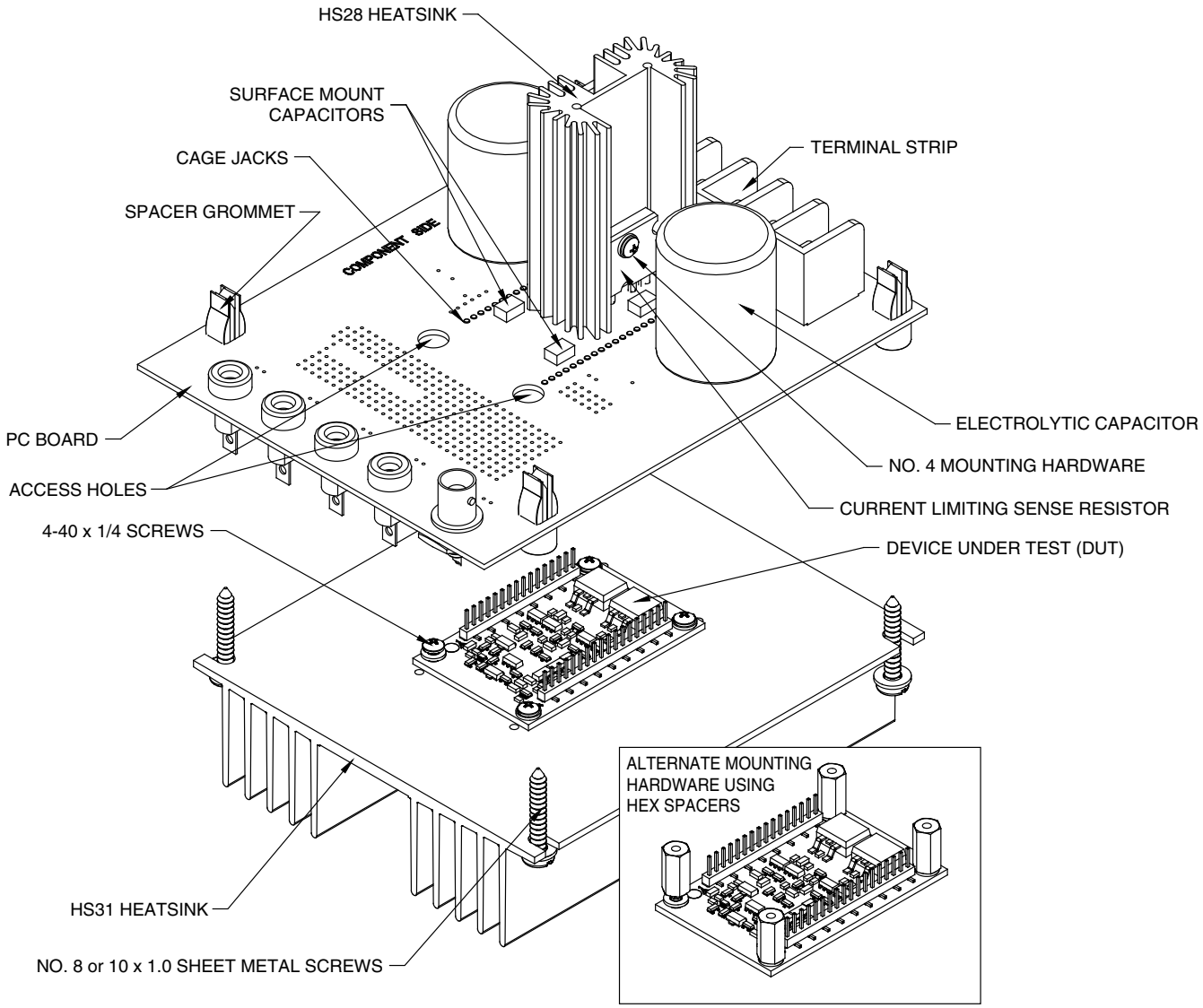


FIGURE 3:


HS28 HEATSINK
SURFACE MOUNT CAPACITORS
CAGE JACKS
SPACER GROMMET
COMPONENT SIDE
TERMINAL STRIP
ELECTROLYTIC CAPACITOR
NO. 4 MOUNTING HARDWARE
CURRENT LIMITING SENSE RESISTOR
DEVICE UNDER TEST (DUT)
PC BOARD
ACCESS HOLES
4-40 x 1/4 SCREWS
HS31 HEATSINK
NO. 8 or 10 x 1.0 SHEET METAL SCREWS
ALTERNATE MOUNTING HARDWARE USING HEX SPACERS

Evaluation Kit for MP38CL and MP39CL

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the MP38CL-39CL pin- out. With ample bread boarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal block and terminal pads at the edges of the circuit board. The terminal pads are suitable for soldering standard banana jacks or direct wiring of wires. Additionally, banana jacks and a BNC connector can be inserted into the holes at the edge of the board and wired to the numbered terminal pads.

BEFORE YOU GET STARTED

- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.

PARTS LIST

Ref	Apex Part #	Description/Vendor	Qty
NA	HS28	Heat Sink	1
NA	HS18	Heat Sink	1
NA	MS11	Strip of 30 cage jacks	1
NA	EVAL59	PC Board	1
NA	60SPG00004	Spacer Grommets/ Micro Plastics	4
C1-4	OX7R105KWN	1uF Cap/ Novacap 1825B105K201N	4
TS1	TS02	Terminal Strip	1
C2,3	EC03	680uF 200V/ United Chemi-Con KMH200VN681M25MX40T	2
R_{LIM}*	CSR18	0.050 Ohm Resistor/ Isotek PBV-R050-1	1
R_{LIM}*	CSR19	0.100 Ohm Resistor/ Isotek PBV-R100-1	1

ASSEMBLY

During assembly refer to Figure 1 and the data sheet for the MP38CL & MP39CL.

1. Note that each side of the circuit board is identified as either the "component side" or "DUT side".
2. Cut the MS11 into groups of 14 and 16 cage jacks and insert from the "DUT side" of the board. On the "component side" of the board, solder all cage jacks having solder pads (3, 5, 7-11, 21, 22, and 27 have no solder pads). Make sure the cage jacks are fully seated before soldering. Be careful that solder does not flow into the cage jacks. Remove the unsoldered cage jacks with the carrier strip segments.
3. Solder the surface mount capacitors at C1, C4, C5, and C6 on the "component side" of the board.
4. Mount diodes at D1 and D2 and transorbs at D3 and D4 on the "component side" of the board (none supplied) as needed by your application. See Application Note 1 paragraphs 4.3 and 9.1.
5. Mount the electrolytic capacitors at C2 and C3 from the "component side" of the PCB. Match the polarity markings on the capacitor with the polarity markings on the PCB. Be sure the capacitors have snapped into the PCB and solder from the "DUT side" of the PCB. Be sure to fill the holes with solder.
6. Low ohm value resistors are provided with this evaluation kit: 0.050 ohm and 0.100 ohm. These are used to implement current limiting in the output circuit. Select the value most appropriate for your application. Refer to the product data sheet to determine which resistor value you should use.
7. Mount the HS28 heat sink to the PCB and solder the mounting tabs of the heat sink.
8. Apply a thin layer of thermal grease on the back of the chosen current limiting sense resistor, insert the resistor into the PCB and mount the resistor to the HS28 heat sink using #4 screw and nut hardware (not supplied). **Be sure to cut off the excess resistor lead lengths.**
9. Mount the terminal strip to the "component side" of the PCB. Make sure the terminal strip is fully seated and solder the pins from the "DUT side" of the PCB. Be sure to fill the mounting holes with solder.
10. Mount and wire the banana jacks and BNC connector (neither supplied) to the PCB pads at locations 1-5 as needed or desired.
11. Mount other components to complete your application circuit using the pads and holes provided.
12. From the "DUT side" of the PCB snap the spacer- grommets into the holes at the four corners of the PCB. Notice that the holes are slightly rectangular and match the spacer-grommet's long and short sides to the holes in the PCB.
13. Apply a thin, uniform layer of thermal grease to the amplifier; a straight edge may be useful here. Position the amplifier over the mounting holes in the heatsink. Firmly push the amplifier onto the heatsink while slightly rotating the amplifier back and forth, ending with the mounting holes of the amplifier over the mounting holes in the heatsink.
14. Attach the amplifier to the heatsink with 4-40x½' male-female hex spacers (not supplied). These spacers serve as alignment pins and aide in the assembly of the PCB to the heatsink. Alternatively, use 4-40x¼' machine screws to mount the amplifier to the heatsink. Do not over-tighten the spacers or screws as this provides no thermal benefit and may break the hardware.
15. Place the PCB assembly on the heatsink/amplifier assembly so that the hex spacers come through the aligning holes near the corners of the amplifier location in the PCB. Carefully lower the PCB assembly until the pins of the amplifier engage the cage jacks. Alternately, sight through the aligning holes in the PCB and match-up the PCB to the screws

ASSEMBLY CONT.

used to mount the amplifier. In either case be sure the pins of the amplifier are engaged with the cage jacks and then continue pushing the PCB assembly in the area between the amplifier's pins until the four spacer grommets at the four corners of the PCB touch the heatsink. At this point the PCB should not be bowed.

16. Use #8 X 1" sheet metal screws (not provided) to mount the PCB to the heat sink at the four spacer-grommets.
17. Inspect the assembly from the side and check that the PCB is not bowed toward the heat sink. If the PCB is bowed use a small tool to carefully pry the PCB away from the heat sink until the PCB is flat.
18. Hook up power and signals as necessary. The amplifier is now ready for testing.

FIGURE 1: SCHEMATIC DIAGRAM

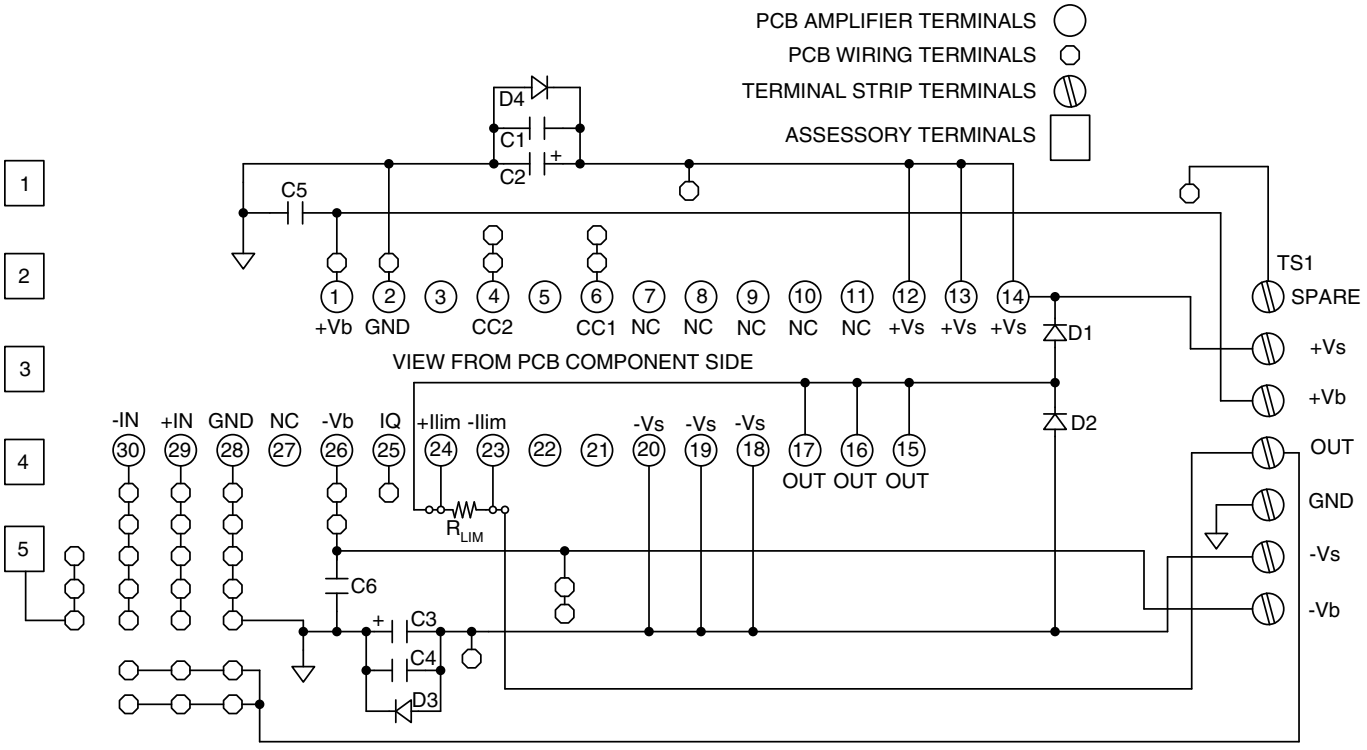


FIGURE 2:

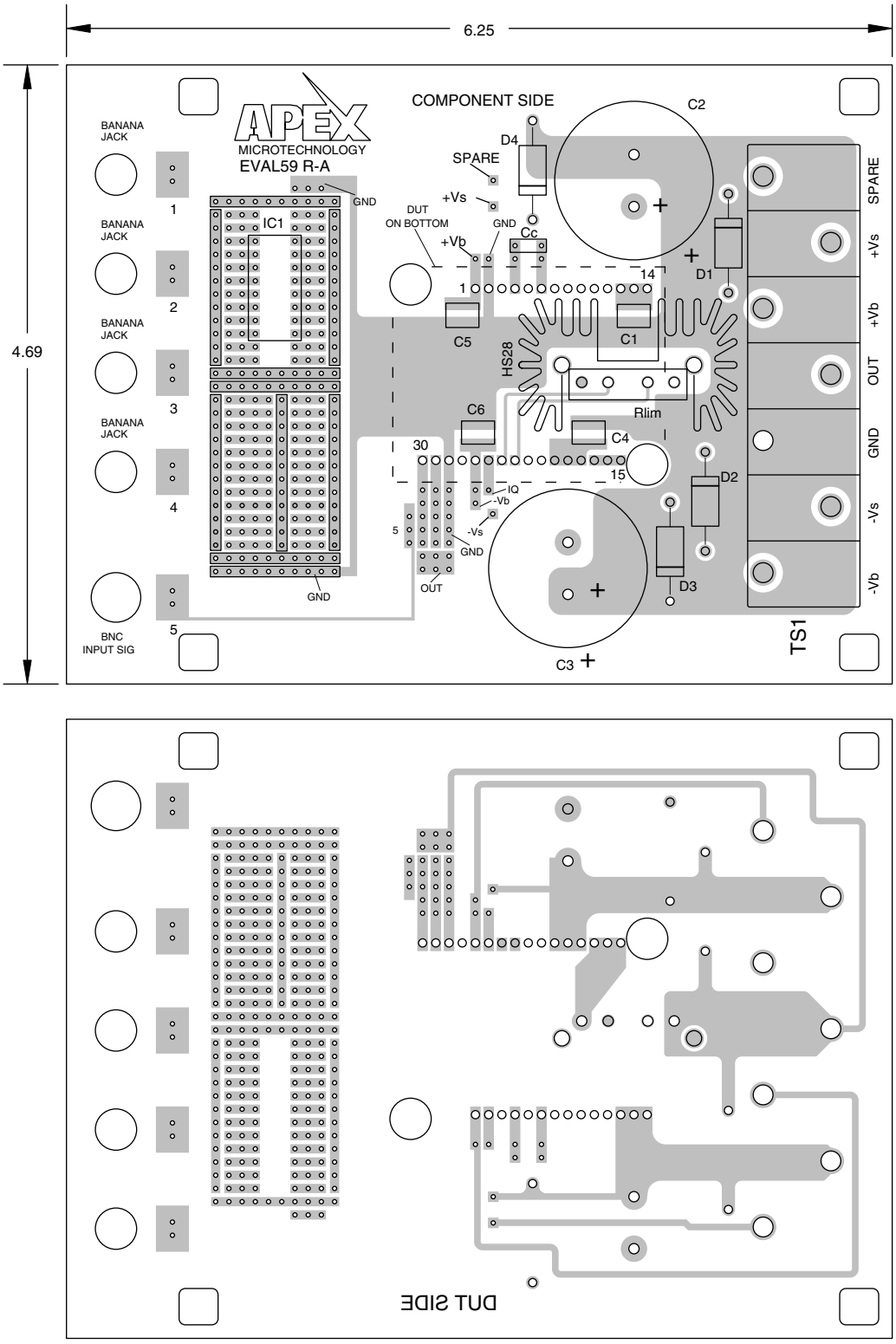
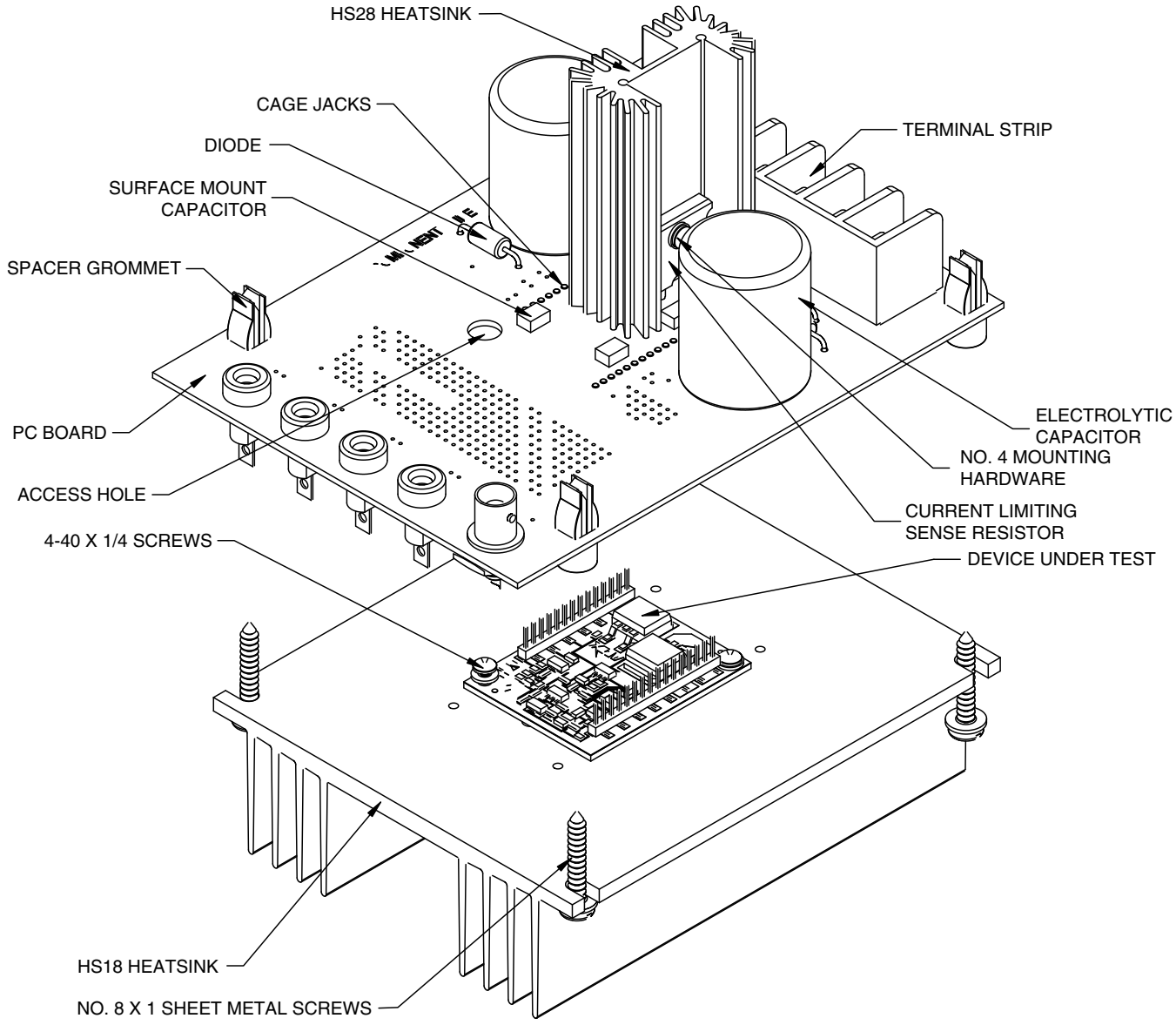

6.25
4.69
COMPONENT SIDE
MICROTECHNOLOGY
EVAL59 R-A
BANANA JACK
BNC INPUT SIG
IC1
GND
SPARE
+Vs
DUT ON BOTTOM
+Vb
Cc
D4
C2
D1
C5
C1
HS28
C6
Rlim
C4
D2
D3
C3
IQ
-Vb
-Vs
OUT
TS1
DUT SIDE

FIGURE 3:


HS28 HEATSINK
CAGE JACKS
DIODE
SURFACE MOUNT CAPACITOR
SPACER GROMMET
PC BOARD
ACCESS HOLE
4-40 X 1/4 SCREWS
HS18 HEATSINK
NO. 8 X 1 SHEET METAL SCREWS
TERMINAL STRIP
ELECTROLYTIC CAPACITOR
NO. 4 MOUNTING HARDWARE
CURRENT LIMITING SENSE RESISTOR
DEVICE UNDER TEST

F

Evaluation Kit for PA78EU Pin-Out

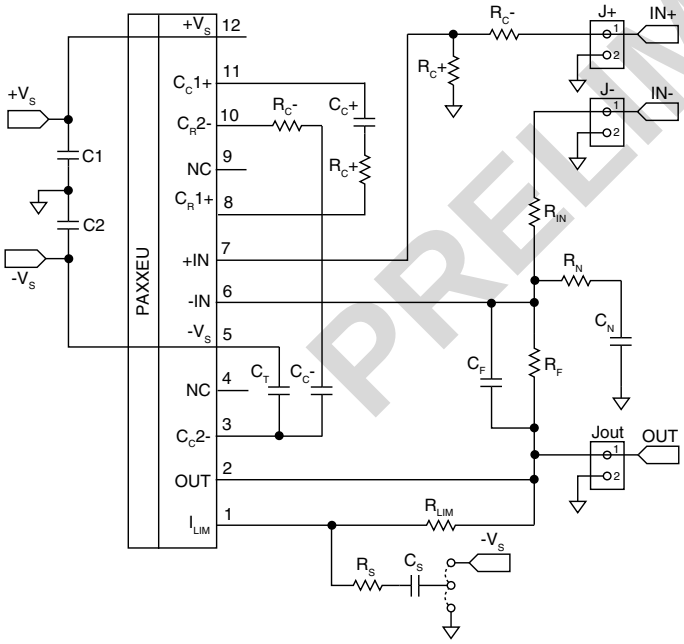
INTRODUCTION

The EK60 evaluation kit is designed to provide a convenient way to breadboard design ideas for the PA78EU power operational amplifiers. The EVAL60 evaluation board is pre-wired for all required and recommended external components including the ones for power supply bypassing, compensation and current limiting. The EVAL60 also includes a breadboard area for constructing your application circuit with provisions for a preamplifier to drive the PA78 inputs.

PARTS LIST

Apex Part #	Description	Quantity
HS27	Heatsink, Apex	1
EVAL60	PC Board, Apex	1
TW12	Thermal Washer, Apex	1 Box
OX7R105KWN	1 uF Cap 3530B105K501N Novacap, ***200V Breakdown***	2
140-500N5-330J	33pF Cap CDR-500N5-330KS XICON	1
146510CJ	BNC Connector	3
MS02	Socket Strip	1 bag
MS11	Socket Strip	1 bag

EK60 SCHEMATIC



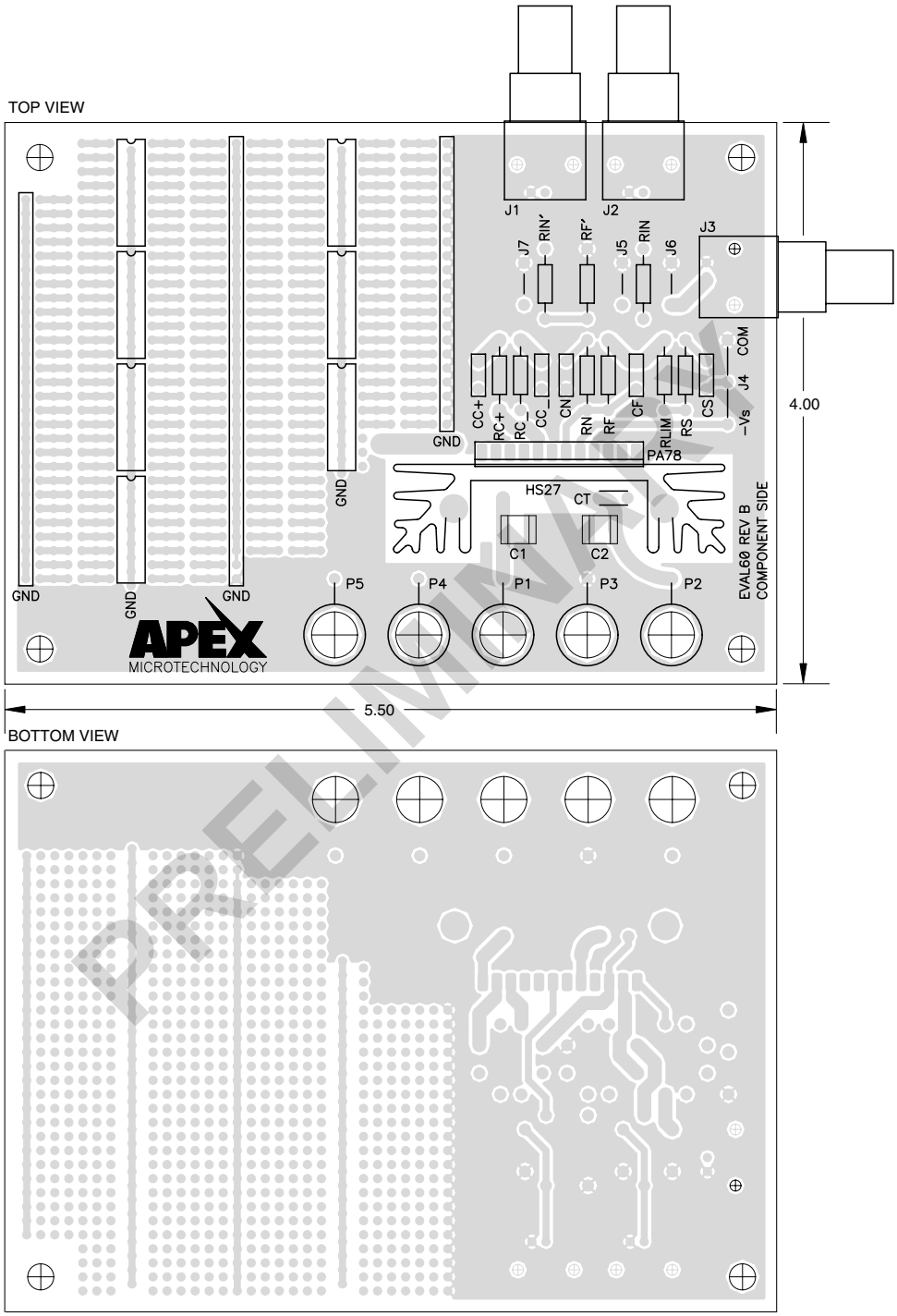
Jumper Cs to GND or -Vs for snubber if needed.
PACKAGE TAB CONNECTED TO STABLE REFERENCE
Breakdown voltage of C1 & C2 is 200V max.

ASSEMBLY

During assembly refer to Figure 1 and Figure 2.

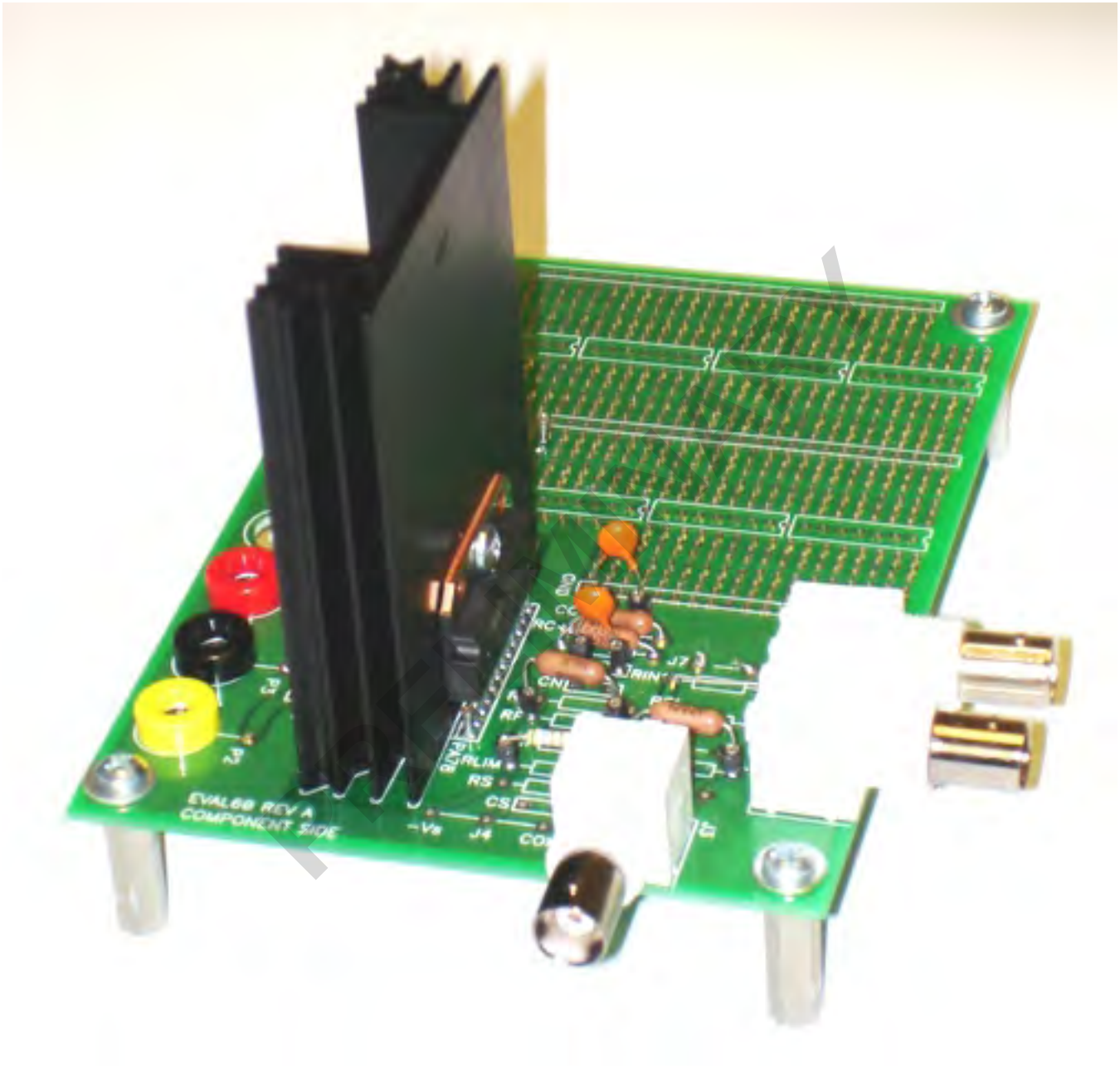
1. Solder surface mount ceramic capacitors C4 and C5 on the DUT side of the board.
2. Add components for compensation (CC-, CC+, RC- and RC+) based on the closed loop gain and capacitive load. Add the current limit resistor (RLIM) based on load requirements (a minimum value of 4.5 ohms should be used to protect the PA78 internal output devices). It is recommended to use MSO2 sockets for the components for quick component changes on the board. Add 33pF capacitor (CT) between DUT pins 3 and 5.
3. While developing your application circuit you will probably want to use the mating socket strip. Use the MS11 socket strip for mounting the PA78 EU. Clip off the strip after the 12th position. Insert the strip into the circuit board on the DUT side and solder one pin on the reverse side. Check whether the mating socket strip is fully seated against the circuit board and then solder the remaining pins. Insert the amplifier fully into the socket strip, noting the pin 1 location on the amplifier and the circuit board.
4. For high power applications (see PA78EU datasheet for SOA considerations) mount the heat sink (HS27) in the outlined area on the circuit board.
5. If a heat sink is used, position the thermal washer behind the amplifier in such a way that the hole on the washer coincides with the hole on the tab and the heat sink.
6. **For high slew rate performance connect the heat tab to a stable reference (see PA78U datasheet for details).**
7. Install the banana jacks for P1 (+Vs), P2 (-Vs) and P3 (GND) as shown in figure 1 and 2. There are provisions for two extra banana jacks (P4 and P5) and can be used if desired for external connections.

Figure 1: PCB Layout



F

Figure 2: Assembled PCB



Evaluation Kit for PA78DK & PA79DK

INTRODUCTION

Fast and easy breadboarding of circuits using the PA78DK or PA79DK is possible with the EK61 evaluation kit. The EK61 includes both the universal EVAL36 board and the EVAL61 substrate. The use of EVAL36 and EVAL61 allows for a large area of breadboarding space to work with while allowing a surface mount substrate for the PA78DK or PA79DK. The PA78DK or PA79DK amplifier may be surface mounted directly to the EVAL61, a thermally conductive but electrically isolated substrate. The PA78DK or PA79DK is soldered to a DUT foil footprint area the size of the heatslug as shown in Figure 1. The metal substrate is cost effective and can allow the PA78DK or PA79DK to dissipate power up to the datasheet rating.

Part Number	Alternate P/N	Designator/Reference	Quantity
C1206X103K631RT	ECJ-3FB2J103K	C1,C5,C9,C10	4
C1210N4R7C501N	SQCB7M4R7CAJME	C3,C4,C6,C7	4
C1206N330J501RT	12067A330JAT2A	C2,C8	2
R1206000ZRT	ERJ-8GEYJR00V	J2 (GND)	1
R1206302JRT	ERJ-8GEYJ302V	R1,R2,R3.R4	4
EVAL61		Evaluation substrate	1
EVAL36		Universal PC Board	1
TSM-116-01-T-SV		Terminal Strip, 16 PIN	2
SSW-116-01-T-S		Socket Strip, 16 PIN	2
PA79DK		DUT	1
*031606		5V, 10mA, 3.4°C/W heatsink with fan, AAVID	1

* Parts are not supplied. Parts are application dependant. Suggested part numbers are provided.

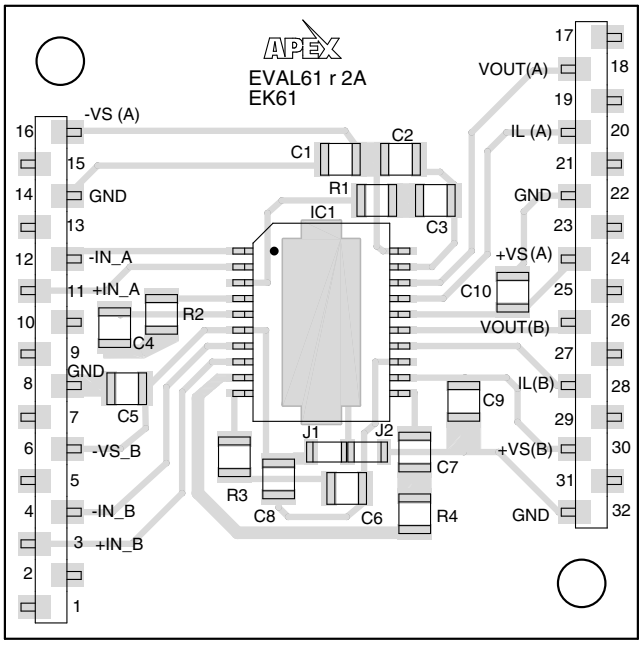


Figure 1 - PCB

BEFORE YOU GET STARTED

- All Apex Precision Power™ amplifiers should be handled using ESD precaution.
- Review the Apex Precision Power™ product datasheet and operating conditions.
- Always provide the appropriate heat sinking. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
- Always use adequate power supply bypass capacitors, Apex Precision Power™ recommends at least 10µF per amp of output current.
- Do not change connections while the circuit is powered
- In case -Vs is disconnected before +Vs, a diode between -Vs and ground is recommended to avoid damage.
- Initially set all power supplies to the minimum operating levels allowed in the product datasheet.
- Check for oscillations up to and above the unity gain bandwidth of the amplifier.

ASSEMBLY

The PA78DK & PA79DK are surface mount device and should be assembled to the EVAL61 substrate using surface mount processes. Solder paste may be dispensed or screen-printed on the DUT pads. The heat slug on the back of the PA78DK & PA79DK provides maximum heat dissipation capabilities when soldered to the foil footprint area. The PA78DK & PA79DK should be reflowed to the substrate using a solder reflow furnace. If this is not available, a heat plate capable of solder reflow temperatures may be used.

In accordance with the PA78DK and PA79DK datasheets, the package tab must be connected to a stable voltage reference in order to achieve high slew rates. Jumpers J1 and J2 allow convenient connection of the tab to -Vs or GND, respectively. Connect only one jumper to avoid a short circuit of the power supply.

Once the amplifier is mounted on the top of the substrate, the heat sink fan or selected heat sink can then be mounted to the back of the substrate. A heat sink is not supplied with the kit, but several options are available through AAVID Thermal Product, Inc. High thermal conductive thermal grease should be used when mounting the heat sink fan or heat sink to the evaluation board.

Review Figure 3 on next page for other possible assembly methods to construct this evaluation kit.

NOTE: All grounds must be tied together on the EVAL36 board.

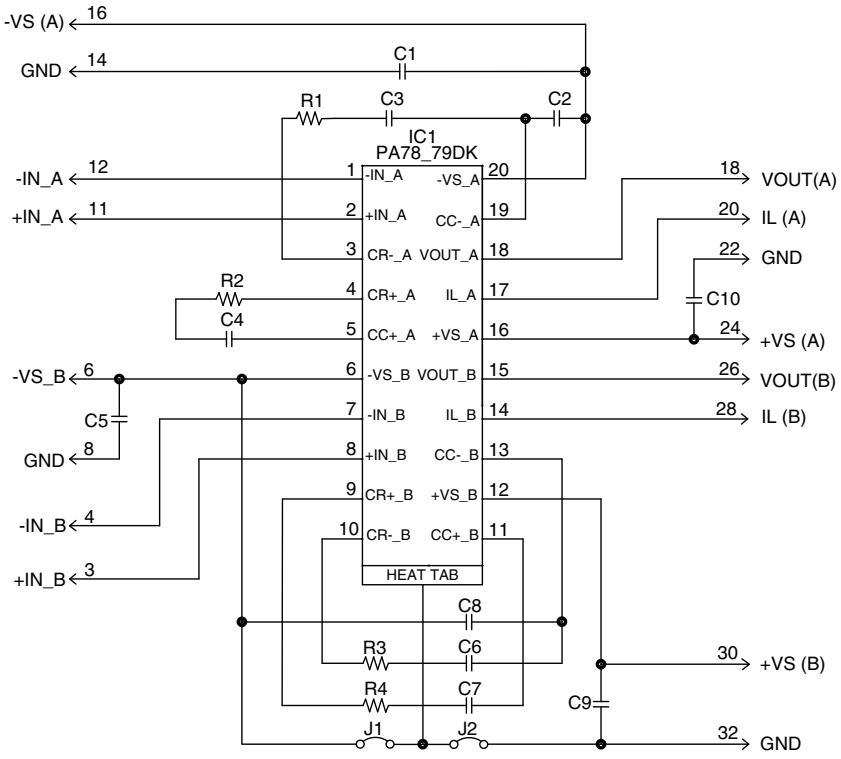


Figure 2 - Schematic

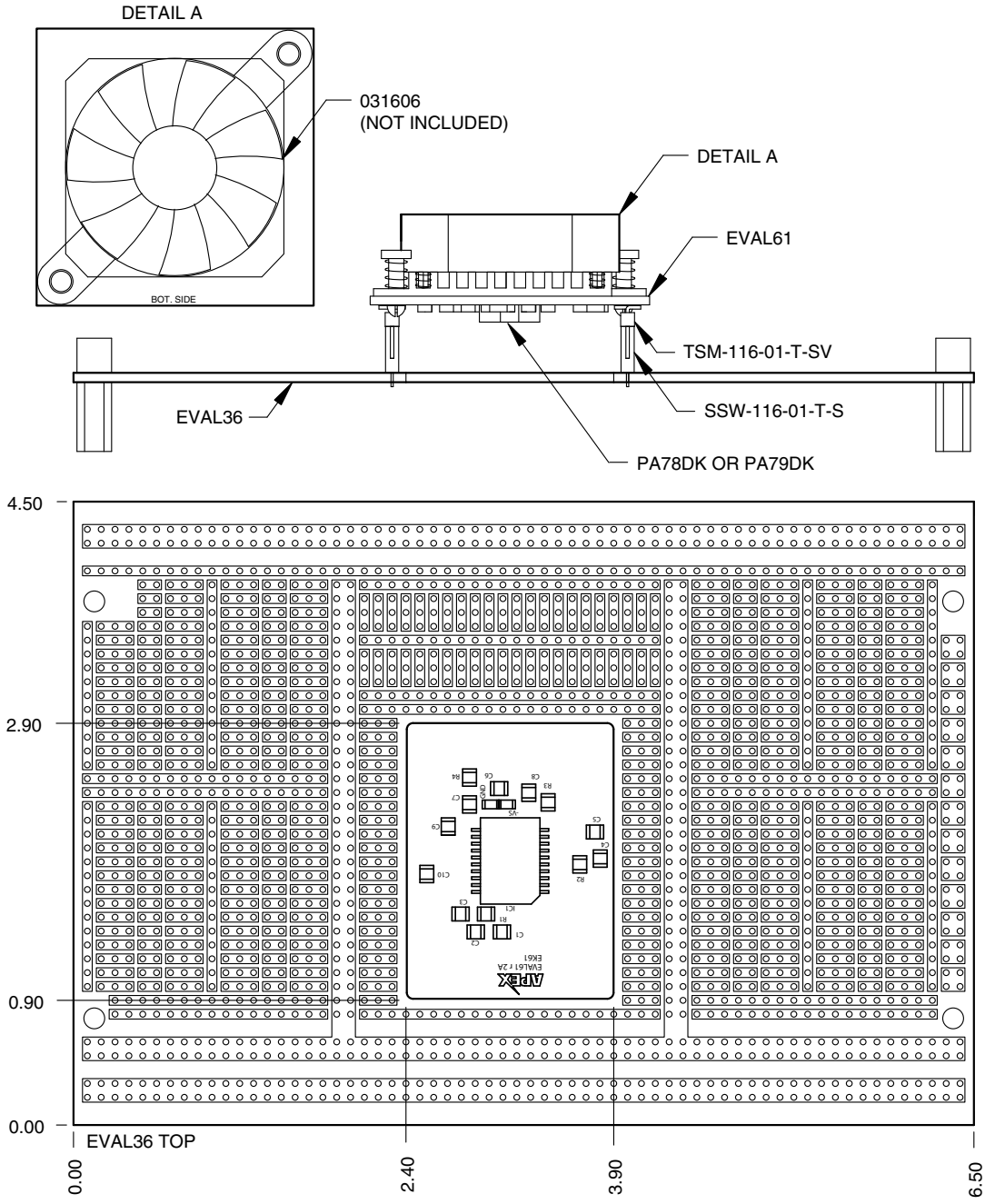


Figure 3 - Assembly

Evaluation Kit for MP400FC

Introduction

The EK65 Evaluation kit is designed to provide a convenient way to breadboard and evaluate design ideas for the MP400FC power operational amplifier. The evaluation board is pre-wired for all required external components. The evaluation board has been laid out and labeled to easily configure the high voltage operational amplifier in a non-inverting differential configuration for single supply operation using the MP400FC boost supply (Refer to Application Note 21). However, the evaluation board is flexible enough to analyze a multitude of standard or proprietary circuit configurations.

Before You Get Started

- Please read this data sheet in it's entirety before starting to construct your evaluation board.
- All APEX amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.
- The MP400FC is a high voltage amplifier with an integrated switch mode power supply. Though the input voltage will be 50V or less, the MP400FC can generate voltages greater then 350V. The high generated voltage will be present on the evaluation board. Caution must be used when working with the evaluation board.

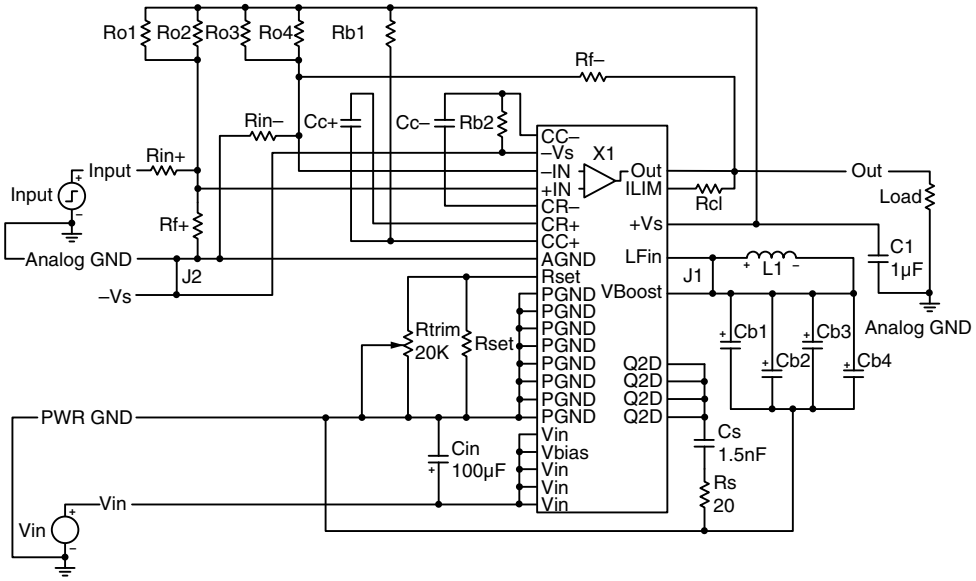


Figure 1 - EK65 Schematic

Parts List (Included with kit)

Ref.	Apex P/N	Description/Vendor	Qty.
N/C	HS26	Heat Sink	1
N/C	MS11	Strip of 30 cage jacks	2
N/C	EVAL65	PC board	1
N/C	93505A430	Hex standoff, 4-40x1/4	4
N/C	90272A105	Screw, 4-40x3/16	4
BJ1-6	571-0100	Banana Jack, PC	6
BN1	146510CJ	BNC, PC mount	1
C1	ZX7R105KTL	Cap. 1 µF, 500V Novacap ST2225B105K501LLXW	1
Cb1	EKMQ401VSN121MP30S	Cap. 120µF, 400V	1
Rtrim	T93YA203KT20	Trim Pot, 20K	1

Required Components (Not included with kit)

Ref. Description

Cin Capacitor, Low ESR electrolytic, 100µF or greater with voltage rating greater then the anticipated input voltage.

Cb1-4 Cboost capacitor, Low ESR electrolytic with voltage rating greater then the anticipated boost voltage. Refer to the MP400FC data sheet for Cboost selection. One 120µF, 400V electrolytic capacitor (Cb1) is supplied with the kit and is adequate for most applications. The value of Cboost is selected to meet required boost supply ripple voltage specifications for the application and to minimize switching noise on the boost supply. Cboost will be as large as reasonably possible, in the range of 100µF to 500µF. An area on the evaluation board large enough for 4 parallel 22mm diameter capacitors is provided. This allows maximum flexibility in the select of the capacitors for Cboost. Capacitors with snap in terminals should still be soldered to the evaluation board to minimize resistance.

Rset Boost voltage programming resistor. Refer to the MP400FC data sheet for calculation of Rset. Select a higher standard value resistor and use Rtrim (supplied) to calibrate the boost voltage to the exact desired value. Alternatively, Rtrim can be used alone for a fully adjustable boost supply.

Rcl Operational amplifier current limit resistor. Refer to the MP400FC data sheet for selection of the current limit resistor.

Optional Components (Not included with kit)

Ref. Description

Lf Boost supply filter inductor. The MP400FC includes a 47µH inductor in series with the LFin pin and the +Vs supply of the high voltage op amp. This on board inductor forms a 2 pole LC filter with C1 and an on board parallel 0.1µF capacitor. Combined with a properly selected Cboost, the high voltage DC boost voltage will be sµfficiently clean for most applications. However an external inductor between Vboost and LFin, or Vboost and +Vs can be used for additional filtering of the Boost supply voltage if necessary. Addition capacitance can be added to the filter between +Vs and AGND.

Cs, Rs Also useful for boost supply filtering. These components form an RC snubber from drain to source of the boost supply MOSFET switch. This snubber will help reduce or eliminate overshoot and ringing of the MOSFET switch at switch turn-off that can appear on the boost supply voltage. The component values shown on the schematic are adequate for most applications but can be adjusted for your specific application. The power in the resistor can be estimated by the formula PD = F*C*V2, where

F = 100 KHz of the switching supply

C = the value of Cs

V = the anticipated Vboost voltage.

Rs must be non-inductive. MP900 and MP9000 series resistors from Caddock Electronics or equivalent resistors can be used.

Rs may require a heat sink such as Apex part number HS28 or HS23. Mounting holes for a heat sink are provided on the evaluation board that will accommodate either of these heat sinks.

Cc+, Cc- High voltage op amp compensation capacitors. Refer to the MP400FC data sheet for component selection.

Ro1-4, Rf+, Rf-, Ri+, Ri- Op amp gain setting and input bias resistors used for the single supply differential configuration described in applications note 21. Appendix A of apps note 21 provides a procedure for the design of the differential configuration and selection of these components. Apps note 21 can be down loaded from the Apex web site. The locations on the board for Ro1-4 are large enough for up to a 3W resistor. 3W 1% resistor style CPF from Vishay Dale are widely available through distribution. RN60, RN65 or RN70 style 1/2W 1% resistors can be used for the other resistors.

Assembly

During assembly, refer to Figure 1, Figure 2 and the MP400FC data sheet.

1. Note that the silk screen side of the circuit board is labeled as the “component side”. The other side of the circuit board will be referred to in these instructions as the “DUT side” of the board.

2. The Analog ground AGND and power ground PGND are clearly labeled on the boards. All components for the on board boost supply are referenced to PGND, and all components for the high voltage op amp are referenced to AGND. The board has been designed to keep switching currents from the boost supply out of the analog ground. AGND and PGND are common at only one point on the MP400, and are not connected at all on the evaluation board. To avoid ground loops and switching currents in the analog ground, avoid making any connections between these two ground references at the board level. Note the dashed line on the component side of the board showing the dividing line between the analog ground side of the board and the power ground side.
3. Cut one of the MS11 strips to a length of 20 cage jacks and the other MS11 to a length of 22 cage jacks. From the DUT side of the board, insert the strips into the appropriate row of holes for the DUT pins. On the component side of the board, solder all cage jacks having solder pads (pins 3, 5, 7, 9, 11, and 16 have no solder pads). Make sure the cage jacks are fully seated before soldering. Be careful that solder does not flow into the cage jacks. Remove the unsoldered cage jacks with the carrier strip segments.
4. Solder the ZX7R105KTL surface mount capacitor at C1 on the component side of the board.
5. Insert BJ1 – BJ6 from the component side of the board as desired for your application. The banana jack locations are labeled with the associated input or output. BJ1 is provided for use as an input for a negative bias supply voltage to –Vs for bipolar supply operation. It also could be used as an alternative to the BNC connector for the input signal or other inputs to your application circuit. If you do not anticipate using BJ1 it should be left off. Solder the banana jacks to the board from the DUT side.

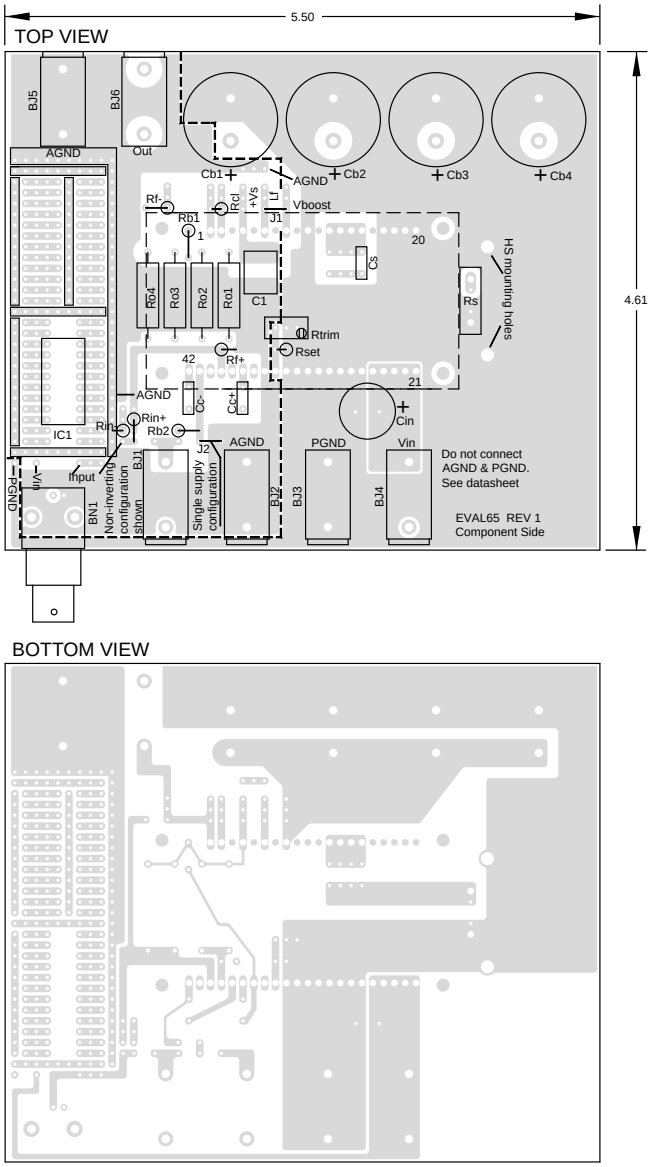


Figure 2 - EVAL65 PCB Layout

6. Insert the BNC connector BN1 from the component side of the board. Solder to the board from the DUT side. BN1 can be left off if you do not intend to use it for an input to your circuit.
7. Select and insert Rset from the component side of the board at the location shown near pin 34 of the DUT and solder from the DUT side. Rtrim may be installed for calibration of the boost supply voltage or as an alternative to Rset. If installed as shown on the board with the knob toward Cin, a CW turn will increase Vboost and a CCW turn will decrease Vboost.
8. Select and insert Rcl from the component side at the location marked for Rcl between pins 1 and 2 of the DUT. Solder from the DUT side.
9. Select and insert other components as required for your application. J1 is required to supply Vboost to the high voltage op amp through the on board 47µH filter inductor. Vboost can be jumpered to the +Vs pin if the filter is not to be used. Alternatives are to replace the jumper with an external inductor between the Vboost pin and LFin or +Vs. A filter capacitor can be added between +Vs and AGND. You may want to start with J1 as shown and try other options as you are evaluating your design.

10. J2 is required to connect the high voltage op amp –Vs to AGND for single supply operation. If an external negative supply voltage will be used, replace J2 with a high quality ceramic bypass capacitor of at least 1µF, and jumper –Vs to BJ1. BJ1 can be used to connect the negative supply to the evaluation board.
11. Rin+ and Rin- when installed as marked on the component side of the board near BJ1 and BN1, will configure the op amp in the non-inverting configuration with Rin- to AGND and Rin+ to the input BNC. For an inverting configuration, rotate Rin+ to AGND and Rin- to the input.
12. If the snubber Cs and Rs will be used, select and insert the components at the location marked near DUT pins 12 – 15. If the calculated power dissipation indicates that a heat sink is required for Rs, install it with Rs. Cs and Rs can be installed after you have started evaluating your design if they are found to be needed.
13. Vin power can be supplied to your circuitry in the breadboard area. There are two pads located below the breadboard area near BN1. One labeled Vin and one labeled PGND can be jumpered into your circuit as needed.
14. Mount the electrolytic capacitors at Cin, and Cboost from the component side of the PCB. Match the polarity markings on the PCB. Solder from the DUT side of the PCB. Be sure to fill the holes with solder.
15. Apply a thin, uniform layer of thermal grease to the back side of the MP400FC. Position the amplifier over the mounting holes of the HS26 heat sink. Firmly push the amplifier onto the heat sink while slightly rotating the amplifier back and forth, ending with the mounting holes of the amplifier over the mounting holes in the heat sink.
16. Attach the amplifier to the heat sink with the supplied 4-40 x 1/4” male-female hex spacer. Tightened with a hex nut driver. Make the hex spacers snug but do not over tighten as this provides no benefit and may break the hardware.
17. Carefully lower the PCB assemblies onto the heat sink/amplifier assembly until the pins of the amplifier engage in and are fully seated in the cage jacks aligning the mounting holes in the PCB to the hex spacers. Use the supplied 4-40 x 3/16” screws to attach the PCB assembly to the hex spacers.
18. Hook up power and signals as necessary. The amplifier is now ready for testing.

Figure 3 - EK65 Assembly

Evaluation Kit for the PA107

INTRODUCTION

The EK71 Evaluation kit is designed to provide a convenient way to breadboard and evaluate design ideas for the PA107 power operational amplifier. The evaluation board is pre-wired for all required external components. The evaluation board has been laid out and labeled to easily configure the high voltage operational amplifier in an inverting configuration. However, the evaluation board is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminal connectors at the edge of the circuit board. These connectors are suitable for standard banana plugs. The schematic is shown in Figure 1.

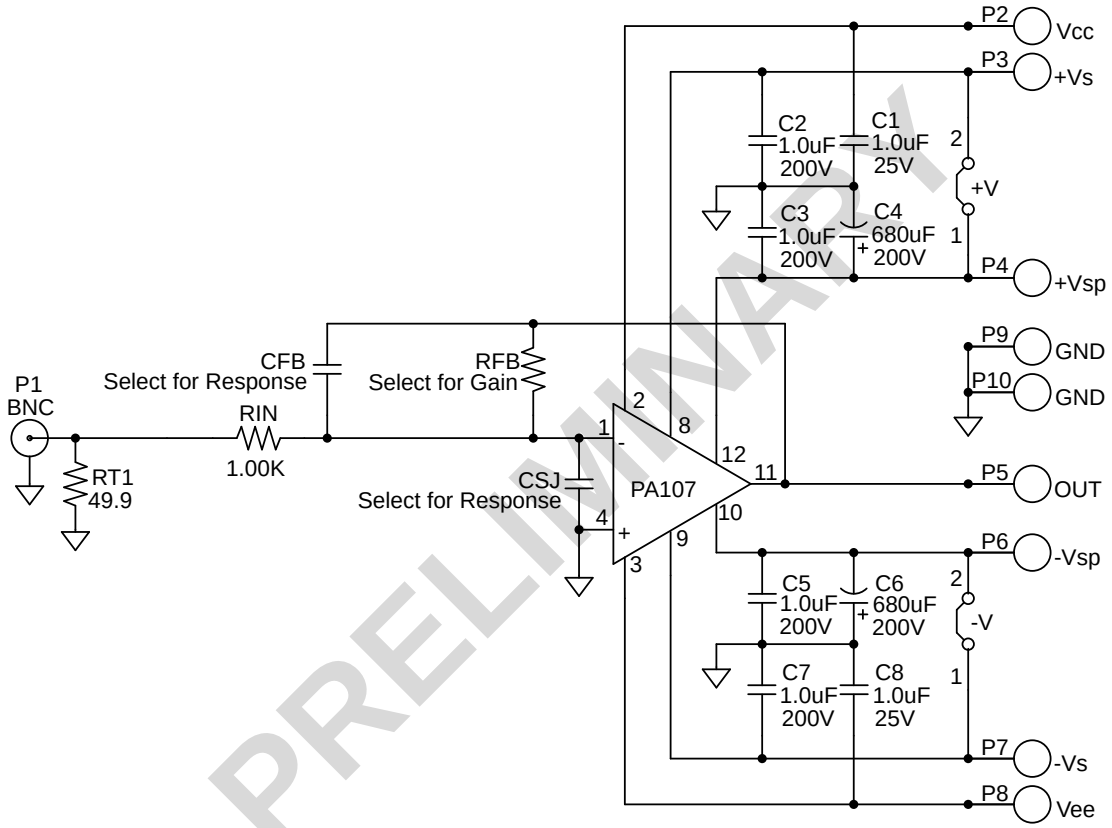


FIGURE 1 – EK71 Schematic

PARTS LIST

Part #	Description, Vendor	Quantity
146510CJ	Connector, BNC, PCB Mount	1
571-0100	4mm Black PCB Socket Single	10
EC03	Capacitor, 680 µF	2
EVAL71	PC Board	1
HS20	Heatsink	1
MS06	Mating Socket	1
OX7R105KWN	Cap, 1µF	4
TW07	Thermal Washer, PSIP	1

BEFORE YOU GET STARTED

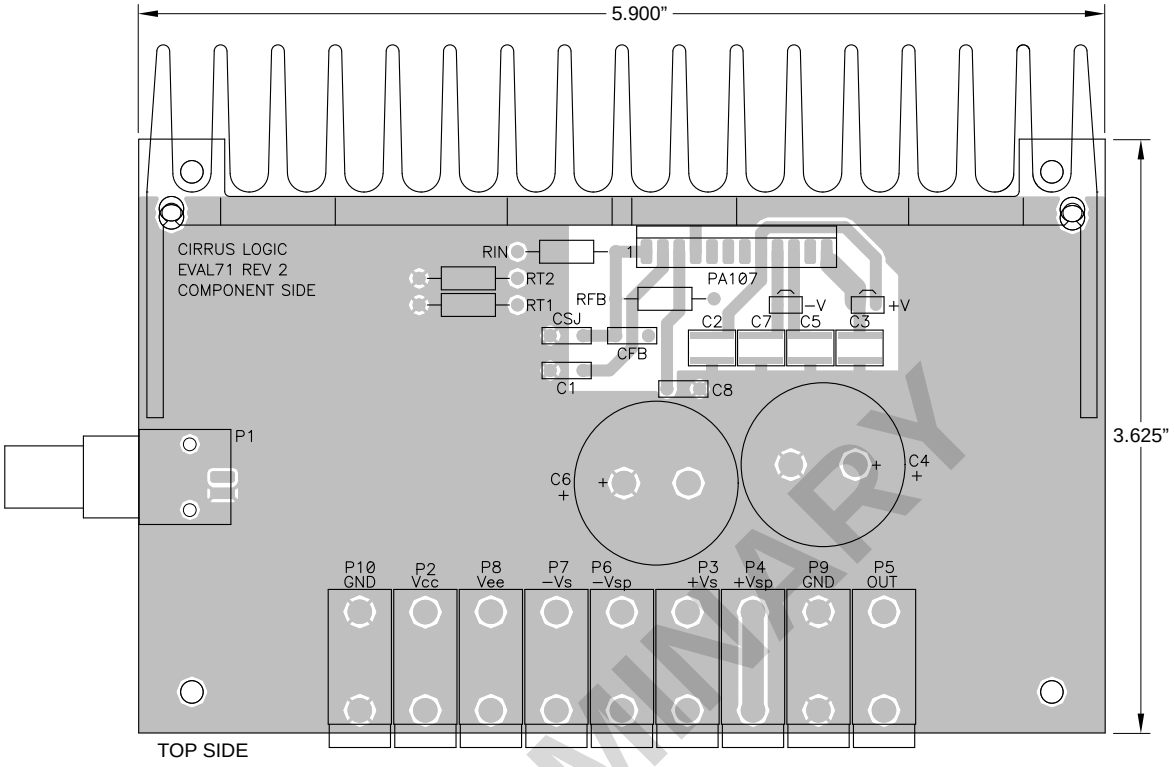
- Please read this data sheet in it's entirety before starting to construct your evaluation board.
- All Apex Precision Power amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.
- Always use adequate power supply bypass capacitors, Apex Precision Power recommends 1µF ceramic in parallel with at least 10µF per ampere of output current electrolytic/tantalum.
- Always provide the adequate heat sinking. Power dissipation must be considered to ensure maximum junction temperature is not exceeded.

ASSEMBLY

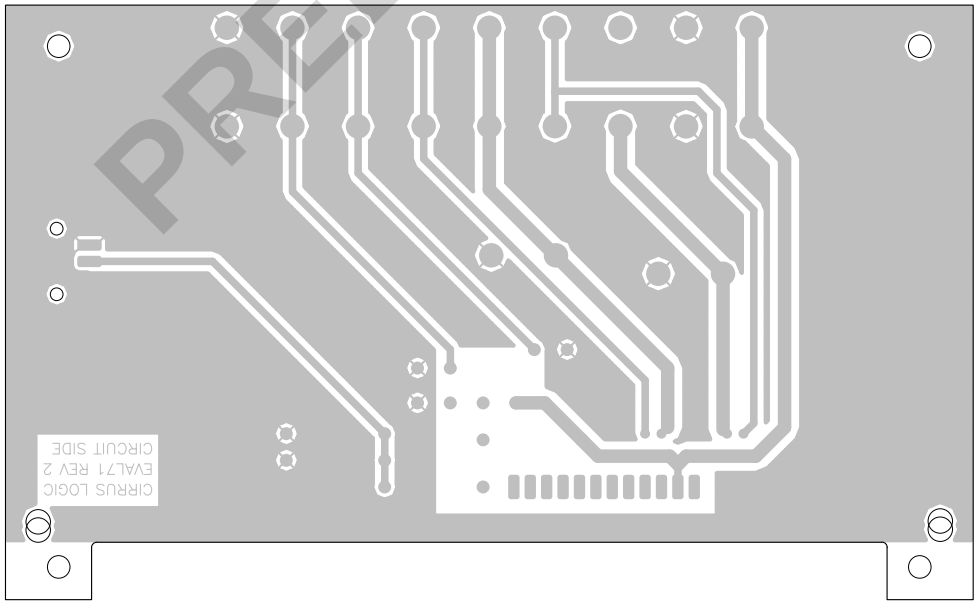
1. See Figure 1 and Figure 2. Solder the surface mount ceramic capacitors to the DUT side of the circuit board at C2, C7, C5 and C3.
2. C1 and C8 are user supplied pin-through-hole bypass capacitors for Vcc and Vee respectively. Insert C1 and C8 from the component side and solder from the circuit side.
3. Solder the electrolytic capacitors to the circuit board at C4 and C6. Match the polarity markings on the circuit board with those on the capacitor body.
4. Clip off the mating socket strip after the 12th position. Insert the strip into the circuit board from the DUT side and solder one pin on the reverse side. Check that the mating socket strip is fully seated against the circuit board then solder the remaining pins. Insert the amplifier fully into the mating socket strip, noting the pin 1 locations on the amplifier and the circuit board.
5. Examine the large heat sink. Notice that there are several holes in the face of the heat sink. These are for mounting various Apex Precision Power amplifier models. The circuit board aligns the amplifier with the correct mounting hole once the heat sink is attached to the circuit board.
6. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired. The remaining two slotted holes are for mounting the large heat sink to the DUT side of the circuit board. Temporarily mount the heat sink with 2 #6 x 1/2" self tapping screws from the opposite side of the circuit board. Do not fully tighten the screws at this time. Check for alignment of the slot in the mounting tab of the amplifier with a hole in the heat sink. Dismount and rotate the heat sink if necessary to achieve an alignment with a hole in the heat sink. Position the heat sink so that the back of the amplifier mounting tab is flush with the heat sink then tighten the heat sink mounting screws.
7. Hang the thermal washer near the end of a 6-32 x 1/2" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heat sink. Secure the screw from the opposite side of the heat sink using a nut holder.
8. To select the values of feedback resistor (RFB), feedback capacitor (CFB) and summing junction capacitor (CSJ), please refer to the section titled "FEEDBACK CONSIDERATIONS" in the PA107DP data sheet.
9. Add other components as necessary to complete your application circuit.

FIGURE 2 - EK71 Assembly

FIGURE 3 – EVAL71 PCB Layout



TOP SIDE



BOTTOM SIDE

F

Evaluation Kit for SA50

INTRODUCTION

Fast, easy breadboarding of circuits using the SA50 are possible with the EVAL05 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. Components are labeled on both sides of the board for ease in probing.

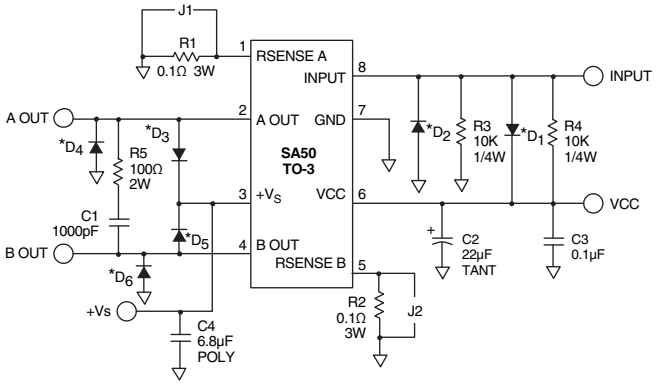
TYPICAL COMPONENT FUNCTIONS

C2, C3, C4 Power supply bypass capacitors
R3, R4 Resistor divider to set the input voltage at 50% of Vcc under nominal conditons
R5, C1 Snubber network
R1, R2 Current sensing resistors or jumpered to ground

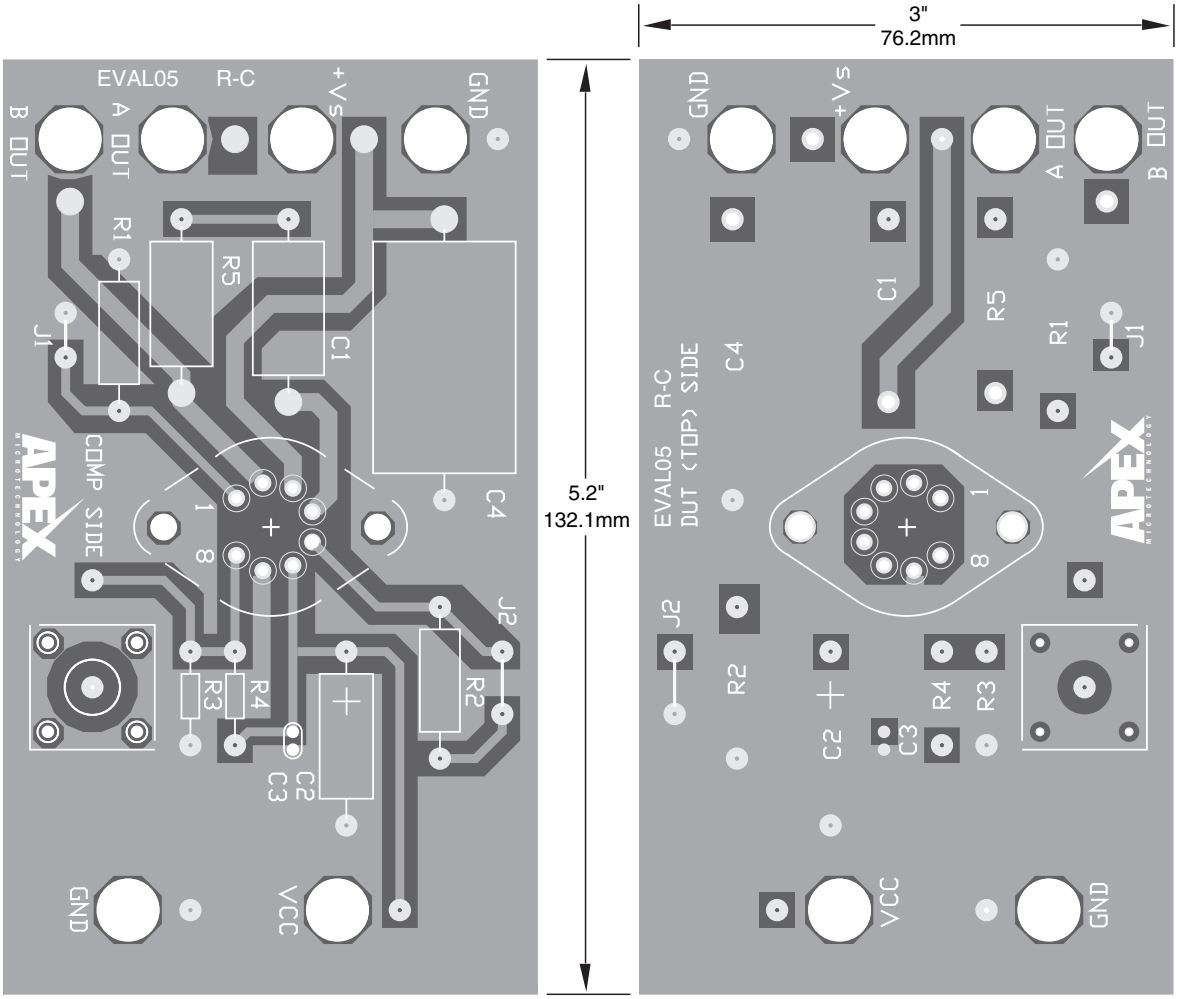
PARTS LIST

Part #	Description	Quantity
EVAL05	P.C. Board	1
HS14	Heatsink	1
MS03	Mating Socket	1
TW03	Thermal Washers	1 bag of 10

EQUIVALENT SCHEMATIC



* D_1 and D_2 – Input protection, high speed such as IN4148.
D_3 through D_6 – Flyback protection, high speed (<200nS). Solder as close to SA50 as possible.



NOTE: Illustration only, not to exact scale.

Demonstration Board for the SA53-IHZ

RoHS COMPLIANT

INTRODUCTION

The DB53R is designed to demonstrate the capabilities of the SA53 DC brush motor driver IC. This fully assembled demonstration allows the user to directly control the speed and direction of the motor. An onboard circuit controls the direction and provides four quadrant PWM signals to control the power outputs of the SA53. LEDs provide feedback for motor control status and fault indications. Provisions on the DB53R allow the user to bypass the onboard control circuit and directly interface with the SA53 motor driver.

The DB53R demonstrates proper layout techniques for the SA53 high current switching amplifier. The economical construction uses only a two-sided PCB and allows the SA53 to deliver peak power of over 500W.

THERMAL CONSIDERATIONS:

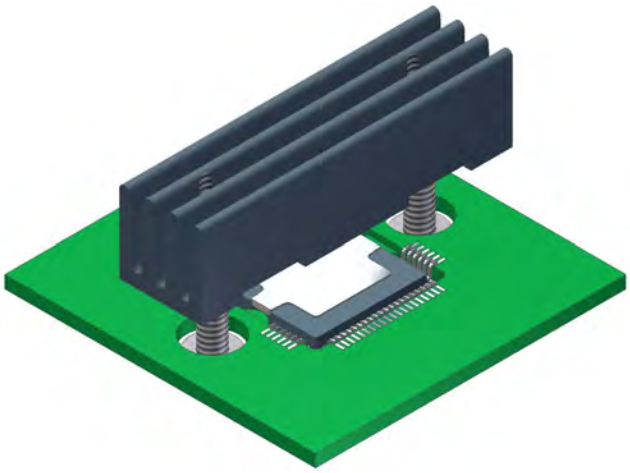
The SA53 is available in a surface mount package which can deliver peak power of over 1kW. This presents an obvious and significant thermal challenge. The DB53R offers a compact design which can deliver 17A peak current by using a patent pending mounting technique. Mounting the SA53 in an inverted fashion as shown in Figure 1 reduces the profile height of the assembly and provides a direct interface between the thermal tab of the PowerQuad package (package outline drawing HQ) and the small HS33 heatsink. The DB53R assembly can dissipate 7-9W in still air at 25ºC ambient temperature, depending on the orientation of the heatsink fins.

CIRCUIT OPERATION

The DB53R control circuit receives power via two terminal block connections. The Vs connection supplies power to drive the motor and must be above the under-voltage lockout threshold of the SA53, approximately 8.3V. The control circuit requires 12V for proper operation a regulator on the DB53R provides the 5V logic supply for the SA53. There are no special considerations for sequencing the two supplies.

Figure 2 (next page) shows the user control features of the DB53R. The PWM duty cycle is controlled with the potentiometer (1 in figure 2). The power LED (2) will illuminate when the 12V supply is connected. The DB53R will power up with the SA53 disabled. The enable button (3) will toggle the SA53 on and off with the LED (4) illuminating to indicate the enable status. Direction of the motor is similarly controlled with the button (5) and is indicated by the LED (6).

Figure 1 – Mounting Technique
PATENT PENDING



F

The DB53R monitors the Temperature warning status pin of the SA53. If this pin goes high an LED (7) illuminates and the enable circuit is forced to a disable status. The temperature LED is not latched and may stay illuminated only briefly while the temperature of the SA53 is above 135ºC. The temperature decrease rapidly via the heatsink once the SA53 is disabled.

The SA53 current limit feature is set to limit at approximately 5A to provide a demonstration of the full capabilities of the SA53. An LED (8) will illuminate if the SA53 cycle-by-cycle current limit circuit engages. The thermal and current limit features are robust, but will not protect the SA53 in all circumstances. The user must consider the worst case thermal and power dissipation conditions.

Push-button switches 1 and 2 trigger latches (U4) for direction and enable control, respectively. Diodes D7 & D8 and resistors R24, 25, 29 & 30 provide a means of bypassing the DB53R control circuit. The 5V regulator, U3, provides 5V to the SA53, the latches and the status LEDs.

Figure 2 – User Control Features

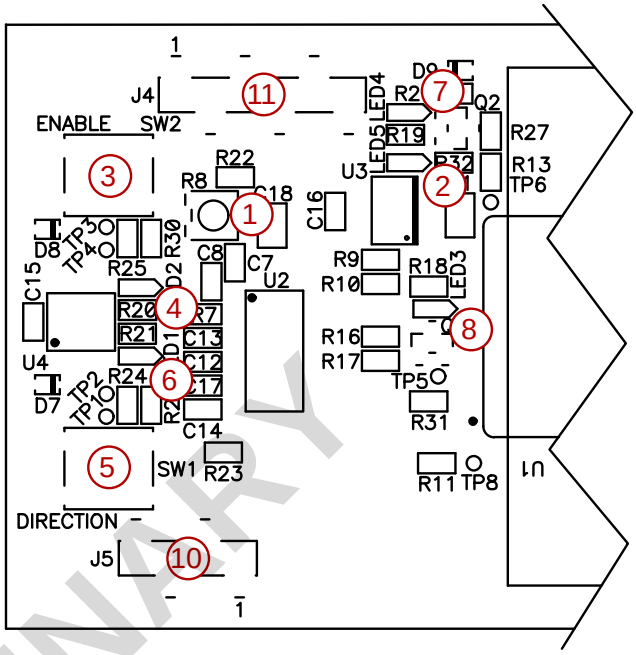
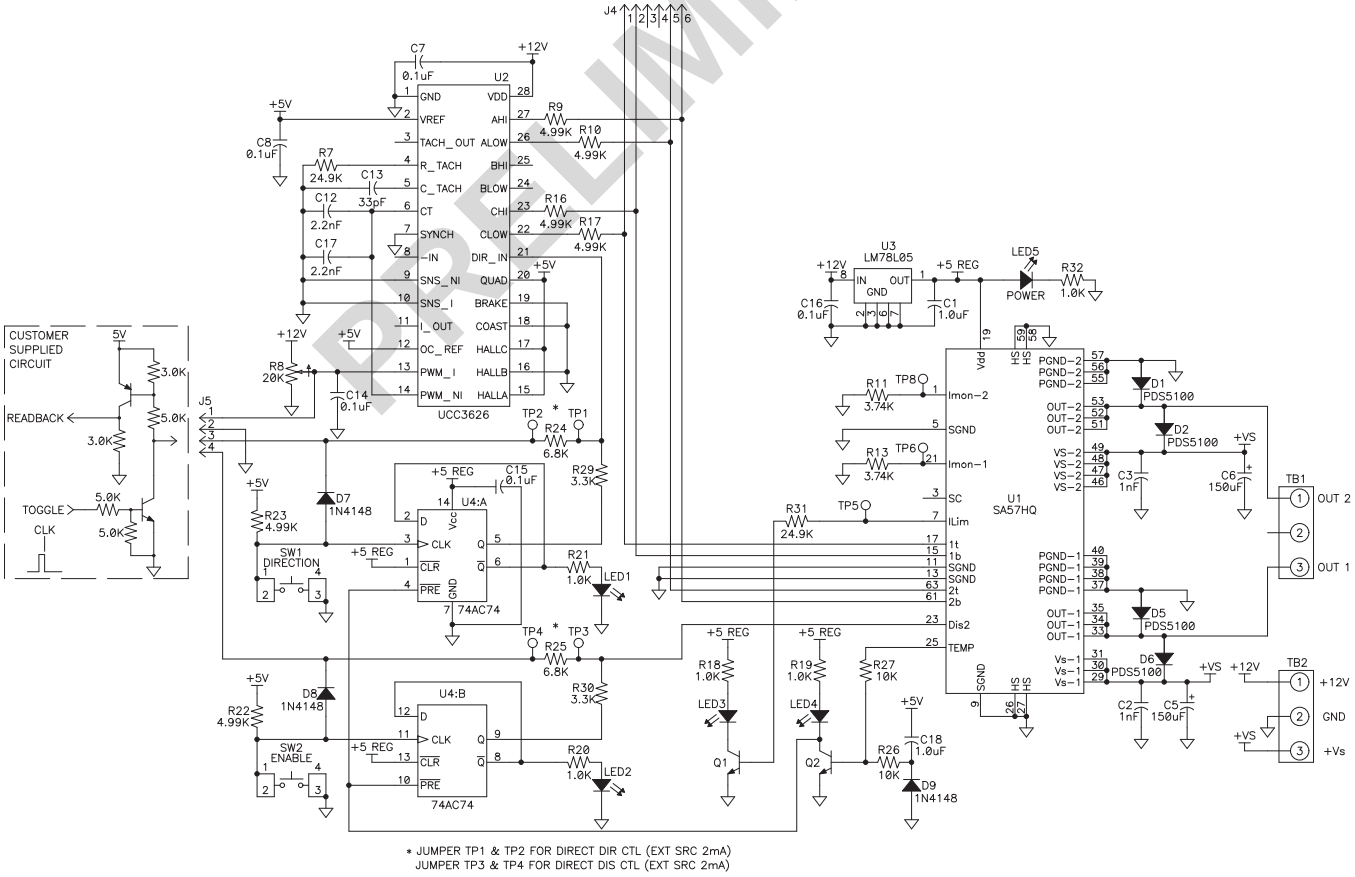


Figure 3 – Schematic



ENHANCING & BYPASSING THE DB53R CONTROL CIRCUIT:

Connector J5 allows the user to bypass many of the manual control features of the DB53R. A signal generator can control the duty cycle with a 2.5 to 7.5V signal, overriding the control potentiometer. A rising 5V edge on pin 3 or 4 of connector J5 will toggle the Direction or Enable latches, respectively. By jumping resistors R24 & R25, the latches are bypassed completely and the logic signals on pins 3 & 4 will directly control the direction and enable functions of the DB53R. With these resistors jumped, the direction and enable LEDs will not represent the states of the DB53R and the pushbuttons will have no effect on the operation. The Temperature disable feature of the DB53R will also not function, although the LED will continue to provide over-temperature status.

Connector J4 is connected directly to the PWM input pins of the SA53. This connector may be used to monitor the signals or to bypass the control IC on the DB53R. The enable function is not controlled via these pins, although pulling all four input pins low provides the same effect. The Enable pushbutton and the connection via J5 are also effective as previously described. The circuit shown in figure 3 in the dashed box is a simple circuit that allows the user to monitor and control the enable or direction status remotely. Either feature can be toggled on the falling edge of the signal at the node labeled TOGGLE.

LAYOUT CONSIDERATIONS

A simple two layer construction is sufficient because of the convenient pinout of the SA53 PowerQuad package. Input signals are routed into one side of the package and high power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise may corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. 1nF capacitors with excellent high frequency characteristics bypass the Vs motor supplies on each phase. Two 150µF electrolytic capacitors provide a local, low inductance source to accommodate surge currents. Six 100V Schottky diodes conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA53. These diodes are rated for 5A continuous and are mounted close to the SA53 to reduce inductance in the commutating current loop. For applications with continuous currents less than 5A, the Schottky diodes may not be necessary if the higher forward voltage internal body diodes and the associated power dissipation are manageable during commutation cycles.

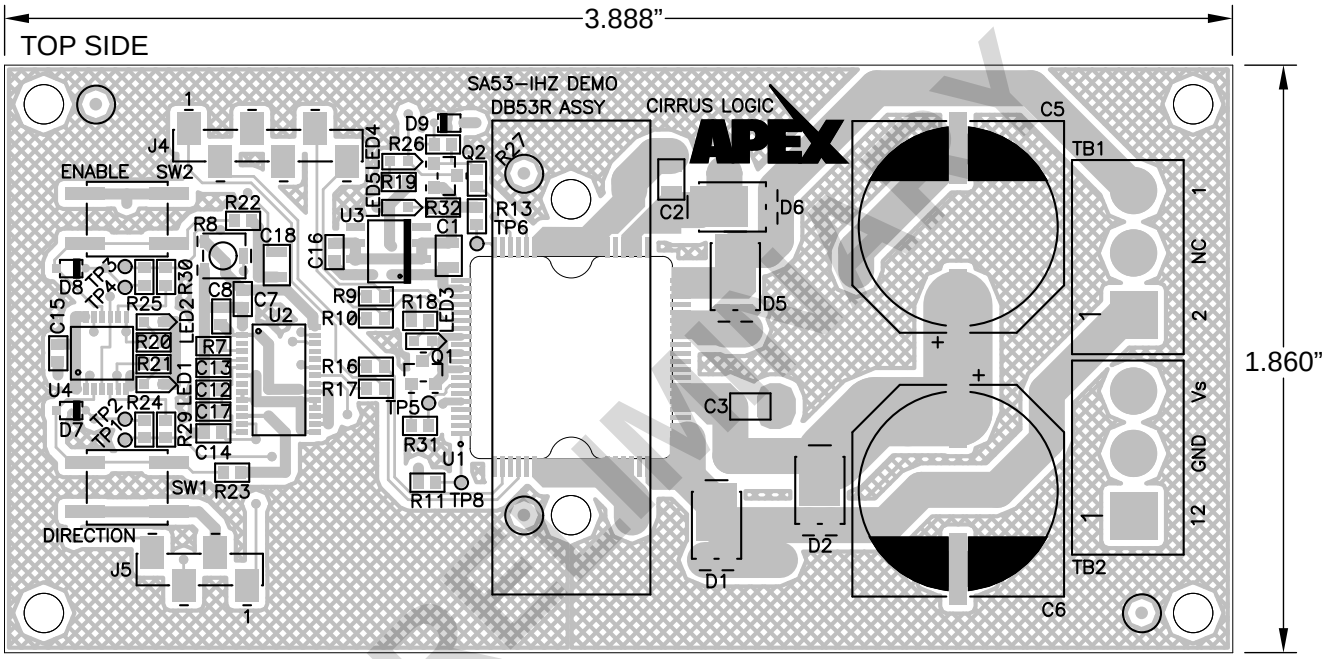
Figure 4 (next page) shows the top and bottom layouts of the DB53R. Gerber files for the circuit board are available upon request.

BILL OF MATERIALS

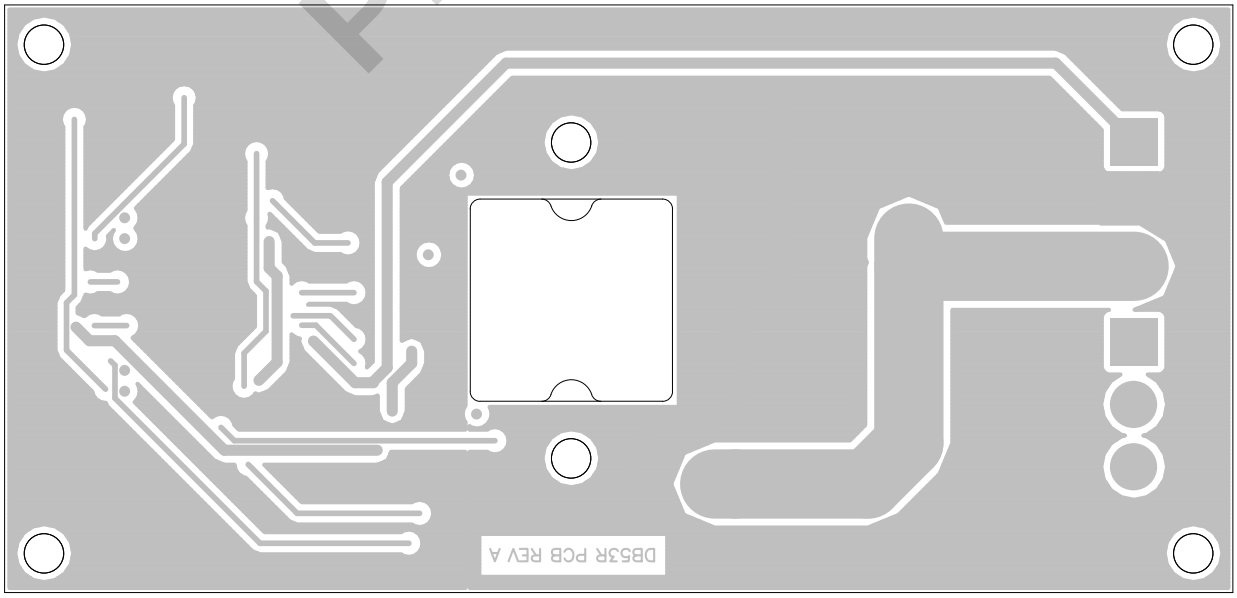
Designation	Description	P/N
C1,C18	CAP, 1.0uF, 16V	Kemet, C0805C105K4RAC
C13	CAP, 33pF, 50V	Kemet, C0603C330J5GACTU
C2,C3	CAP, 1.0nF,100V	Kemet,C0805C102J1GACTU
C5,C6	CAP, 150uF, 100V	Panasonic, EEVFK2A151M
C7,C8,C14,C15,C16	CAP, 0.1uF,16V	GRM188F51C104ZA01D
C12,C17	CAP, 2.2nF,50V	GRM188R71H222KA01D
D1,D2,D3,D5,D6	Diode, 5A Schottky	Diodes Inc., DS5100
D7,D8,D9	IN4148	Vishay, 1N4148WS-V-GS08
J4	Conn, 6 pin .100 ctrs	Samtec, TSM-106-01-T-SV
J5	Conn, 4 pin .100 ctrs	Samtec, TSM-104-01-T-SV
LED1-5	LED, Red	Lite-On, LTST-C190CKT
Q1,Q2	XTR, NPN	MMBT3904
R11,R13	RES 3.74K, 1%	Vishay,CRCW06033K74FKEA
R24,R25	RES, 6.8K	Vishay,CRCW06036K80FKEA
R26,R27	RES, 10K	Vishay,CRCW060310K0FKEA
R29,R30	RES, 3.3K	Vishay,CRCW06033K30FKEA
R18,R19,R20,R21,R32	RES, 1.0K, 5%	RK73B1JTTD102J
R7,R31	RES, 24.9K,1/10W, 1%	RK73H1JTTD2492F
R8	POT, 20K	muRata, PVG3A203C01
R9,R10,R16,R17,R22,R23	RES, 4.99K	CRCW06034K99FKEA
SW1,SW2	Pushbutton, SPST-NO	Panasonic, EVQ-Q2B01W

Designation	Description	P/N
TB1,TB2	Terminal Block, 3 pin, 5mm	On Shore Tech, OSTTA034163
Thermal Grease	Heatsink compound	N/A
U1	SA53-IHZ	Apex Precision Power, SA53-IHZ
U2	UCC3626	Texas Instruments, UCC3626PW
U3	LM78L05	National Semiconductor, LM78L05ACMX/NOPB
U4	74AC74	Texas Instruments, SN74AC74PW
	Heatsink	Apex Precision Power, HS33
	PCB, 1.75” x 3.75”	Apex Precision Power, DB53R
	Screw, #4-40 x ¼”	N/A

Figure 4 – PCB Layout (not to scale)



BOTTOM SIDE



DB53R QUICK START GUIDE

1. Connect the following:

Connection	Location	Indicator	Comment
Vs	TB2-3		9-60V
Ground	TB2-2		
Vctrl	TB2-1	LED 2	12V
Motor Phase A	TB1-1		
Motor Phase B	TB1-2		

2. Apply 12V to Vctrl. LED 2 should light.
3. Apply voltage to Vs based on rated motor voltage, normally 12-48V.
4. Press ENABLE switch 3. LED 4 will light and motor should start.

ORDERING INFORMATION

DB53R Demonstration Board includes one populated DB53R PCB and one SA53-IHZ sample.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
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DB63R

Demonstration Board for the SA57-IHZ

RoHS COMPLIANT

INTRODUCTION

The DB63R is designed to demonstrate the capabilities of the SA57 DC brush motor driver IC. This fully assembled demonstration allows the user to directly control the speed and direction of the motor. An onboard circuit controls the direction and provides four quadrant PWM signals to control the power outputs of the SA57. LEDs provide feedback for motor control status and fault indications. Provisions on the DB63R allow the user to bypass the onboard control circuit and directly interface with the SA57 motor driver.

The DB63R demonstrates proper layout techniques for the SA57 high current switching amplifier. The economical construction uses only a two-sided PCB and allows the SA57 to deliver peak currents of over 1kW.

THERMAL CONSIDERATIONS:

The SA57 is available in a surface mount package which can deliver peak power of over 1kW. This presents an obvious and significant thermal challenge. The DB63R offers a compact design which can deliver 17A peak current by using a patent pending mounting technique. Mounting the SA57 in an inverted fashion as shown in Figure 1 reduces the profile height of the assembly and provides a direct interface between the thermal tab of the PowerQuad package (package outline drawing HQ) and the small HS33 heatsink. The DB63R assembly can dissipate 7-9W in still air at 25ºC ambient temperature, depending on the orientation of the heatsink fins. To use the DB63R in higher power applications, use a fan or mount a heatsink with larger thermal mass. Although the SA57 is rated for operation from -25 to +85ºC, the other components on the DB63R are limited to 0 to 70ºC ambient temperature.

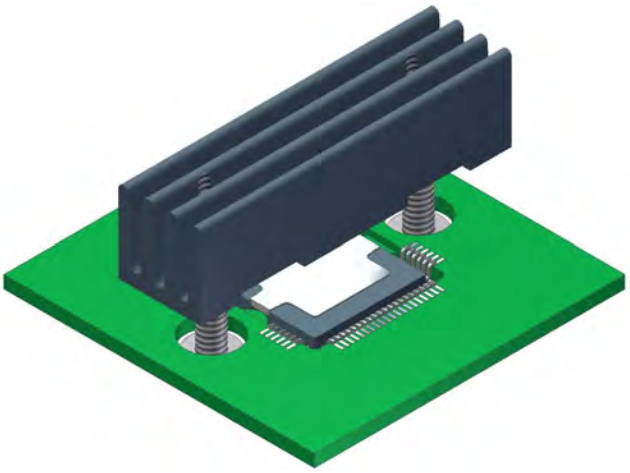
Figure 1 – Mounting Technique

PATENT PENDING

CIRCUIT OPERATION

The DB63R control circuit receives power via two terminal block connections. The Vs connection supplies power to drive the motor and must be above the under-voltage lockout threshold of the SA57, approximately 8.3V. The control circuit requires 12V for proper operation a regulator on the DB63R provides the 5V logic supply for the SA57. There are no special considerations for sequencing the two supplies.

Figure 2 (next page) shows the user control features of the DB63R. The PWM duty cycle is controlled with the potentiometer (1 in figure 2). The power LED (2) will illuminate when the 12V supply is connected. The DB63R will power up with the SA57 disabled. The enable button (3) will toggle the SA57 on and off with the LED (4) illuminating to indicate the enable status. Direction of the motor is similarly controlled with the button (5) and is indicated by the LED (6).



The DB63R monitors the Temperature warning status pin of the SA57. If this pin goes high an LED (7) illuminates and the enable circuit is forced to a disable status. The temperature LED is not latched and may stay illuminated only briefly while the temperature of the SA57 is above 135ºC. The temperature decrease rapidly via the heatsink once the SA57 is disabled.

The SA57 current limit feature is set to limit at approximately 15A to provide a demonstration of the full capabilities of the SA57. An LED (8) will illuminate if the SA57 cycle-by-cycle current limit circuit engages. The thermal and current limit features are robust, but will not protect the SA57 in all circumstances. The user must consider the worst case thermal and power dissipation conditions. Push-button switches 1 and 2 trigger latches (U4) for direction and enable control, respectively. Diodes D7 & D8 and resistors R24, 25, 29 & 30 provide a means of bypassing the DB63R control circuit. The 5V regulator, U3, provides 5V to the SA57, the latches and the status LEDs.

Figure 2 – User Control Features

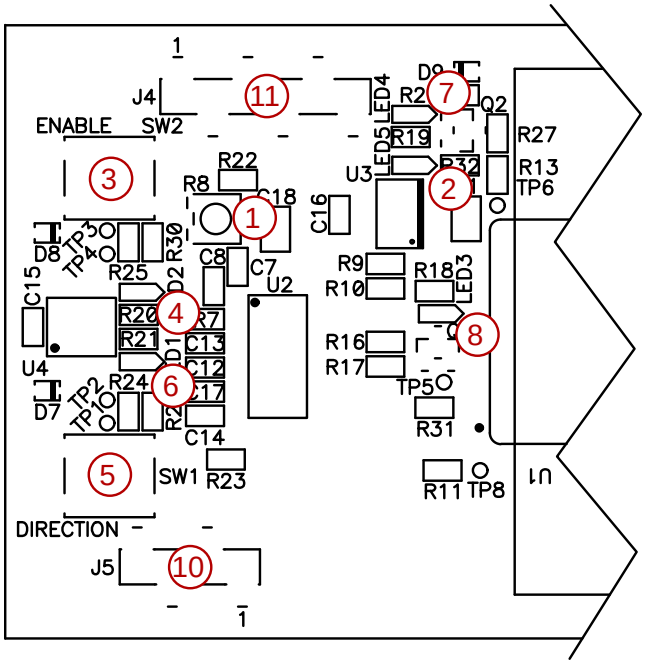
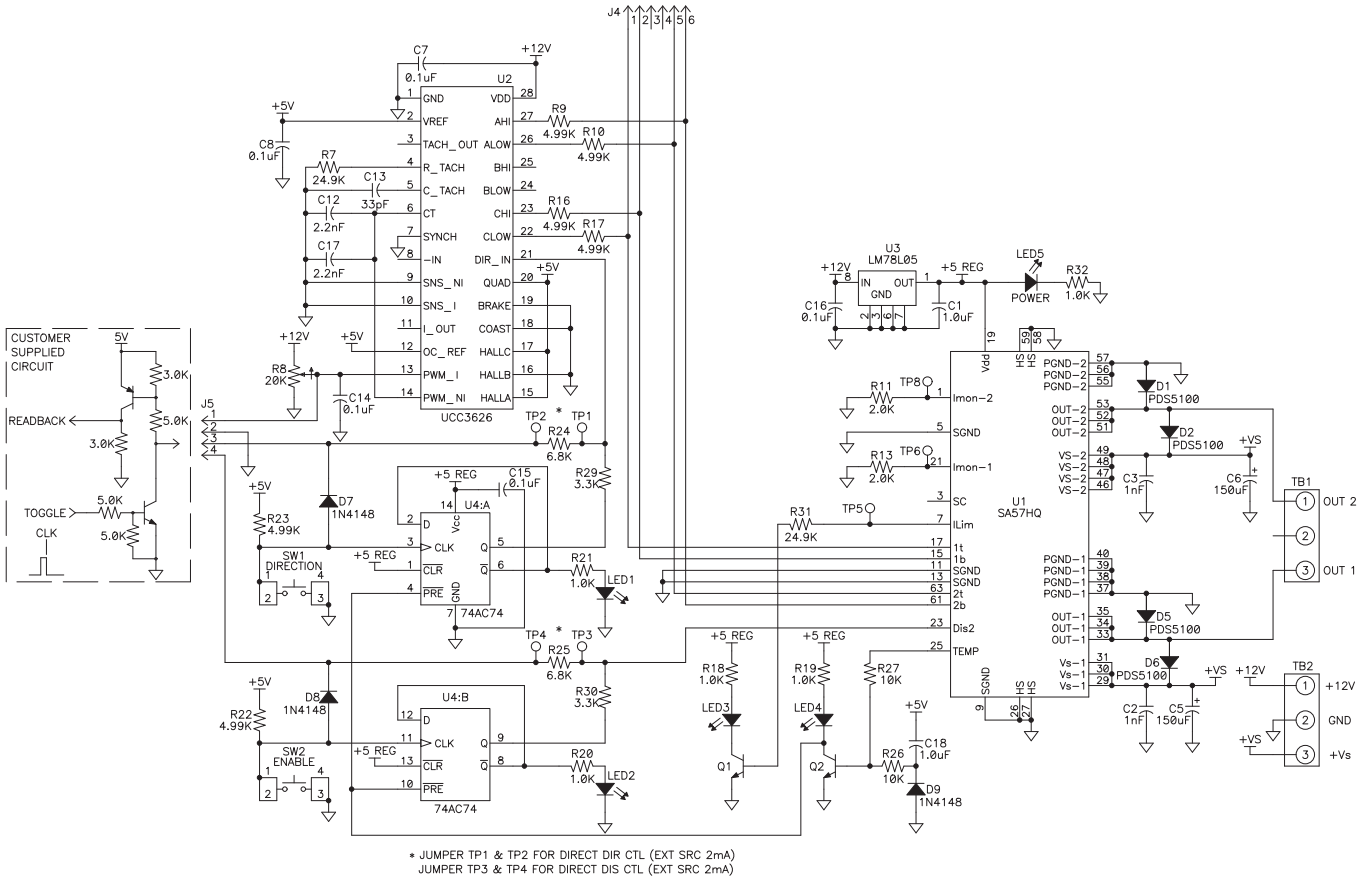


Figure 3 – Schematic



ENHANCING & BYPASSING THE DB63R CONTROL CIRCUIT:

Connector J5 allows the user to bypass many of the manual control features of the DB63R. A signal generator can control the duty cycle with a 2.5 to 7.5V signal, overriding the control potentiometer. A rising 5V edge on pin 3 or 4 of connector J5 will toggle the Direction or Enable latches, respectively. By jumping resistors R24 & R25, the latches are bypassed completely and the logic signals on pins 3 & 4 will directly control the direction and enable functions of the DB63R. With these resistors jumped, the direction and enable LEDs will not represent the states of the DB63R and the pushbuttons will have no effect on the operation. The Temperature disable feature of the DB63R will also not function, although the LED will continue to provide over-temperature status.

Connector J4 is connected directly to the PWM input pins of the SA57. This connector may be used to monitor the signals or to bypass the control IC on the DB63R. The enable function is not controlled via these pins, although pulling all four input pins low provides the same effect. The Enable pushbutton and the connection via J5 are also effective as previously described. The circuit shown in figure 3 in the dashed box is a simple circuit that allows the user to monitor and control the enable or direction status remotely. Either feature can be toggled on the falling edge of the signal at the node labeled TOGGLE.

LAYOUT CONSIDERATIONS

A simple two layer construction is sufficient because of the convenient pinout of the SA57 PowerQuad package. Input signals are routed into one side of the package and high power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise may corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. 1nF capacitors with excellent high frequency characteristics bypass the Vs motor supplies on each phase. Two 150µF electrolytic capacitors provide a local, low inductance source to accommodate surge currents up to 17A. Six 100V Schottky diodes conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA57. These diodes are rated for 5A continuous and are mounted close to the SA57 to reduce inductance in the commutating current loop. For applications with continuous currents less than 5A, the Schottky diodes may not be necessary if the higher forward voltage internal body diodes and the associated power dissipation are manageable during commutation cycles.

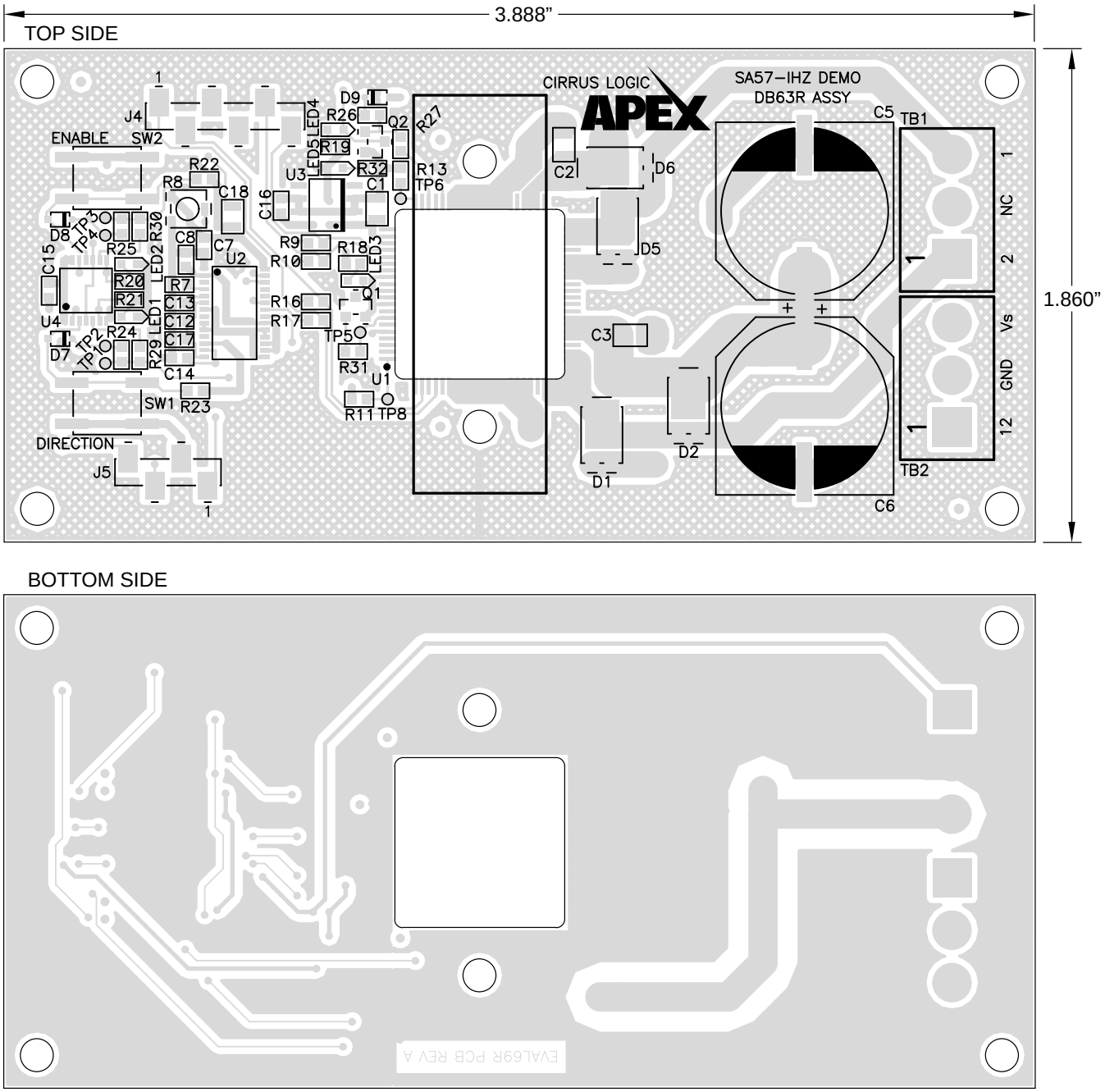
Figure 4 (next page) shows the top and bottom layouts of the DB63R. Gerber files for the circuit board are available upon request.

BILL OF MATERIALS

Designation	Description	P/N
C1,C18	CAP, 1.0uF, 16V	Kemet, C0805C105K4RAC
C13	CAP, 33pF, 50V	Kemet, C0603C330J5GACTU
C2,C3	CAP, 1.0nF,100V	Kemet,C0805C102J1GACTU
C5,C6	CAP, 150uF, 100V	Panasonic, EEVFK2A151M
C7,C8,C14,C15,C16	CAP, 0.1uF,16V	GRM188F51C104ZA01D
C12,C17	CAP, 2.2nF,50V	GRM188R71H222KA01D
D1,D2,D3,D5,D6	Diode, 5A Schottky	Diodes Inc., DS5100
D7,D8,D9	IN4148	Vishay, 1N4148WS-V-GS08
J4	Conn, 6 pin .100 ctrs	Samtec, TSM-106-01-T-SV
J5	Conn, 4 pin .100 ctrs	Samtec, TSM-104-01-T-SV
LED1-5	LED, Red	Lite-On, LTST-C190CKT
Q1,Q2	XTR, NPN	MMBT3904
R11,R12,R13	RES 2.0K, 1%	Vishay,CRCW06032K00FKEA
R24,R25	RES, 6.8K	Vishay,CRCW06036K80FKEA
R26,R27	RES, 10K	Vishay,CRCW060310K0FKEA
R29,R30	RES, 3.3K	Vishay,CRCW06033K30FKEA
R18,R19,R20,R21,R32	RES, 1.0K, 5%	RK73B1JTTD102J
R7,R31	RES, 24.9K,1/10W, 1%	RK73H1JTTD2492F
R8	POT, 20K	muRata, PVG3A203C01
R9,R10,R16,R17,R22,R23	RES, 4.99K	CRCW06034K99FKEA
SW1,SW2	Pushbutton, SPST-NO	Panasonic, EVQ-Q2B01W
TB1,TB2	Terminal Block, 3 pin, 5mm	On Shore Tech, OSTTA034163

Designation	Description	P/N
Thermal Grease	Heatsink compound	N/A
U1	SA57-IHZ	Apex Precision Power, SA57-IHZ
U2	UCC3626	Texas Instruments, UCC3626PW
U3	LM78L05	National Semiconductor, LM78L05ACMX/NOPB
U4	74AC74	Texas Instruments, SN74AC74PW
	Heatsink	Apex Precision Power, HS33
	PCB, 1.75” x 3.75”	Apex Precision Power, EVAL69R
	Screw, #4-40 x ¼”	N/A

Figure 4 – PCB Layout (not to scale)



DB63R QUICK START GUIDE

1. Connect the following:

Connection	Location	Indicator	Comment
Vs	TB2-3		9-60V
Ground	TB2-2		
Vctrl	TB2-1	LED 2	12V
Motor Phase A	TB1-1		
Motor Phase B	TB1-2		

2. Apply 12V to Vctrl. LED 2 should light.
3. Apply voltage to Vs based on rated motor voltage, normally 12-48V.
4. Press ENABLE switch 3. LED 4 will light and motor should start.

ORDERING INFORMATION

DB63R Demonstration Board includes one populated EVAL69R PCB and one SA57-IHZ sample.

CONTACTING CIRRUS LOGIC SUPPORT

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Demonstration Board for the SA306-IHZ

RoHS COMPLIANT

INTRODUCTION

The DB64R is designed to demonstrate the capabilities of the SA306 3 phase brushless DC (BLDC) motor driver IC. This fully assembled demonstration allows the user to directly control the speed and direction of the motor. An onboard controller decodes HALL Effect sensor inputs for commutation in either direction and provides four quadrant PWM signals to control the power outputs of the SA306. LEDs provide feedback for motor control status and fault indications. Provisions on the DB64R allow the user to bypass the onboard control circuit and directly interface with the SA306 brushless motor driver.

The DB64R demonstrates proper layout techniques for the SA306 high current switching amplifier. The economical construction uses only a two-sided PCB and allows the SA306 to deliver peak currents of over 1kW.

THERMAL CONSIDERATIONS

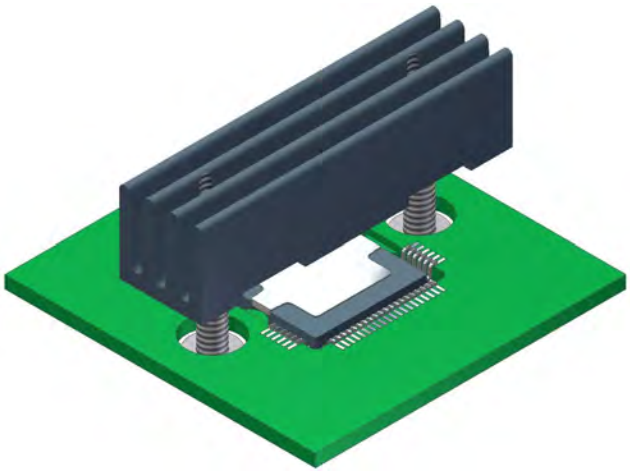
The SA306 is available in a surface mount package which can deliver peak power of over 1kW. This presents an obvious and significant thermal challenge. The DB64R offers a compact design which can deliver 17A peak current by using a patent pending mounting technique. Mounting the SA306 in an inverted fashion as shown in Figure 1 reduces the profile height of the assembly and provides a direct interface between the thermal tab of the PowerQuad package (package outline drawing HQ) and the small HS33 heatsink. The DB64R assembly can dissipate 7-9W in still air at 25ºC ambient temperature, depending on the orientation of the heatsink fins. To use the DB64R in higher power applications, use a fan or mount a heatsink with larger thermal mass. Although the SA306 is rated for operation from -25 to +85ºC, the other components on the DB64R are limited to 0 to 70ºC ambient temperature.

Figure 1 – Mounting Technique
PATENT PENDING

CIRCUIT OPERATION

The DB64R control circuit receives power via two terminal block connections. The Vs connection supplies power to drive the motor and must be above the under-voltage lockout threshold of the SA306, approximately 8.3V. The control circuit requires 12V for proper operation a regulator on the DB64R provides the 5V logic supply for the SA306. There are no special considerations for sequencing the two supplies.

Figure 2 (next Page) shows the user control features of the DB64R. The PWM duty cycle is controlled with the potentiometer (1 in figure 2). The power LED (2) will illuminate when the 12V supply is connected. The DB64R will power up with the SA306 disabled. The enable button (3) will toggle the SA306 on and off with the LED (4) illuminating to indicate the enable status. Direction of the motor is similarly controlled with the button (5) and is indicated by the LED (6).



The DB64R monitors the Temperature warning status pin of the SA306. If this pin goes high an LED (7) illuminates and the enable circuit is forced to a disable status. The temperature LED is not latched and may stay illuminated only briefly while the temperature of the SA306 is above 135ºC. The temperature decrease rapidly via the heatsink once the SA306 is disabled.

The SA306 current limit feature is set to limit at approximately 15A to provide a demonstration of the full capabilities of the SA306. An LED (8) will illuminate if the SA306 cycle-by-cycle current limit circuit engages. The thermal and current limit features are robust, but will not protect the SA306 in all circumstances. The user must consider the worst case thermal and power dissipation conditions. Hall Effect inputs to connector J3 (9) are required to commutate the motor correctly. Filtering networks and 5V pull-up are provided for glitch-free operation. The Hall sensor connector, J3 (9), also includes a tachometer output which is based on the commutation signals from the Hall inputs. Power for the Hall sensors is provided by U2 in figure 3, an integrated brushless motor controller IC. The controller decodes the Hall sensor inputs and generates six PWM control signals directly to the SA306. Push-button switches 1 and 2 trigger latches (U4) for direction and enable control, respectively. Diodes D7 & D8 and resistors R24, 25, 29 & 30 provide a means of bypassing the DB64R control circuit. The 5V regulator, U3, provides 5V to the SA306, the latches and the status LEDs.

Figure 2 – User Control Features

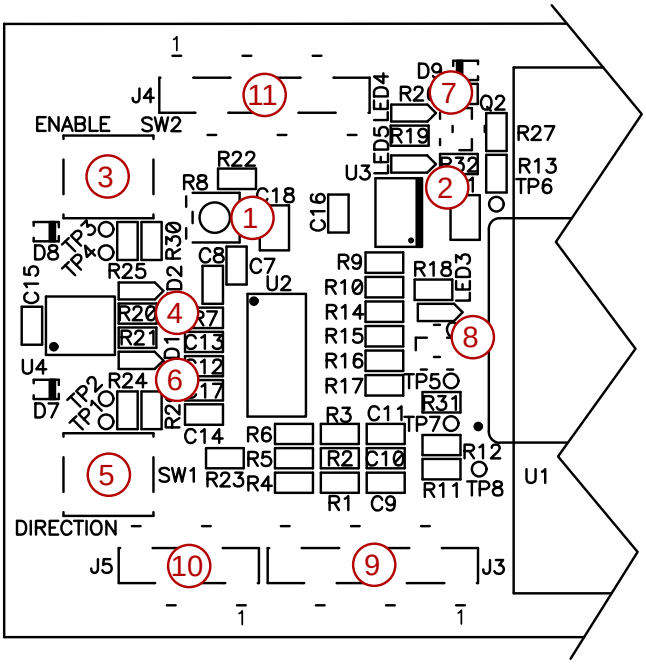
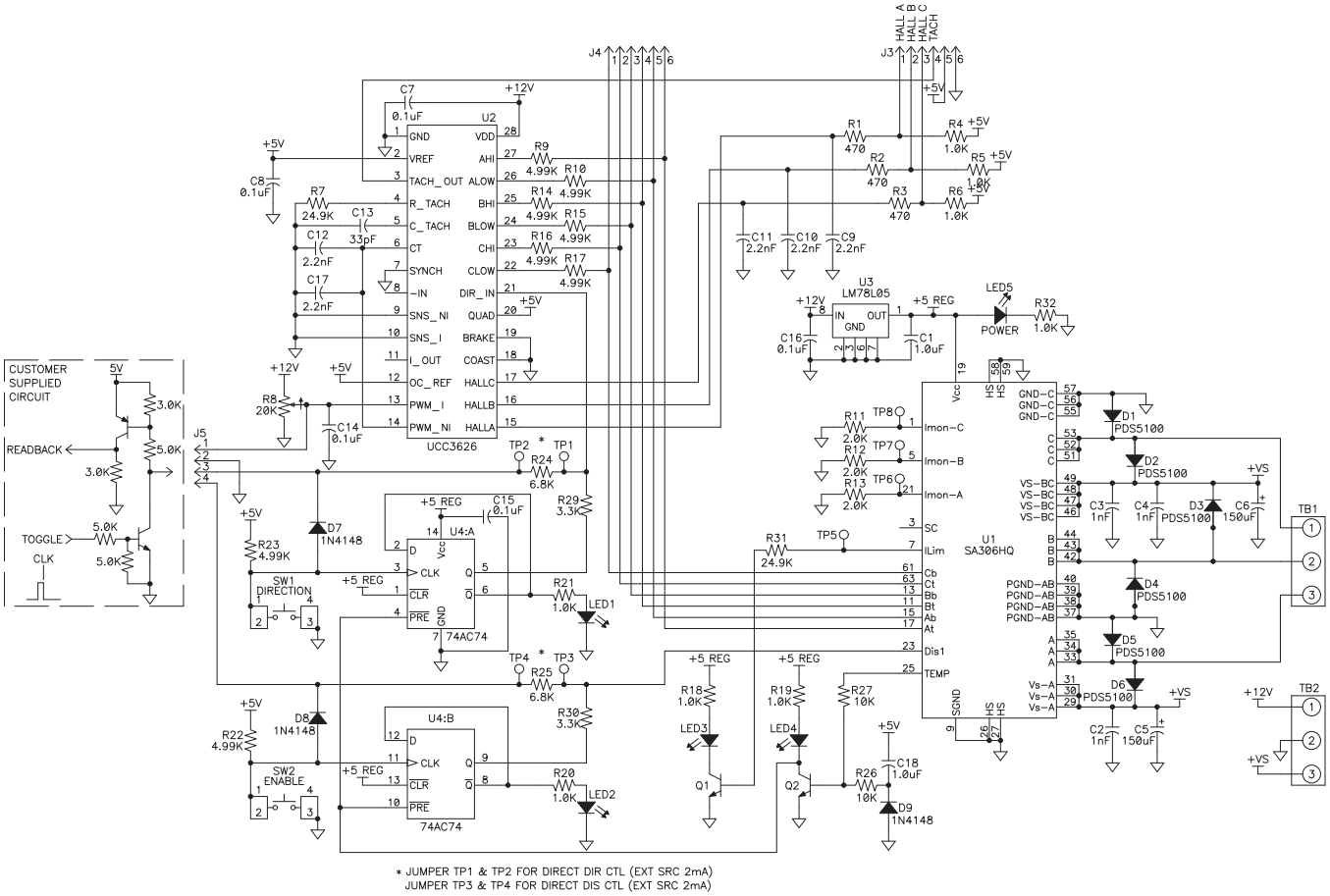


Figure 3 – Schematic



ENHANCING & BYPASSING THE DB64R CONTROL CIRCUIT

Connector J5 allows the user to bypass many of the manual control features of the DB64R. A signal generator can control the duty cycle with a 2.5 to 7.5V signal, overriding the control potentiometer. A rising 5V edge on pin 3 or 4 of connector J5 will toggle the Direction or Enable latches, respectively. By jumping resistors R24 & R25, the latches are bypassed completely and the logic signals on pins 3 & 4 will directly control the direction and enable functions of the DB64R. With these resistors jumped, the direction and enable LEDs will not represent the states of the DB64R and the pushbuttons will have no effect on the operation. The Temperature disable feature of the DB64R will also not function, although the LED will continue to provide over-temperature status.

Connector J4 is connected directly to the PWM input pins of the SA306. This connector may be used to monitor the signals or to bypass the control IC on the DB64R. The enable function is not controlled via these pins, although pulling all six input pins low provides the same effect. The Enable pushbutton and the connection via J5 are also effective as previously described. The circuit shown in figure 3 in the dashed box is a simple circuit that allows the user to monitor and control the enable or direction status remotely. Either feature can be toggled on the falling edge of the signal at the node labeled TOGGLE.

LAYOUT CONSIDERATIONS

A simple two layer construction is sufficient because of the convenient pinout of the SA306 PowerQuad package. Input signals are routed into one side of the package and high power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise may corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. 1nF capacitors with excellent high frequency characteristics bypass the Vs motor supplies on each phase. Two 150µF electrolytic capacitors provide a local, low inductance source to accommodate surge currents up to 17A. Six 100V Schottky diodes conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA306. These diodes are rated for 5A continuous and are mounted close to the SA306 to reduce inductance in the commutating current loop. For applications with continuous currents less than 5A, the Schottky diodes may not be necessary if the higher forward voltage internal body diodes and the associated power dissipation are manageable during commutation cycles.

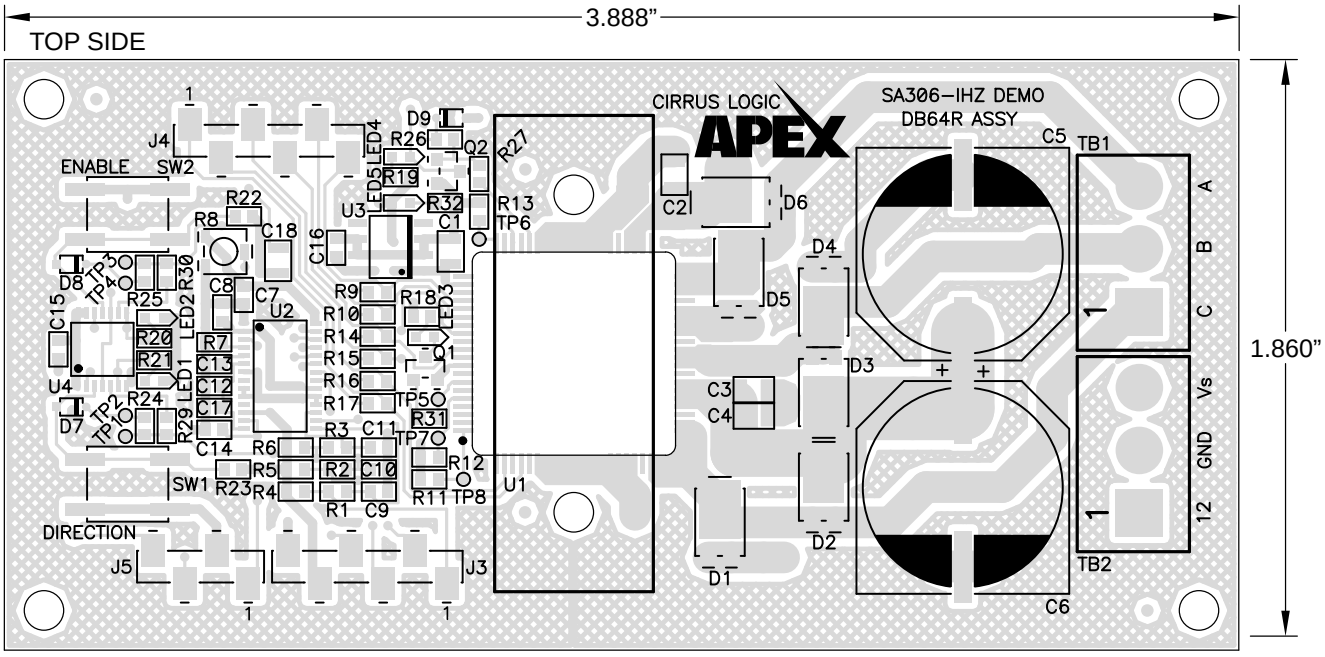
Figure 4 shows the top and bottom layouts of the DB64R. Gerber files for the circuit board are available upon request.

BILL OF MATERIALS

Designation	Description	P/N
C1,C18	CAP, 1.0uF, 16V	Kemet, C0805C105K4RAC
C13	CAP, 33pF, 50V	Kemet C0603C330J5GACTU
C2,C3,C4	CAP, 1.0nF,100V	Kemet,C0805C102J1GACTU
C5,C6	CAP, 150uF, 100V	Panasonic, EEVFK2A151M
C7,C8,C14,C15,C16	CAP, 0.1uF, 16V	GRM188F51C104ZA01D
C9,C10,C11,C12,C17	CAP, 2.2nF, 50V	GRM188R71H222KA01D
D1,D2,D3,D4,D5,D6	Diode, 5A Schottky	Diodes Inc. DS5100
D7,D8,D9	IN4148	Vishay, 1N4148WS-V-GS08
J3,J4	Conn, 6 pin .100 ctrs	Samtec TSM-106-01-T-SV
J5	Conn, 4 pin .100 ctrs	Samtec TSM-104-01-T-SV
LED1-5	LED, Red	Lite-On LTST-C190CKT
Q1,Q2	XTR, NPN	MMBT3904
R1,R2,R3	RES, 470, 5%	RK73B1JTTDD471J
R11,R12,R13	RES 2.0K, 1%	Vishay,CRCW06032K00FKEA
R24,R25	RES, 6.8K	Vishay,CRCW06036K80FKEA
R26,R27	RES, 10K	Vishay,CRCW060310K0FKEA
R29,R30	RES, 3.3K	Vishay,CRCW06033K30FKEA
R4,R5,R6,R18,R19,R20,R21,R32	RES, 1.0K, 5%	RK73B1JTTD102J
R7,R31	RES, 24.9K,1/10W, 1%	RK73H1JTTD2492F
R8	POT, 20K	muRata, PVG3A203C01
R9,R10,R14,R15,R16,R17,R22,R23	RES, 4.99K	Vishay,CRCW06034K99FKEA

Designation	Description	P/N
SW1,SW2	Pushbutton, SPST-NO	Panasonic, EVQ-Q2B01W
TB1,TB2	Term. Blk., 3 pin, 5mm	On Shore Tech, OSTTA034163
Thermal Grease	Heatsink compound	N/A
U1	SA306-IHZ	Apex Precision Power, SA306-IHZ
U2	UCC3626	Texas Instruments, UCC3626PW
U3	LM78L05	National Semiconductor, LM78L05ACMX/NOPB
U4	74AC74	Texas Instruments, SN74AC74PW
	Heatsink	Apex Precision Power, HS33
	PCB, 1.75” x 3.75”	Apex Precision Power, EVAL67R
	Screw, #4-40 x ¼”	N/A
	Solder	Tin/Silver 96/4

TOP SIDE



BOTTOM SIDE

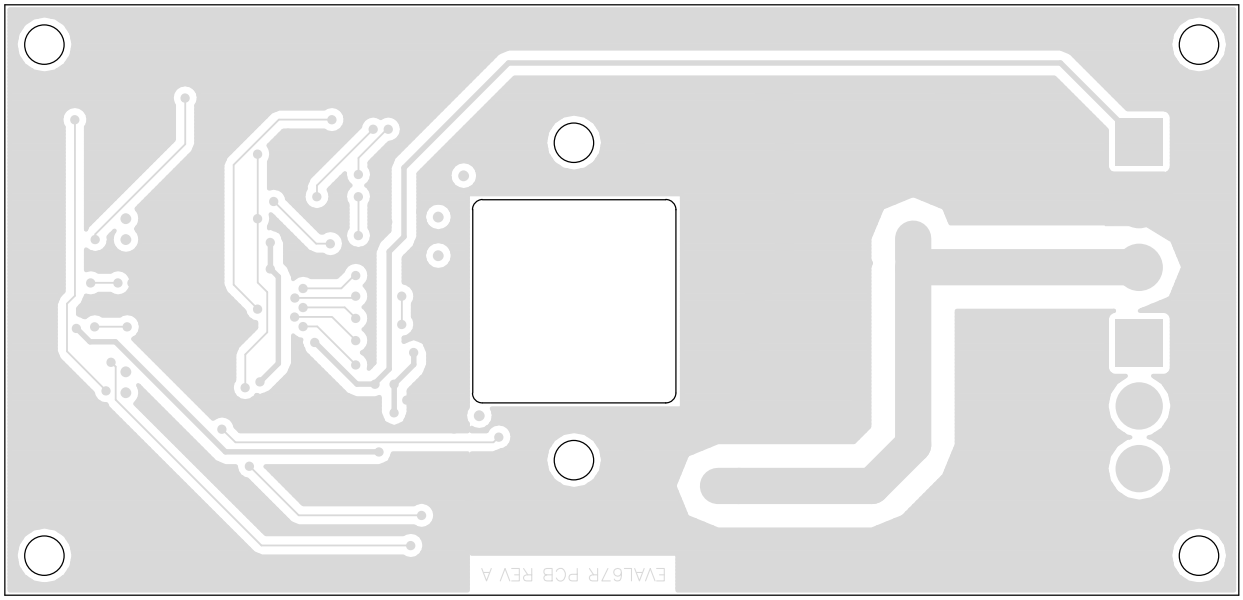


Figure 4 – PCB Layout (not to scale)

DB64R Quick Start Guide

1. Connect the following:

Connection	Location	Indicator	Comment
Vs	TB2-3		9-60V
Ground	TB2-2		
Vctrl	TB2-1	LED 2	12V
Motor Phase A	TB1-1		
Motor Phase B	TB1-2		
Motor Phase C	TB1-3		
Hall Sensor A	J3-1		
Hall Sensor B	J3-2		
Hall Sensor C	J3-3		
Hall 5V	J3-5		Output from PCB
Hall ground	J3-6		

2. Apply 12V to Vctrl. LED 2 should light.
3. Apply voltage to Vs based on rated motor voltage, normally 12-48V.
4. Press ENABLE switch 3. LED 4 will light and motor should start.

ORDERING INFORMATION

DB64R Demonstration Board includes one populated EVAL67R PCB and one SA306-IHZ sample

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DB303R

Demonstration Board for the SA303-IHZ

RoHS COMPLIANT

INTRODUCTION

The DB303R is designed to demonstrate the capabilities of the SA303 3 phase brushless DC (BLDC) motor driver IC. This fully assembled demonstration allows the user to directly control the speed and direction of the motor. An onboard controller decodes HALL Effect sensor inputs for commutation in either direction and provides four quadrant PWM signals to control the power outputs of the SA303. LEDs provide feedback for motor control status and fault indications. Provisions on the DB303R allow the user to bypass the onboard control circuit and directly interface with the SA303 brushless motor driver.

The DB303R demonstrates proper layout techniques for the SA303 high current switching amplifier. The economical construction uses only a two-sided PCB and allows the SA303 to deliver peak power of over 500W.

THERMAL CONSIDERATIONS

The SA303 is available in a surface mount package which can deliver peak power of over 1kW. This presents an obvious and significant thermal challenge. The DB303R offers a compact design which can deliver 17A peak current by using a patent pending mounting technique. Mounting the SA303 in an inverted fashion as shown in Figure 1 reduces the profile height of the assembly and provides a direct interface between the thermal tab of the PowerQuad package (package outline drawing HQ) and the small HS33 heatsink. The DB303R assembly can dissipate 7-9W in still air at 25ºC ambient temperature, depending on the orientation of the heatsink fins.

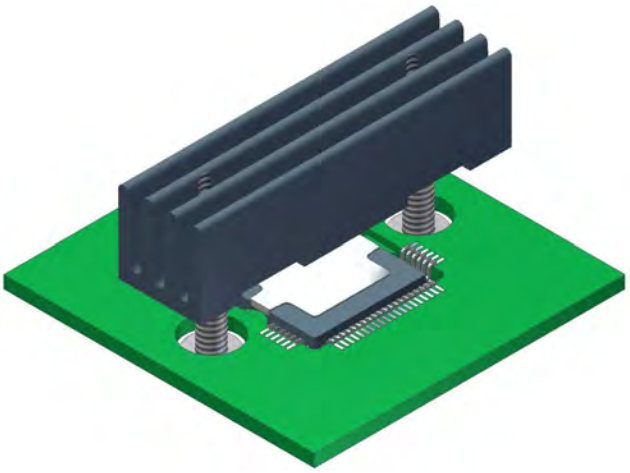
Figure 1 – Mounting Technique
PATENT PENDING

CIRCUIT OPERATION

The DB303R control circuit receives power via two terminal block connections. The Vs connection supplies power to drive the motor and must be above the under-voltage lockout threshold of the SA303, approximately 8.3V. The control circuit requires 12V for proper operation a regulator on the DB303R provides the 5V logic supply for the SA303. There are no special considerations for sequencing the two supplies.

Figure 2 (next Page) shows the user control features of the DB303R. The PWM duty cycle is controlled with the potentiometer (1 in figure 2). The power LED (2) will illuminate when the 12V supply is connected. The DB303R will power up with the SA303 disabled. The enable button (3) will toggle the SA303 on and off with the LED (4) illuminating to indicate the enable status. Direction of the motor is similarly controlled with the button (5) and is indicated by the LED (6).

The DB303R monitors the Temperature warning status pin of the SA303. If this pin goes high an LED (7) illuminates and the enable circuit is forced to a disable status. The temperature LED is not latched and may stay illuminated only briefly while the temperature of the SA303 is above 135ºC. The temperature decrease rapidly via the heatsink once the SA303 is disabled.



The SA303 current limit feature is set to limit at approximately 5A to provide a demonstration of the full capabilities of the SA303. An LED (8) will illuminate if the SA303 cycle-by-cycle current limit circuit engages. The thermal and current limit features are robust, but will not protect the SA303 in all circumstances. The user must consider the worst case thermal and power dissipation conditions. Hall Effect inputs to connector J3 (9) are required to commutate the motor correctly. Filtering networks and 5V pull-up are provided for glitch-free operation. The Hall sensor connector, J3 (9), also includes a tachometer output which is based on the commutation signals from the Hall inputs. Power for the Hall sensors is provided by U2 in figure 3, an integrated brushless motor controller IC. The controller decodes the Hall sensor inputs and generates six PWM control signals directly to the SA303. Push-button switches 1 and 2 trigger latches (U4) for direction and enable control, respectively. Diodes D7 & D8 and resistors R24, 25, 29 & 30 provide a means of bypassing the DB303R control circuit. The 5V regulator, U3, provides 5V to the SA303, the latches and the status LEDs.

Figure 2 – User Control Features

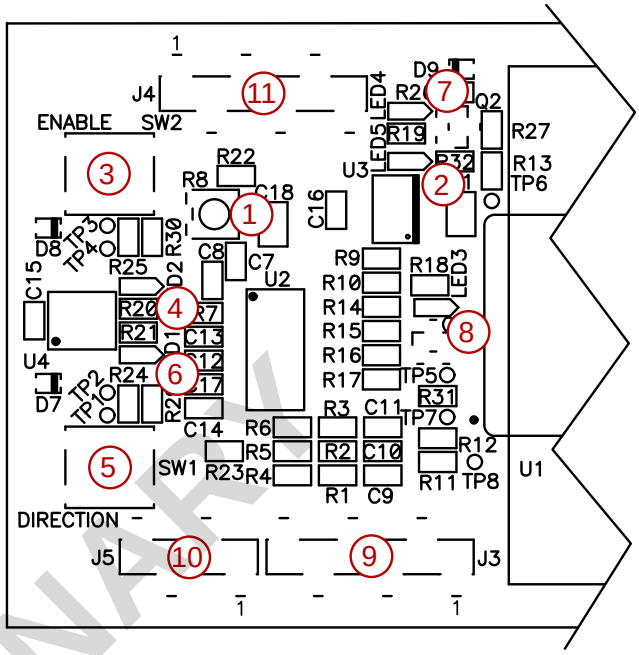
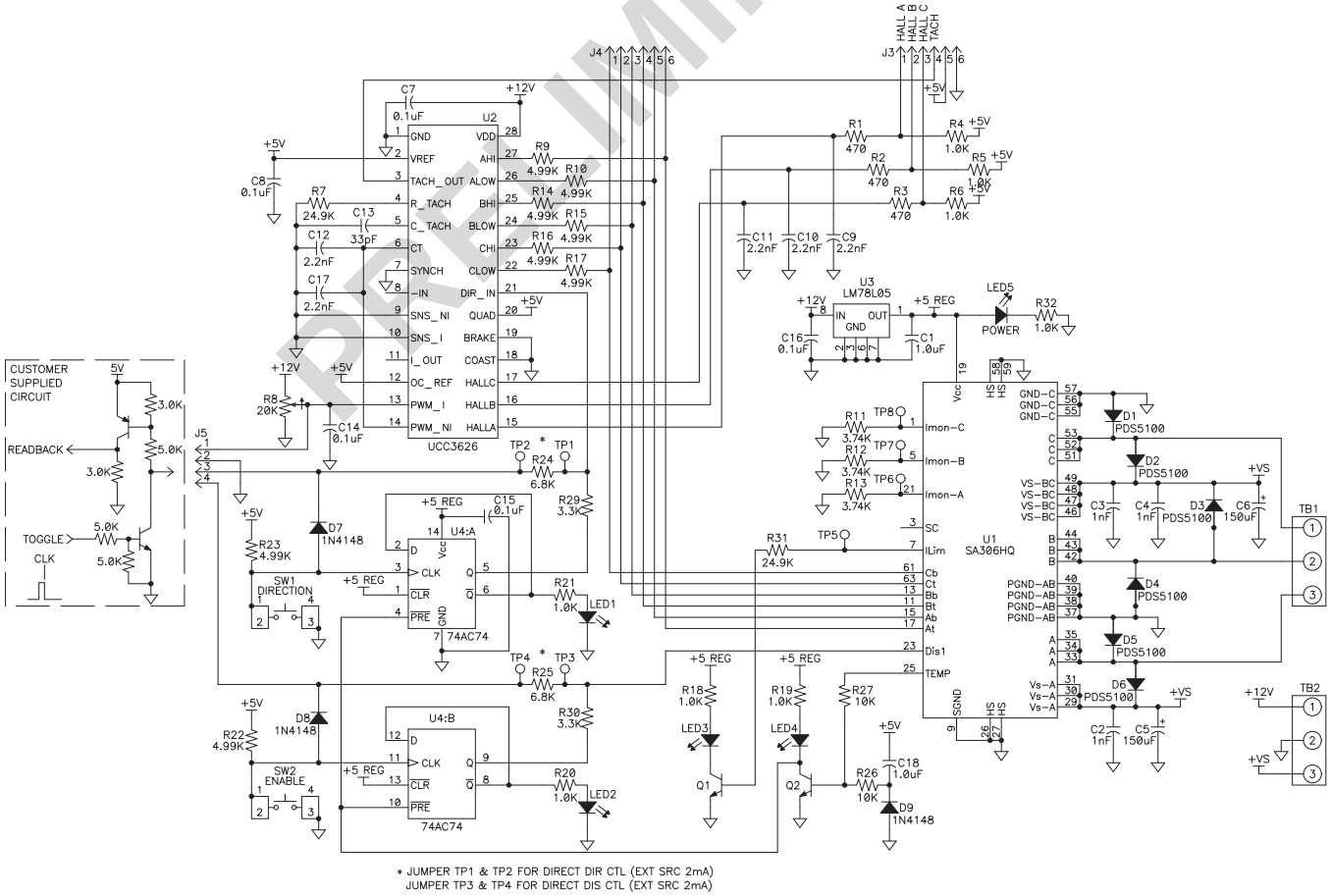


Figure 3 – Schematic



ENHANCING & BYPASSING THE DB303R CONTROL CIRCUIT

Connector J5 allows the user to bypass many of the manual control features of the DB303R. A signal generator can control the duty cycle with a 2.5 to 7.5V signal, overriding the control potentiometer. A rising 5V edge on pin 3 or 4 of connector J5 will toggle the Direction or Enable latches, respectively. By jumping resistors R24 & R25, the latches are bypassed completely and the logic signals on pins 3 & 4 will directly control the direction and enable functions of the DB303R. With these resistors jumped, the direction and enable LEDs will not represent the states of the DB303R and the pushbuttons will have no effect on the operation. The Temperature disable feature of the DB303R will also not function, although the LED will continue to provide over-temperature status.

Connector J4 is connected directly to the PWM input pins of the SA303. This connector may be used to monitor the signals or to bypass the control IC on the DB303R. The enable function is not controlled via these pins, although pulling all six input pins low provides the same effect. The Enable pushbutton and the connection via J5 are also effective as previously described. The circuit shown in figure 3 in the dashed box is a simple circuit that allows the user to monitor and control the enable or direction status remotely. Either feature can be toggled on the falling edge of the signal at the node labeled TOGGLE.

LAYOUT CONSIDERATIONS

A simple two layer construction is sufficient because of the convenient pinout of the SA303 PowerQuad package. Input signals are routed into one side of the package and high power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise may corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. 1nF capacitors with excellent high frequency characteristics bypass the Vs motor supplies on each phase. Two 150µF electrolytic capacitors provide a local, low inductance source to accommodate surge currents. Six 100V Schottky diodes conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA303. These diodes are rated for 5A continuous and are mounted close to the SA303 to reduce inductance in the commutating current loop. For applications with continuous currents less than 5A, the Schottky diodes may not be necessary if the higher forward voltage internal body diodes and the associated power dissipation are manageable during commutation cycles.

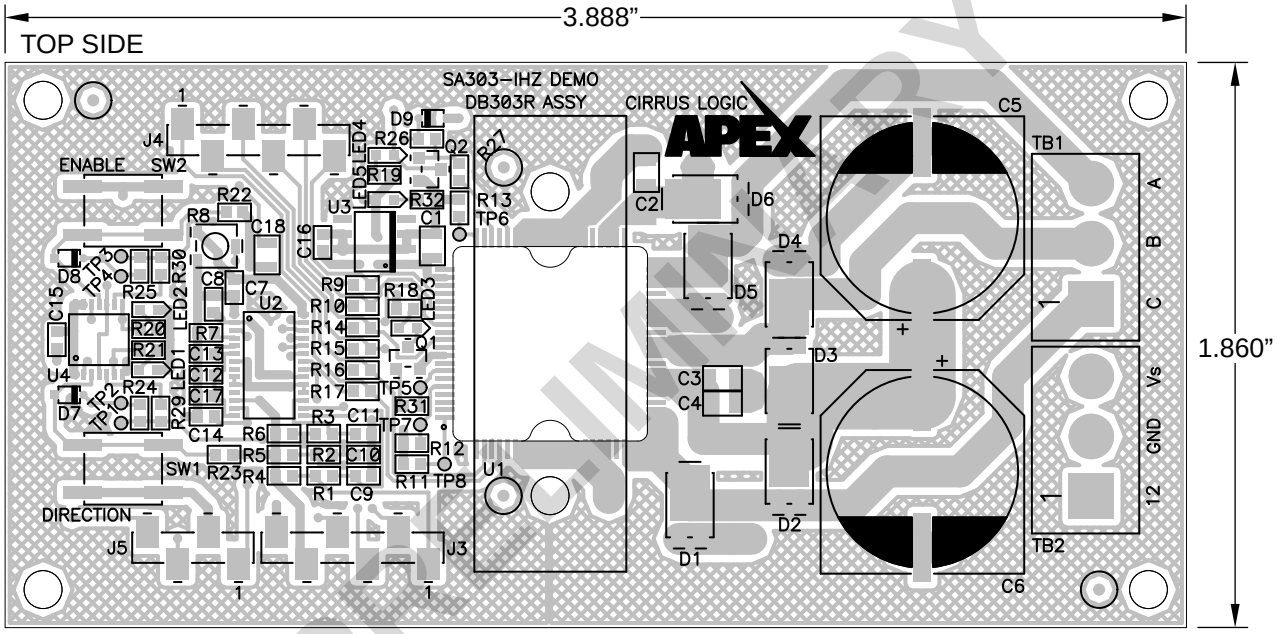
Figure 4 (next Page) shows the top and bottom layouts of the DB303R. Gerber files for the circuit board are available upon request.

BILL OF MATERIALS

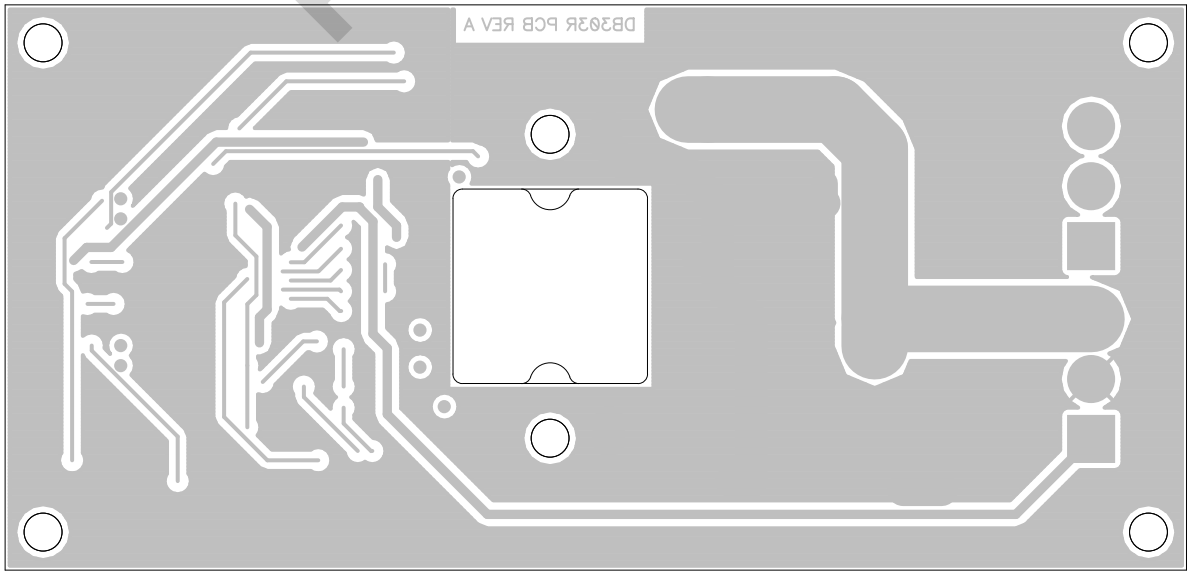
Designation	Description	P/N
C1,C18	CAP, 1.0uF, 16V	Kemet, C0805C105K4RAC
C13	CAP, 33pF, 50V	Kemet C0603C330J5GACTU
C2,C3,C4	CAP, 1.0nF,100V	Kemet,C0805C102J1GACTU
C5,C6	CAP, 150uF, 100V	Panasonic, EEVFK2A151M
C7,C8,C14,C15,C16	CAP, 0.1uF, 16V	GRM188F51C104ZA01D
C9,C10,C11,C12,C17	CAP, 2.2nF, 50V	GRM188R71H222KA01D
D1,D2,D3,D4,D5,D6	Diode, 5A Schottky	Diodes Inc. DS5100
D7,D8,D9	IN4148	Vishay, 1N4148WS-V-GS08
J3,J4	Conn, 6 pin .100 ctrs	Samtec TSM-106-01-T-SV
J5	Conn, 4 pin .100 ctrs	Samtec TSM-104-01-T-SV
LED1-5	LED, Red	Lite-On LTST-C190CKT
Q1,Q2	XTR, NPN	MMBT3904
R1,R2,R3	RES, 470, 5%	RK73B1JTTDD471J
R11,R12,R13	RES 2.0K, 1%	Vishay,CRCW06032K00FKEA
R24,R25	RES, 6.8K	Vishay,CRCW06036K80FKEA
R26,R27	RES, 10K	Vishay,CRCW060310K0FKEA
R29,R30	RES, 3.3K	Vishay,CRCW06033K30FKEA
R4,R5,R6,R18,R19,R20,R21,R32	RES, 1.0K, 5%	RK73B1JTTD102J
R7,R31	RES, 24.9K,1/10W, 1%	RK73H1JTTD2492F
R8	POT, 20K	muRata, PVG3A203C01
R9,R10,R14,R15,R16,R17,R22,R23	RES, 4.99K	Vishay,CRCW06034K99FKEA

Designation	Description	P/N
SW1,SW2	Pushbutton, SPST-NO	Panasonic, EVQ-Q2B01W
TB1,TB2	Term. Blk., 3 pin, 5mm	On Shore Tech, OSTTA034163
Thermal Grease	Heatsink compound	N/A
U1	SA303-IHZ	Apex Precision Power, SA303-IHZ
U2	UCC3626	Texas Instruments, UCC3626PW
U3	LM78L05	National Semiconductor, LM78L05ACMX/NOPB
U4	74AC74	Texas Instruments, SN74AC74PW
	Heatsink	Apex Precision Power, HS33
	PCB, 1.75” x 3.75”	Apex Precision Power, DB303R
	Screw, #4-40 x ¼”	N/A
	Solder	Tin/Silver 96/4

Figure 4 – PCB Layout (not to scale)



BOTTOM SIDE



F

DB303R Quick Start Guide

1. Connect the following:

Connection	Location	Indicator	Comment
Vs	TB2-3		9-60V
Ground	TB2-2		
Vctrl	TB2-1	LED 2	12V
Motor Phase A	TB1-1		
Motor Phase B	TB1-2		
Motor Phase C	TB1-3		
Hall Sensor A	J3-1		
Hall Sensor B	J3-2		
Hall Sensor C	J3-3		
Hall 5V	J3-5		Output from PCB
Hall ground	J3-6		

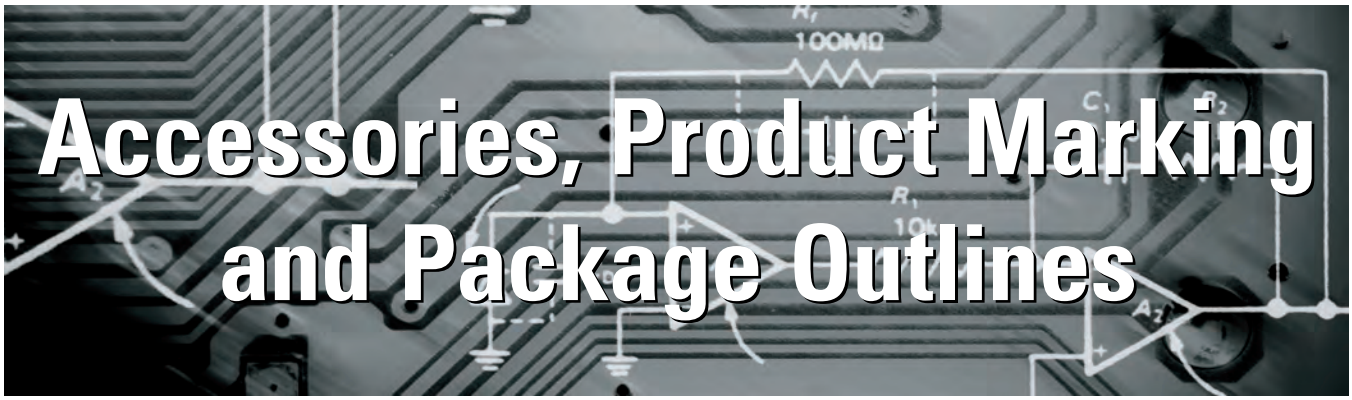
2. Apply 12V to Vctrl. LED 2 should light.
3. Apply voltage to Vs based on rated motor voltage, normally 12-48V.
4. Press ENABLE switch 3. LED 4 will light and motor should start.

ORDERING INFORMATION

DB303R Demonstration Board includes one populated DB303R PCB and one SA303-IHZ sample

CONTACTING CIRRUS LOGIC SUPPORT

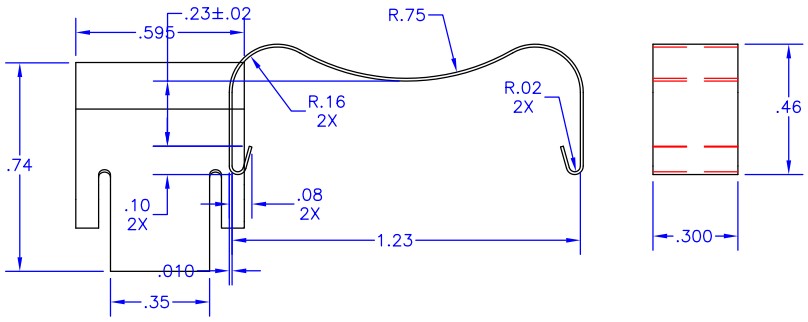
For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

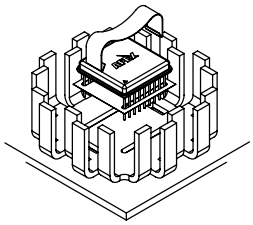


Accessories, Product Marking and Package Outlines

Accessories For Apex Precision Power

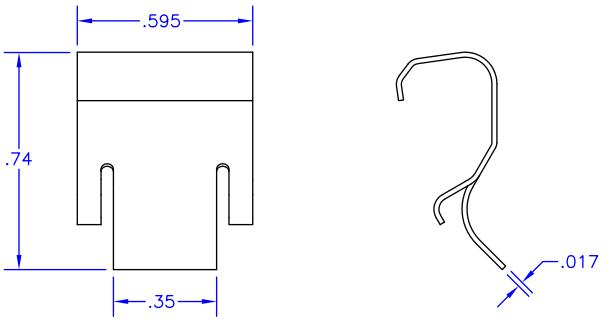
DIP Clamp CLAMP02

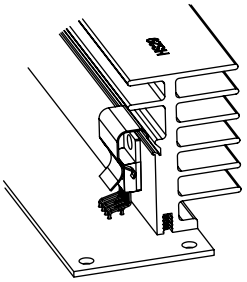




NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Break all sharp edges, de−burr and remove loose chips.
3. Material: ,010 thick 302 stainless, full hard
4. Finish: None
5. Used with HS21 heatsink.
6. Approximate weight: .03 oz. [.85 g]

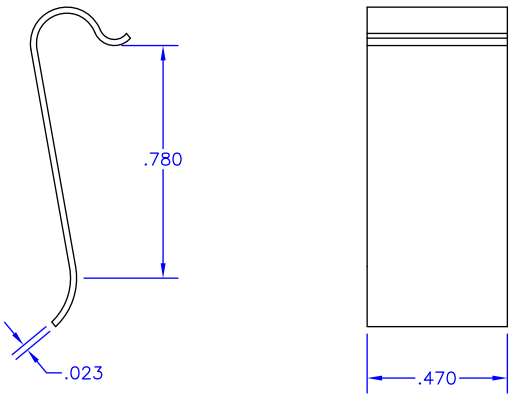
TO-220 Clamp CLAMP04

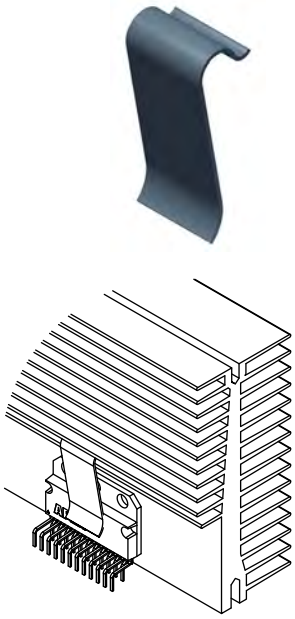




NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Break all sharp edges, de−burr and remove loose chips.
3. Aavid Thermalloy part number 4426.
4. Material: Black oxide finished spring steel
5. Used with HS29 heatsink.
6. Approximate weight: .05 oz. [1.4 g]

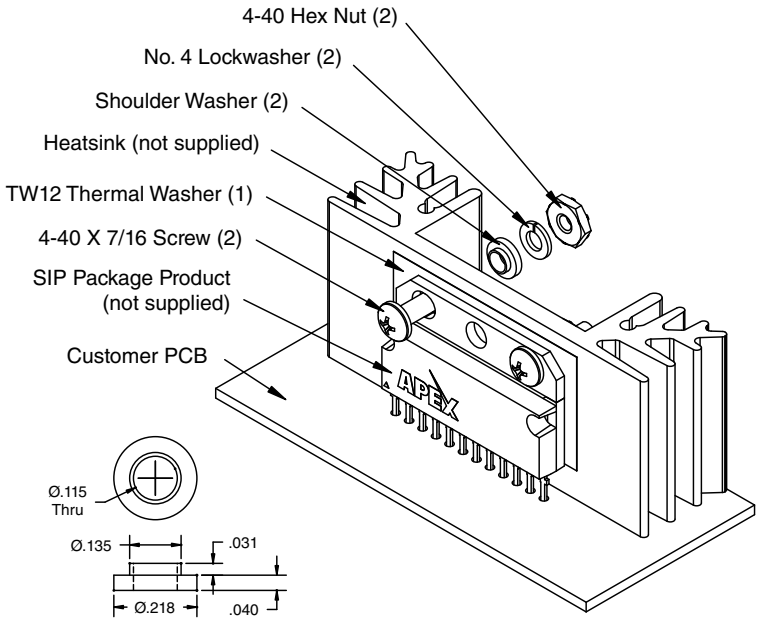
SIP Clamp CLAMP05





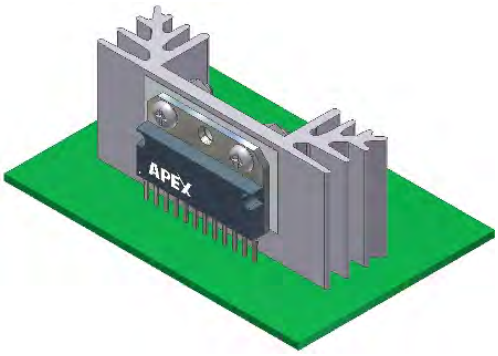
NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Break all sharp edges, de-burr and remove loose chips.
3. Aavid Thermalloy part number MAX10.
4. Used with HS32 heatsink.

SIP Mounting Kit HK26



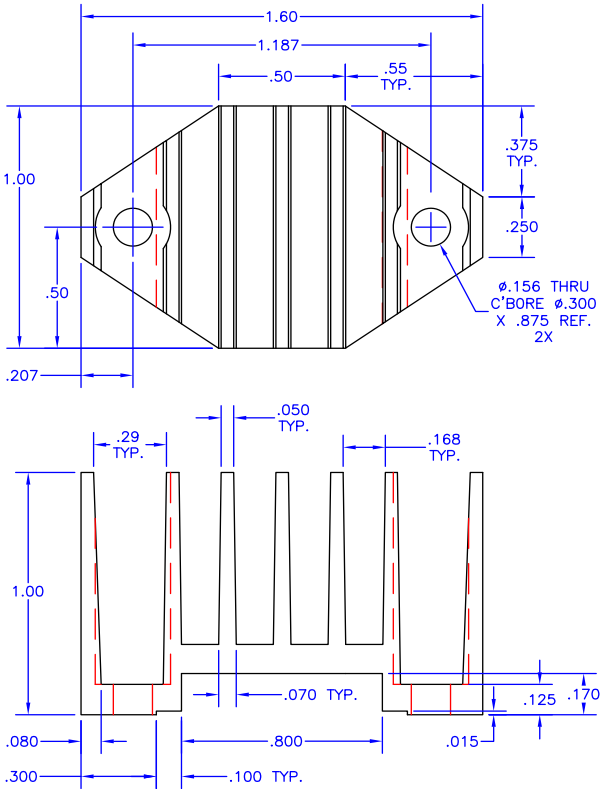
Shoulder Washer Dimensions

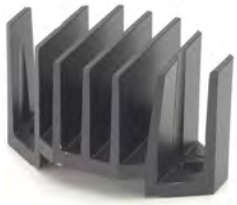
Keystone Part No. 3049
Nylon 6/6 per ASTM D4066

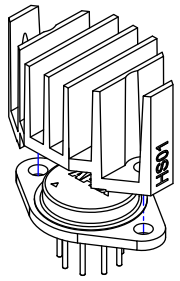


G

TO-3 Heatsink HS01

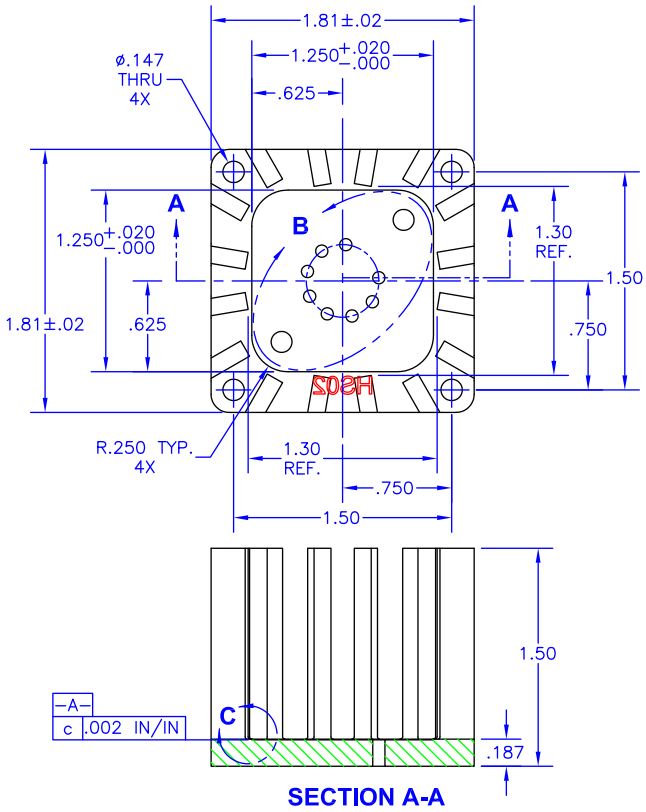


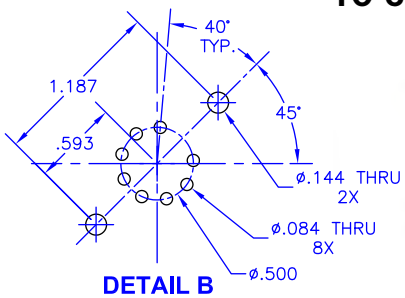




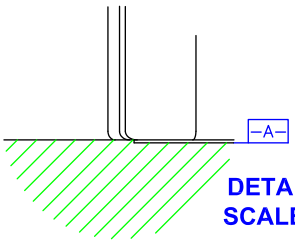
NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: Aluminum (M/F AAVID Thermalloy NP971944)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 0.6 oz [17g]

TO-3 Heatsink HS02

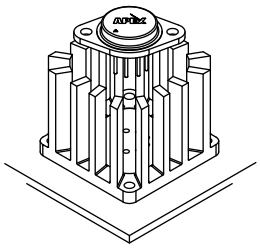




DETAIL B
SCALE 1:1

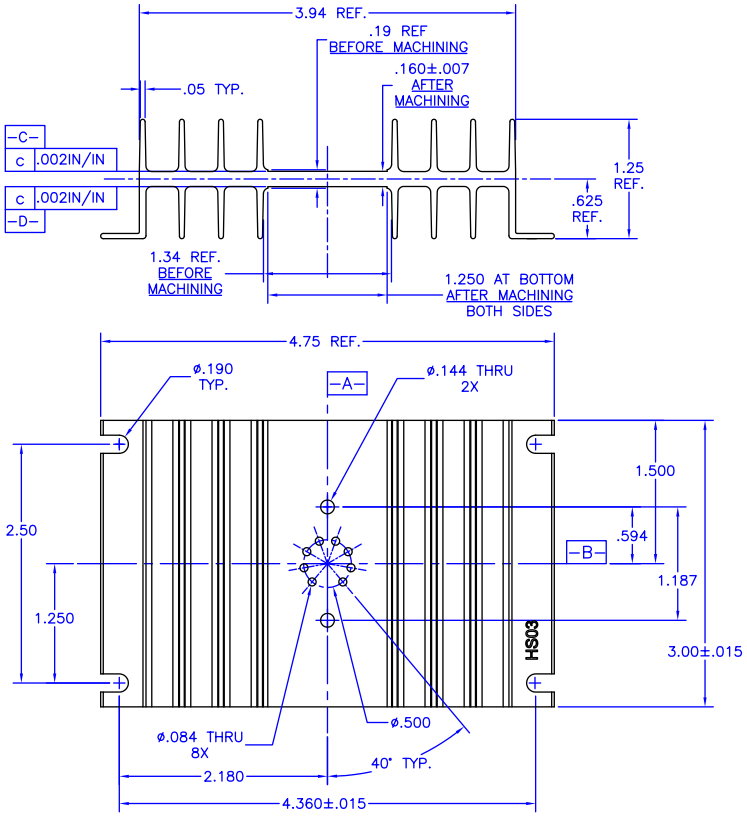


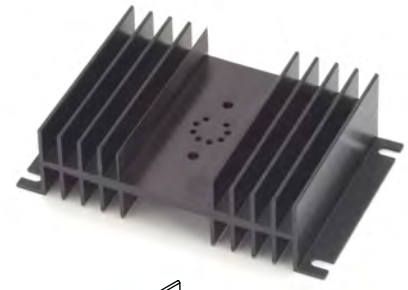
DETAIL C
SCALE 4:1

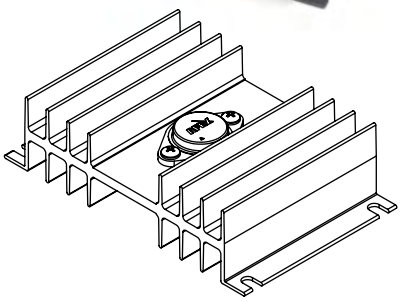


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: Aluminum (M/F AAVID Thermalloy 5684 stamping blank)
4. Machine 1.25x1.25 area of surface –A– flat to within .002 in/in.
5. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
6. Mark with contrasting ink as shown, if specified by P.O.
7. Approximate Weight: 1.9 oz [54g]

TO-3 Heatsink HS03



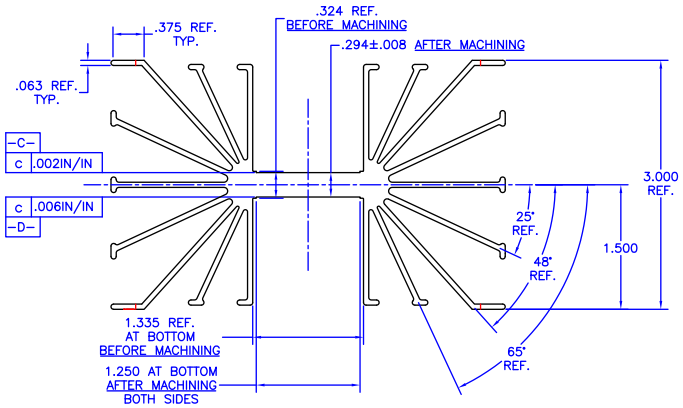


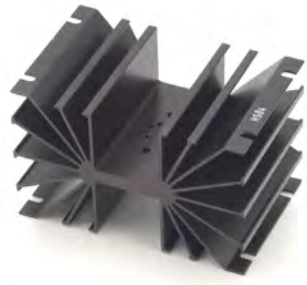


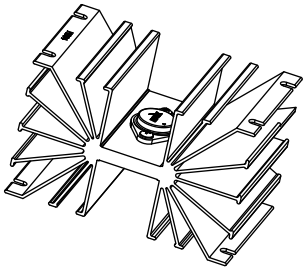
NOTES:

1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum
   (AAVID Thermalloy extrusion 60050)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 6.2 oz [176g]

TO-3 Heatsink HS04





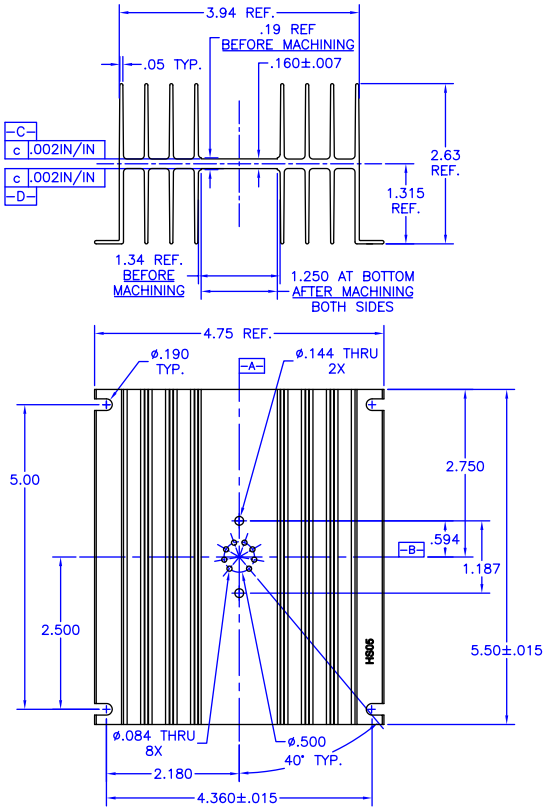


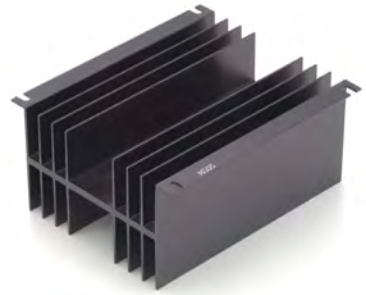
NOTES:

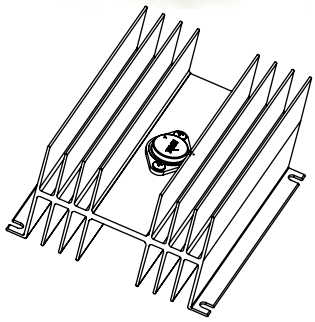
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum (AAVID Thermalloy extrusion 60650)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 11.6 oz [329g]

G

TO-3 Heatsink HS05

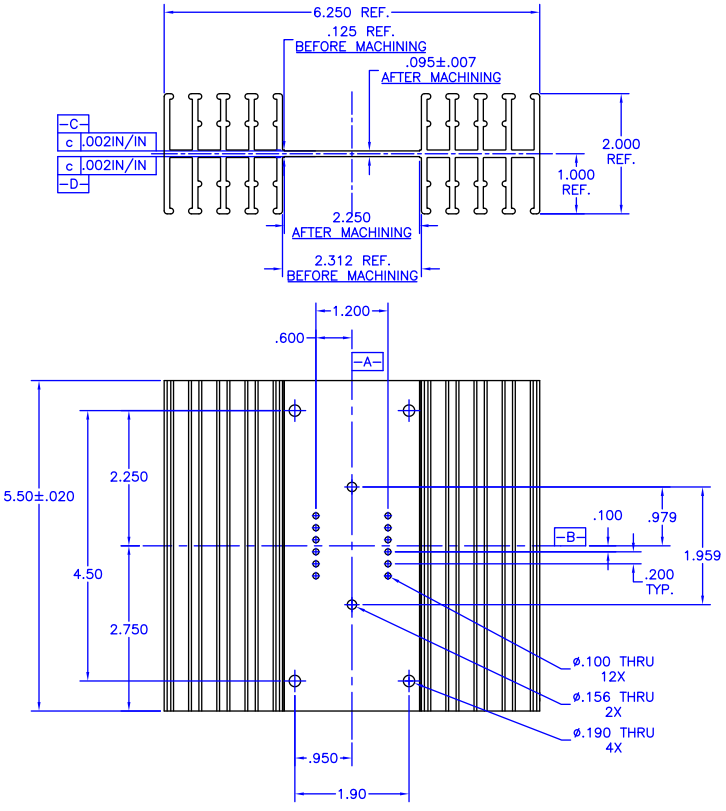


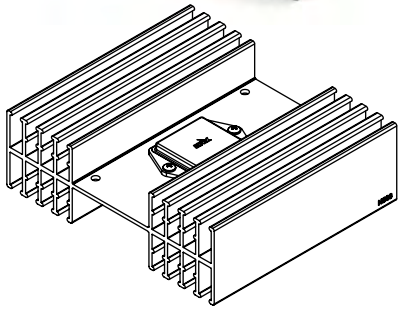




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 60055)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 16.3 oz [462g]

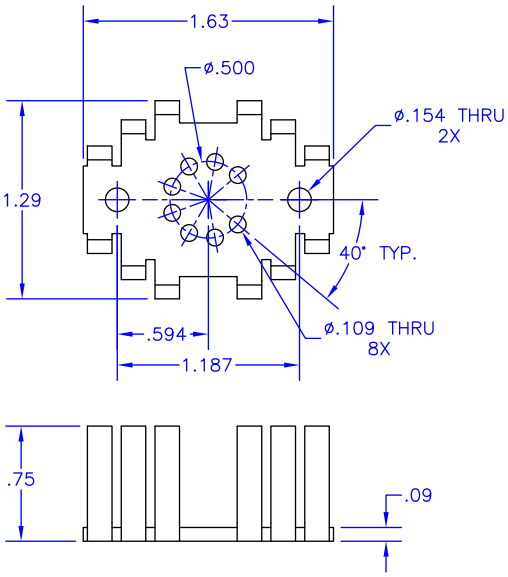
Power DIP Heatsink HS06





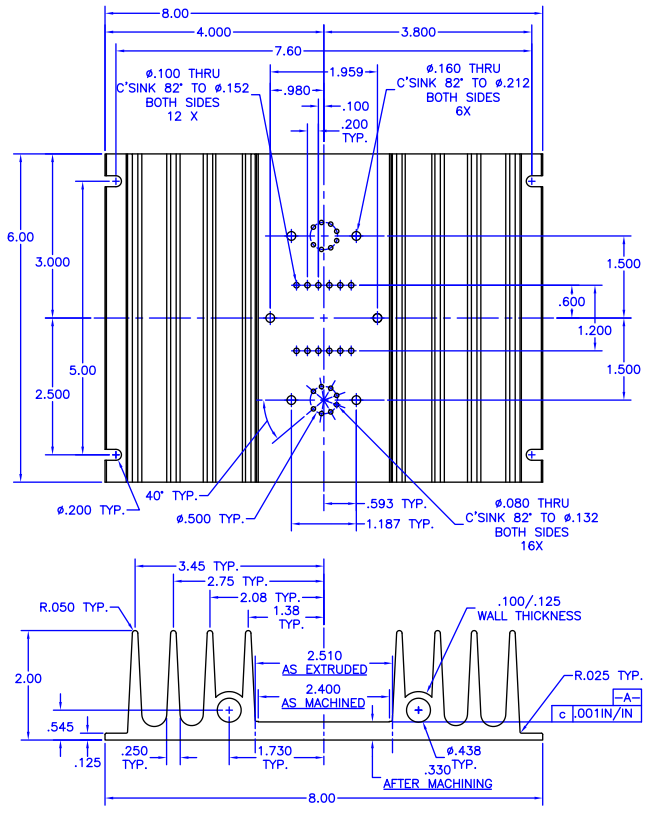
NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 60315)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 24.2 oz [686g]

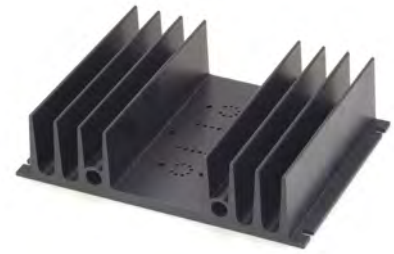
TO-3 Heatsink HS09

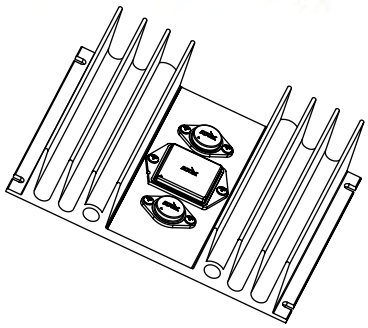


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: Aluminum alloy
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 0.4 oz [11g]

TO-3 + Power DIP Heatsink HS11



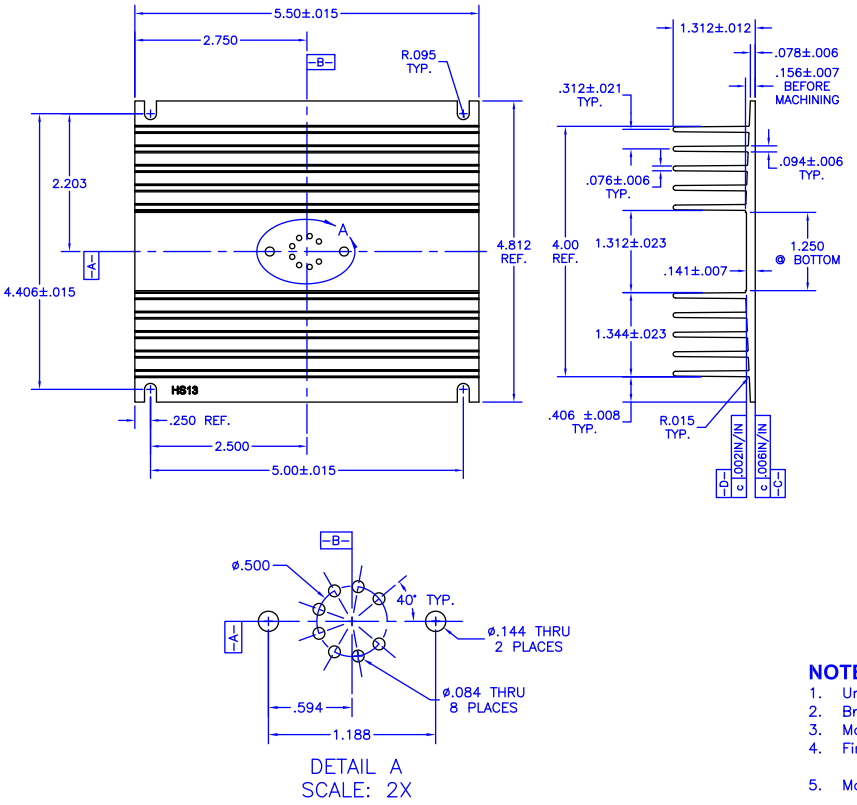


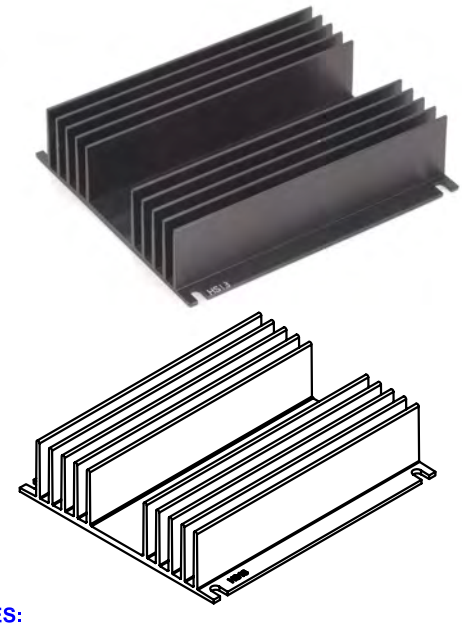


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 46.2 oz [1310g]

G

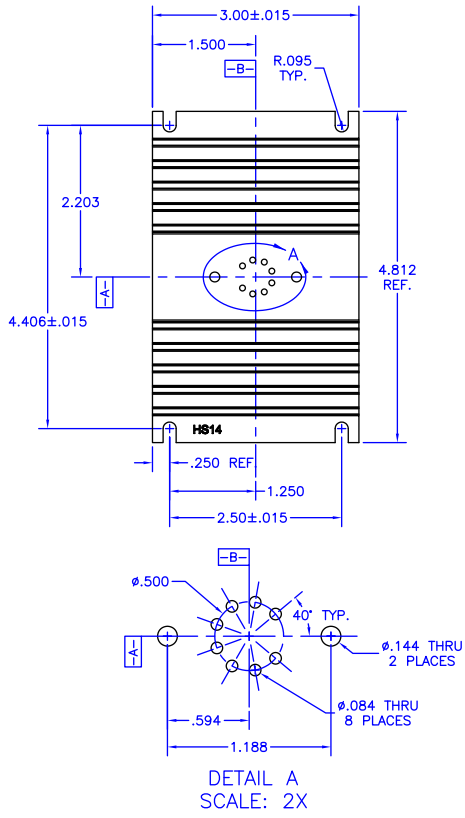
TO-3 Heatsink HS13

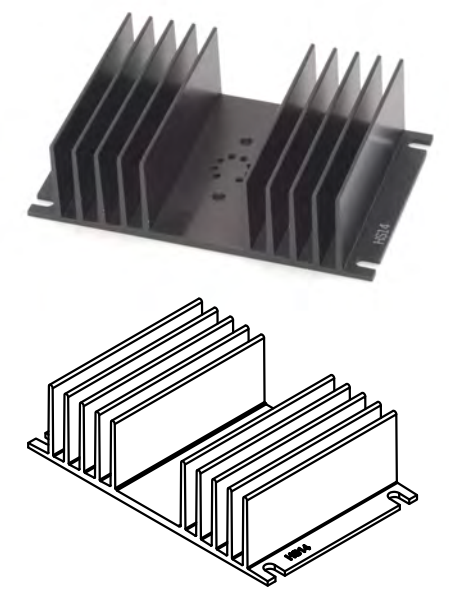




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum (AAVID Thermalloy extrusion 60840)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

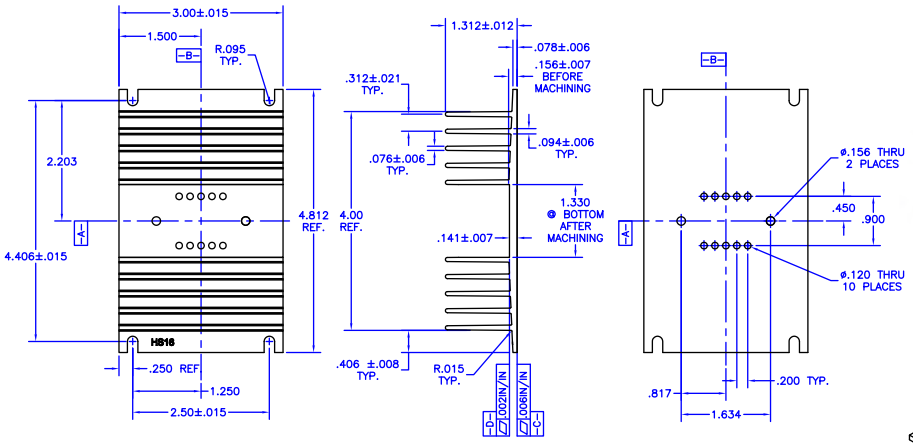
TO-3 Heatsink HS14

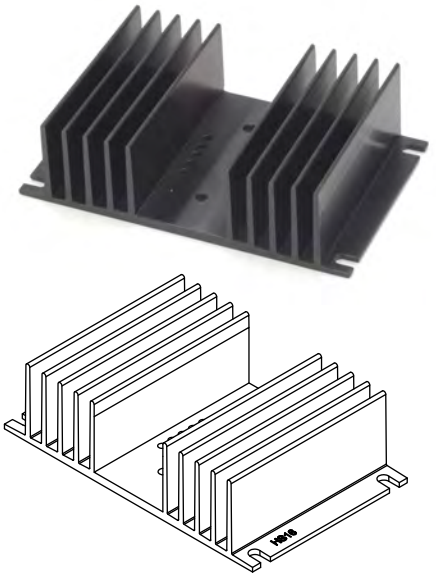




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum (AAVID Thermalloy extrusion 60840)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

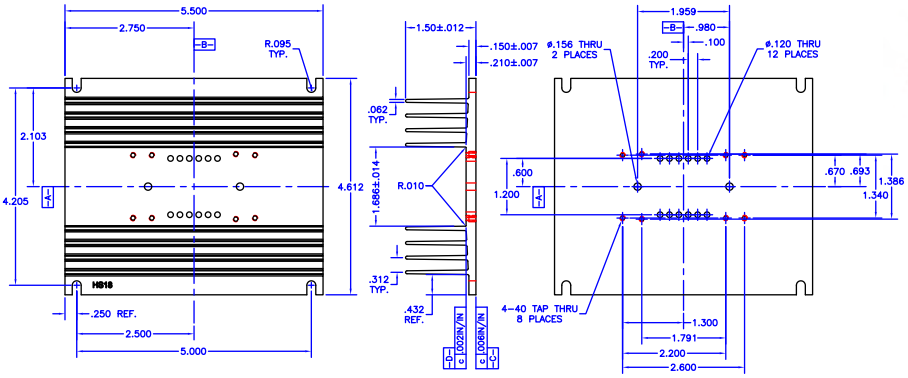
10-Pin Power DIP Heatsink HS16

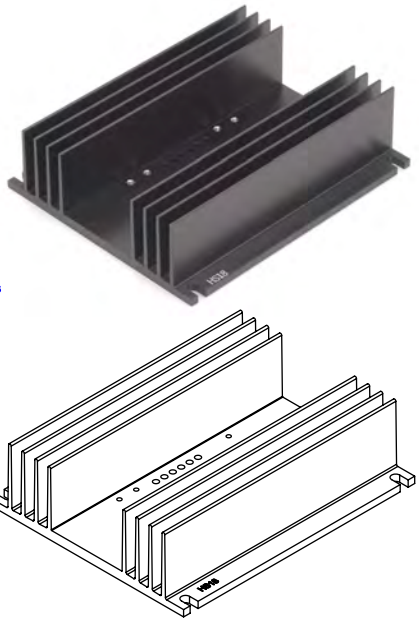




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 60840)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

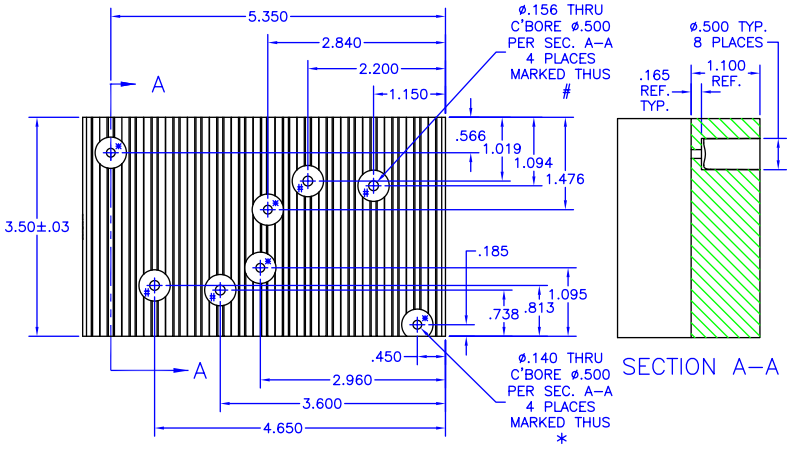
Open Frame Heatsink HS18

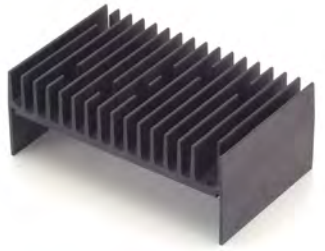


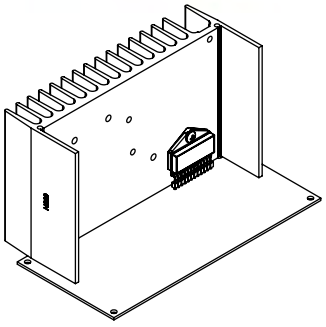


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 72555)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

Power SIP Heatsink HS20

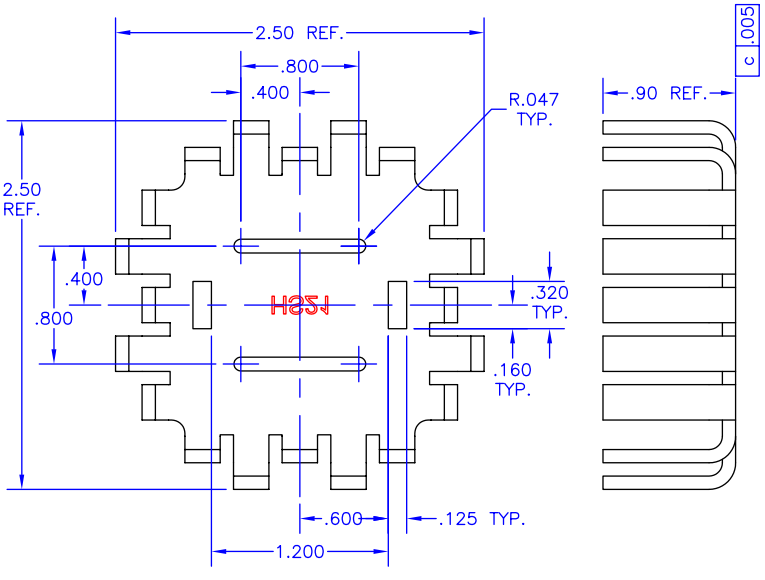


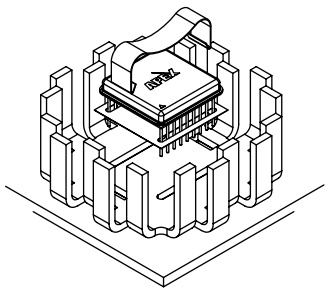




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum (AAVID Thermalloy extrusion 79510)
4. As extruded, this dimension is .075. It is approximately .050 after machining for flatness.
5. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
6. Mark with contrasting ink as shown, if specified by P.O.
7. Approximate Weight: 15.7 oz [445g]

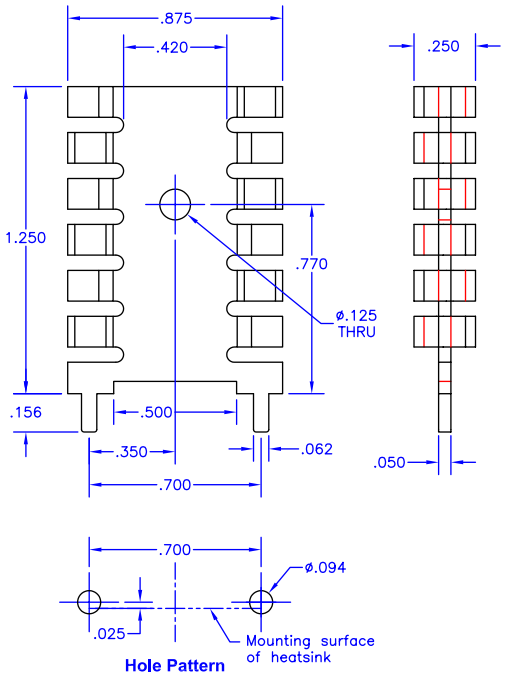
DIP Heatsink HS21

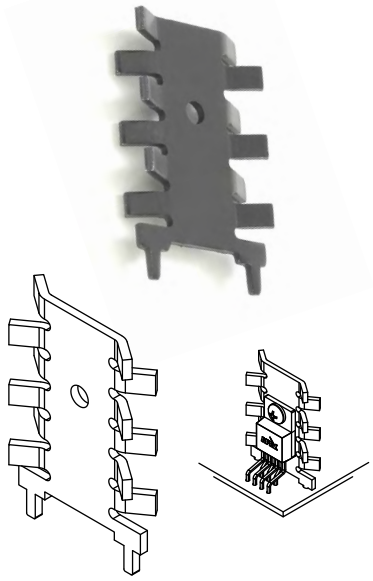




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: 6063–T5 aluminum (M/F CTS/IERC HP1–218 series)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 1.1 oz. [31g]

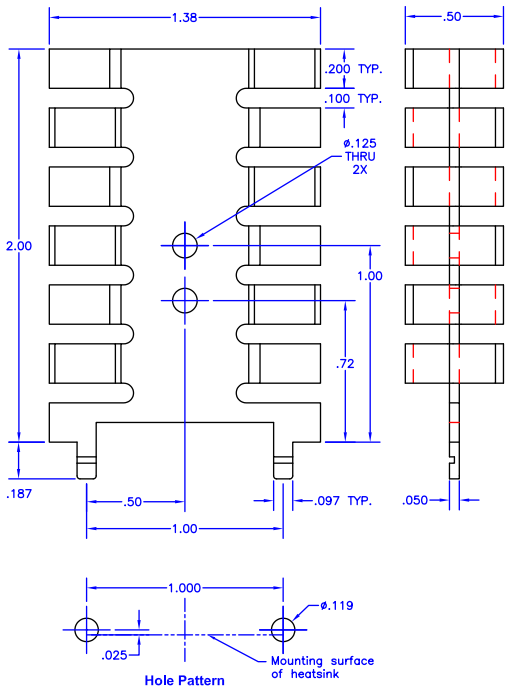
TO-220 Heatsink HS22

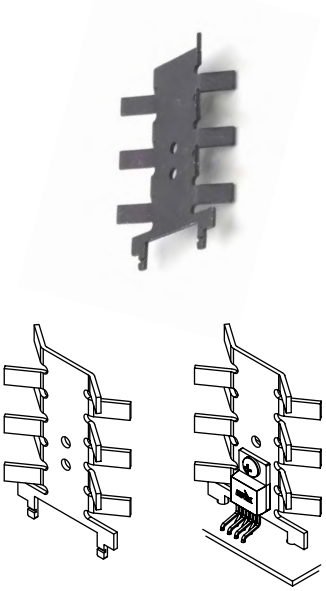




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: Aluminum (AAVID Thermalloy #542502b00000)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 0.1 oz [3g]

TO-220 Heatsink HS23

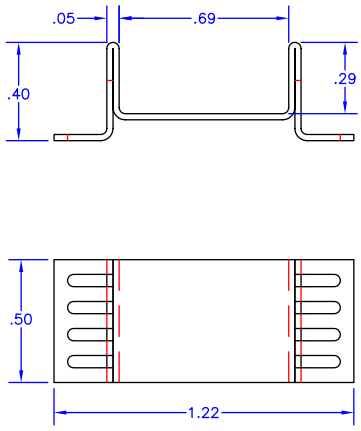


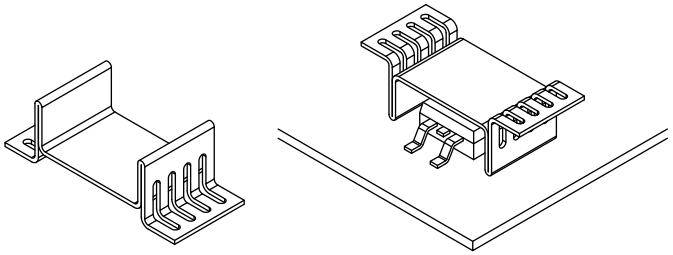


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de–burr & remove loose chips.
3. Material: Aluminum (AAVID Thermalloy #563202b00000)
4. Finish: Anodize per MIL–A–8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 0.2 oz [6g]

G

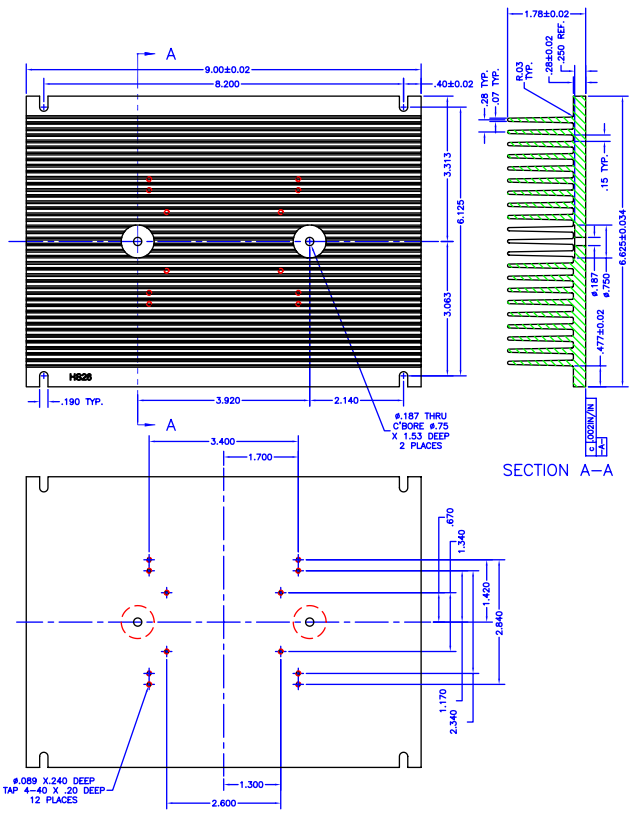
SMT Heatsink HS24

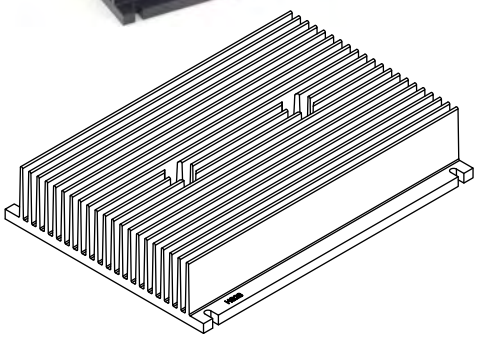




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: Copper (AAVID Thermalloy #573400d00000)
4. Solderable finish
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 0.2 oz [6g]

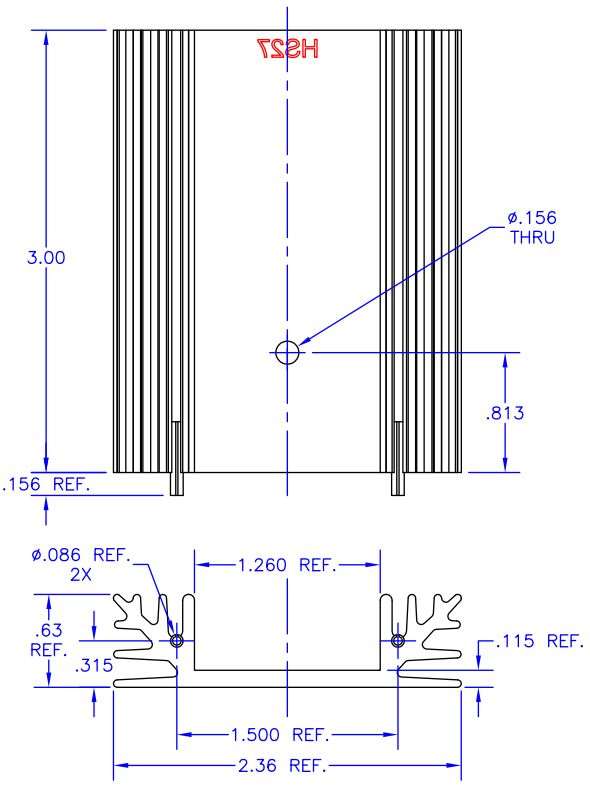
Open Frame Heatsink HS26

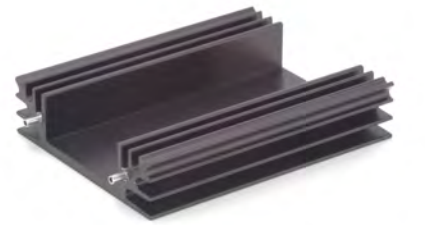


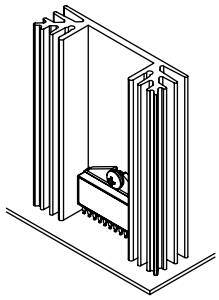


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 69800)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

Power SIP Heatsink HS27

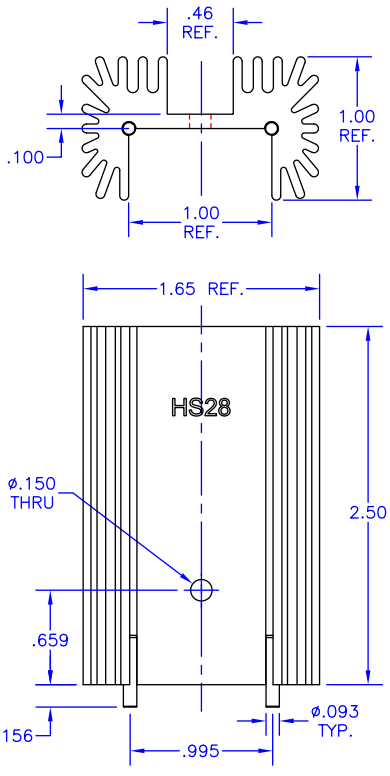


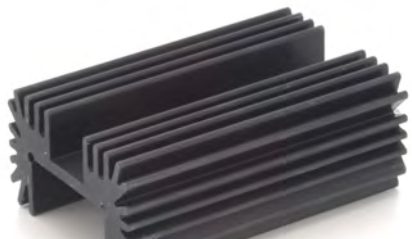


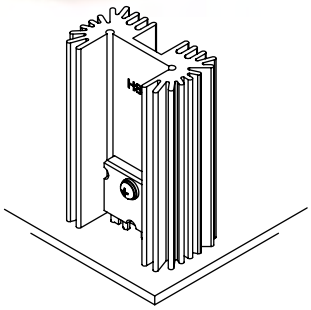


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy #6374B with custom length and hole.)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 2.5 oz. [71g]

Power SIP Heatsink HS28



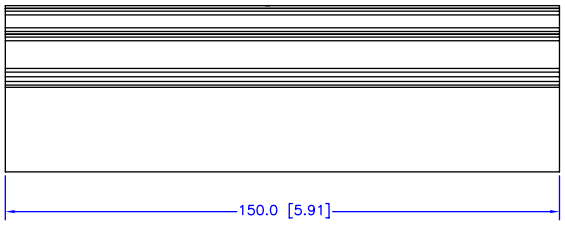


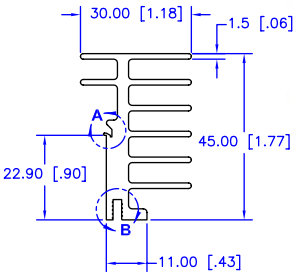


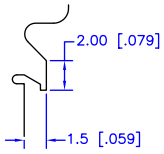
NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 63485)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Approximate Weight: 2.6 oz. [74g]

G

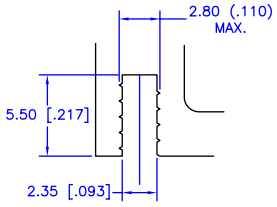
TO-220 Heatsink HS29



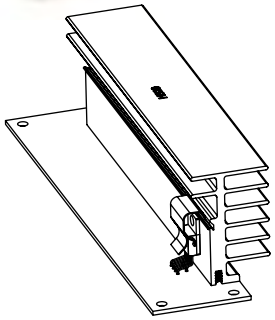




DETAIL A

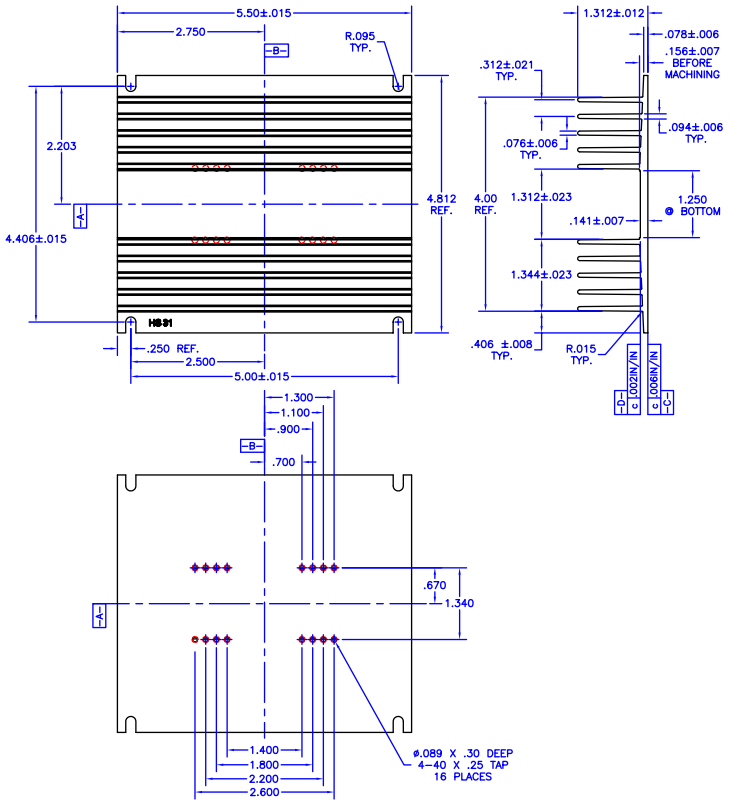


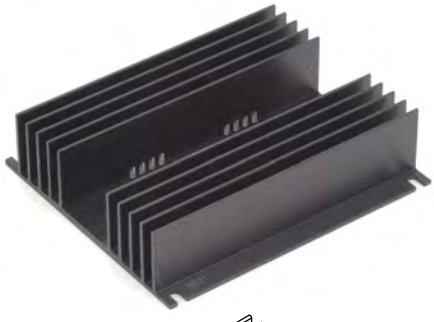
DETAIL B

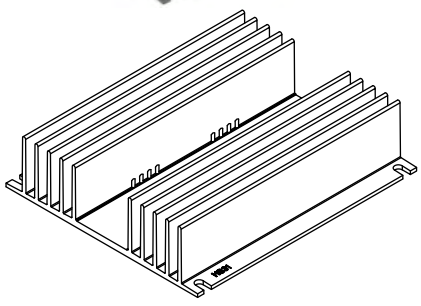


NOTES:
1. Dimensions are in millimeters; alternate units are inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 Aluminum (AAVID Thermalloy #KM150-1)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.
6. Heatsink is used with AAVID Thermalloy part #4426 (Apex CLAMP04).
7. Approximate Weight: 164g [5.8 oz.]

Open Frame Heatsink HS31

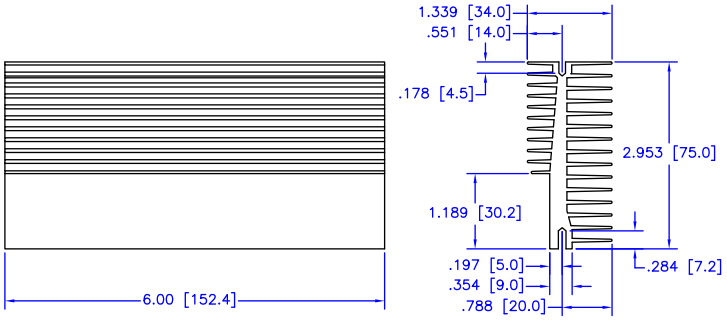


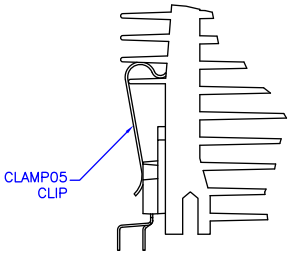


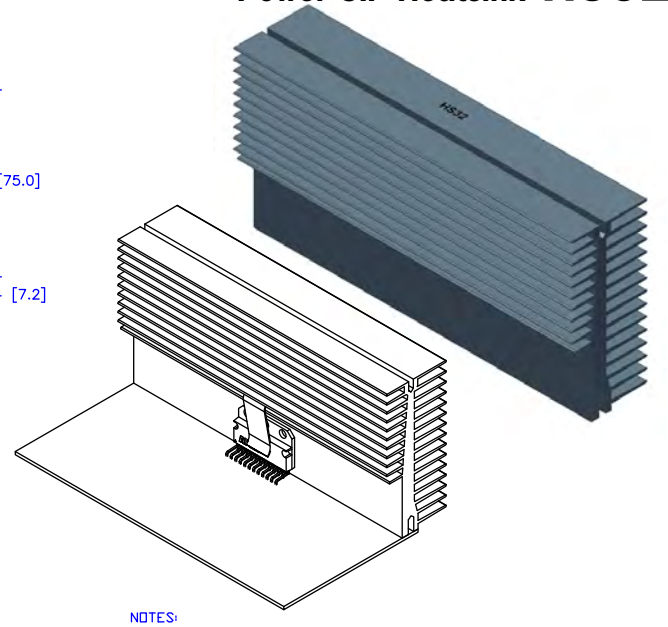


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum (AAVID Thermalloy extrusion 60840)
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black
   Typical breakdown voltage > 300V
5. Mark with contrasting ink as shown, if specified by P.O.

Power SIP Heatsink HS32

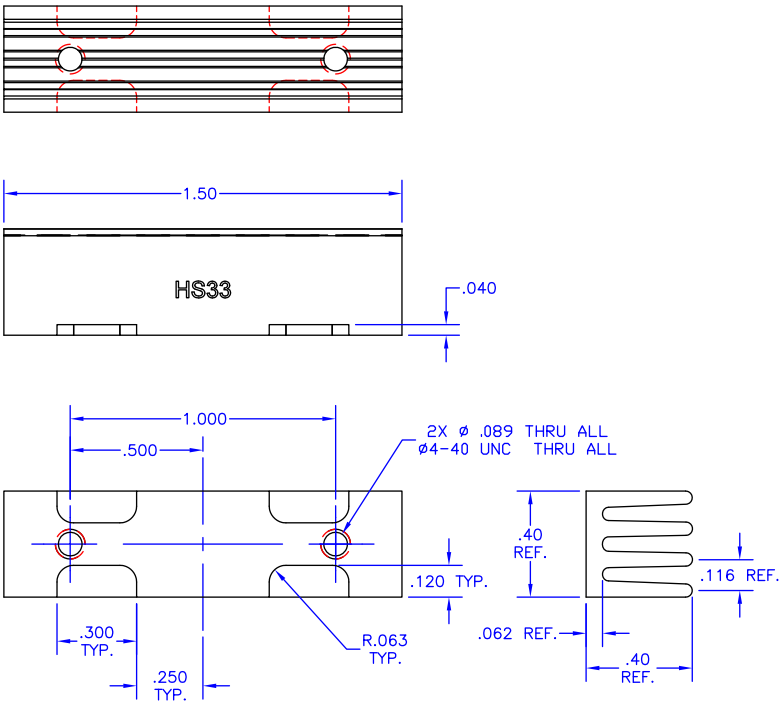




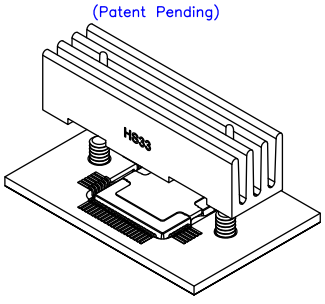


NOTES:
1. Dimensions are in inches; alternate units are millimeters.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 Aluminum (AAVID Thermalloy #780103B06000.
4. Finish: Anodize per MIL-A-8625, Type II, Class 2, Black. Typical breakdown voltage > 300V.
5. Mark with contrasting ink as shown, if specified by P.O.
6. DUT is secured to heatsink using APEX part CLAMP05 (AAVID Thermalloy #MAX10).
7. Approximate Weight: 362g [12.8 oz.]
8. Thermal resistance: 1.33°C/W

Flip SMT Heatsink HS33



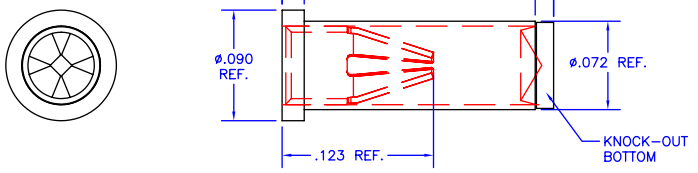
INVERTED THROUGH CIRCUIT BOARD
MOUNTING WITH HEAT SINK
(Patent Pending)

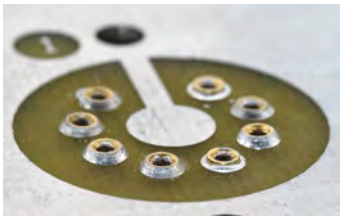


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Break all sharp edges, de-burr & remove loose chips.
3. Material: 6063-T5 aluminum alloy.
   Make from Aavid extrusion 70920
4. Mark with contrasting ink as shown, if specified by P.O.
5. Approximate Weight: 0.22 oz [6.3g]

G

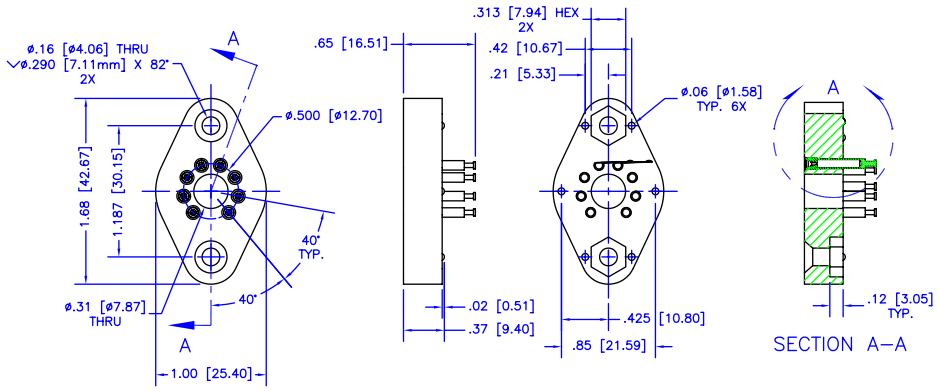
Pin Receptacle MS02

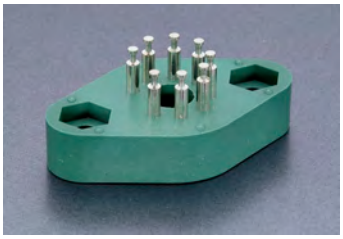


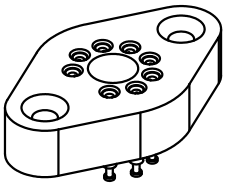


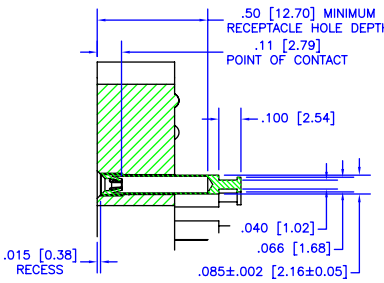
NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Shell: 360 brass, half–hard, with 10 µin gold over nickel
3. Contacts: Beryllium copper with 30 µin gold over nickel
4. Current rating: 8 amps, for 10°C temperature rise.
5. Solder mount in minimum .075 diameter mounting hole.
6. Mill–Max Part No. 0329–0–15–15–34–27–10–0

TO-3 Socket MS03





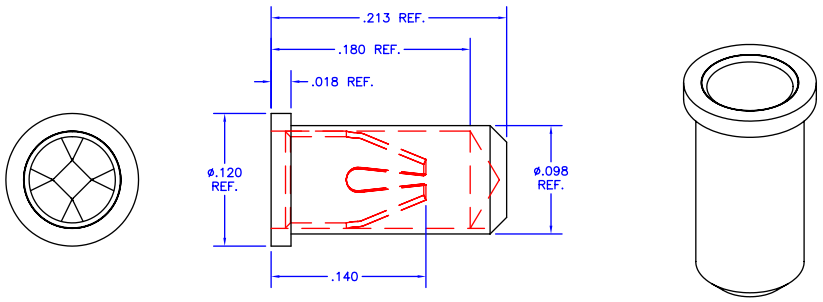


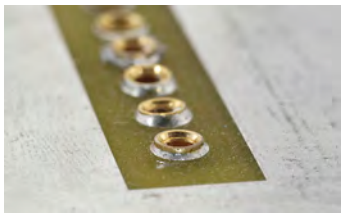


DETAIL A
SCALE 2:1

NOTES:
1. Dimensions are in inches & [mm].
2. Socket body: Glass–filled polyester, 94 VO rating, green in color
3. Receptacle shell: 360 brass, with 200 µin tin over 100 µin nickel
4. Receptacle contacts: Beryllium copper with 30 µin gold over 50 µin nickel
5. The continuous temperature rating of the socket shall be 150° C.
6. Contact resistance: 20 milliohms or less.

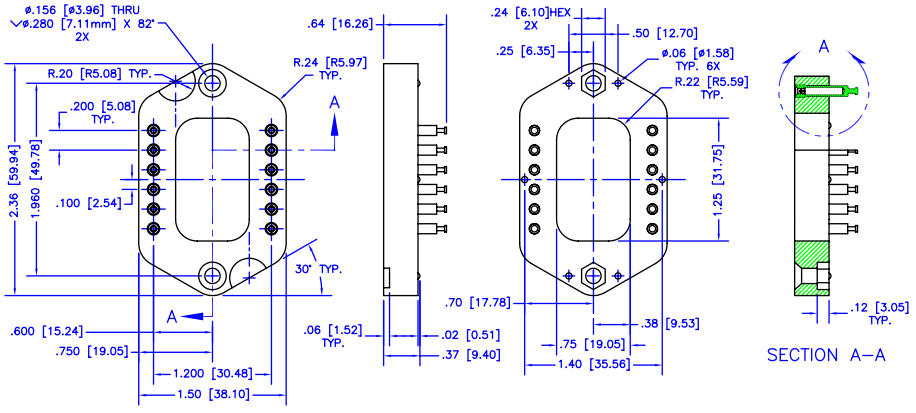
Pin Receptacle MS04

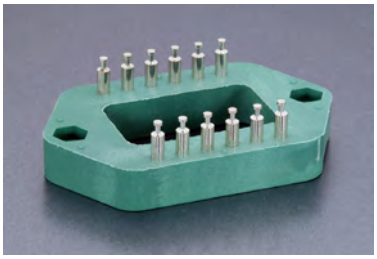


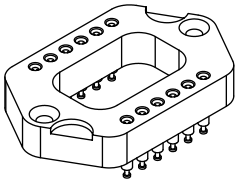


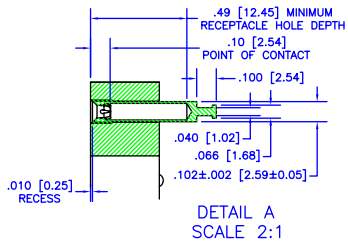
NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Shell: 360 brass, half-hard, with 10 µin gold over nickel
3. Contacts: Beryllium copper with 30 µin gold over nickel
4. Current rating: 11.2 amps, for 10°C temperature rise.
5. Solder mount in minimum .100 diameter mounting hole.
6. Mill-Max Part No. 0364-0-15-15-13-27-10-0

Power DIP Socket MS05







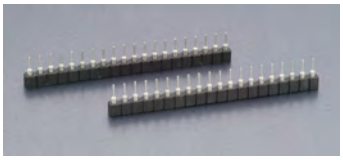


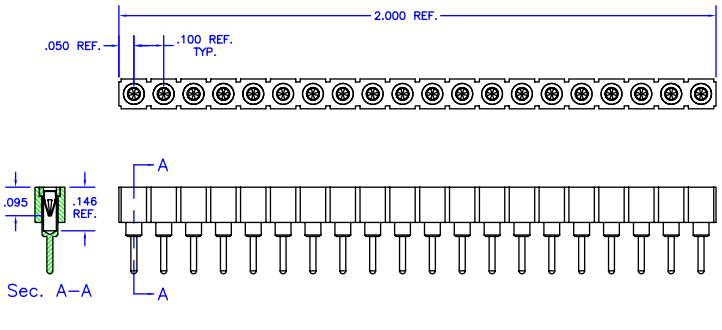
DETAIL A
SCALE 2:1

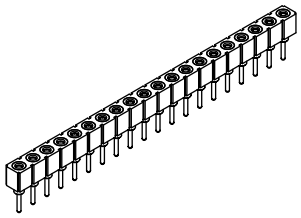
NOTES:
1. Dimensions are in inches & [mm].
2. Socket body: Glass-filled polyester, 94 VO rating, green in color
3. Receptacle shell: 360 brass, with 200 µin tin over 100 µin nickel
4. Receptacle contacts: Beryllium copper with 30 µin gold over 50 µin nickel
5. The continuous temperature rating of the socket shall be 150° C.
6. Contact resistance: 20 milliohms or less.

G

Mating Socket MS06

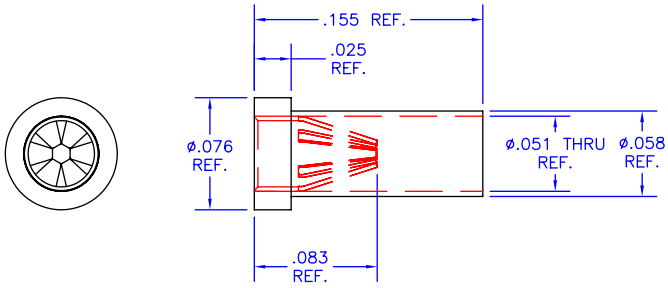


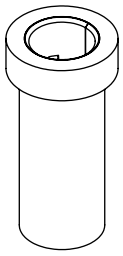


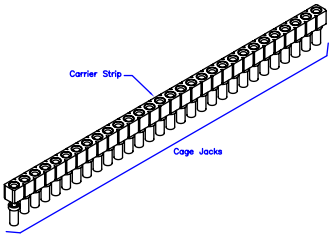


NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Shell: 360 brass, half-hard, with 200 µin tin/lead over nickel
3. Contacts: Beryllium copper with 30 µin gold over nickel
4. Body: Glass-filled black polyester, rated UL94V-0
5. Current rating: 3 amps, for 10°C temperature rise.
6. Solder mount in .028–.035 diameter hole.
7. Cut to length to suit application.
8. Mill-Max Part No. 310-93-120-41-001000

Pin Receptacle MS11

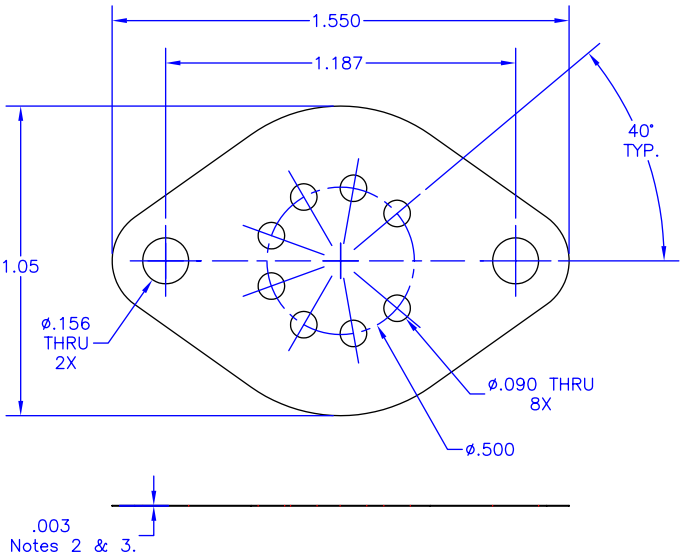


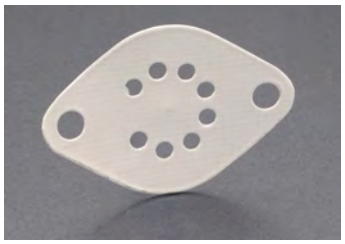


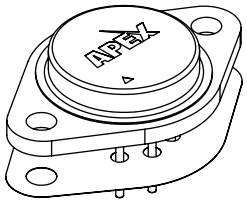


NOTES:
1. Unless otherwise noted, dimensions are in inches.
2. Shell: 360 brass, half-hard, with 200 µin tin/lead over nickel
3. Contacts: Beryllium copper with 10 µin gold over nickel
4. Current rating: 4.5 amps, for 10°C temperature rise.
5. Solder mount in minimum .059/.061 diameter mounting hole.
6. Mill-Max Part No. 0305-2-15-01-47-14-10-0
7. This receptacle is supplied on a 30-position carrier strip as Mill-Max part number S 703-93-130-47-050000.

TO-3 Thermal Washer TW03

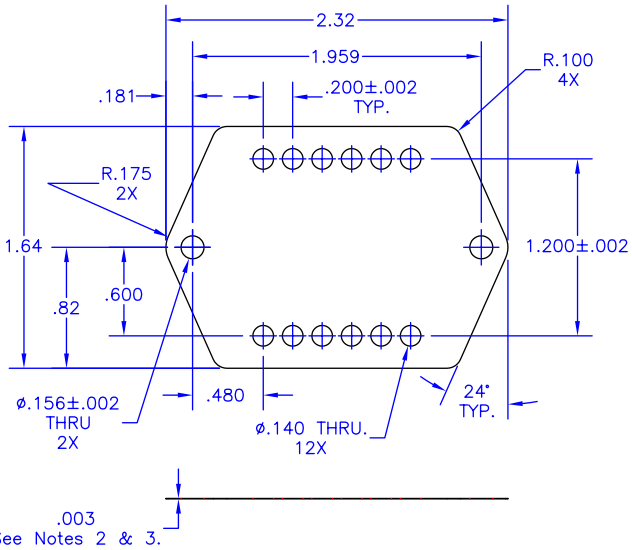


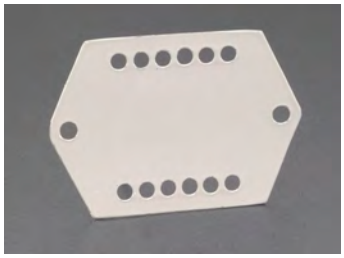


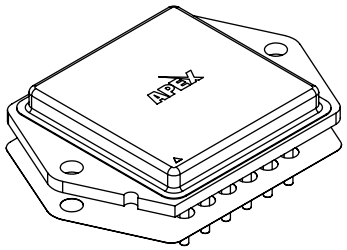


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Foil Material: .002 thick 1145 aluminum
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .030 °C–in²/W (.194 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with TO3 packages (Apex designator: CE).
7. Power Devices part no. AL–155–10C

Power DIP Thermal Washer TW05

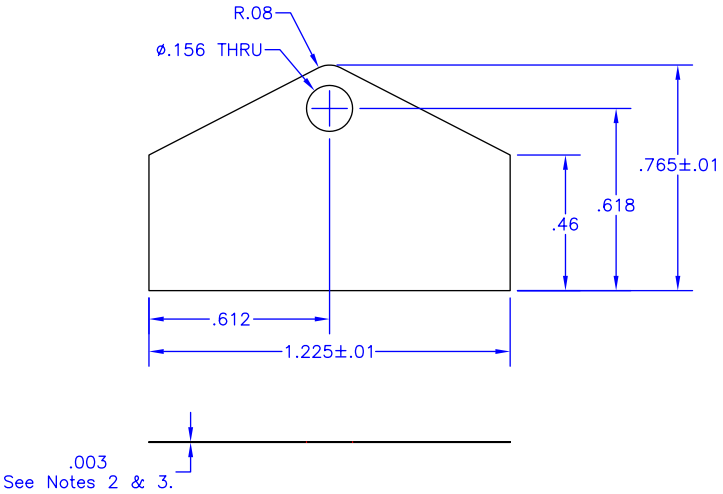


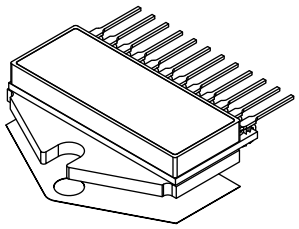




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Foil Material: .002 thick 1145 aluminum
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .030 °C–in²/W (.194 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with Power DIP packages (Apex designators: CR, CU, DC & DD).
7. Power Devices part no. AL–232–164

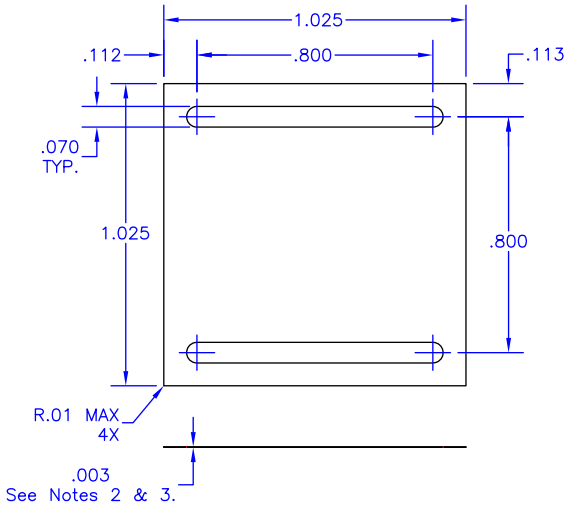
Power SIP Thermal Washer TW07

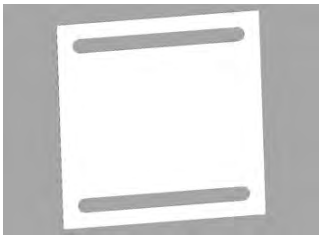


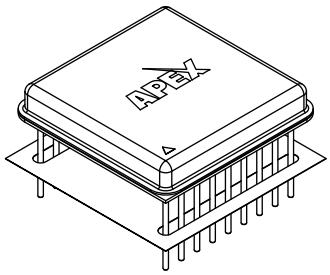


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Foil Material: .002 thick 1145 aluminum
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .030 °C–in²/W (.194 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with 12–pin PSIP packages (Apex designators: DP, ED, EE & EQ).
7. Power Devices part no. AL–123–077

DIP Thermal Washer TW09

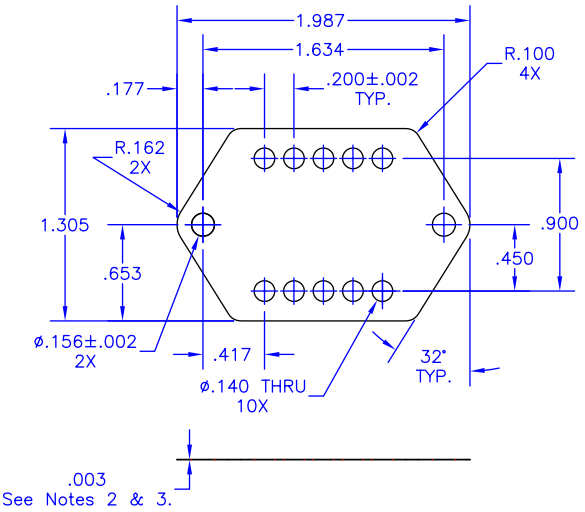


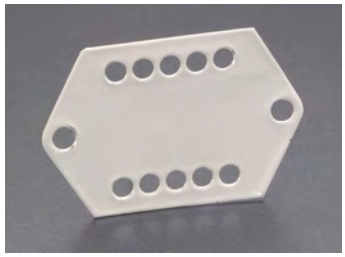


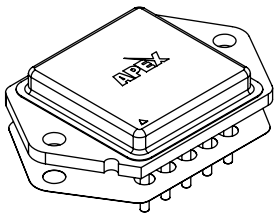


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Foil Material: .002 thick 1145 aluminum
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .030 °C–in²/W (.194 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with 18–pin DIP package (Apex designator: EL).
7. Power Devices part no. AL–103–103–APX

Power DIP Thermal Washer TW10

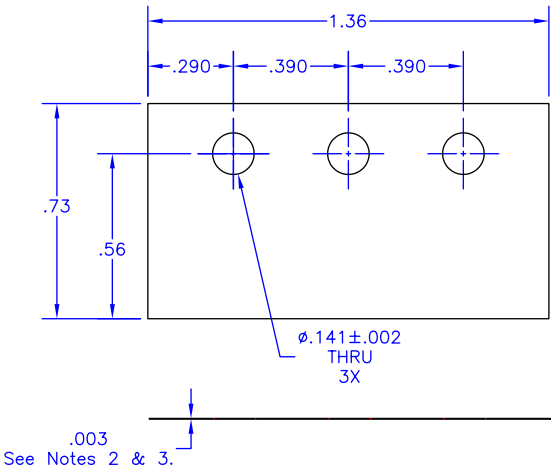


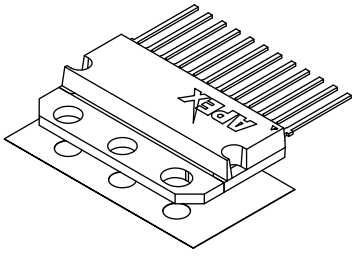




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Foil Material: .002 thick 1145 aluminum
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .030 °C–in²/W (.194 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with 10–pin Power DIP package (Apex designator: DE).
7. Power Devices part no. AL–199–131

Power SIP Thermal Washer TW12

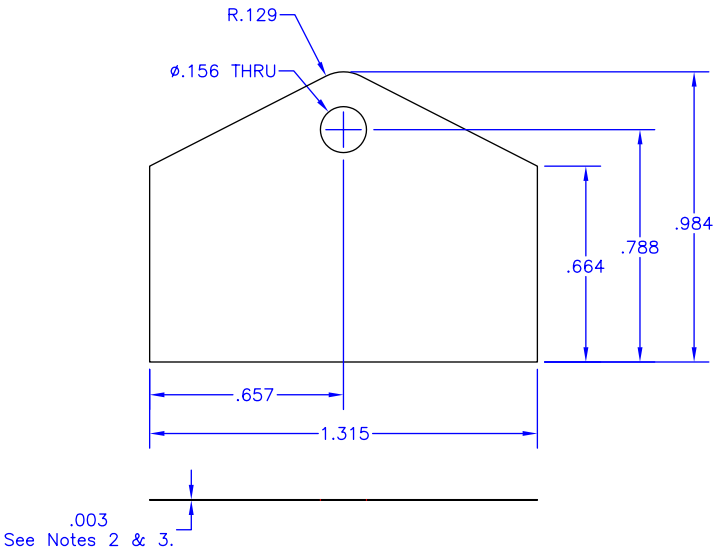


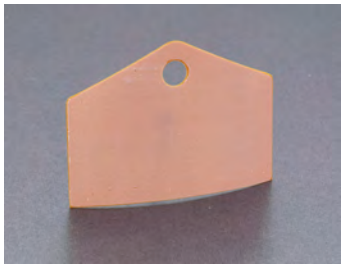


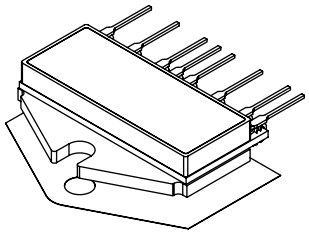
NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Film Material: .002 thick Kapton® MT
   Dielectric strength – 5200 VAC/mil
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .201 °C–in²/W (1.30 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with SIP package (Apex designators: DX, EU, EW & EX).
7. Power Devices part no. KA–136–073

G

SIP Thermal Washer TW13

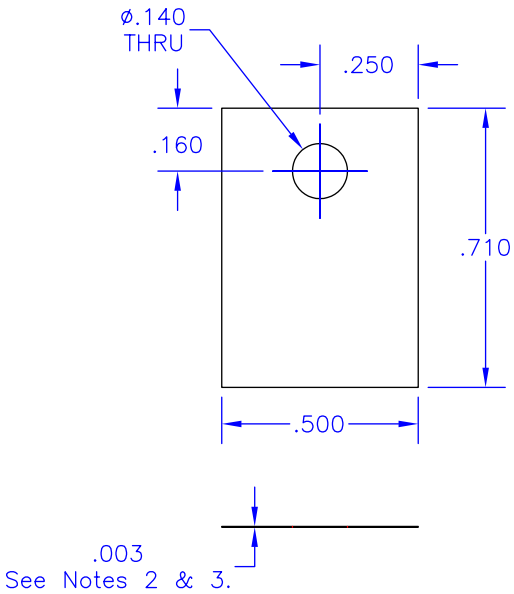


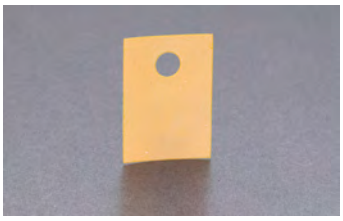


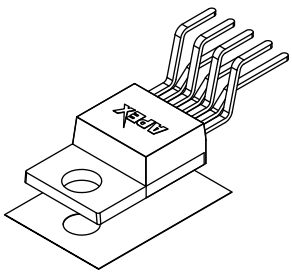


NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Film Material: .002 thick Kapton® MT
   Dielectric strength – 5200 VAC/mil
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .201 °C–in²/W (1.30 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with SIP packages (Apex designators: DQ & DR).
7. Power Devices part no. KA–132–098

TO-220 Thermal Washer TW14

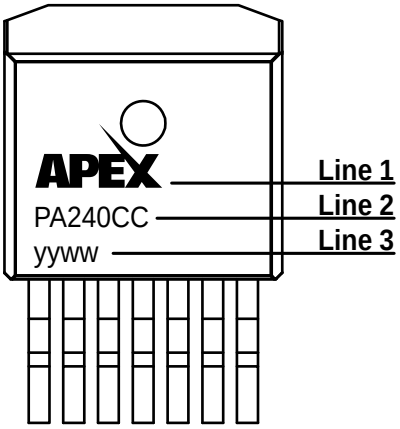


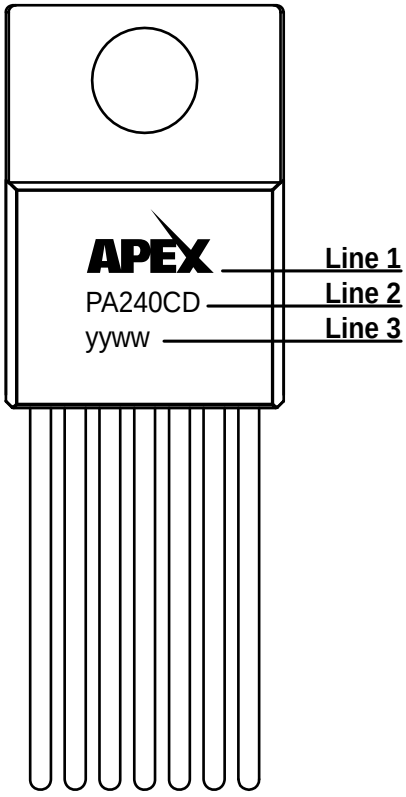




NOTES:
1. Unless otherwise noted, all dimensions are in inches.
2. Film Material: .002 thick Kapton® MT
   Dielectric strength – 5200 VAC/mil
3. Interface Material: .0005 thick phase–change thermal compound, both sides.
   Maximum shipping & storage temperature – 40°C
   Reflow temperature – 60°C
   Maximum recommended service temperature – 200°C
4. Thermal impedance: .201 °C–in²/W (1.30 °C–cm²/W) @ 20psi
5. Thermal washers shall be packaged in quantities of 10 with oversize separators between them.
6. Used with TO220 packages (Apex designators: CD & CX).
7. Power Devices part no. KA–070–050

CC PACKAGE (7DDPAK)
CD PACKAGE (7TO220)
CX PACKAGE (7TO220) STAGGERED LEADS





Line 1
Apex Logo

Line 2
Apex Part Number

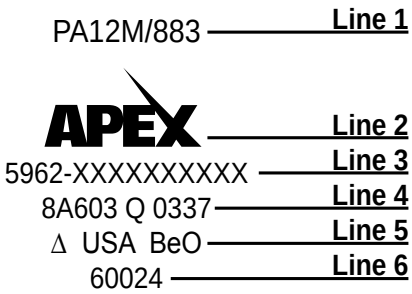
Line 3
All Parts: Date Code

0329

2003 Work Week 29

G

CE PACKAGE (TO-3),
DC, DD, CR, CU PACKAGE (MO-127 SERIES)
DE PACKAGE (10-PIN DIP SERIES)
EL PACKAGE (12-Pin DIP SERIES)



Line 1
SMD* Parts: Apex Part Number
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 2
All Parts: APEX Logo

Line 3
SMD Parts: DSCC SMD Part Number
Standard Parts: Blank
Custom Parts: Apex Part Number

Line 4
All Parts: Lot Code → 8A603

Compliance Indicator → Q
- Q = DSCC QML Compliant
- C = MIL-H-38534 Compliant
- None = Not Compliant

Date Code → 0337
- 2003
- Work Week 37

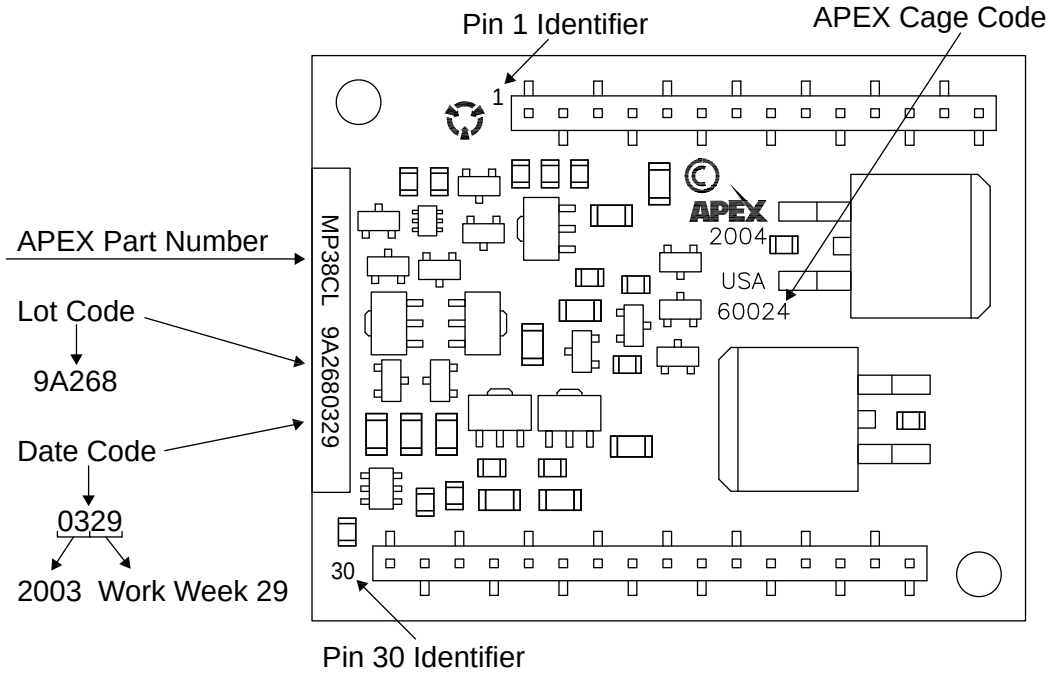
Line 5
All Parts: Δ USA → ESD & Pin 1 Identifier

Δ USA BeO
- ESD & Pin 1 Identifier
- BeO Identifier

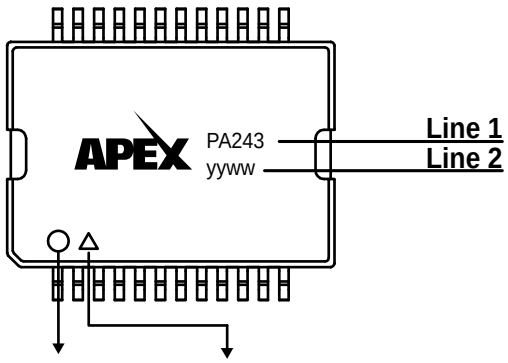
Line 6
All Parts: 60024 = APEX CAGE Code

* SMD = Standardized Military Drawing

CL PACKAGE



DF PACKAGE (24 Pin PSOP)

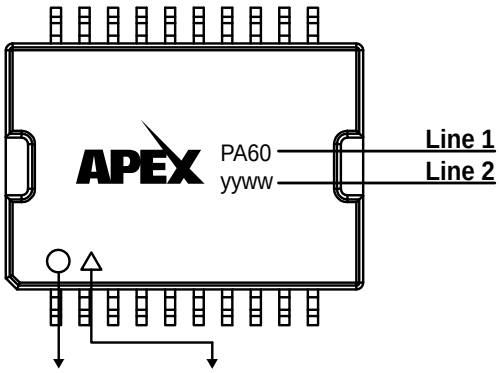


Line 1
Apex Part Number

Line 2
All Parts: Date Code

0309
2003 Work Week 9

DK PACKAGE (20 Pin PSOP)



Line 1
Apex Part Number

Line 2
All Parts: Date Code

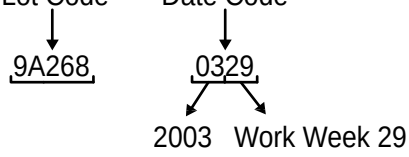
0309
2003 Work Week 9

G

DN, DP, DQ, DR, EC, ED, EE, EP, ET, FL, FP, FU PACKAGE (Hybrid SIP Series)

Line 1
Standard Parts: Apex Part Number
Custom Parts: Blank

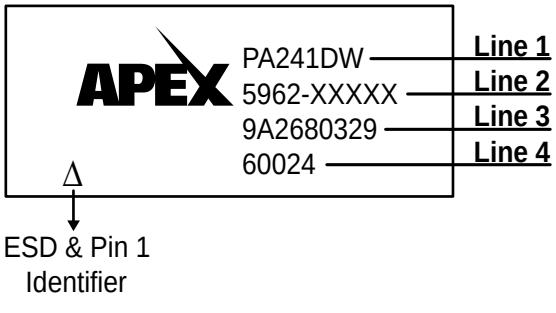
Line 2
All Parts: Lot Code Date Code



Line 3
Made in U.S.A., BeO Identifier

Line 4
All Parts: 60024 = APEX CAGE Code

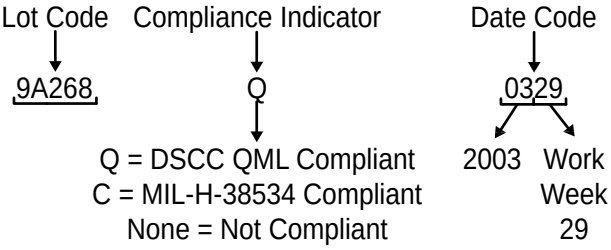
DW PACKAGE (Hermetic SIP)



Line 1
SMD* Parts: Apex Part Number
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 2
SMD Parts: DSCC SMD Part Number
Standard Parts: Blank
Custom Parts: Apex Part Number

Line 3
All Parts:



Line 4
All Parts: 60024 = APEX CAGE Code

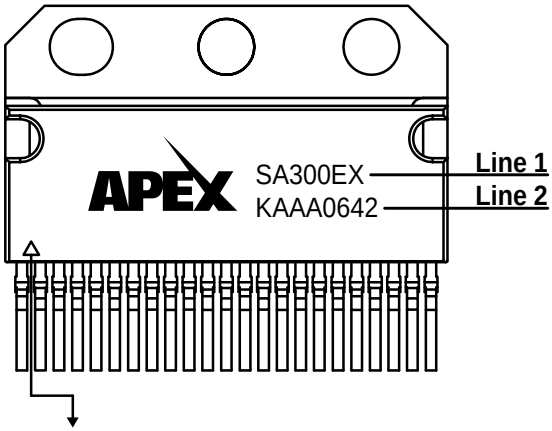
* SMD = Standardized Military Drawing

EU, EW PACKAGE (Monolithic SIP)

Line 1
Apex Part Number

Line 2
Lot Code

EX PACKAGE (23 PIN MOLDED SIP)



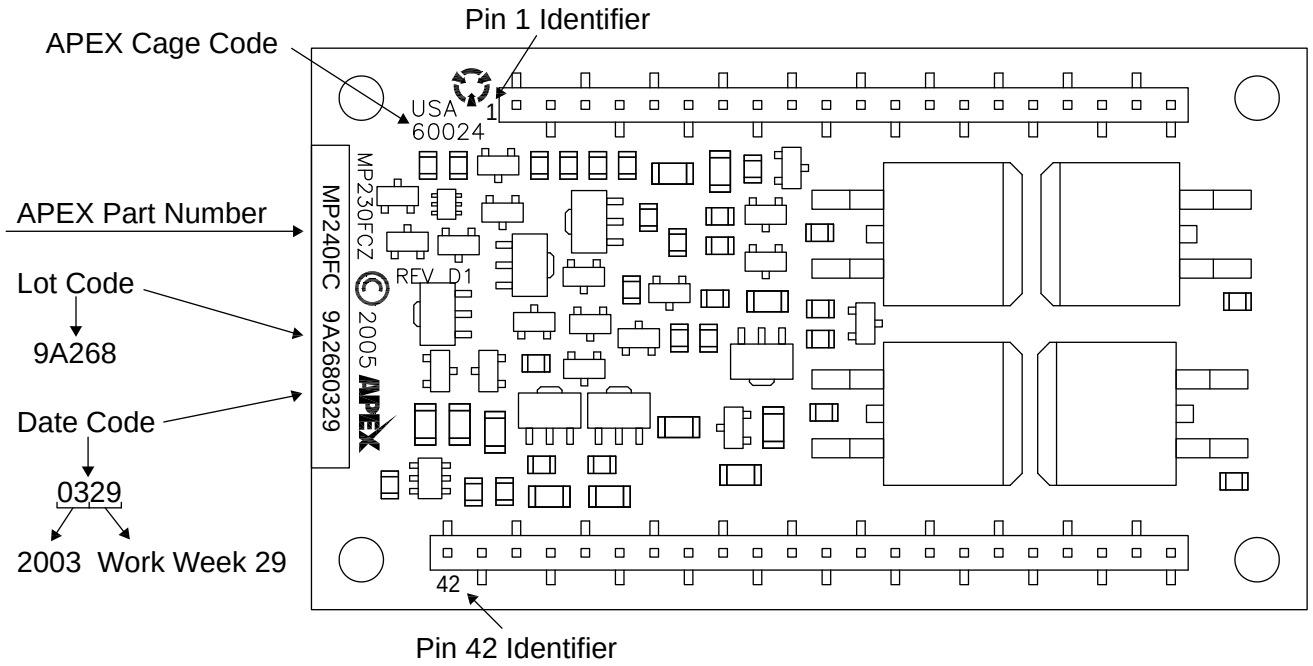
Line 1
Apex Part Number

Line 2
Lot Code Date Code

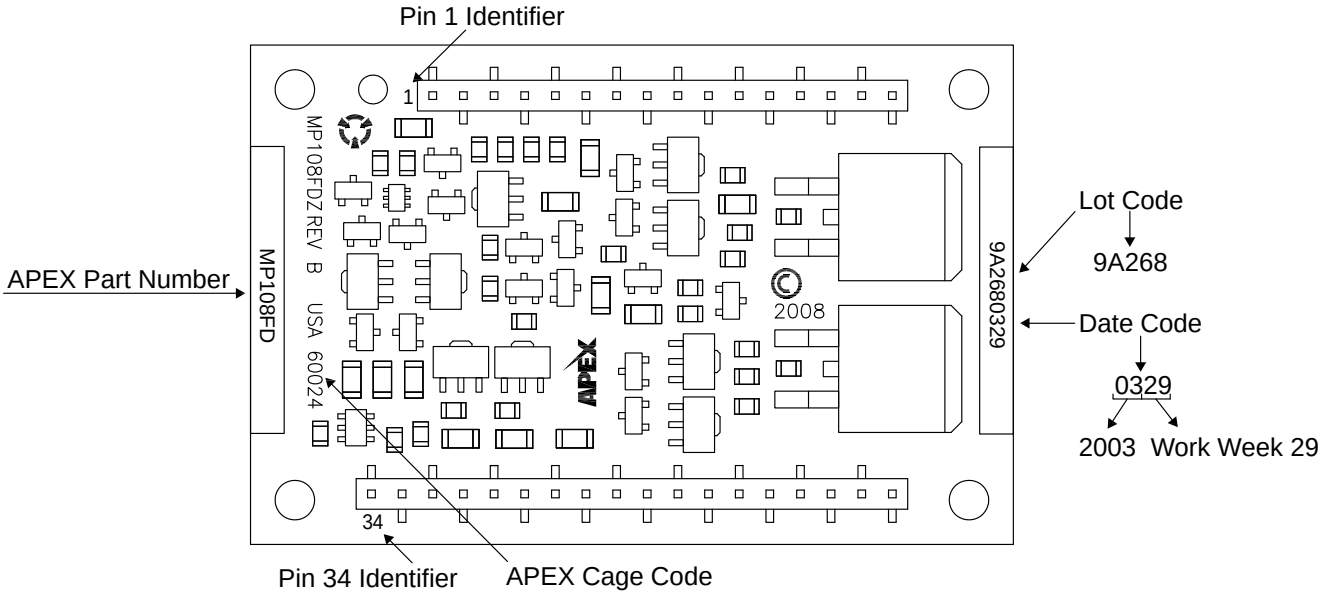
KAAA 0642

2006 Work Week 42

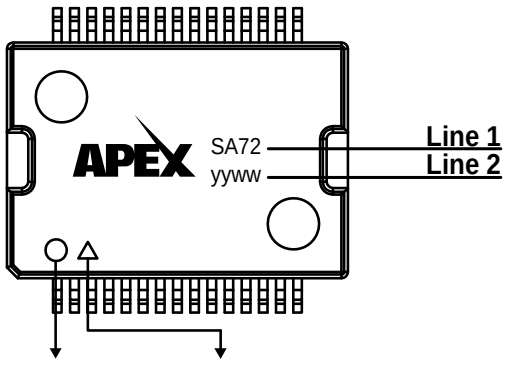
FC PACKAGE



FD PACKAGE

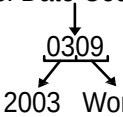


FN PACKAGE (30 pin PSOP)

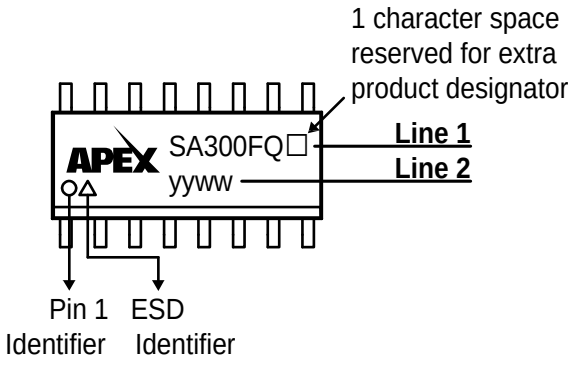


Line 1
Apex Part Number

Line 2
All Parts: Date Code

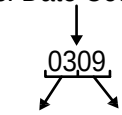


FQ PACKAGE (16 pin SOIC with HEATSLUG)

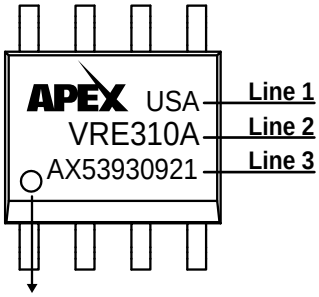


Line 1
Apex Part Number

Line 2
All Parts: Date Code



FX PACKAGE (8-pin SOIC)



Pin 1 Identifier

Line 1
Made in U.S.A.

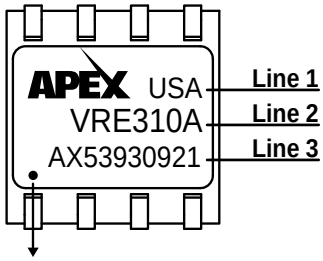
Line 2
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 3
All Parts: Lot Code Date Code

AX5393 0921

2009 Work Week 21

GD, GF PACKAGE (8-pin DIP SMT)
KD PACKAGE (8-pin DIP)



Pin 1 Identifier

Line 1
Made in U.S.A.

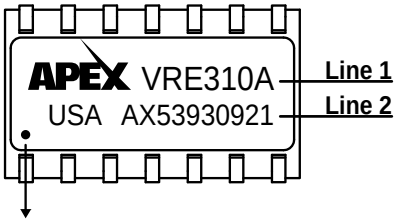
Line 2
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 3
All Parts: Lot Code Date Code

AX5393 0921

2009 Work Week 21

GE PACKAGE (14-pin DIP SMT)
KE PACKAGE (14-pin DIP)



Pin 1 Identifier

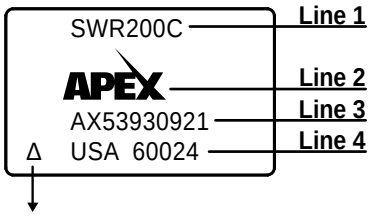
Line 1
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 2
Made in U.S.A. Lot Code Date Code

AX5393 0921

2009 Work Week 21

HC PACKAGE (14-pin HERMETIC DIP)



ESD & Pin 1
Identifier

Line 1
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 2
All Parts: Apex Logo

Line 3
All Parts: Lot Code Date Code

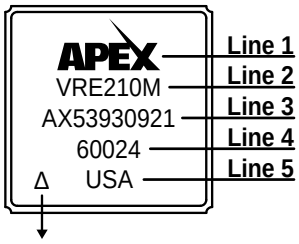
AX5393 0921

2009 Work Week 21

Line 4
Made in U.S.A., 60024 = APEX CAGE Code

G

HD PACKAGE (20-pin CERAMIC LCC)



Line 1
All Parts: Apex Logo

Line 2
Standard Parts: Apex Part Number
Custom Parts: Blank

Line 3
All Parts: Lot Code Date Code

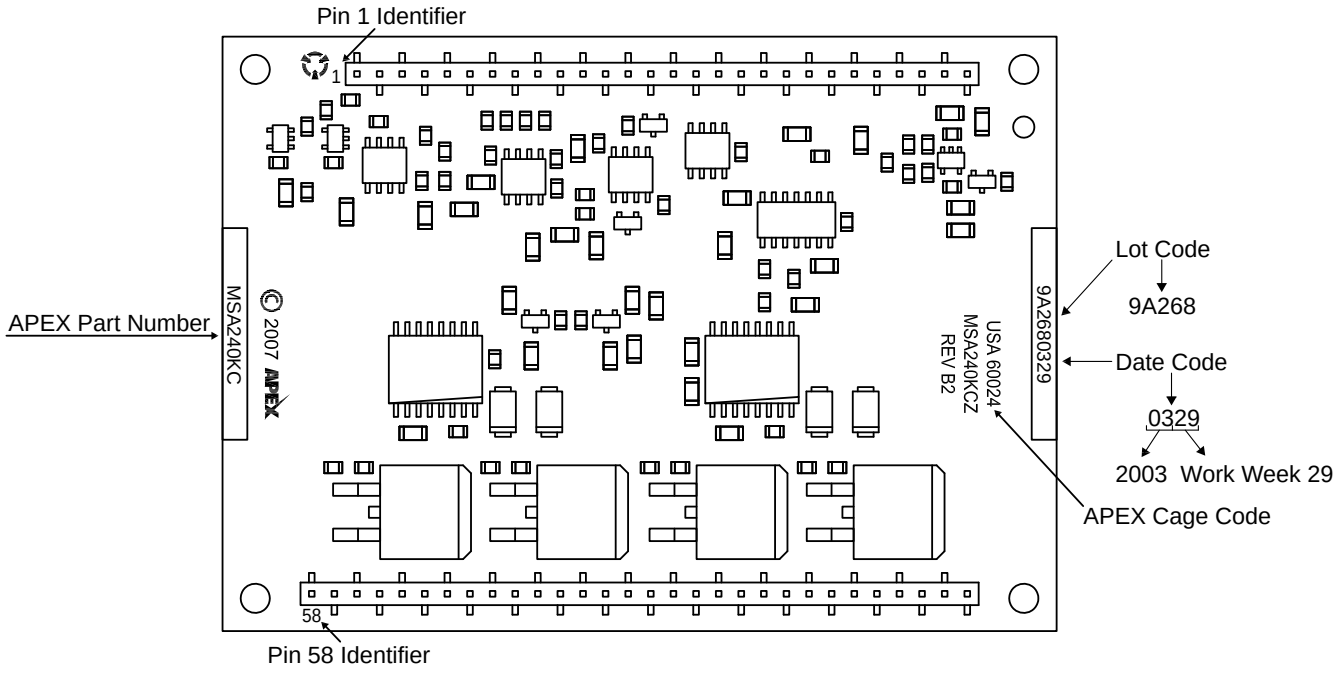
AX5393 0921

2009 Work Week 21

Line 4
All Parts: 60024 = APEX CAGE Code

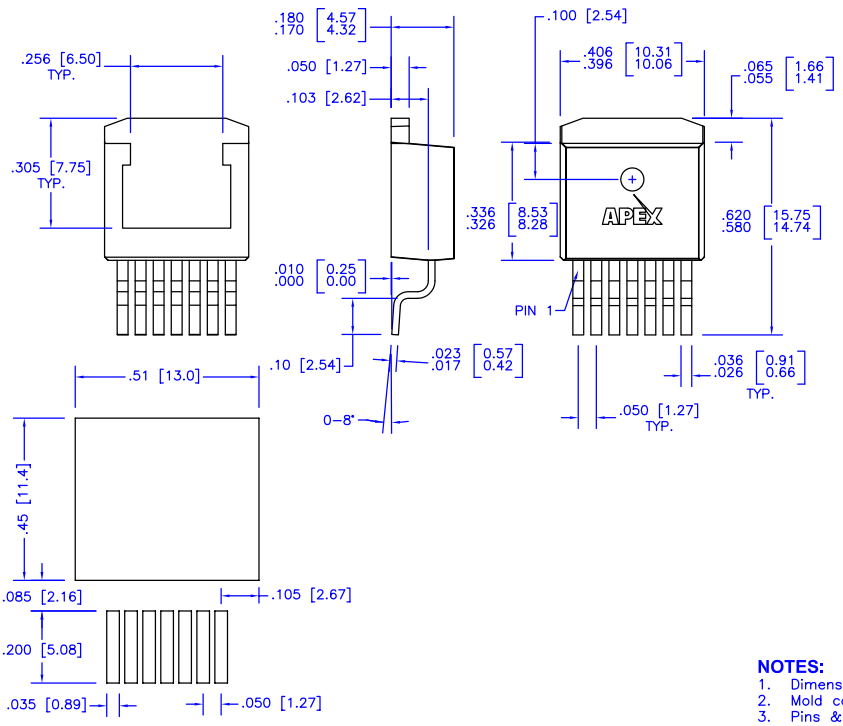
Line 5
Made in U.S.A.

KC PACKAGE

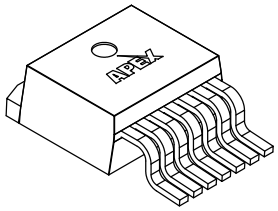


Package Outlines For Apex Precision Power

7-Pin TO-220 SMT CC

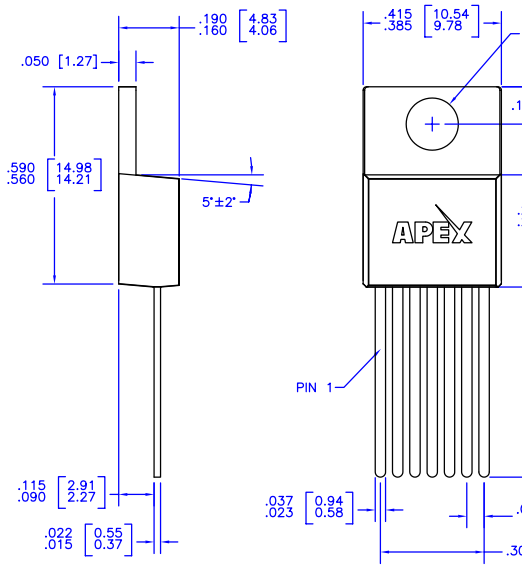


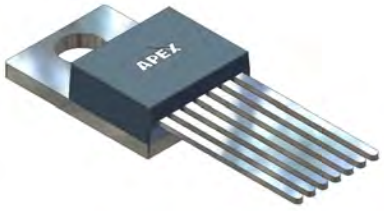
Surface Mount Layout

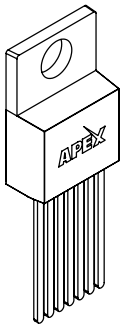


NOTES:
1. Dimensions are in inches & [mm].
2. Mold compound: MPC8000CH epoxy
3. Pins & Heat Slug: HCL–12S Cu alloy, 100% MATTE Sn FINISH
4. Package weight: .051 oz. [1.46 g]
5. Suggested surface mount layout for reference only.

7-Pin TO-220 CD



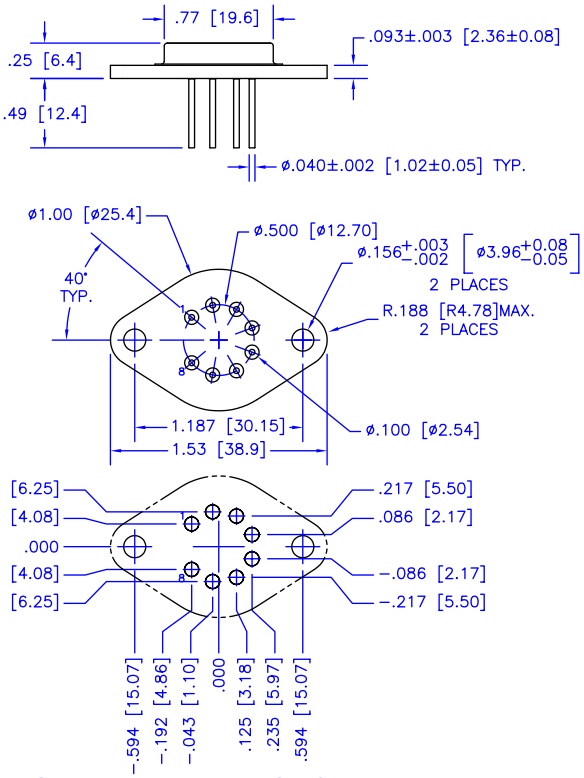




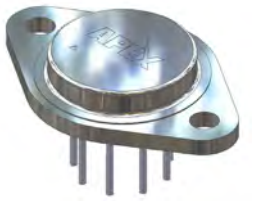
NOTES:
1. Dimensions are in inches & [mm].
2. Mold compound: MPC8000CH epoxy
3. Pins & Heat Slug: HCL–12S Cu alloy, 100% MATTE Sn FINISH.
4. Package weight: .072 oz. [2.05 g]

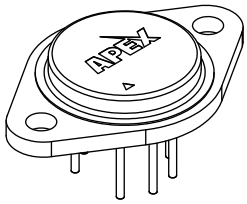
G

8-Pin TO-3 CE



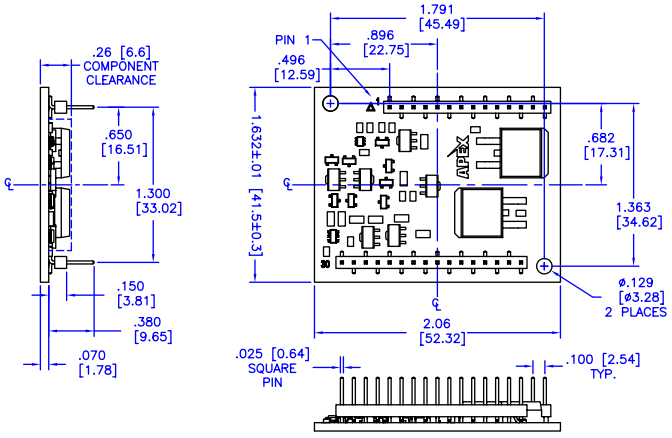
Ordinate dimensions for CAD layout

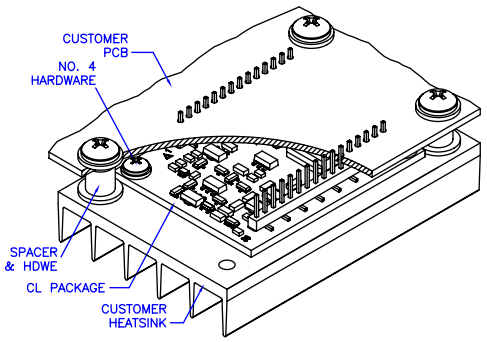




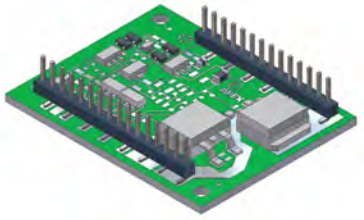
NOTES:
1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel–plated Alloy 52.
6. Header material: Nickel–plated cold–rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

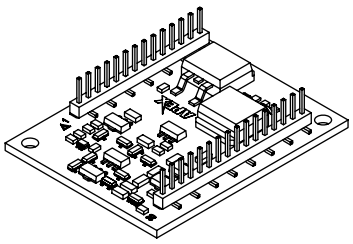
30-Pin Open Frame CL





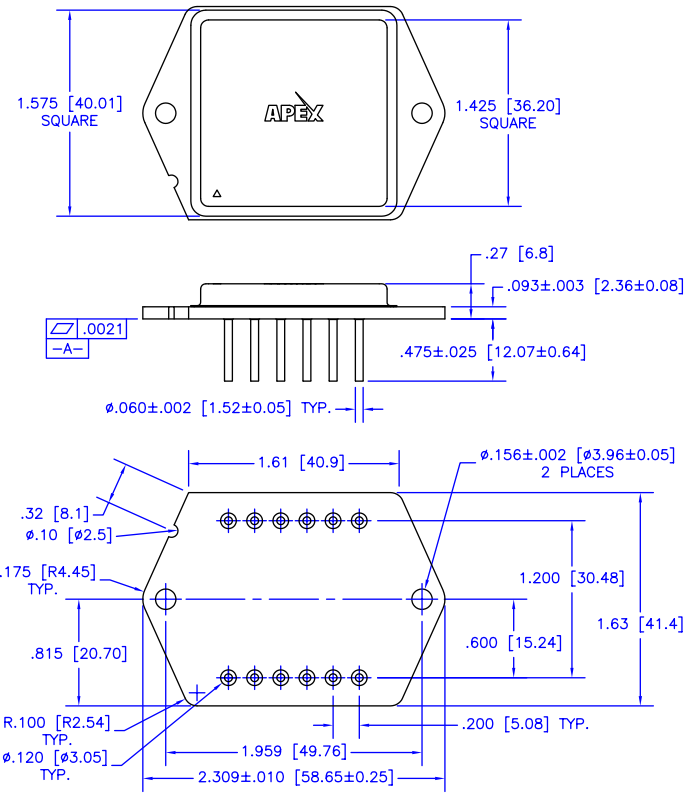
SUGGESTED MOUNTING METHOD

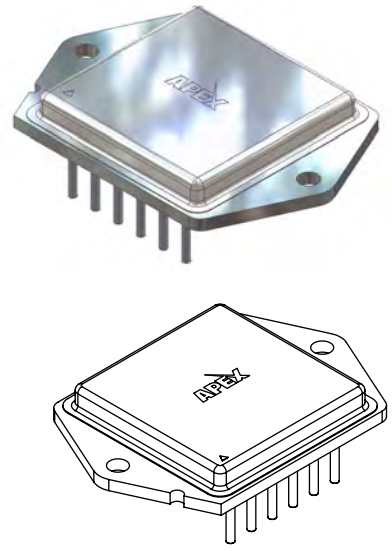




NOTES:
1. Dimensions are inches; alternate units are [mm].
2. Recommended PCB hole diameter for pins: .050"
3. 2 oz. copper over 600V dielectric over aluminum substrate
4. Tin–nickel plated phosphor bronze pins
5. Package weight: 0.56 oz. [15.9 g]
6. Mount with #4 or equivalent screws.
7. It is not recommended that mounting of the package rely on the pins for mechanical support. The mounting method shown does not represent a specific design solution or the only way to mount the package.
8. Care must be exercised in designing the mating board, to avoid interference among board components.

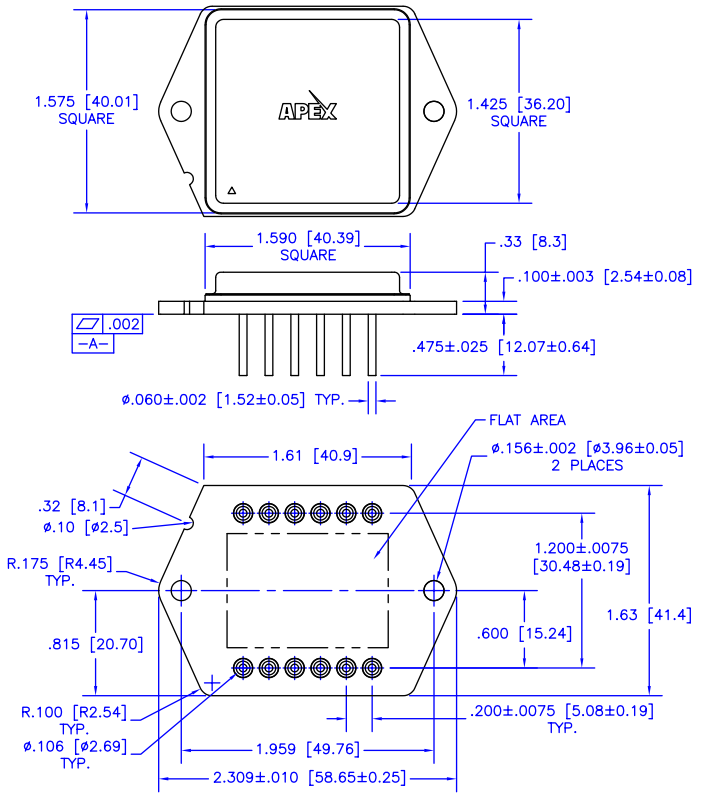
MO-127 60 mil Pin CR

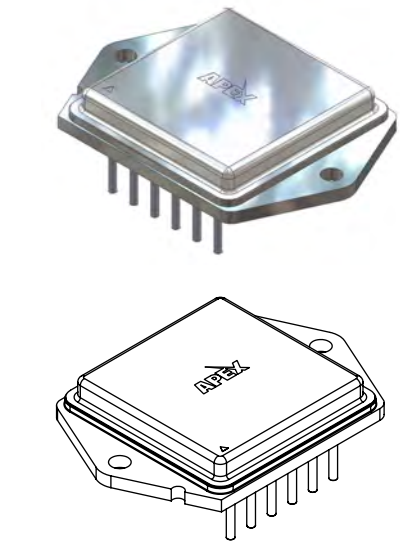




NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid and notch in header denote pin 1.
3. Header material: Nickel–plated CRS
4. Lid material: Solid nickel
5. Pin material: Solderable nickel–plated Alloy 52
6. Welded hermetic package seal
7. Isolation: 1000 VDC any pin to case
8. Package weight: 1.87 oz [53 g]

MO-127 60 mil Pin Copper CU

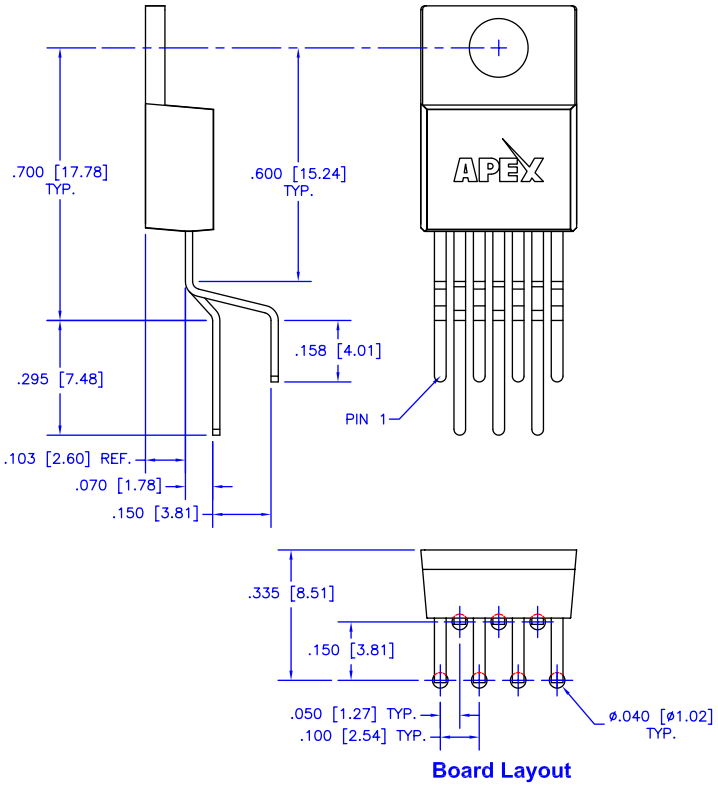




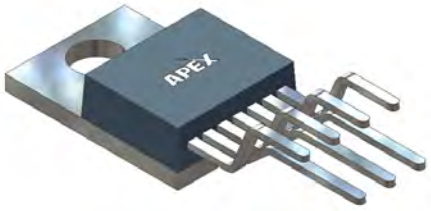
NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid and notch in header denote pin 1.
3. Header material: Copper, with brazed–on CRS weld ring and overall nickel plating
4. Header flatness tolerance applies over rectangular area shown in bottom view.
5. Lid material: Solid nickel
6. Pin material: Solderable nickel–plated Alloy 52
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case
9. Package weight: 2.05 oz [58 g]

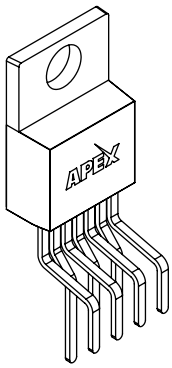
G

7-Pin TO-220 Staggered Leads CX



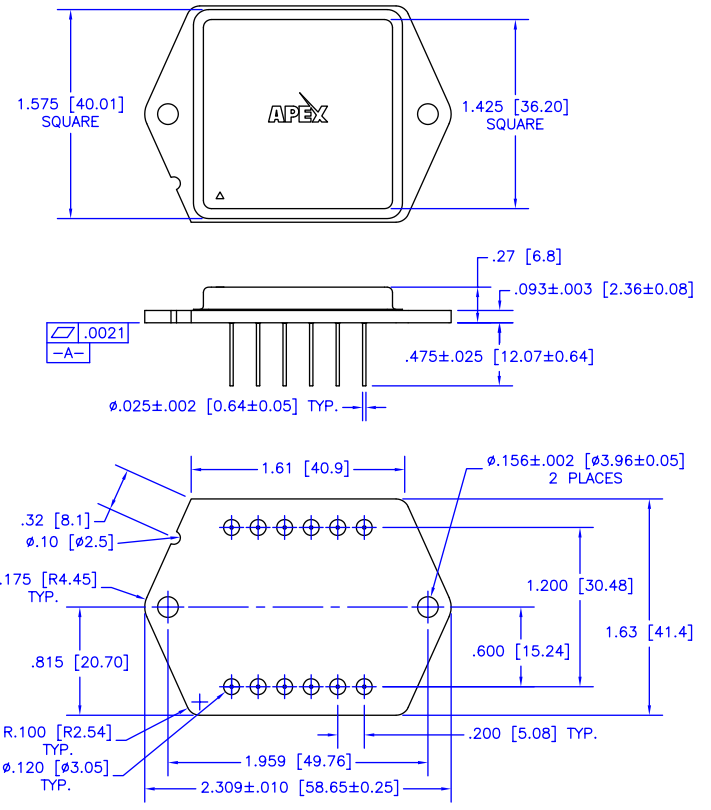
Board Layout

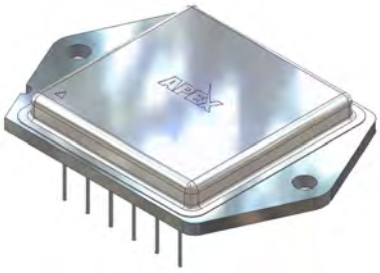


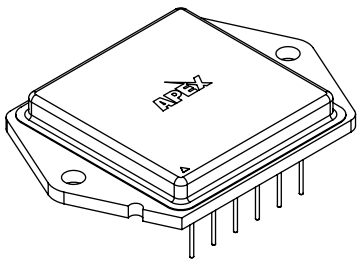


NOTES:
1. Dimensions are inches & [mm].
2. For other information on this package with unformed leads, see package CD.
3. Suggested board layout for reference only.

MO-127 High Voltage DC

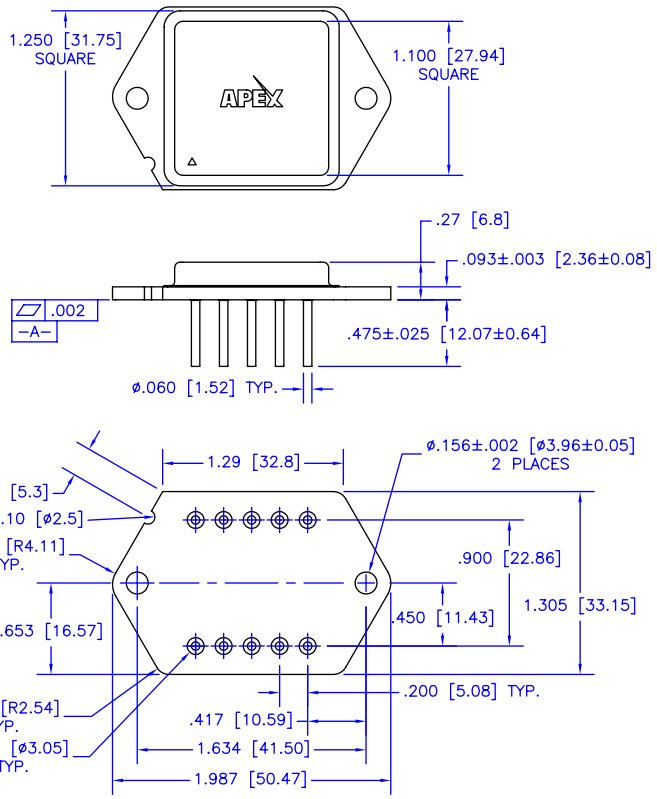


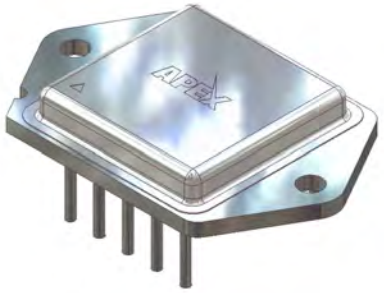


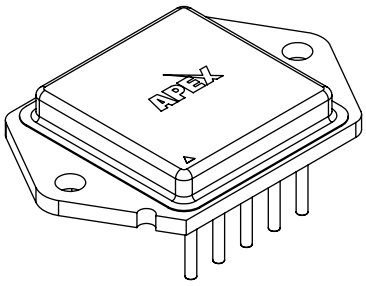


NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid and notch in header denote pin 1.
3. Header material: Nickel–plated CRS
4. Lid material: Solid nickel
5. Pin material: Solderable nickel–plated Alloy 52
6. Welded hermetic package seal
7. Isolation: 1200 VDC any pin to case
8. Package weight: 1.87 oz [53 g]

10-Pin Power DIP 60 mil Pin DE

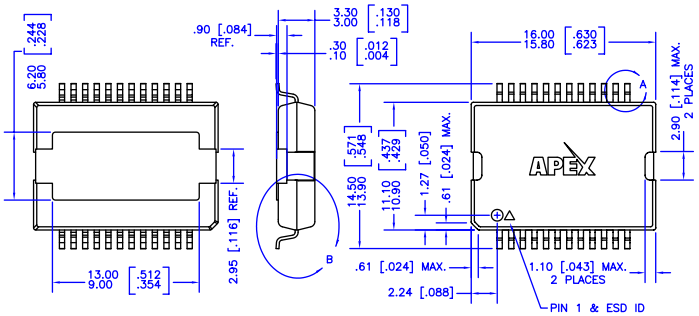


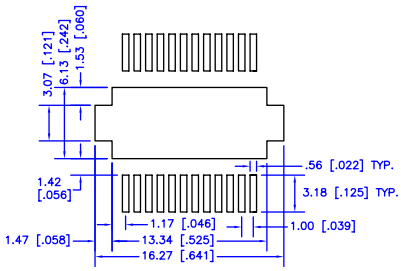




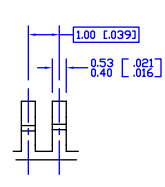
NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid and notch in header denote pin 1.
3. Header and lid material: Nickel–plated CRS
4. Pin material: Solderable nickel–plated Alloy 52
5. Welded hermetic package seal
6. Isolation: 1000 VDC any pin to case
7. Package weight: 1.27 oz [36 g]

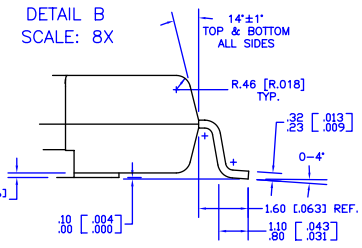
MO-166 24-Pin PSOP DF

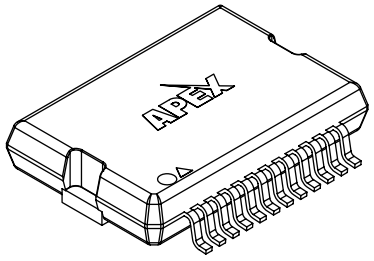




Surface Mount Layout

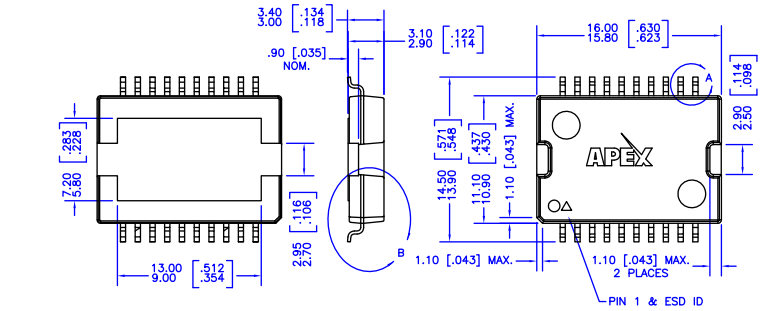


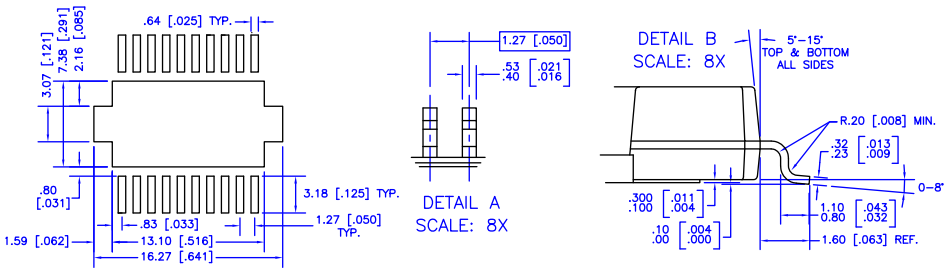


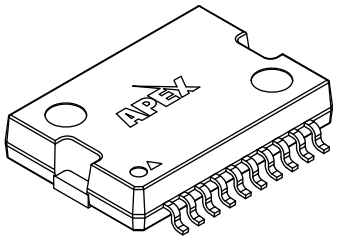


NOTES:
1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Pins & Heat Slug: CDA 194 copper with bismuth solder finish
5. Mold compound: MP–8000AN epoxy
6. Package weight: .086 oz. [2.44 g]
7. Suggested surface mount layout for reference only.

MO-166 20-Pin PSOP DK

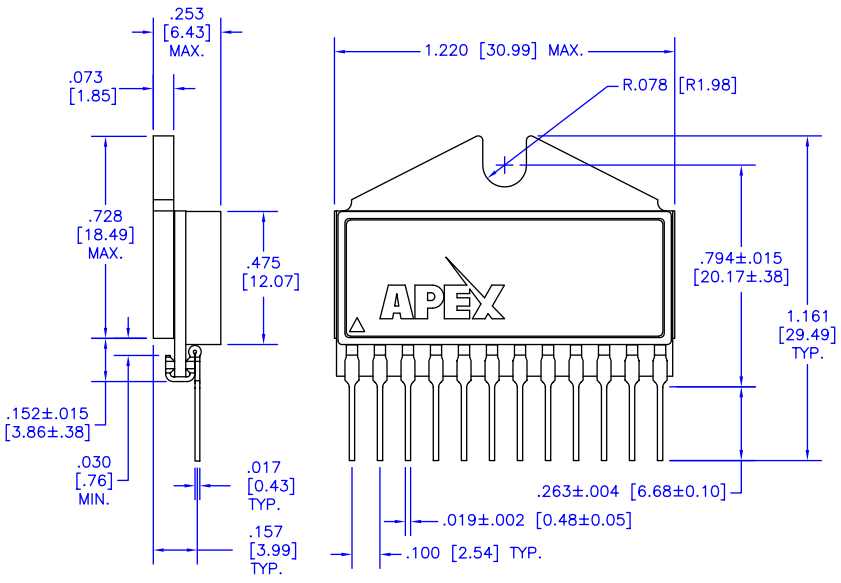


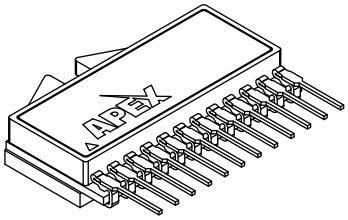




NOTES:
1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Heat Slug: C10200 copper with Ni–Pd–Au plating
5. Lead frame: C19400 copper with Ni–Pd–Au plating.
6. Mold compound: MP–8000AN or EME6600HR epoxy
7. Package weight: .086 oz. [2.44 g]
8. Suggested surface mount layout for reference only.

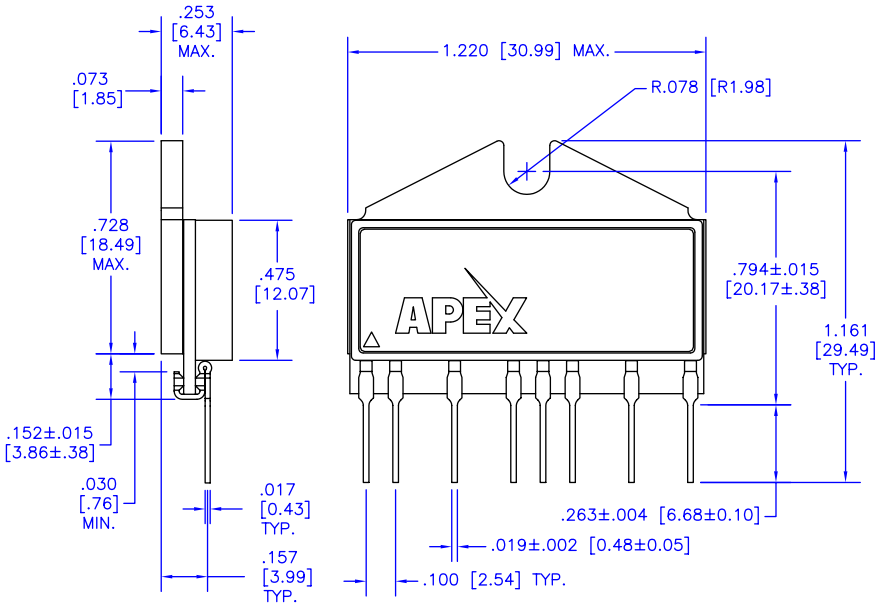
12-Pin Power SIP DP

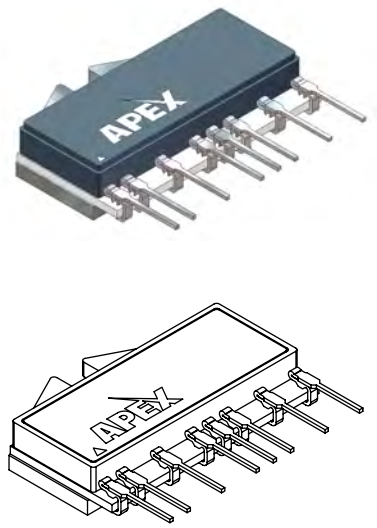




NOTES:
1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: CDA 510 phosphor bronze with tin–lead solder finish
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .367 oz. [11.41 g]

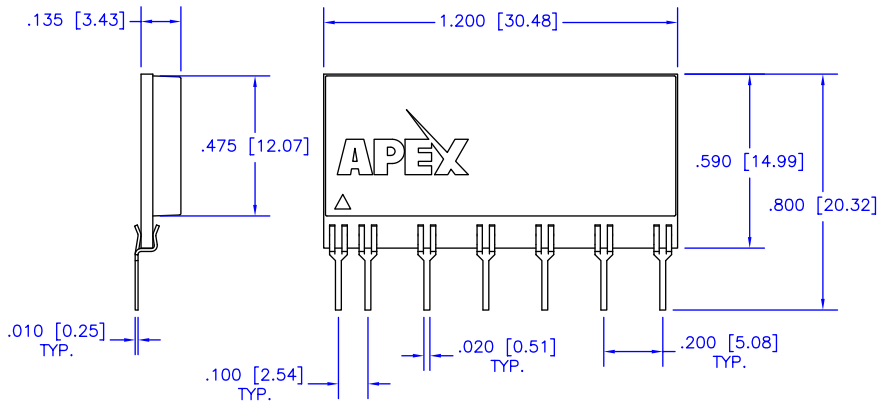
9-Pin Power SIP DQ

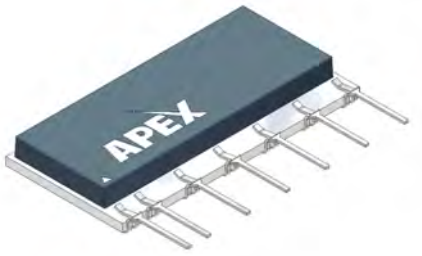




NOTES:
1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: CDA 510 phosphor bronze with tin–lead solder finish
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .39 oz [11 g]

7-Pin SIP DR

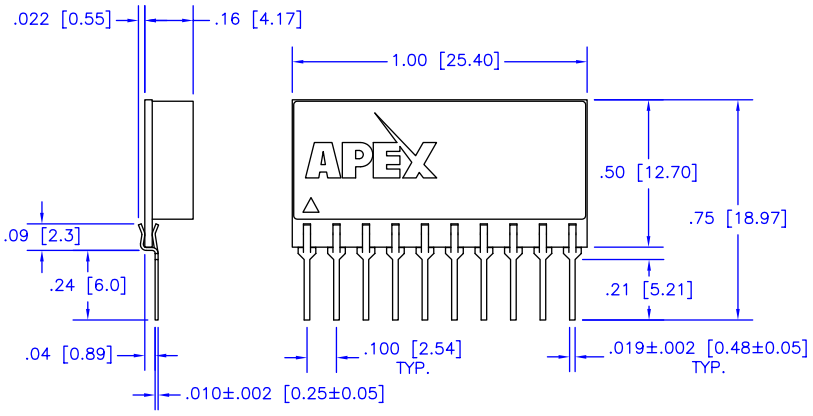


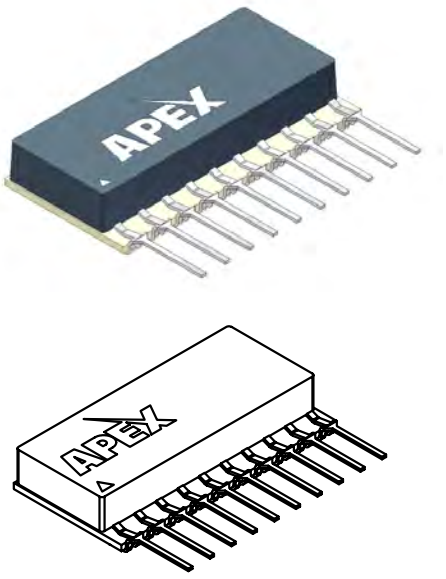


NOTES:
1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Standard pin material: CDA 510 phosphor bronze
4. Package Material: Alumina substrate with plastic lidl.
5. Package weight: .11 oz [3.0 g]

G

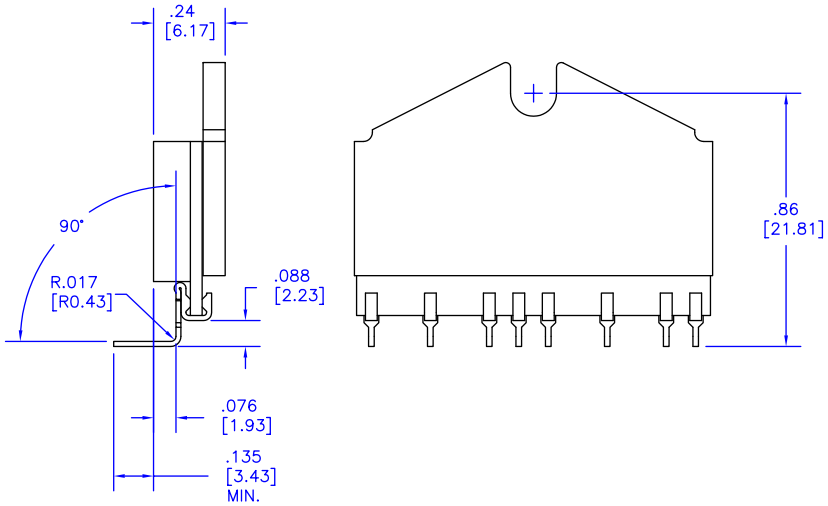
10-Pin Ceramic SIP DW

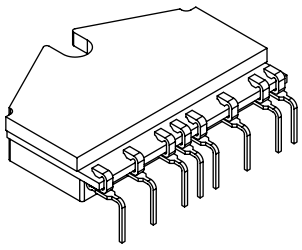




NOTES:
1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Standard pin material: CDA 510 phosphor bronze
4. Package Material: Alumina with hermetic glass seal.
5. Package weight: .1 oz [2.8 g]

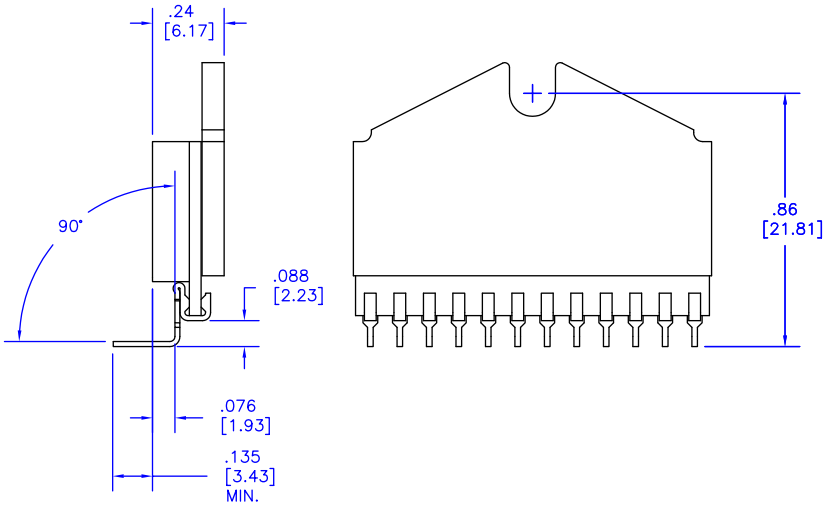
8-Pin PSIP 90° Leads EC

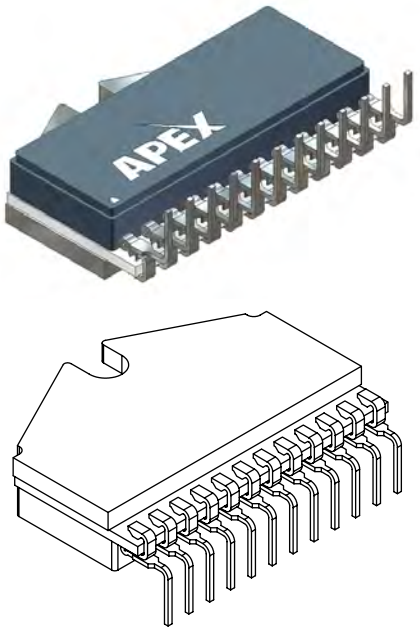




NOTES:
1. Dimensions are inches & [mm].
2. For other information on this package with unformed leads, see package DQ.

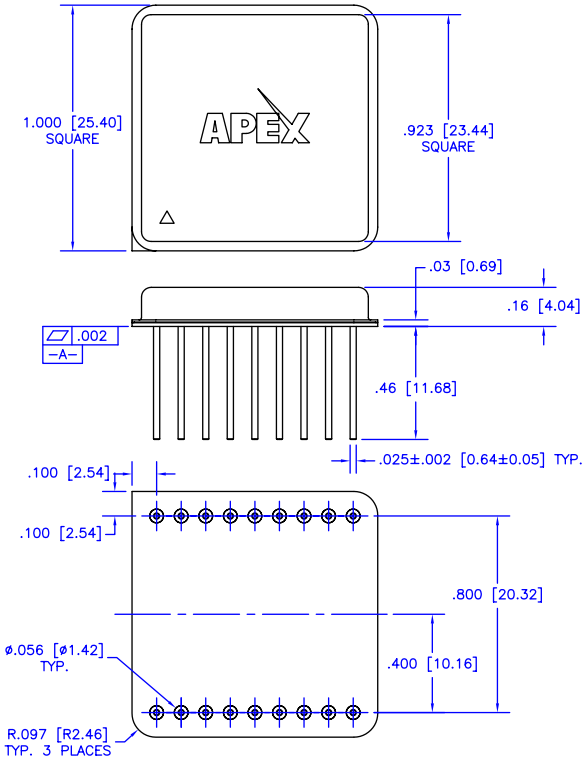
12-Pin PSIP 90° Leads EE

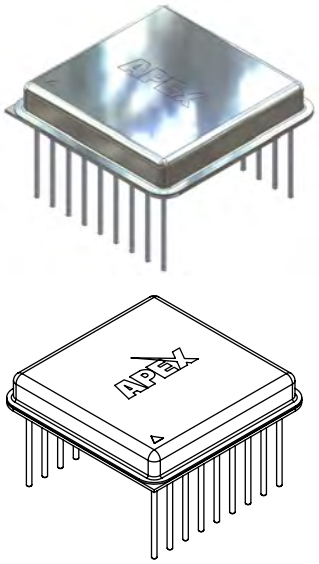




NOTES:
1. Dimensions are inches & [mm].
2. For other information on this package with unformed leads, see package DP.

18-Pin DIP 25 mil Pins EL

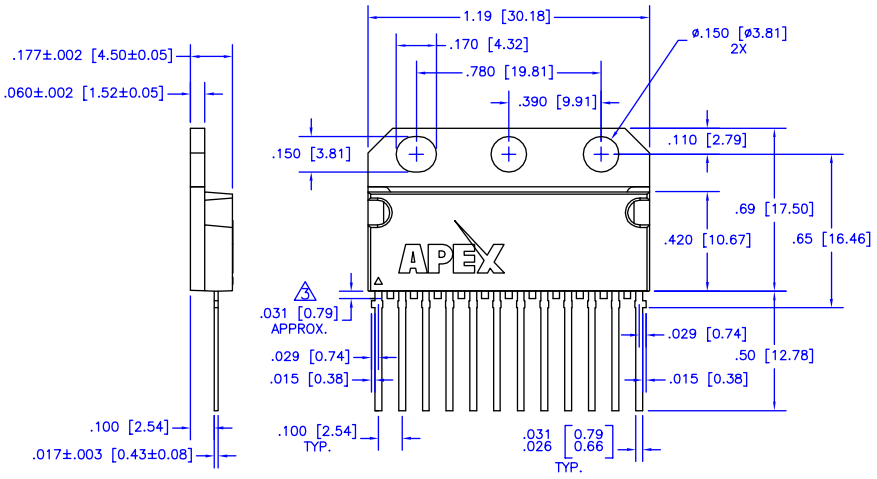


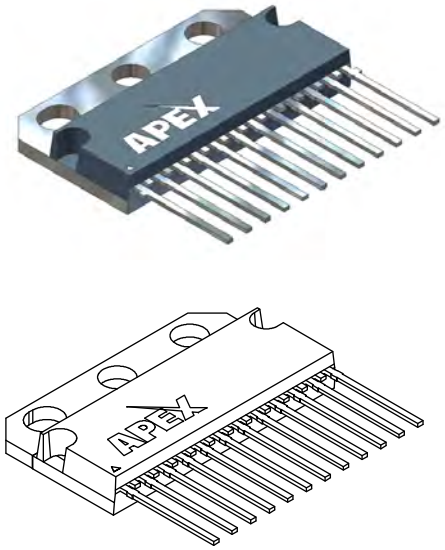


NOTES:
1. Dimensions are in inches & [mm].
2. Triangle on lid and square corner denote pin 1.
3. Header material: Nickel-plated CRS
4. Lid material: Nickel-plated CRS
5. Pin material: Solderable nickel-plated Alloy 52
6. Welded hermetic package seal
7. Isolation: 750 VDC any pin to case
8. Package weight: 0.37 oz [10.4 g]

G

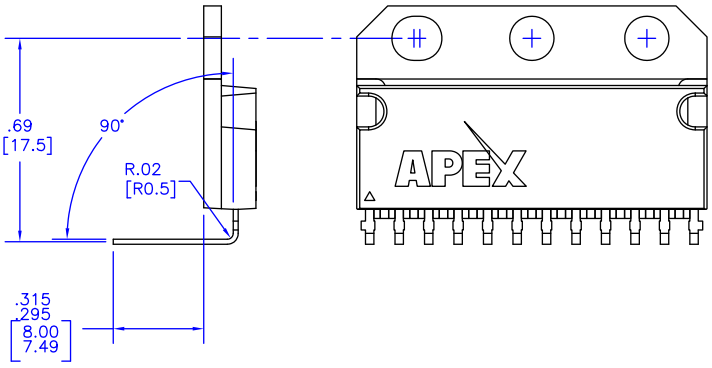
12-Pin Plastic SIP EU

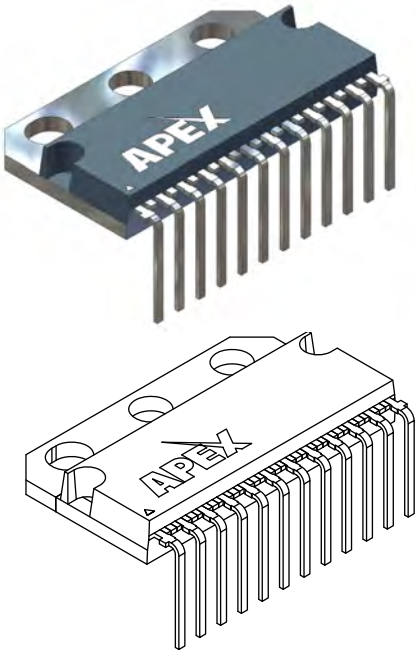




NOTES:
1. Dimensions are inches & [mm].
2. Triangle denotes pin 1.
3. Assemble with care to avoid solder bridging across stub pins.
4. Plastic may be present between leads and stub pins.
5. Pins & finish: Nickel/Palladium plated CDA19400 copper.
6. Mold compound: Sumitomo EME6300HX
7. Package weight: 0.29 oz [8.3 g]

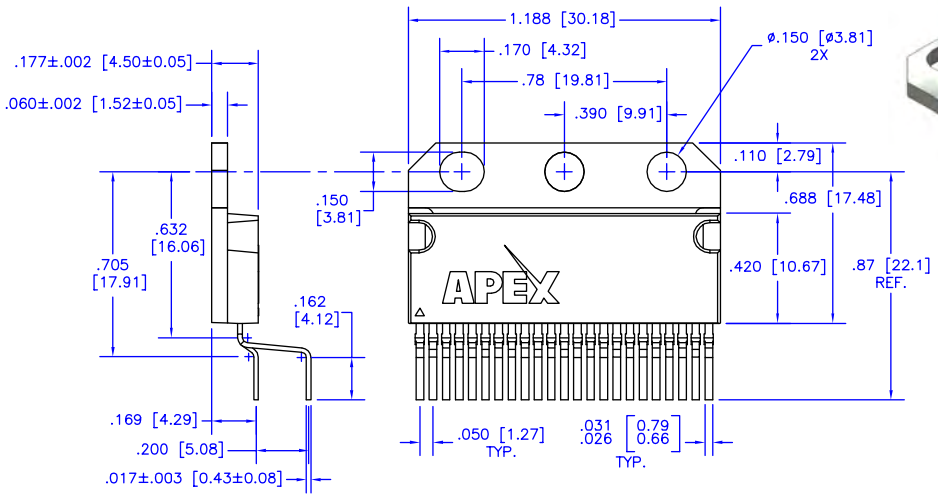
12-Pin Plastic SIP 90° Leads EW

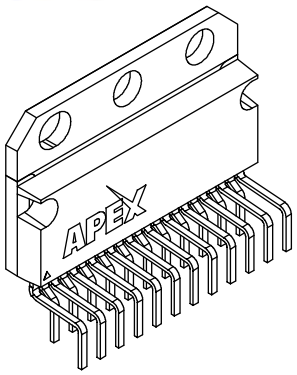




NOTES:
1. Dimensions are inches & [mm].
2. For other information on this package with unformed leads, see package EU.

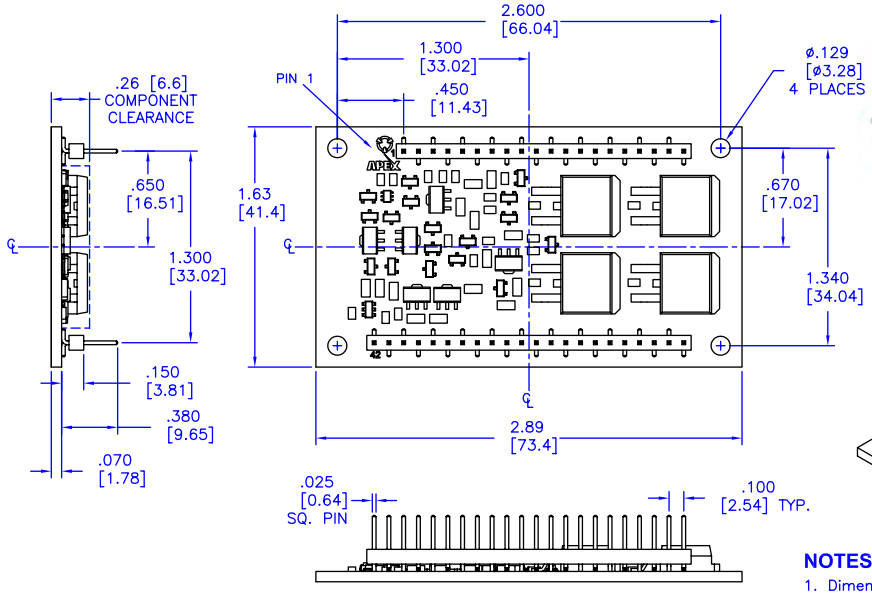
23-Pin Plastic SIP Staggered Leads EX

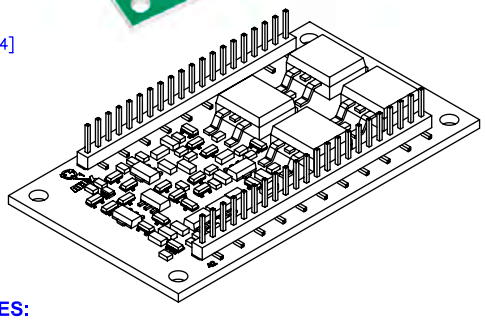




NOTES:
1. Dimensions are inches & [mm].
2. Triangle denotes pin 1.
3. Pins & finish: Nickel/Palladium plated CDA19400 copper.
4. Mold compound: Sumitomo EME6300HX
5. Package weight: 0.29 oz [8.3 g]

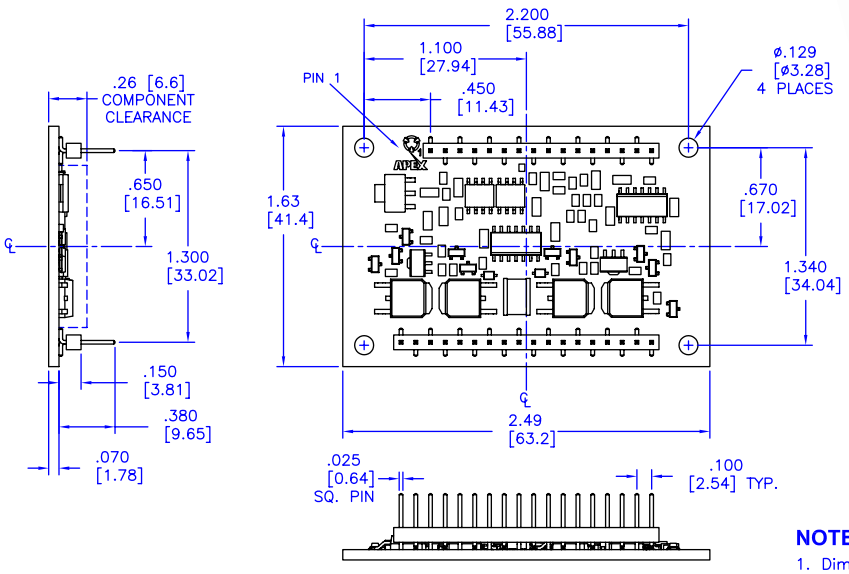
42-Pin Open Frame FC

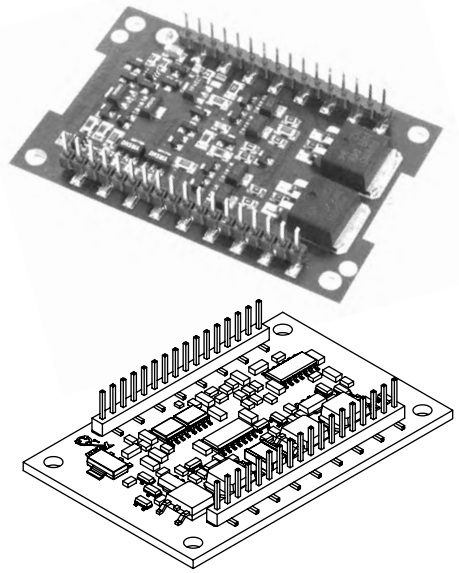




NOTES:
1. Dimensions are inches; alternate units are [mm].
2. Recommended PCB hole diameter for pins: .050 [1.27].
3. 2oz. copper over 600V dielectric over aluminum substrate.
4. Tin over nickel plated phosphor bronze pins.
5. Package weight:
6. Mount with #4 or equivalent screws.
7. It is not recommended that mounting of the package rely on the pins for mechanical support.

34-Pin Open Frame FD

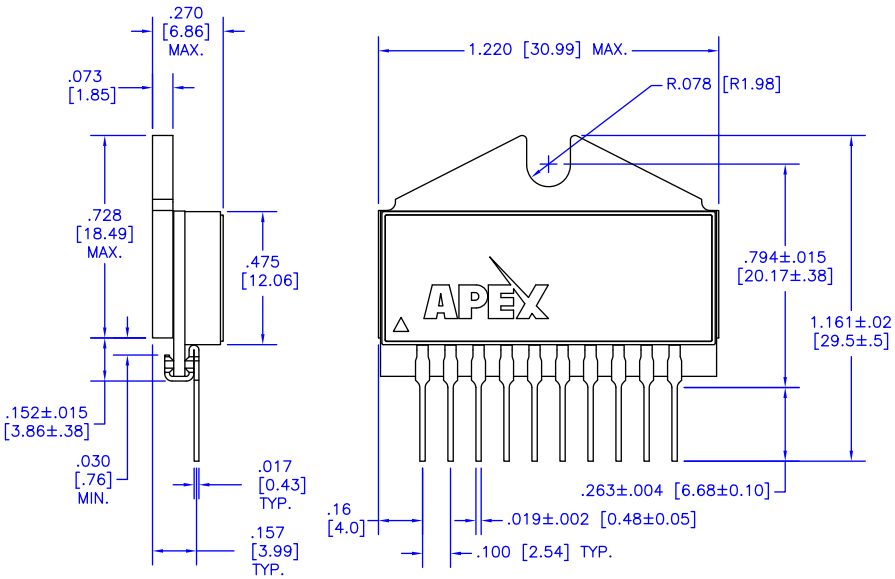


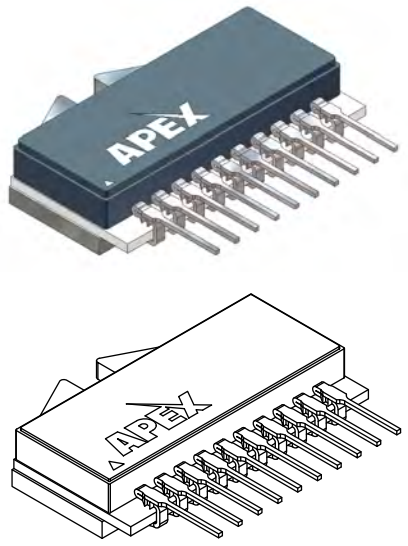


NOTES:

1. Dimensions are inches; alternate units are [mm].
2. Recommended PCB hole diameter for pins: .050 [1.27].
3. 2oz. copper over 600V dielectric over aluminum substrate.
4. Tin over nickel plated phosphor bronze pins.
5. Package weight: 18g or .63oz.
6. Mount with #4 or equivalent screws.
7. It is not recommended that mounting of the package rely on the pins for mechanical support.

10-Pin Power SIP FL

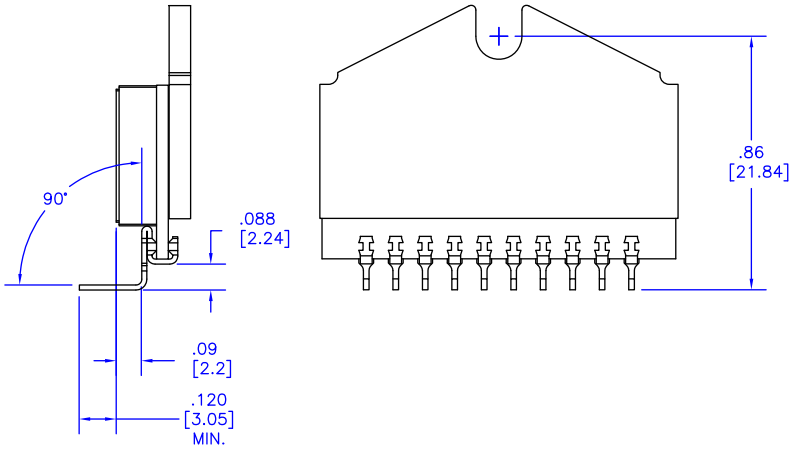


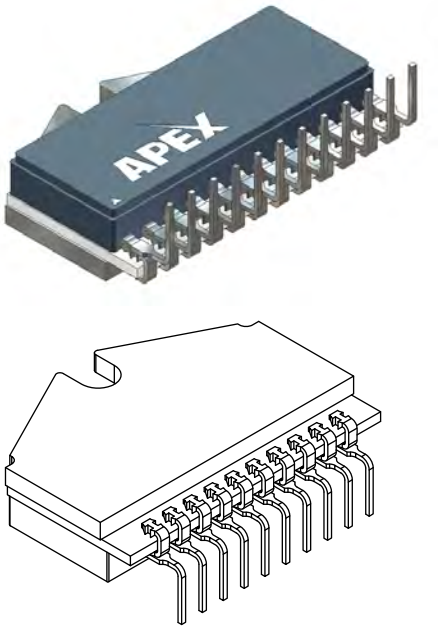


NOTES:

1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: CDA 510 phosphor bronze with tin–lead solder finish
4. Package: Vectra liquid crystal polymer, black
5. Epoxy–sealed & ultrasonically welded non–hermetic package.
6. Package weight: .367 oz. [11.41 g]

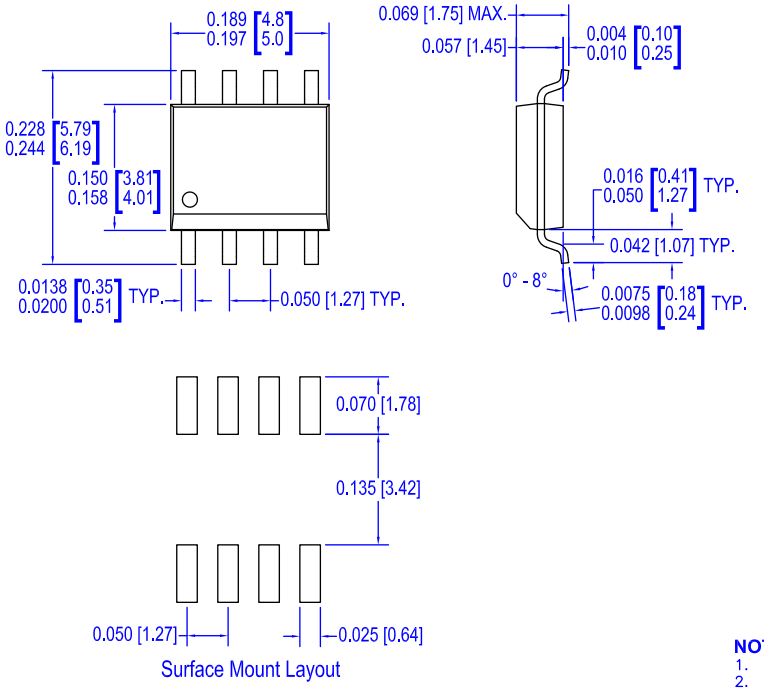
10-Pin Power SIP 90° Leads FU

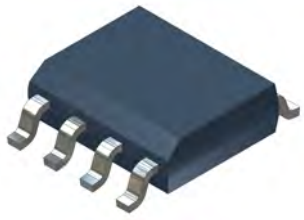


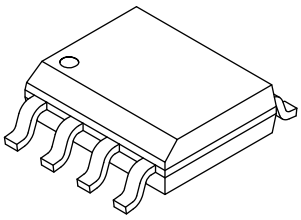


NOTES:
1. Dimensions are inches & [mm].
2. For other dimensions and information on this package with unformed leads, see package FL.

MS-012 8-Lead SOIC FX

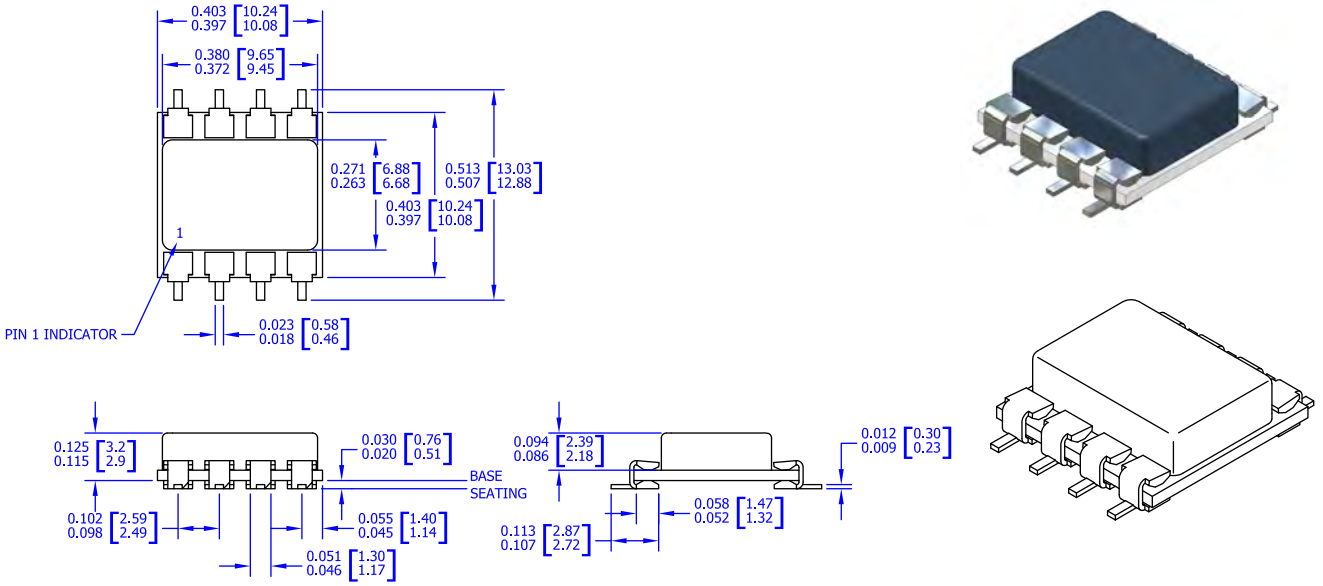






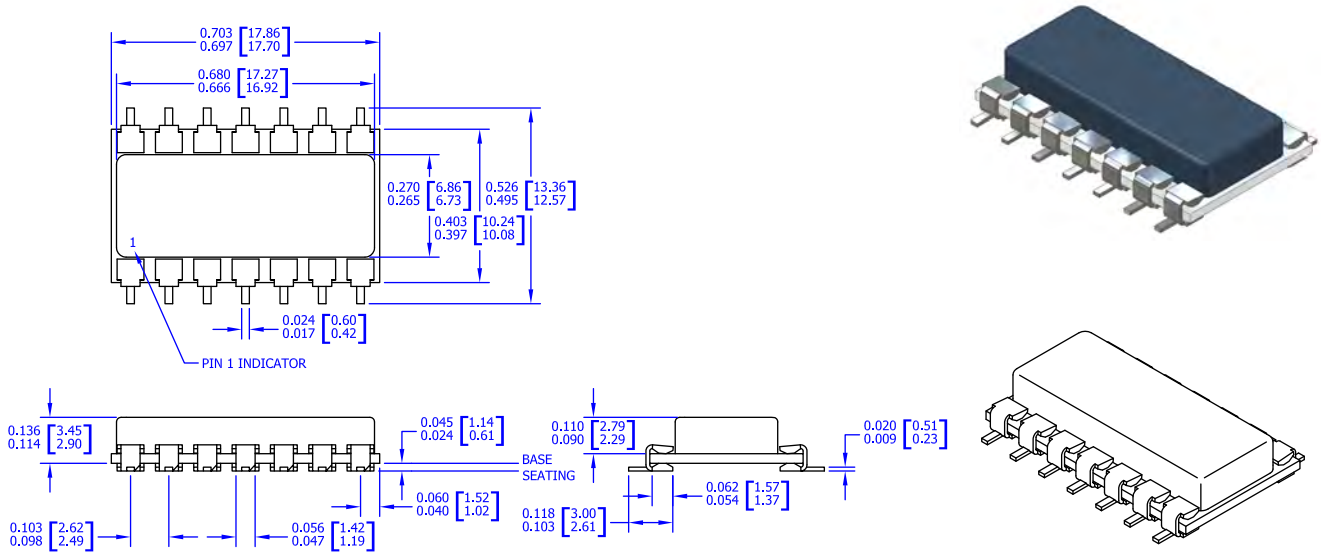
NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Dimple on lid denotes pin 1.
4. Dimensions do not include end flash, mold flash, material protrusion.
5. Package weight: 0.003 oz. [0.075 g].
6. Suggested surface mount layout for reference only.

8-Pin DIP SMT GD



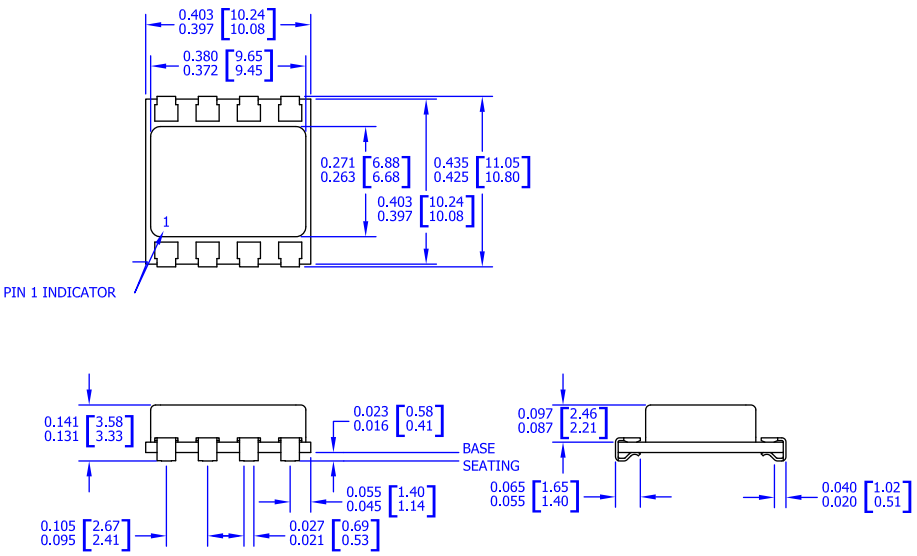
NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.028 oz. [0.783 g].

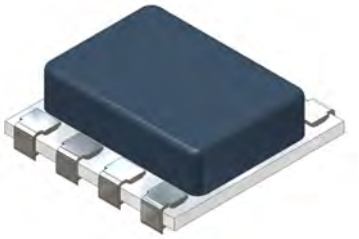
14-Pin DIP SMT GE

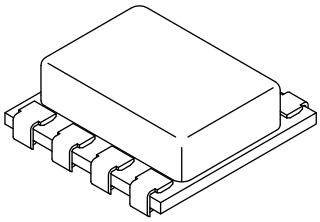


NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.049 oz. [1.382 g].

8-Pin DIP SMT GF

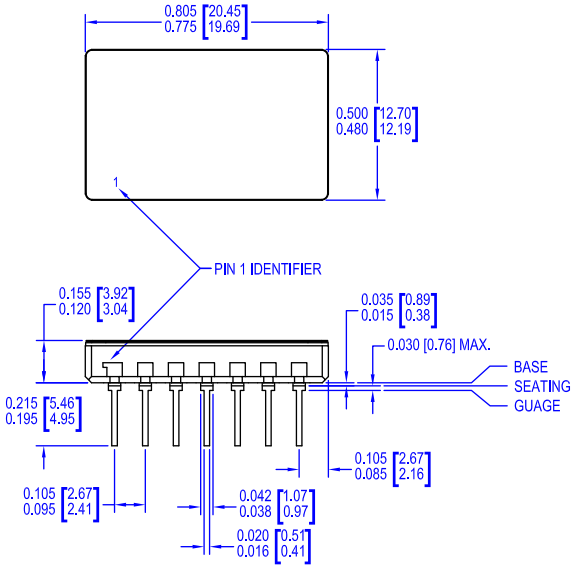


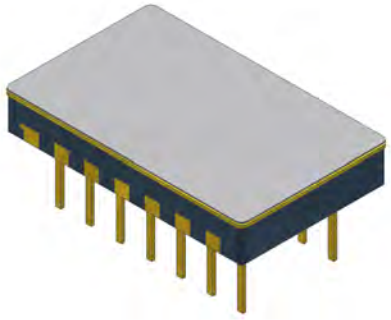


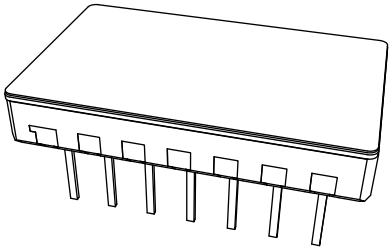


NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Nickel Iron, Tin over Nickel plated.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.026 oz. [0.736 g].

14-Pin Hermetic Ceramic DIP HC

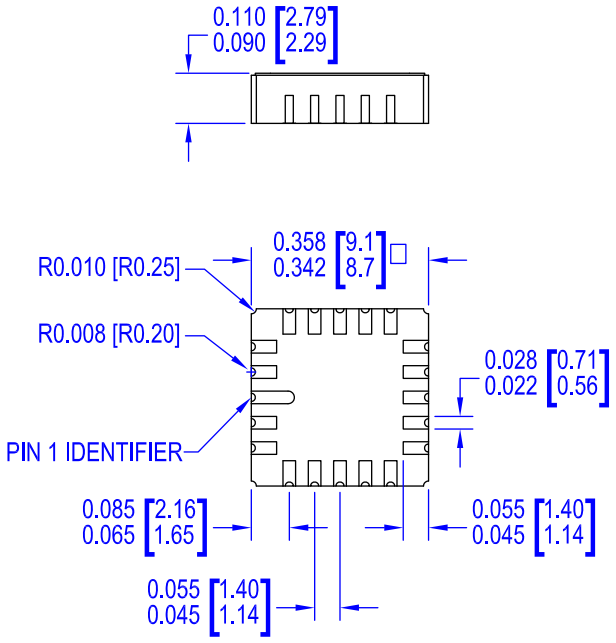


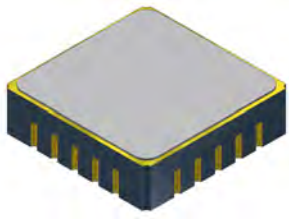


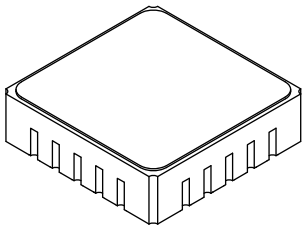


NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Gold over Nickel plated.
4. Material: Alumina Ceramic substrate and cover.
5. Cover: Electroless Nickel plated.
6. Package weight: 0.092 oz. [2.605 g].

20-Lead Ceramic LCC HD

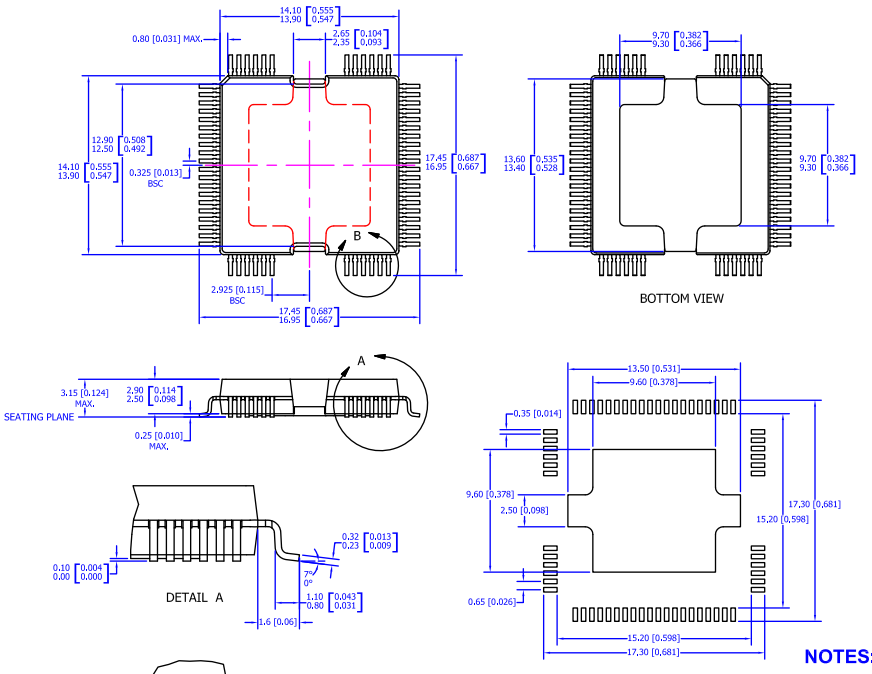


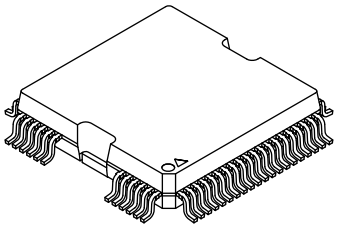




NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Contacts: Gold over Nickel plate.
4. Material: Alumina Ceramic substrate and cover.
5. Cover: Electroless Nickel plated.
6. Package weight: 0.024 oz. [0.680 g].

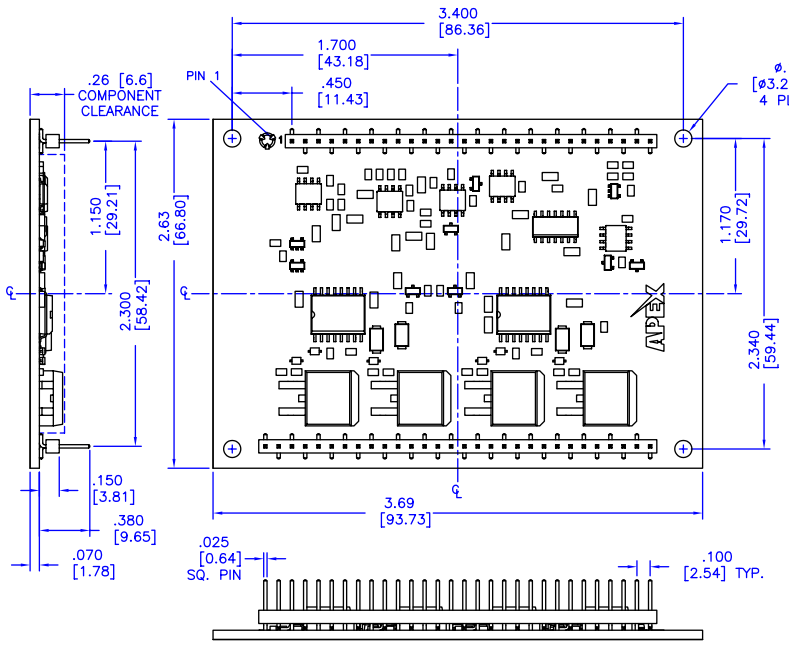
MO-188 64-Pin QFP HQ

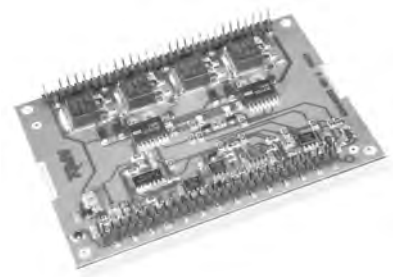


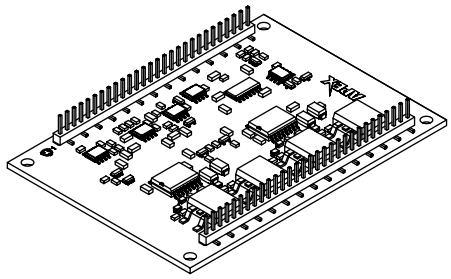


NOTES:
1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Chamfered corner denotes pin 1.
4. Heat slug: C10200 copper.
5. Lead frame: C19400 copper.
6. Mold compound: EME6600CSP epoxy.
7. Package weight (estimated): 0.71 oz. [2 g].
8. Suggested surface mount layout for reference only.

58-Pin Open Frame DIP KC

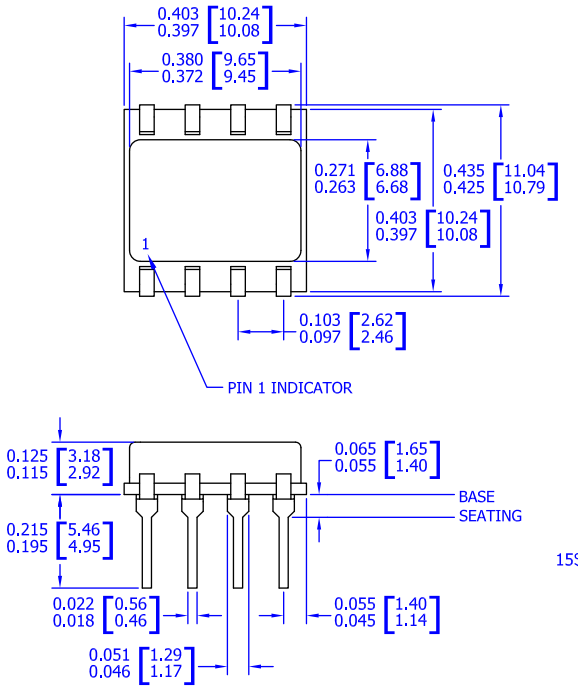


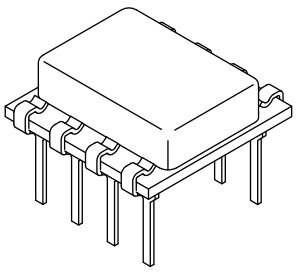




NOTES:
1. Dimensions are in inches & [mm].
2. Mold compound: MPC8000CH epoxy
3. Pins & Heat Slug: HCL–12S Cu alloy, 100% MATTE Sn FINISH
4. Package weight: .051 oz. [1.46 g]
5. Suggested surface mount layout for reference only.

8-Pin DIP KD

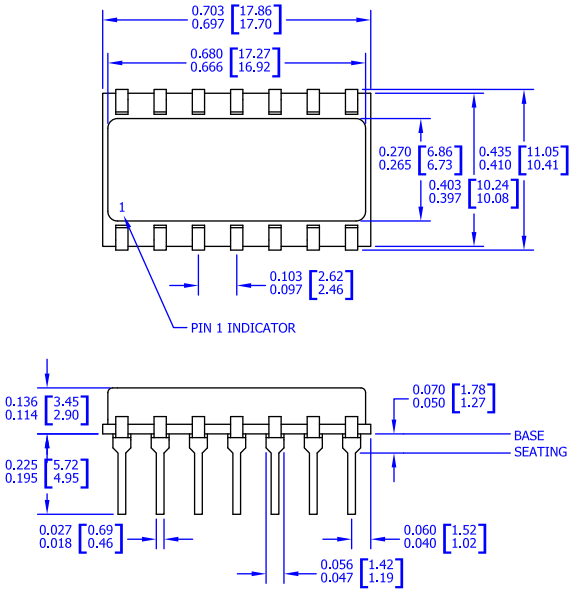


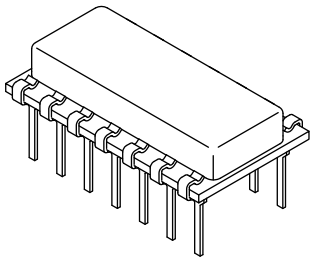


NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.028 oz. [0.785 g].

G

14-Pin DIP KE





NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.049 oz. [1.386 g].

Application Notes

Application Notes Cross Reference

The following Application Notes Cross Reference provides recommendations for specific applications.

General Application Topic	Recommended Application Note(s)
Basics of Power Amplifiers	App Note 1 - General Operating Considerations
Motor/Valve/Actuator	App Notes 11, 22, 24, 30, 45, 46, 49
Programmable Power Supply	App Notes 6, 7, 22
Electromagnetic Deflection	App Notes 5, 22
Electrostatic Deflection	App Note 22
Piezo, Electrofluorescent Display, Capacitive Load	App Note 22, 44
Audio	App Notes 3, 8, 11, 17, 22
Wideband	App Note 17, Consult Factory
Power Delivery and Power Dissipation	App Notes 8, 11, 30, 48
Power Booster or Composite Amplifier Applications	App Notes 14, 19, 48
PA12 and PA10 Applications	App Note 9
Safe Operating Area	App Notes 16, 22
Bridge Circuit Applications	App Notes 3, 20, 30
Stability	App Notes 19, 25, 47
Basics of PWM	App Note 30
PWM Low Pass Filtering	App Note 32
Spice Model and PWM Amplifier Applications	App Note 33

General Operating Considerations

SAVE HOURS OF VALUABLE TIME

This applications information is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. We highly recommend that you take the small amount of time required to read this section so that you can avoid the common pitfalls in designing and testing power operational amplifier circuits. As a minimum, you should read all oblique print and the first paragraph in each numbered subsection. The majority of these problem areas have been identified from Apex Precision Power Design Support Request discussions of actual circuits. They range from higher than expected errors to total destruction of the amplifier.

1.0 ENVIRONMENTAL AND HANDLING PRECAUTIONS

Most of this document concerns design and application practices that will ensure the long and productive life of an Apex Precision Power amplifier. However, not all design flaws can be seen on a schematic diagram. This is a list of the most serious handling and environmental hazards to an Apex Precision Power product.

1) ESD - All Apex Precision Power amplifiers should be handled using proper ESD Precautions. Many of our amplifiers include MOSFET devices which are particularly susceptible to damage from ESD.
2) Condensation - If the operating environment is capable of producing condensation on the amplifier use conformal coating to prevent a short between leads. The pin construction on the PowerSIP package is such that condensation can be trapped between the leads affecting performance and reducing the life of the device.
3) Compressible Thermal Washers - On package types with more than one point of attachment to a heatsink, compressible thermal pads can cause internal mechanical damage to the amplifier. There is more discussion in section 8.0.
4) Over-torque on the case - Follow the recommended torque guidelines when mounting screws are used to attach the package to the heatsink. There is more discussion in section 8.0.
5) Heatsink pin clearance - Be sure to protect pins from the heatsink. Use plastic or Teflon tubing on the pins to insulate them from the heatsink with packages requiring the pins to pass through the heatsink. There is more discussion in section 8.0.

2.0 BEFORE YOU APPLY POWER

In the design/prototype phase of an application, many dangers exist which will be eliminated by the time the circuit is ready for production. Pins may be wired in reverse order, connections may be missing, or test probes may cause momentary shorts. Any of these can destroy power amplifiers or other components in short order.

Five procedures can be employed to substantially reduce these dangers:

1) *Set power supplies to the minimum operating levels allowed by the data sheet.*
2) *Set amplifier current limit to very low levels* (i.e. use a current limit resistor of approximately 2.2 ohms for high current models and 47 ohms for high voltage models). Consult Section 5, "Current Limit," as well as the individual data sheet to determine the proper values for the current limit resistor(s). Do not depend on the variable current limit feature of your lab power supply for protecting the amplifier.

   It is much safer to install current limit resistors. Setting the current limit to a low value on a commercial lab supply will not protect the amplifier against the surge current available from the output filter capacitors. Even when average power dissipation is low, SOA violations can occur due to secondary breakdown of bipolar output stages. This mode of output stage destruction results from simultaneous application of high current and voltage to the conducting transistor. See Section 6 on SOA and the individual data sheets to better understand SOA limits.
3) *Check for oscillations.* With low voltage applied and reduced current limits in place, set the input signal to zero and connect a wide bandwidth (100 MHz or greater) oscilloscope to the output of the op amp. With the time base set to the microsecond region, check for oscillations present at any amplitude settings. Next, inject a signal into the circuit and monitor the output for oscillations. Excessive ringing on small signal square wave response indicates marginal stability.

   If an oscillation is found, measure the frequency and amplitude of oscillation. Also note whether the oscillation only shows up on the positive or negative half of the output. Refer to Section 10, "Stability," for diagnosing and fixing the cause of instability.

   With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions, i.e. motor reversal, square wave drive of reactive loads, or driving the output to V_S /2 for resistive loads. Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific voltages and power levels.
4) *Use the largest possible heatsink for your prototype work.* This precaution provides the best environment to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations, you may decide to use a smaller heatsink for your final circuit. Consult Section 7, **"Internal Power Dissipation And Heatsinking,"** for information on calculating heatsink requirements for your application.
5) *Avoid switching while the circuit is under power.* This includes plugging/unplugging banana jacks, switching relays in high current lines, switching within a feedback loop, etc. See Sections 9.1 and 9.3 for a further discussion of the dangers of switching.
6) When using an externally compensated amplifier, be aware that the compensation capacitor will be stressed to nearly the total supply voltage. A check of the equivalent circuit diagram will show one compensation terminal is within a few volts of one of the supply rails (often connected to the

gate of a FET) and the other is very close to the output voltage. At 300V and below, normal voltage margins are adequate. Above this it is advisable to rate the capacitor at twice the supply voltage. In this area, partial discharge and corona effect can take place. A good way to visualize the problem is to think of little packets of energy jumping across the capacitor. The FET gate can be destroyed long before incremental damage to the capacitor is ever seen.

3.0 ABSOLUTE MAXIMUM SPECIFICATIONS

Amplifiers should always operate below their Absolute Maximum Ratings to prevent permanent damage. If operation results in one of these maximums being reached, no permanent damage will result. *Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier.* Note that proper operation is only guaranteed over the ranges listed in the Specifications table.

Example: Most amplifiers have an Absolute Maximum case temperature rating of +125°C. If the Specifications table gives an operating temperature range of up to +85°C, then the parameter limits in the Specifications table are not valid between +85°C and +125°C. In addition, the amplifier may not even be operational in this range, (for example, the amplifier may latch to one of its supply rails when above +85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area.

The absolute maximum power dissipation rating used by Apex Precision Power is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, it is not a reasonable operating point because it requires an ideal (infinite) heatsink. Furthermore, even with the best heatsink, *sustained operation at the maximum rated junction temperature will result in reduced product life.* Refer to Section 7, **"Linear Power Dissipation And Heatsinking,"** for information regarding operating junction temperatures and relative product life. Apex Precision Power generally recommends operating at a case temperature that keeps maximum junction temperatures at 150°C or below.

Absolute Maximum Common Mode Voltage is another rating that illustrates the difference between the rated absolute maximum and the specified operating range. On many amplifiers, the rated absolute maximum voltage applied to both inputs simultaneously is equal to the power supply voltage. However, the linear operating range is 5V to 30V less than each power supply rail. This means that inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, may start to distort the signal, or could even latch the output to one of the supply rails.

For more information on specifications and limits, see Section 9, **"Amplifier Protection And Performance Limitations,"** Section 6, **"SOA,"** Section 4, **"Power Supplies,"** and the **"Parameter Definitions"** section.

4.0 POWER SUPPLIES

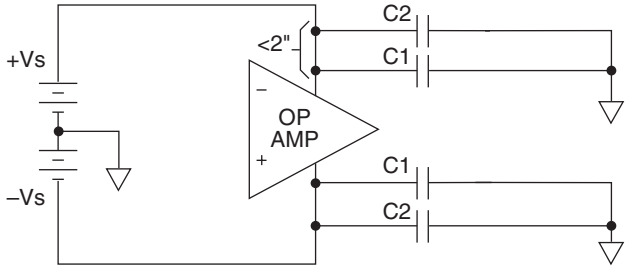
4.1 VOLTAGE SPECIFICATION

The specified voltage (±Vs) applies for a dual supply having equal voltages (±30V). An asymmetrical (+50V/–10V) or a single supply (60V) may be used as long as the total voltage between +Vs and –Vs does not exceed the maximum rating. Never allow reverse voltage on a supply pin. On a dual supply circuit, do not operate with only one supply connected.

4.2 POWER SUPPLY BYPASSING

Inadequate power supply bypassing can lead to power amplifier circuit oscillations. Each supply pin should be bypassed to common with a "low frequency bypass" capacitance of 10µF per Ampere of peak output current. Tantalum capacitors should be used, although computer grade aluminum electrolytics can be substituted for operating temperatures above 0°C.

In addition, a "high frequency bypass," .1µF to 1µF ceramic capacitor, should be added in parallel with the low frequency bypass capacitors from each supply rail to common. Refer to Figure 1. The ceramic capacitors must be mounted as close as possible (1/4" is good) to the supply pins. The larger capacitors should be within a few inches.



C1 = .1 to .1µF, Ceramic, High Frequency Bypass
C2 = 10µF/Amp out (peak), Electrolytic/Tantalum, Low Frequency Bypass

FIGURE 1. POWER SUPPLY BYPASSING

4.3 OVERVOLTAGE PROTECTION

The amplifier should not be stressed beyond its Absolute Maximum supply voltage rating. The amplifier should be protected against any condition that may lead to this voltage stress level. Two common sources of overvoltage are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply and AC main transients passing through a power supply to appear at the op amp supply pins.

Unipolar devices also protect against reverse polarity. Note that an open supply pin can cause supply reversal and sometimes amplifier destruction. Transient suppressors with a voltage rating greater than the maximum power supply voltage expected but less than the breakdown voltage of the amplifier will prevent the amplifier from damage.

Transients from the AC mains can be clamped through the use of MOVs (Metal Oxide Varistors) such as those made by General Electric, or bipolar TransZorbs. Connect either of these devices across the inputs to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors used in power supply filters will pass all high frequency energy and capacitors used in the filter are usually electrolytics which have high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will avoid the capacitor with little reduction. Refer to Figure 2 (next page).

5.0 CURRENT LIMIT

The primary function of current limit is to keep an amplifier within its SOA. See Section 6, **"Safe Operating Area."** Some models of Apex Precision Power Power Op Amps have an internal current limit, while most of our models have an adjustable limit that is set with one or two external resistors.

Any attempt to limit current with a circuit external to the amplifier must be approached with extreme caution. The pitfalls are generally time related and are often catastrophic. Most power supply current limit circuits are effective only AFTER stored energy in a large output filter capacitor has been depleted. This energy plus energy in local supply bypass capacitors is often more than enough to destroy the amplifier.

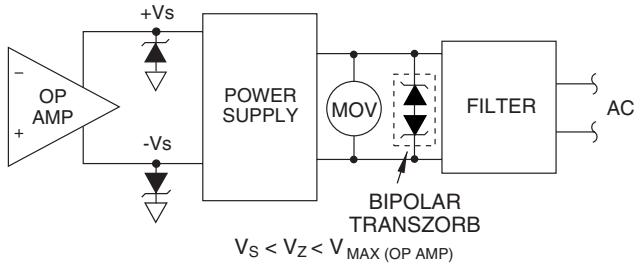


FIGURE 2. OVERVOLTAGE PROTECTION

Slow response time is also a problem with even the fastest fuses. A 15 second response time to a 200% over current is common. In most applications the amplifier will give its life protecting the fuse. Even if the fuse does blow, the amplifier may still be damaged. The blowing fuse is a mechanical interruption in a current carrying line which can cause voltage spikes above the supply rating of the amplifier.

5.1 CURRENT LIMIT PRECISION

Standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow ±20% variation at room temperature. Furthermore, the current limit varies over temperature. This temperature dependence is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the current limit equation given in Section 5.3 with –2.2mV per degree (Centigrade) of case temperature rise above 25°C. For example, at a case temperature of 125°C, this term becomes 0.43V rather than 0.65V; (650mV–(125°C–25°C)(–2.2mV)). When working with high currents, the impedance of PCB traces, lead lengths and solder joints must be included in the current limit calculations.

5.2 EXTERNALLY ADJUSTABLE CURRENT LIMIT

Models with provisions to adjust current limit externally must have the current limit resistors connected as shown in the external connection diagram.

Current limit should never be set at a value greater than the rated maximum output current of the power op amp. This maximum is due to the current density limitations of conductors in the package and exceeding it can destroy the amplifier. Also, using a very low resistance (such as a jumper wire) will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to second breakdown, thereby destroying reliability.

Operation without current limit resistors installed (current limit pins left open) can also cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for most of the high voltage, low current series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors.

5.3 CALCULATING CURRENT LIMIT

Power op amps with provisions to adjust current limit externally require one or two current limit resistors (R_{CL}) which must be connected as shown in the applicable external connection diagram below. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Some amplifier data sheets provide model specific equations, but in general each resistor and its power dissipation is calculated as follows:

$$R_{CL}\ (\text{ohms}) = \frac{0.65}{I_{LIM}\ (\text{A})}$$

$$P_{R_{CL}}\ (\text{watts}) = 0.65 \bullet I_{LIM}$$

I_{LIM} is the value of current limit desired and should be chosen to provide the amount of protection required for the specific application. For details on choosing "safe" levels of current limit and the protection/performance trade offs involved, see Section 6.3, **"Fault Protection Using Current Limit."**

For two resistor current limit schemes, asymmetrical current limiting ($R_{CL+} \neq R_{CL-}$) is permissible.

Foldover current limit, discussed in detail in AN #9, Current Limiting, provides a lower current limit for short circuit conditions while increasing current limit for load drive. Apex Precision Power power amplifiers, the PA10, PA12 PA04 and PA05, have this feature. Foldover reduces the protection/performance trade-off inherent in setting current limit. The Power Design Tool will calculate and plot current limit on an SOA graph for most linear amplifier models. It is available free at www.Cirrus.com.

6.0 SAFE OPERATING AREA (SOA)

6.1 READING THE SOA GRAPH

The horizontal axis on the SOA curve, V_S–V_O, defines the voltage stress across the output device that is conducting. It does n*ot* define a supply voltage or total supply voltage or the output voltage. V_S–V_O is the magnitude of the differential voltage from the supply to the output across the transistor that is conducting current to the load. Put another way: if the amplifier is sourcing current, use $(+V_S)$–V_O. If the amplifier is sinking current, use $(–V_S)$–V_O. Refer to Figures 3a & 3b.

The vertical axis represents the current that the amplifier is sourcing or sinking through the Output pin.

The Safe Operating Area curves show the limitations on the power handling capability of the amplifier. Refer to Figure 4 . There are three basic limitations:

1) *Current handling capability.T*his horizontal line near the top of the SOA CURVE represents the limit on output current imposed by current density constraints in the wire bonds, die junction area and thick film conductors.
2) *Power dissipation capability.* This is the power dissipation capability of the amplifier output stage. Note that the product of output current on the vertical axis and V_S–V_O on the horizontal axis is constant over this line. In other words, this portion of the SOA curve is a "constant power line." For T_C = 25°C, this line represents the maximum power dissipation capability of the amplifier at maximum junction temperature using an infinite heatsink. As case temperature increases, this constant power/thermal line moves toward the origin. The new constant power line can be determined from the Power Derating curves on the data sheet. The case temperature is primarily a function of the heatsink used. For more details, refer to Section 7, "**Linear Power Dissipation And Heatsinking.**"

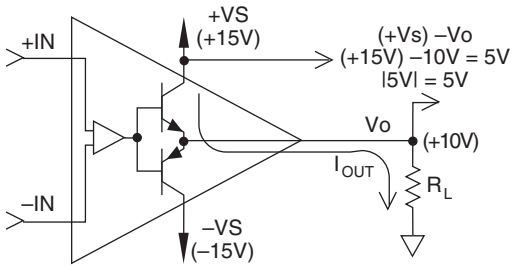


FIGURE 3A. SOURCING CURRENT

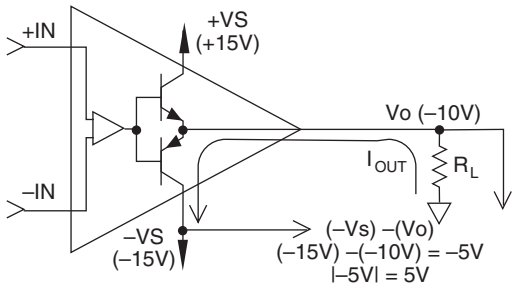


FIGURE 3B. SINKING CURRENT

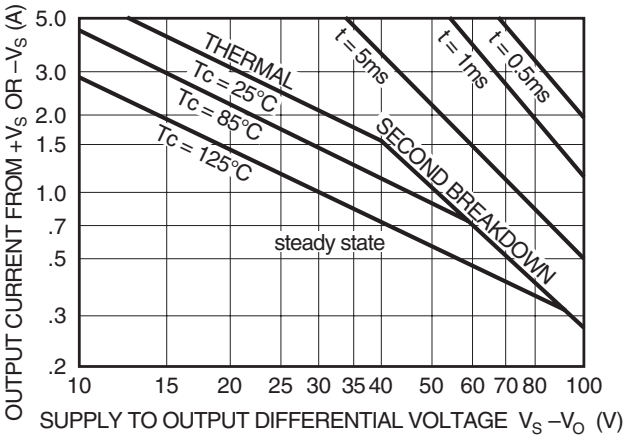


FIGURE 4. TYPICAL SOA CURVE

3) *Second Breakdown.* Second breakdown is a phenomenon exhibited by bipolar transistors when they are simultaneously stressed with high collector-emitter voltage and high collector current. Non-uniform current density in the emitter results in localized heating and "hot spots" at the junction. The temperature dependence of junction current results in increased current density at the hot spots. This concentration of current tends to further increase the temperature. The process is cumulative, leading to thermal runaway and transistor failure. Note that MOSFET power transistors do not have this second breakdown limitation.

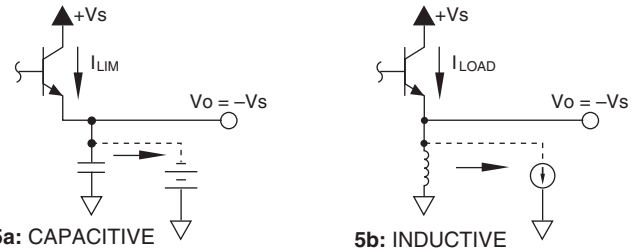
The transient second breakdown lines (t = 0.5ms, t = 1ms, and t = 5ms) are based on a 10% duty cycle. For instance, in Figure 4, the amplifier may deliver 1.5A at a V_S–V_O of 60V for 5ms but then must wait for 50ms before repeating this stress level. It is highly recommended to avoid entering the region beyond the DC second breakdown limits. Operation outside steady state limits in transient SOA regions is difficult to analyze adequately enough to insure best possible reliability.

6.2 HIGH SOA STRESS CONDITIONS

For resistive loads tied to ground, calculating power dissipation in the amplifier is reasonably simple. Refer to Section 7.1, "**DC Power Dissipation,**" and Section 7.2, "**AC Power Dissipation.**" However, with reactive loads, the voltage/current phase difference results in higher power being dissipated in the amplifier.

An example of an excessive transient stress condition created by a capacitive load is shown in Figure 5a. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a "go positive" signal. Immediately the amplifier will deliver its maximum allowed output current ($IL_{IM)}$ into the capacitor, which can be modeled at time t=0+ as a voltage source. This leads to a voltage stress across the conducting device equal to the rail-to-rail supply voltage. Simultaneously, the amplifier will be conducting its maximum (current-limited) value of current.

Figure 5b shows a similar transient stress condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the inductor has built up to some value $I_{LOAD.}$ Now the amplifier is given a "go negative" signal which causes the output voltage to swing down to the negative supply. However, the inductor at time t=0+ can be modeled as a current source that requires the amplifier to continue to source $I_{LOAD.}$ This leads to the same situation as before, that is, total supply voltage across a device conducting maximum rated current.



5a: CAPACITIVE **5b:** INDUCTIVE

FIGURE 5. TRANSIENT STRESS WITH REACTIVE LOADS

Note also that reactive loads cause higher thermal stress levels than resistive loads even under steady state sinusoidal conditions. *For purely reactive loads, all of the power is dissipated in the amplifier, none in the load.*

6.3 FAULT PROTECTION USING CURRENT LIMIT

With a given supply voltage, current limit can be used to keep the amplifier within its Safe Operating Area. This allows amplifier protection during fault conditions such as shorts to ground or shorts to either supply. The cost of protection is lowered output current capability.

For short-to-ground fault protection, set current limit to the value given by the intersection of the supply voltage and the DC SOA curve for the appropriate case temperature. Simply find the supply voltage on the horizontal axis. When the output is shorted to ground, $V_O = 0$; therefore, V_S–$V_O = V_{S,}$ follow up to the SOA curve intersection and then across to the output current. Referring to Figure 6, we see that in this example, a 2A current limit provides short circuit protection to ground at a case temperature of 25°C with ±30V supplies. Note that better heatsinking allows higher values of current limit.

For short-to-either supply protection, set current limit to the value given by the intersection of the rail-to-rail supply voltage ($V_{SS)}$ and the DC SOA curve. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the V_S–V_O axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of cur-

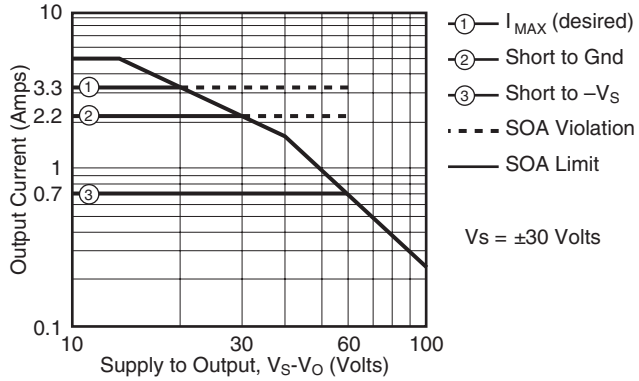


FIGURE 6. CURRENT LIMIT FAULT PROTECTION

rent limit. Referring to Figure 6, we see that in this example, a 0.7A current limit allows short protection to either supply.

It is often the case that requirements for fault protection and maximum output current may conflict. Under these conditions there are only four options. The first is to simply go to an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called "foldover" or "foldback." This is available on some amplifiers such as the PA10 and PA12. For a detailed discussion of foldover current limit and SOA fault protection refer to Application Note 9, "**Current Limiting.**" For an explanation of how to choose current limit resistors to adjust current limit, see Section 5.3, "**Calculating Current Limit.**"

7.0 LINEAR POWER DISSIPATION AND HEATSINKING

It is important to not confuse Internal Power Dissipation with power delivered to the load. These two power levels are equal only at unique signal levels. Low impedance faults or highly reactive loads will likely result in internal power dissipation being the higher level. Well-designed circuits with less reactance will yield higher efficiency.

There are two main steps in the heatsink selection process. First, the maximum internal power dissipation must be calculated. Secondly, the maximum desired junction and case temperatures must be chosen and the thermal model used to calculate the required thermal conductance of the heatsink. The following four sub-paragraphs deal with finding internal power dissipation in the output transistors generated by delivering current to the load only.

For purposes of power dissipation calculation, DC refers to any signal with a frequency below 60HZ. At true DC, heat is generated in only one output transistor and ability to conduct this heat to the surface of the amplifier case is determined by thermal conductance of materials and square area. As frequency increases, our original transistor now has a time variable heat load and the opposite side output transistor now generates the heat on alternate half cycles. This means the wattage figure can move from peak value toward RMS and more square area is used to conduct heat to the case, implying a lower thermal resistance. At 1HZ, internal thermal time constants are so fast compared to the half-second duration of the conduction cycle of each transistor, that no advantage gained. At 1KHZ, conduction cycles are short compared to internal time constants and thermal averaging allows taking advantage of both RMS power levels and the lower thermal resistance. While physics produces a smooth curve between these frequencies, the math is quite cumbersome. Most manufacturers of power op amps have adopted the 60HZ rule: Below 60HZ, use peak power and DC thermal resistance; otherwise use RMS power and AC thermal resistance.

7.1 DC POWER DISSIPATION

Power in the output transistor is the output current multiplied by the voltage across that transistor, or supply-to-output differential, Vs - Vo. For a purely resistive load, maximum power dissipation occurs at Vo = 1/2Vs and has a value of:

Where:

$$PD\ (max) = \frac{V_S^2}{4R_L}\ [\text{Purely resistive load only}]$$

Vs is the supply magnitude of the conducting transistor.

R_L is the load resistance.

For AC signals below 60HZ driving reactive loads, plot the load line to find stress levels. Use the highest power level from the plot for heatsink selection. Application Note 22 discusses SOA and Load Lines. As an example, consider the PA12A, ±48V supplies, ±40V signal at 50HZ driving a 69mH coil with 12.5Ω resistance, mounted on a 0.3°C/W heatsink. Figure 7 is the load line for this circuit with peak internal dissipation of 67.5W at 1.28A. Load impedance is 25Ω at 60° resulting in apparent power of 32VA and a power factor of 0.5. Quite a limitation for an amplifier boasting an ABSOLUTE MAXIMUM RATING of 125W! The software secret behind this plot will be revealed later.

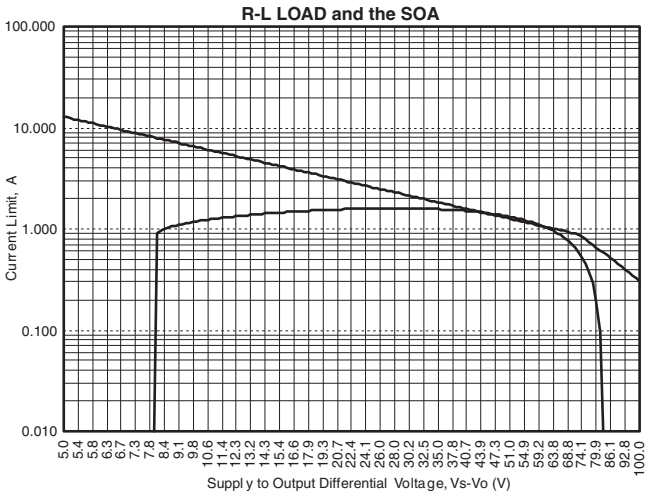


FIGURE 7

ELECTRICAL MEASUREMENT METHOD

Although we present this under the DC heading and it is primarily used at low frequencies, instrumentation errors are the only limitations on frequency. The ideal way to run this test is to have an amplifier/heatsink combination you are certain is large enough to handle all the power. While this may sound like circular cells in a spreadsheet, the test still has its place. Many loads do not change impedance with changing drive amplitude. If this is true, it is possible to replace the power amp in Figure 8 (next page) with a signal generator or a low power amplifier. Set the drive signal to a convenient fraction of the ultimate level, and rescale the voltages and currents measured prior to calculating power levels. If using a programmable signal generator, the actual output amplitude is not likely to match the programmed level because the load impedance is not likely to match the generator output impedance.

1. Use a small value current sense resistor between the load and ground to develop a voltage proportional to I_L. Use this signal to drive one channel of the X–Y display of an oscilloscope.
2. Use the output voltage of the amplifier, V_O, to drive the other channel of the X–Y display.
3. Calculate instantaneous power dissipation in the amplifier for several points on the ellipse using:

$$PD_{OUT} = (V_S - V_O)\ I_{LOAD}$$

4. Plot the points on the SOA curve and check for violations.

7.2 AC POWER DISSIPATION

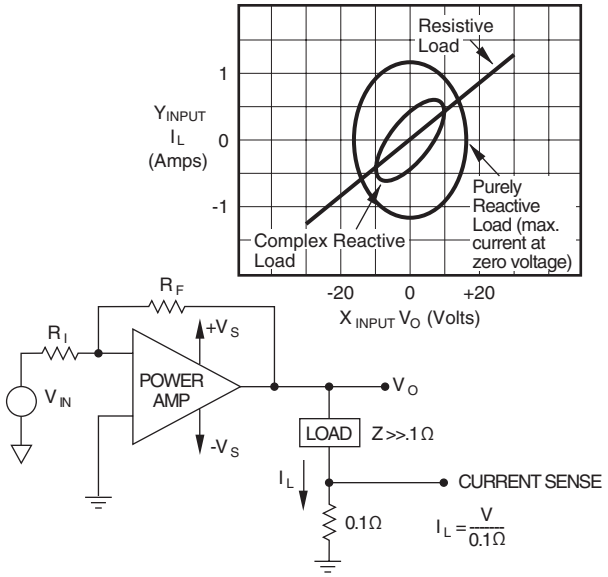


FIGURE 8. AC PD_{OUT}: ELECTRICAL MEASUREMENT

Again, "AC" for the purpose of determining power dissipation means at least 60HZ. For the moment, we will also confine the discussion to sinusoidal signals and symmetric supplies. Starting with the simple: When driving a pure resistance, power dissipation is maximum when the sine wave peak is 0.637*Vs. Refer to Figure 9 to see how the heat load on the amplifier decreases as signal amplitude varies in either direction. This equation yields maximum power:

Where:

$$PD\ (max) = \frac{2V_S^{\ 2}}{\pi^2 R_L}\ [\text{Purely resistive load only}]$$

V_S is the magnitude of each supply.
R_L is load resistance.

SIMPLE APPROXIMATION FOR REACTIVE LOADS

As loads move from pure resistance toward pure reactance, three changes should be noted:

1) The fraction of Vs corresponding to maximum power dissipation goes from 0.637 toward one. See Figure 10.
2) Power factor goes from one toward zero. With a pure reactance, no heat is generated in the load (no work is done).
3) The difference between load VA and true watts is dissipated in the amplifier.

Even with these changes, one of the two following formulas can be used to approximate internal power dissipation. The key is knowing the phase difference between V & I in the load, to find the power factor, COSØ, where ø is the angle between the voltage and the current. With only one reactive element in the load it is easy to determine what frequency will produce

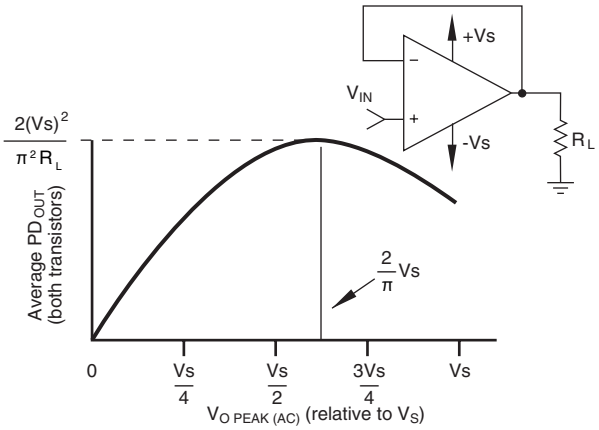


FIGURE 9. AC POWER DISSIPATION VS. PEAK OUTPUT VOLTAGE

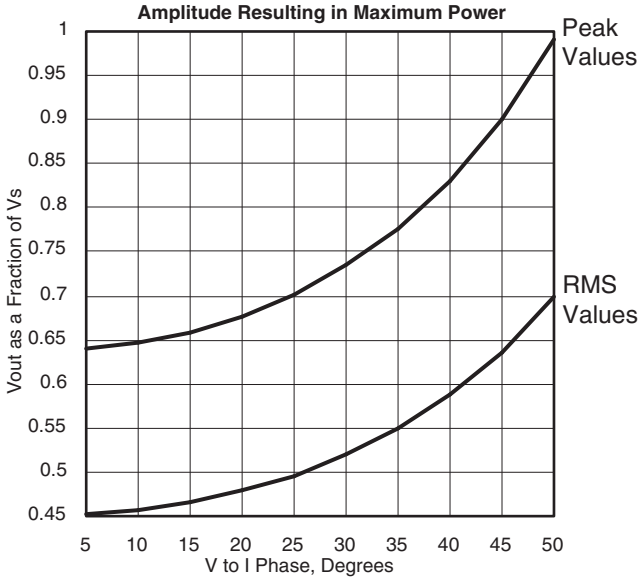


FIGURE 10. AMPLITUDE PRODUCING MAXIMUM POWER MOVES WITH PHASE ANGLE

the largest power dissipation. With the power factor and load impedance measured or calculated, the formulas are:

$$PD\ (max) = \frac{2V_S^{\ 2}}{\pi^2 Z_L\ COS\emptyset}\ [\text{Primarily resistive loads, } \emptyset < 40°]$$

$$PD\ (max) = \frac{V_S^{\ 2}}{2\ Z_L}\left[\frac{4}{\pi} - COS\emptyset\right]\ [\text{Primarily reactive loads, } \emptyset > 40°]$$

Where:
V_S is the magnitude of each supply.
Z_L is load impedance magnitude.

MORE ACCURATE METHODS

This method can be used analytically or on the bench as long as the test amplifier and heatsink are large enough to accommodate any errors in the first pass estimate of the circuit operation. Just as in the previous method, phase angle of the load must be known. Not only is it a term of the equations, but it is needed to determine the proper signal amplitude. Find the maximum power producing amplitude from Figure 10. If this is lower than the maximum amplitude your circuit will drive, use it. If not, use the circuit maximum.

1) Find the power delivered TO the amplifier from the supply:

2) Find the power delivered *from* the amplifier *to* the load:

$$P_{OUT} = (1/2)V_{PEAK}\ I_{PEAK}COS\O$$

$$P_{IN} = \frac{2V_S I_{PEAK}}{\pi}$$

3) Calculate power left in the amplifier:

$$PD_{INT} = P_{IN} - P_{OUT}$$

7.3 "OTHER" POWER DISSIPATION

For waveforms other than sinusoids, or for more complex energy storing loads such as motors, a Spice analysis and an electrical test method as described under DC Power Dissipation is recommended. Application Note 24, Brush Type DC Motor Drive may also prove useful.

7.4 "EASY" POWER DISSIPATION

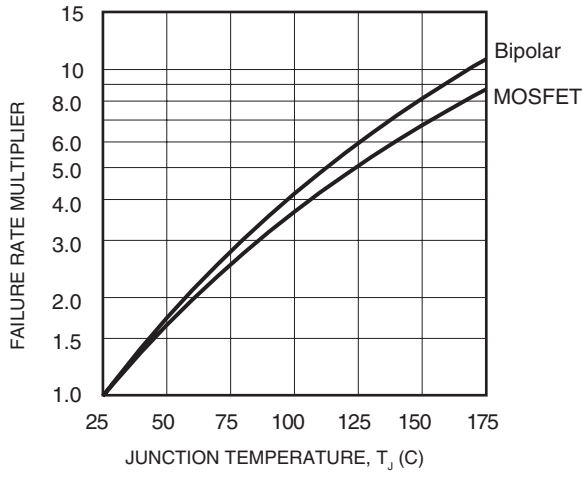
Power Design is an Excel spreadsheet available free from www.Cirrus.com. It remembers all the rules and formulas presented here, has a data base of model capabilities and finds the critical phase angle for you. Answers for simple loads are tabulated and load line plotted as fast as you can enter the data. Frequency sweeps on up to 54 component complex loads take a little longer. It also does calculations in the following paragraphs on heatsink selection plus, has sheets for stability, model selection, PWM filters and PWM power dissipation.

7.5 WHERE TO SET T_J MAX

For that matter, what is $T_J$max? In the ABSOLUTE MAXIMUM RATINGS area of a data sheet, it is the temperature limit set by the transistor manufacturer to insure leakage of that transistor does not become destructive. Especially on older bipolar models, 200°C appears frequently. This is not a good place to be on a continuous basis. From here on, T_J max will mean the design maximum for the circuit.

Reliability is a strong function of temperature. Figure 11, based on data from MIL-HDBK-217F, shows that a bipolar transistor operated a junction temperature of 175°C will have a mean failure rate more than ten times higher than with a junction temperature of 25°C. A MOSFET can be expected to fail almost nine times as often with the same temperature rise.

Apex Precision Power has seen applications required by military contract to meet a T_J max of 100°C. More often the designer must set T_J max based on application details. Would failure eliminate one bell or whistle on a non-critical piece of equipment, or completely stop a $1M per hour production line? How about consequential damage? Is the amplifier used for 30 seconds each day, or continuously? Can the amplifier be easily replaced, or does this require a space vehicle? Simply trade off these concerns against time, size, weight and cost budgets to arrive at the perfect T_J max.



This data has been extracted from the base failure rate tables of MIL-HDBK-217F, revision of 2 December 1991.

FIGURE 11. MTTF VS. TEMPERATURE

There are three approaches to lowering junction temperatures. The first is to lower internal power dissipation. Application Note 8, Optimizing Output Power, Notes 3 and 20 on bridge circuits and AN26 on parallel operation may prove helpful here. The second method is to lower the ambient temperature. This may involve placement choices inside an equipment enclosure or the use of a chilled liquid cooling system rather than air-cooling. Last on the list, we must minimize thermal resistance from the transistor junctions to the ambient environment.

7.6 THERMO-ELECTRIC MODELS

Thermo-electric models translate power terms into their electrical equivalent. In these models, power is modeled as current, temperature as voltage and thermal resistance as electrical resistance. Since 1980, Apex Precision Power has advocated using a simplified calculation of case and junction temperatures of power op amps. This shortcut assumed quiescent power was added to power dissipated due to output current and the total is used to calculate both temperatures. This yields the correct case temperature but predicts output transistor junction temperatures higher than the real world. This error is in the *safe* direction and generally insignificant until the amplifier combines high voltage and high speed causing quiescent power to be a significant percentage of the power rating of the output transistors alone.

The more accurate model shows that adding all the quiescent power to the calculation for the output transistors is an error because quiescent power is spread among all the components of the amplifier. From the data sheet point of view, the POWER DERATING graphs show power handling capability of the output transistors only, but the simple method produces a temperature rise in the output transistors due to current which does not flow in them. In the PA94, maximum quiescent current times maximum supply voltage develops 21.6W, over 70% of the power rating of the output stage. However, less than 1% of this power is in the output stage and the simple method imposes a false but severe limitation on power handling capability of the output transistors. It is very easy to design a reliable PA94 circuit where total power dissipation is greater than that allowed by the POWER DERATING graph.

THE SIMPLE MODEL

In Figure 12, P_D is the total power dissipation, that is P_D (internal dissipation of the output transistors due only to output current) plus quiescent power of the amplifier. Quiescent power (PD_Q) is quiescent current (I_Q) * total supply voltage.

$$PD_Q = I_Q\ (+V_S + |-V_S|)$$

A MORE ACCURATE MODEL

In Figure 13 (next page), quiescent power has been split according to the actual transistors generating the heat. PD_{Qout} is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case $PD_{Qout.}$

$$PD_{Qout} = I_{Qout}\ (+V_S + |-V_S|)$$

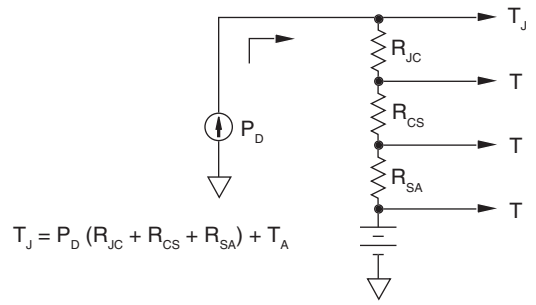


FIGURE 12. SIMPLE THERMO-ELECTRIC MODEL

PD_{Qother} is the current flowing in all the other components and could be found by subtracting PD_{Qout} from $PD_{Q.}$

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex Precision Power for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum "Meets full range specifications" case temperature.

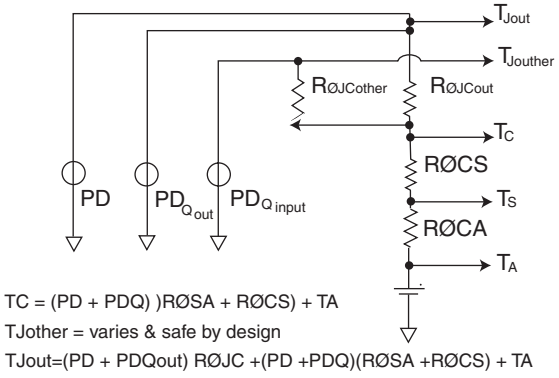


FIGURE 13. MORE ACCURATE THERMO-ELECTRIC MODEL

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:

1) Buy an amplifier with the lowest possible $R_{ØJC}$.
2) Use good mounting practices-see section 8 below.
3) Use the largest practical heatsink.

The amplifier is often a large portion of the thermal resistance budget. Better amplifiers usually cost more and sometimes are larger. Increased amplifier size is usually of little concern when compared to the size and weight of an adequate heatsink solution. If a larger amplifier can eliminate the need for liquid cooling or a fan, increased amplifier cost may not even be an issue. A reasonable starting point for amplifier selection is to find an ABSOLUTE MAXIMUM RATING of twice the power the circuit will actually dissipate.

$R_{ØCS}$ is often overlooked, but consider this: The PA12 with a AC thermal resistance of 0.9°C/W is mounted on the HS11 liquid cooled heatsink boasting thermal resistance of 0.1°C/W. If T_A is 25° and $R_{ØCS}$ is 0.1, 125W will place junctions at 162.5°C. If a mica or plastic washer is used or the amplifier is mounted bare, power to maintain this junction temperature could be cut to less than 70W! Again, see section 8 below.

The heatsink performance is the last element of the thermal resistance challenge. A quick glance at an SOA curve showing the power handling difference between case temperatures of 85°C and 125°C tells a story; but not the whole story. Data sheet SOA curves always assume $T_J$max is allowed to go to the ABSOLUTE MAXIMUM RATING. If your design is more conservative, the difference in power ratings will be even larger. Also be aware that heatsink ratings should be viewed more a guideline than an absolute.

7.7 HEATSINK SELECTION

Let's start with "the" heatsink rating. The HS03 is rated at 1.7°C/W in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you'll find a rating more like 2.3°C/W. On top of that, "free air" means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

Adding a fan to your design improves the thermal resistance rating of heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5-inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air flows through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

The bottom line: Without case temperature measurements, your design effort is NOT complete!

There are two temperature limitations on power amplifiers. A rating for each limitation must be calculated and numerically lower rating used. The most obvious limitation is the junction temperature of the output transistors. The case temperature must also be limited. In addition to reliability concerns (Figure 11 applies to the front end transistors as well as the output stage), DC error budget items of voltage offset drift and bias current drift are based on case temperature. Allowing a case temperature of 85°C as opposed to 40°C will increase voltage offset change by a factor of 4 and may double the failure rate of front end semiconductors. This would be a good time to recommend reading section 3 where the difference between ABSOLUTE MAXIMUM RATINGS and "Meets full range specifications" is discussed.

Here are some case-to-heatsink thermal resistance ratings ($R_{ØCS}$) of various package styles. These ratings assume the amplifier is mounted with either an Apex Precision Power aluminum thermal washer or with a thin coating of fresh thermal grease covering the entire mounting surface. If designing the mounting surface, see the ACCESSORIES INFORMATION data sheet for recommended hole sizes.

TO-3	MO-127	PD10	SIP02,3	SIP12, 04, 5 (Kapton)
0.1°C/W	0.05°C/W	0.08°C/W	0.1°C/W	0.2°C/W

Using either thermal model, the heatsink rating based on case temperature limitations is:

$$R_{ØSA} = \frac{T_C - T_A}{PD + PD_Q} - R_{ØCS}$$

Where:
T_C = maximum case temperature allowed.
PD = output transistor power dissipation due to load current
PD_Q = Total quiescent power.

THE SIMPLE METHOD

If PD_Q is one tenth of less PD, this simple method will work well. If the amplifier has a slew rate of several hundred volts/microsecond and the application is above 300V, use the more accurate method. The simple formula is:

$$R_{\Theta SA} = \frac{T_J - T_A}{PD + PD_Q} - R_{\Theta JC} - R_{\Theta CS}$$

Where:
T_J = maximum junction temperature allowed
$R_{\Theta JC}$ = AC or DC thermal rest from the specification table

THE MORE ACCURATE VERSION

With the unique combination of high voltage and speed such as the 900V and 500V/us of the PA94, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of the amplifier. To more accurately predict operating temperatures use the following procedure.

Look for an output stage only quiescent current rating in the data sheet. If the data sheet does not list this specification, it can be estimated as 5% of the total quiescent current.

Find output stage quiescent power (PD_{QOUT}) by multiplying the output stage only quiescent current by the total supply (V_{ss}). Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower:

$$R_{\Theta SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) \bullet R_{\Theta JC}}{PD + PD_Q} - R_{\Theta CS}$$

Where:
T_J = maximum junction temperature allowed.
$R_{\Theta JC}$=AC or DC thermal resistance from the specification table.

THE EASY AND ACCURATE METHOD

1) Set aside the slide ruler and calculator.
2) Start Power Design, an Excel spreadsheet available free from www.Cirrus.com
3) Enter amplifier, V_S, min/max frequency, output amplitude and load components.
4) Read load, supply and amplifier power levels, heatsink rating & maybe some warnings.
5) Tweak design as desired.
6) Enter design notes and press Print button for documentation.
7) Ask your boss for a raise.

8.0 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

For Power Op Amp designs, high reliability consists of mechanical considerations as well as electrical considerations. Proper mounting is very important for power amplifiers. Once the proper heatsink has been selected as described in Section 7, the following mounting techniques should be used.

All Apex Precision Power metal can products have either an isolated case, ground connected case or a dedicated pin for the case. This means electrical insulating washers are generally not necessary and will likely increase operating temperatures if used.

In addition, Apex Precision Power uses a thin beryllia substrate to get the lowest possible thermal resistance. While this leads to cool running, high reliability amplifiers, it is important not to run the risk of cracking this substrate. In order to prevent this, two major precautions must be observed:

1) *Do not use compressible thermal washers.* These are silicon rubber based pads such as Silpad. The amount of compressibility in a washer over 2 mil thick can lead to header flexing, which can crack the substrate. *The use of these washers voids the warranty.* Also, thermal grease has superior thermal properties.
2) When using reflow soldering with package types DF (PSOP1), DK (PSOP2), EF (QFP01) and EK (QFP02), be aware that these packages are moisture sensitive. These devices should be baked at 125°C for 48 hours and the reflow operation should be performed within 48 hours of baking. Black carriers (EF and EK packages) are suitable for baking. Clear plastic tubes (DF and DK packages) are NOT suitable for baking; the devices need to be removed from these tubes prior to baking. Caution must be exercised to avoid mechanical or ESD damage.
3) *Do not overtorque the case. Recommended mounting torque for the TO-3 and SIP packages is 4-7 in-lbs (.45-.79 N-m) and for the MO-127 Power Dip™ packages (PD10 AND PD12) is 8-10 in-lbs (.90-1.13 N-m).* Refer to Figure 14. Apply a thin, uniform film of thermal grease or an Apex Precision Power thermal washer between the case and heatsink. Apply small increments of torque alternately between each screw when mounting the amplifier.

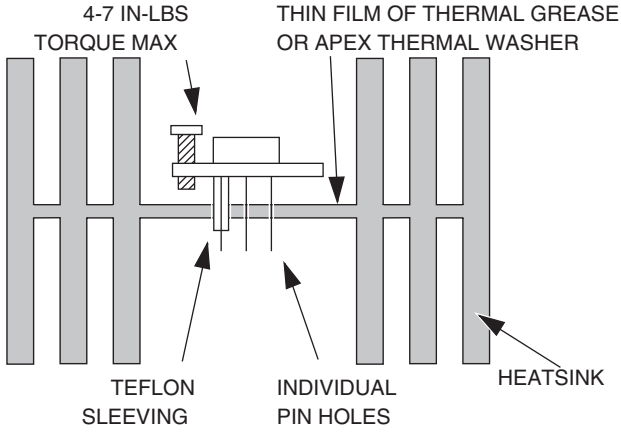


FIGURE 14. MOUNTING CONSIDERATIONS

Due to dimensional tolerances between heatsink thru-holes and power op amp packages, extreme care must be taken not to let the pins touch the heatsink inside the thru-holes. *Do not count on the anodization for insulation* as it can nick easily, exposing bare aluminum, an excellent electrical conductor. *Use plastic tubing to sleeve at least two opposite pins* if you are using a mating socket or printed circuit board. If you are wiring directly to the pins, it is best to sleeve all pins. *Refer to the Package and Accessories Information section of the Hybrid & IC Handbook for further details on sleeving sizes, mating sockets and cage jacks for PC board mounting of power amplifiers. While teflon covers virtually all applications, the actual requirements are to withstand the maximum case temperatures and total supply voltage of the application.*

Never drill out the entire area inside the pin circle, drill individual holes for each pin. Often, heatsinking is accomplished with a custom heatsink or by directly mounting to a bulkhead. These approaches require the use of heatsink thru-holes for the amplifiers pins. For the 8-Pin TO-3 package, the main path for heat flow occurs inside the circumference of 8 pins. Refer to Figure 15. Therefore, a single, large hole, to allow the 8 pins to pass through, will remove the critical heatsinking from where it is most needed. Instead, 8 separate #46 drill size holes must be drilled.

9.0 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

9.1 OUTPUT PROTECTION

Attempting to make sudden changes in current flow in an

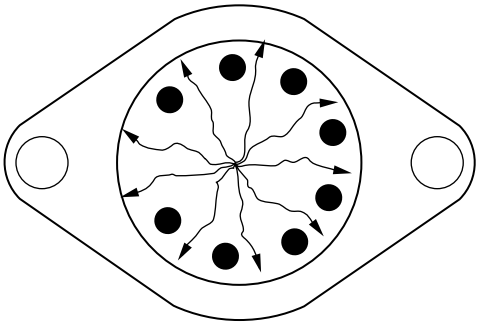


FIGURE 15. MAIN HEAT FLOW PATH: 8-PIN TO 3 PACKAGE

inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. Brush type DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, mechanical shocks to a piezoelectric transducer will cause it to generate a voltage. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes should not be counted on to protect the amplifier against sustained high frequency, high energy kickback pulses. Many of these diodes are intrinsic "epi" diodes that occur as a result of the manufacture of the power darlington output transistor. Epi diodes generally have slow reverse recovery times and may have large forward voltage drops. *Under sustained high energy flyback conditions, high speed, fast reverse recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes.* See Figure 16. These fast recovery diodes should have reverse recovery times of less than 100 nanoseconds and for very high frequency energy should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source when current flows in the opposite direction from normal. Otherwise, the flyback energy, coupled back into the supply pin, will merely result in a voltage spike at the supply pin of the op amp. This would lead to an overvoltage condition and possible destruction. Refer to Section 4.3 for information on overvoltage protection.

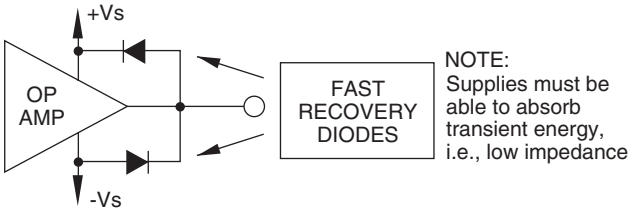


FIGURE 16. OUTPUT PROTECTION

9.2 COMMON MODE VOLTAGE LIMITATIONS

One of the most widely misunderstood parameters on an op amp data sheet is the *Common Mode Voltage Range*, which specifies how close an input voltage *common to both inputs* may approach either supply rail. *When these limits are exceeded, the amplifier is not guaranteed to perform linearly. The Absolute Maximum Common Mode Voltage* specification on most data sheets refers to the voltage above which *the inputs may not exceed or damage will result to the amplifier*.

There are two cases which clearly illustrate the constraints of common mode voltage specifications: single supply operation and asymmetrical supply operation.

Example:

The Apex Precision Power PA82J has a Common Mode Voltage Range of ±Vs – 10. This implies that if the PA82J is to be operated from a single supply, both inputs must be biased at least 10 volts above ground. Figure 17 illustrates an implementation of this which keeps both inputs above 10 volts for the given range of input voltages. Note that for single supply operation, the output of the amplifier is never capable of swinging all the way down to ground. This is due to the output saturation voltage of the amplifier.

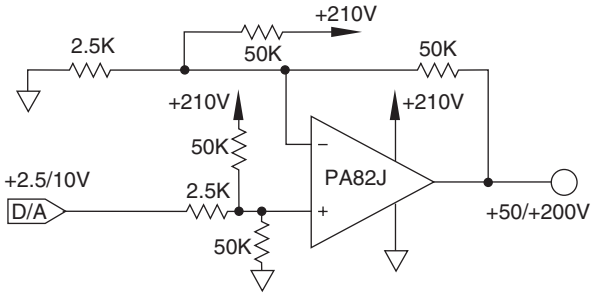


FIGURE 17. SINGLE SUPPLY OPERATION: V_{CM} CONSIDERATIONS

Figure 18 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage source allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar supply. As long as the amplifier remains in the linear region of operation, the common mode voltage will be zero. With the 12V supply the allowed positive common mode voltage range is from 0 to 2V. Note the output of the PA81J can swing all the way to zero now also. The 12V supply in this case need only supply the quiescent current of the power op amp. If the load is reactive or EMF generating, the low voltage supply must also be able to absorb the reverse currents generated by the load.

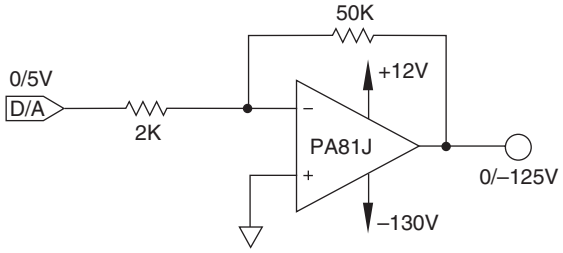


FIGURE 18. NON-SYMMETRICAL SUPPLY OPERATION

9.3 DIFFERENTIAL INPUT VOLTAGE LIMITATIONS AND PROTECTION

Exceeding the Absolute Maximum Differential Input Voltage specified on the data sheet can cause permanent damage to the differential input stage. Failure modes range from increased V_{OS} and V_{OS} drift, I_B and I_B drift, and input offset current, up to input stage destruction. Although the differential input voltage (V_{ID}) under normal closed loop conditions is microvolts, several conditions can cause it to be in the Volt range. Causes of V_{ID}:

1) Fast rise-time inputs.
2) Signal input while not under power.
3) High impedance output states (current limit, thermal shutdown, sleep mode).
4) Switching within the feedback loop.

An example of condition 4 is shown in Figure 19a.

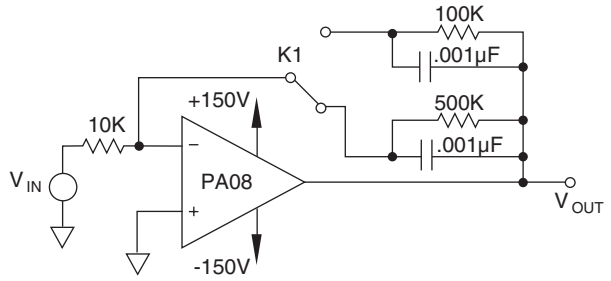


FIGURE 19a. GAIN SWITCHING AND V_{ID} VIOLATION

This configuration is often used in ATE systems for changing the gain of an op amp. The amplifier's full scale transition time (microseconds) is faster than the typical relay switching time (milliseconds); therefore when the relay opens the feedback loop, the Aol of the amplifier will drive the output to one of the supply rails. In the example shown, the output will approach 150V while the relay is still switching. Because the 100K feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the input. Since the Absolute Maximum V_{ID} for the PA08 is ±50V, the input stage will be destroyed.

Effective input protection networks provide two functions:

1) Limit differential voltage to less than the reverse breakdown voltage of the input transistors base-emitter junction, typically ~6V.
2) Limit input transient current flow to less than 150mA.

Figure 19b shows an example of an input V_{ID} protection network. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

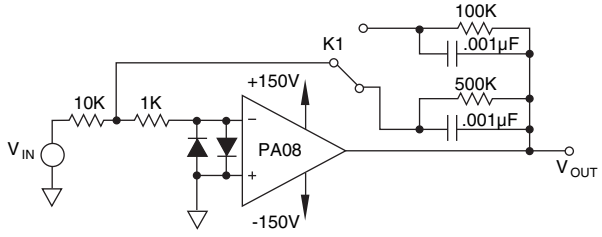


FIGURE 19b. GAIN SWITCHING AND V_{ID} PROTECTION

10.0 STABILITY

The most common application problem when working with power op amps is stability. Although most power op amps are compensated for unity gain stability, they are frequently required to drive reactive loads, deliver high currents, or use high impedances due to high voltage. These conditions make stability more difficult to achieve. However, EVERY circuit can be stabilized if the guidelines given here are followed. Table 1 provides a troubleshooting guide for stability problems. The **"Probable Cause / Possible Solution Key"** gives insight into the origin of the problem and provides guidance as to the appropriate fix.

An amplifier becomes an oscillator when two conditions are met: total phase shift reaches 360° and the amplifier has gain at this frequency. With operational amplifiers using negative feedback, half the required phase shift is provided by the inverting nature of the circuit. This means phase shift from all other sources totals a second 180° when oscillating. The crucial element here is to examine phase shift at frequencies all

CONDITION AND PROBABLE CAUSE TABLE

Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
CLBW f_{osc} UGBW	N	Y	N	A, C, D, B
CLBW f_{osc} UGBW	Y	Y	Y	K, E, F, J
CLBW f_{osc} UGBW	–	N	Y	G
f_{osc} CLBW	N	Y	Y	D
f_{osc} = UGBW	Y	Y	N*	J, C
f_{osc} ≪ UGBW	Y	Y	N	L, C
f_{osc} > UGBW	N	Y	N	B, A
f_{osc} > UGBW	N	N**	N	A, B, I, H

TABLE 1.
CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 20 for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 20) will stop oscillation if Rn << |Zcf| at UGBW
**Only oscillates over a portion of the output cycle.

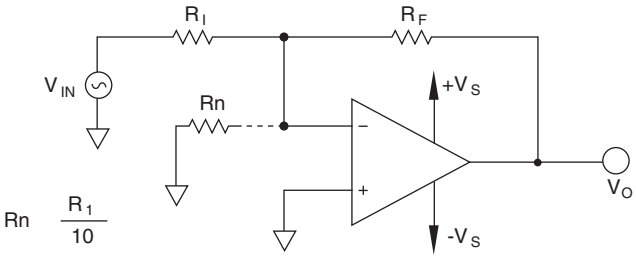


FIGURE 20. LOOP CHECK CIRCUIT

the way out to the intersection of open and closed loop gains. Putting it another way, just because the circuit is designed for DC only, does not preclude it from oscillating at 1MHz. Most Apex Precision Power amplifiers have gain well into the MHz region and phase shifts of both amplifiers and parasitic elements grow rapidly in this area.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
   Solution: Bypass power supplies. See Section 4.2.
B. Cause: Supply lead inductance.
   Solution: Bypass power supplies. See Section 4.2.
C. Cause: Ground loops.
   Solution: Use **"Star"** grounding. See Figure 21.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
   Solution: Raise gain or use input R–C compensation network. See Figure 24.
E. Cause: Inductor within the feedback loop (noise gain zero).
   Solution: Use alternate feedback path. See AN#5, **"Precision Magnetic Deflection,"** or AN#13, **"V–I Conversion."**
F. Cause: Input capacitance reacting with high R_F (noise gain zero).
   Solution: Use Cf in parallel with Rf. (Cf =~Cin). Do not use too much Cf, or you may get problem J.
G. Cause: Output to input coupling.
   Solution: Run output traces away from input traces, ground the case, bypass or eliminate R_B (the bias current

compensation resistor from –IN to ground)

H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 10.1.

I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 10.1.

J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce Cf and/or increase Cc for unity gain stability.

K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use input R–C compensation network. See Figure 24.

L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**

10.1 BASICS OF STABILITY

Some basic practices must be followed to ensure stability. Proper ground practices are mandatory and are illustrated in Figure 21. Improper grounding can lead to oscillations near the unity gain bandwidth frequency of the amplifier. Proper bypassing of power supplies is also illustrated in Figure 21. The local bypassing close to the amplifier with a small electrolytic and ceramic capacitor insure good high frequency grounding of the supply lines. The internal phase compensation on op amps will be referred to one of the supply lines and this is the reason for the importance of good local bypassing.

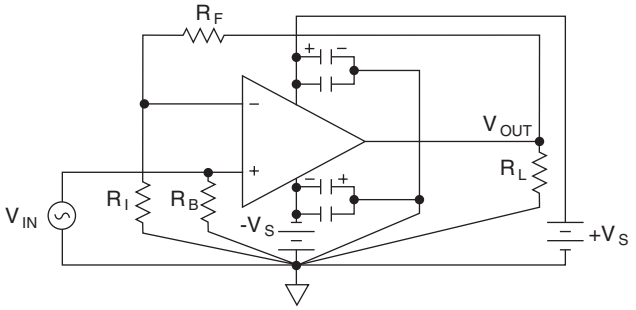


FIGURE 21. BASIC REQUIREMENTS FOR STABILITY

Table 1 shows the frequency of an oscillation is the most important clue about its source. For frequencies above unity gain the amplifier, try a snubber network as shown in Figure 22. For frequencies near the intersection of open and closed loop gains, check for weak high frequency supply bypass or for ground loops. For lower frequencies, perform a loop analysis using Application Notes 19 and 25

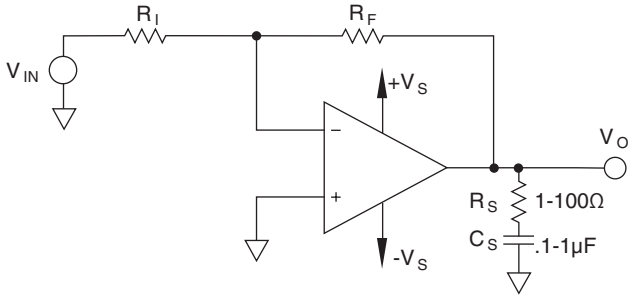


FIGURE 22. OUTPUT R-C-NETWORK ("SNUBBER")

10.2 COMMON SOURCES OF NON-LOOP INSTABILITY

The following is a list of the most common instability situations reported:

1) Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended, but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
2) A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test okay. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the board oscillates. Cross coupling through the supplies is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case, and consider all items in the following section.
3) Ungrounded cases can cause oscillations, especially with faster amplifiers. The cases of most Apex Precision Power metal can amplifiers are electrically isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross-coupling or positive feedback leading to oscillations. Some models have heatsink tabs connected to $-V_S$, serving the same purpose as long as $-V_S$ is clean.
4) A standard inverting circuit includes an impedance matching resistor in series with the non-inverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna, receiving positive feedback, causing oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least .01uF.

10.3 LOOP STABILITY ISSUES

A majority of loop instability problems are due to one or more of the following:

1) Amplifier compensation not matched to the circuit closed loop gain. This includes using amplifiers below their recommended gain, choosing the wrong external compensation or failure to realize high frequency (not DC) gain is what counts. (A feedback or integrating capacitor lowers gain at high frequency).
2) The use of large impedance values for input or feedback networks allows parasitic elements too much control. Consider a 100KΩ feedback resister with a parasitic of 3pF. This places a pole (with an additional 45° phase shift) at about 53KHz!
3) Capacitive loads reacting with amplifier output impedance, effectively adding a pole and corresponding phase shift to the amplifier.
4) Voltage-to-current phase shift of an inductor is inside the feedback loop of current output circuits.
5) Too many amplifiers inside a single loop. Each amplifier contributes to the total as you go around the loop.

Solutions for these include one or more of the following:

1) Change to an amplifier suitable for lower gain, increase external phase compensation, or modify the circuit.
2) Lower impedance values.

3) Add an isolation resistor outside the feedback loop to defeat the effect of the capacitive load as shown in Figure 23. This is the simplest external component solution and has surprisingly little effect on circuit performance.

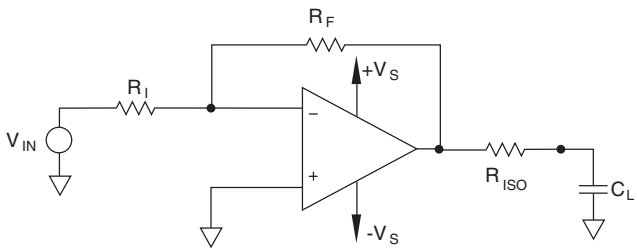


FIGURE 23. CAPACITIVE LOAD ISOLATION

4) Increase DC closed loop gain.
5) Increase AC gain only with noise gain compensation as shown in Figure 24. This technique works well with inverting circuits but is not recommended for non-inverting circuits.

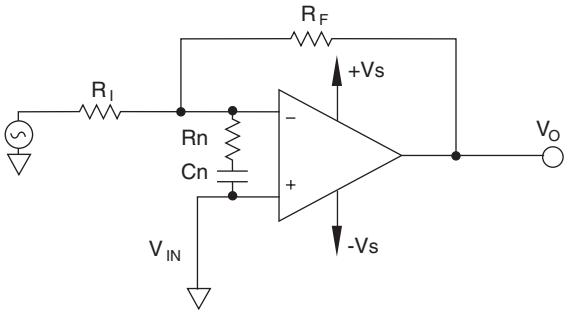


FIGURE 24. INPUT R-C NETWORK COMPENSATION

6) Lower the intersection rate of open and closed loop gains with a properly sized roll off capacitor. Usually, bigger is not better.
7) Add an AC voltage gain limiter to the current output circuit. At the higher frequencies where the inductor demands very high voltages, this R-C network puts the amplifier into a voltage feedback mode.
8) Lower amplifier count.

Most of these solutions tend to negatively impact bandwidth, especially in the current output circuits. Apex Precision Power has been known to boast, "Any circuit can be made stable". Notice that bandwidth trade offs were not part of the quotation; this is where the engineering work lies. Upon looking at the Application Notes mentioned above, some of you may be thinking about the amount of this work, with phrases we can't print here. Have no fear, Power Design takes care of all the tedious math and graphing for you making design iterations a snap.

10.4 A FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply these techniques and ideas under your worst case load conditions and you can conquer your oscillation problems.

THE APEX PRECISION POWER DESIGN SUPPORT REQUEST

The Apex Precision Power Design Support Request provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to Apex Precision Power for a failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Optoelectronic Position Control

INTRODUCTION

Power Op Amps are ideally suited for position control because their response time is fast compared to any mechanical drive train. The optoelectronic technique of position control can move to and maintain fixed index points on linear or rotary motion components while adding no linkages or independently moving parts. The resulting system features high reliability, accuracy and repeatability. If the integration of photodiode currents is required, select a power amplifier with an FET input to maintain very low bias current levels such that the integrating capacitor voltage will remain constant during periods when both photodiodes are not illuminated. Further selection criteria should be based on motor ratings and/or available power.

SEQUENTIAL POSITION CONTROL

In the circuit shown in Figure 1, the PA07 integrates the differential output of the pair of photodiodes and drives the motor in the proper direction until the photodiode currents are equal. This differential configuration negates the well known temperature and time instabilities of optoelectronic devices. To move between index points, a fixed input current is momentarily switched to the amplifier input causing the amplifier to drive the motor in the desired direction. The charge on C_F will maintain motor drive as the input current is switched off prior to reaching the index point. As the first photodiode is illuminated, its output reinforces the current direction of motion. As the second photodiode is illuminated, its current will reverse the motor drive, causing the system to lock to the index point.

As motor response and system inertia vary widely, C_F and R_F must be selected for the individual application to provide proper damping. C_F must be small enough to allow drive reversal before the index point passes the second photodiode or the system will continue on to the next index. Very small values of C_F can cause severe overshoot or oscillation leading to motor burnout and/or drive train failure. R_{F1} and R_{F2} are required to stabilize the control loop at the unity gain point and to minimize overshoot. R_L and C_L form a lead network which may be included to improve response time by enabling the amplifier to modify the motor drive based on a change of the sensor output. In this manner, a braking force can be applied to the motor prior to reaching the index point. The motor shown in Figure 1, having EMF of 14V, will apply a 46V stress across the conducting output transistor when reversed. With a duration longer than 5ms, the steady state secondary breakdown line of the SOA for the PA07 curves requires the current limits to be set to 1A. See PA07 data sheet.

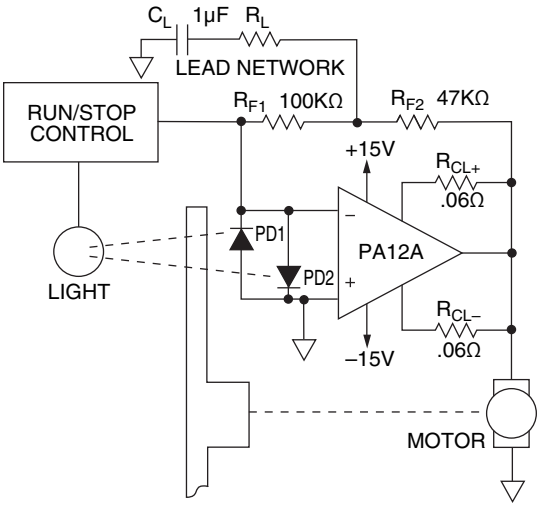


FIGURE 2. SINGLE POINT POSITION CONTROL

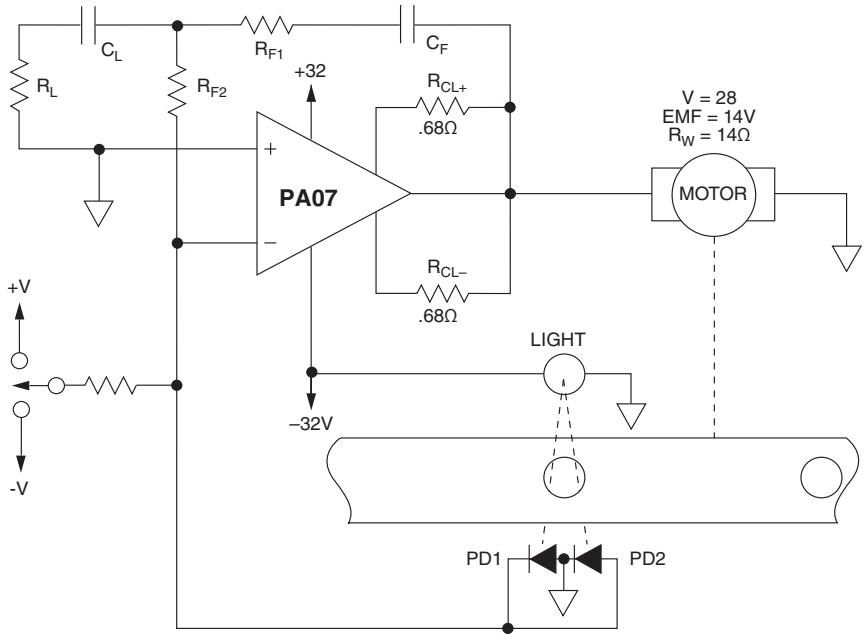


FIGURE 1. SEQUENTIAL POSITION CONTROL

SINGLE POINT POSITION CONTROL

A variation of the above technique shown in Figure 2 can be used to return a wheel to a single index point after rotating in either direction. The low inertia, fast response system will take the shorter route to the index point when switched from run to stop. The PA12A was selected for this application because it provides high power while keeping bias current levels low with respect to the photodiode currents. To improve response time, the lead network compensates for motor response lagging behind any change in drive voltage. A run control current of sufficient amplitude to override the photodiode currents is fed to the amplifier inverting input. Removal of this current restores control to the photosensors.

POSITION CONTROL MASK

Figure 3 shows details of the wheel preparation and sensor placements at the stop index. Arrows indicate direction of rotation when the corresponding photodiode has the higher output. While it is theoretically possible to achieve a stable position on the opposite side of the

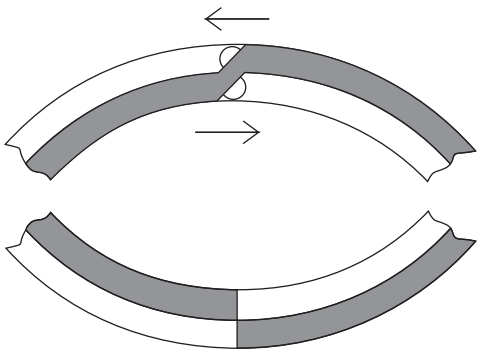


FIGURE 3. SINGLE INDEX POINT DISK

wheel, system noise or a slight movement will imbalance the equal photodiode currents and the higher current sensor will receive even more light. This causes the wheel to seek the desired index point. Masking of the wheel at an angle to the radial softens the control function and prevents overshoot.

SPOT SIZE

Optimum relationship of beam size to active areas of the photodetectors is shown in Figure 4. A centered beam should illuminate half the photosensitive area of each diode. Too large a beam will produce no change of sensor output for a range of positions, while a smaller beam will produce a nonlinear transfer function near the center line between the photosensitive areas. This makes selection of C_F to dampen the circuit difficult and requires a higher intensity light source.

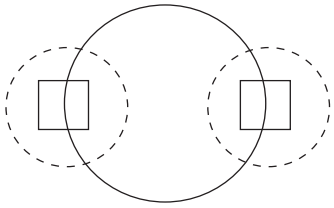


FIGURE 4. BEAM-SENSOR ALIGNMENT

DIGITAL INTERFACING

For systems with digital control, Figure 5 illustrates a method not requiring generation of bipolar control signals thus saving the cost of digital to analog conversion. When logic lines are low, the signal diodes will not conduct. This condition leaves control to the photodiodes. A high level on line 2 will cause current to flow to the summing junction and the amplifier will swing negative. A high level on line 1 will raise the summing junction voltage above ground, and the amplifier will swing positive. Select a resistance value such that a high logic level will provide at least twice the maximum current from each photodiode to insure control override regardless of photodiode signals.

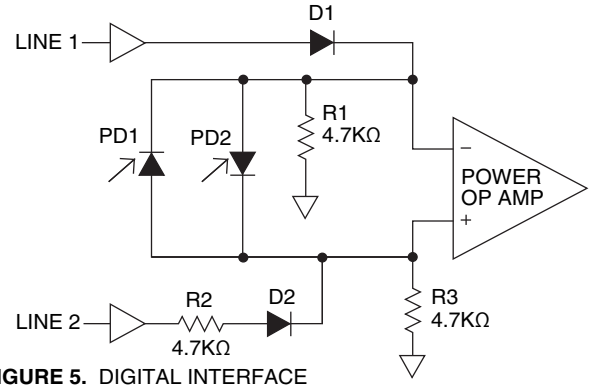


FIGURE 5. DIGITAL INTERFACE

DUAL SENSORS

For applications requiring high precision, the use of a dual element position sensing PD1 (Figure 5) will allow smaller beam size, tighter beam control and provide better thermal equilibrium. The specified resolution of the detector recommended for this application is better than .0127mm (.0005 inch). The detector is a three terminal device requiring a current inverter as shown in Figure 6 to achieve the differential configuration. Two equal resistors, R1 and R2, should be scaled to the maximum photodiode current and swing capability of the signal amplifier.

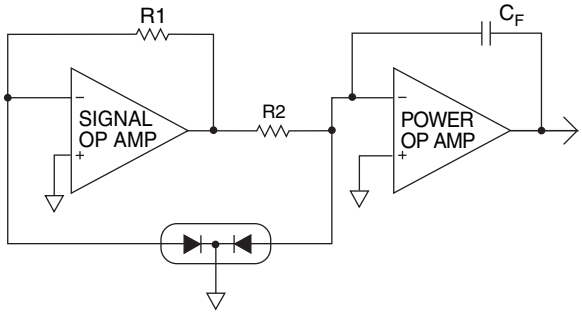


FIGURE 6. CURRENT INVERSION

Bridge Circuit Drives

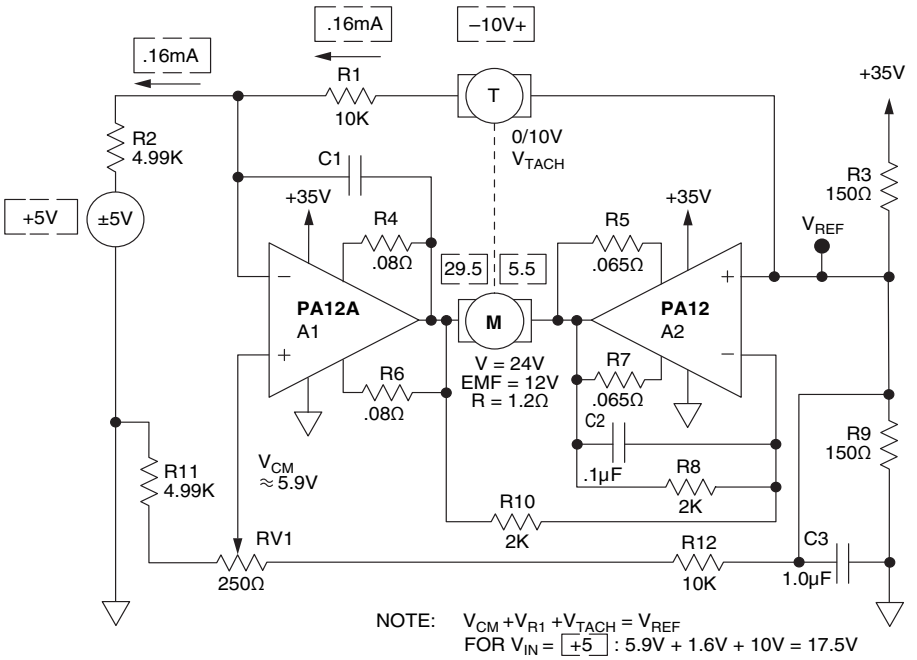


FIGURE 1. BI-DIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

INTRODUCTION

Two power op amps configured in a bridge circuit can provide substantial performance advantages:

1. Bi-directional output with a single supply
2. Twice the output voltage
3. Twice the slew rate
4. Twice the output power
5. Half the power supply requirement

Low current outputs can reach the kilovolt range or mulitple ampere outputs of hundreds of volts can be obtained. To achieve these levels of performance, both terminals of the load must be driven and extra components are required.

BI-DIRECTIONAL DRIVE ON A SINGLE SUPPLY

Figure 1 depicts a bi-directional motor speed control using a single supply which features ground referenced bipolar input signals. A mid-supply reference created by R3 and R9 establishes the DC operating levels for A1 and A2. Inverter A2 drives the load equally in the opposite direction with respect to the output of input amplifier A1. This configuration places both load terminals at the reference voltage with a zero input condition and prevents premature saturation of either amplifier.

To understand the operation of the circuit, consider A1 as having two sets of inputs:

1. Voltage dividers from the supply voltage to establish common mode bias.
2. Actual input signal and tachometer feedback.

One sixth of any supply voltage variation will appear equally at both inputs of the amplifier. However, the common mode rejection (CMR) of the op amp will reduce its response by four orders of magnitude at low frequencies. The low pass function of C3 insures optimum rejection by keeping the common mode inputs in the low frequency spectrum. The common mode voltage (CMV) range of the amplifier sets the minimum common mode bias at the inputs of A1. The circuit shown provides a nominal 5.9V from the supply rail (ground) which allows power supply variations to 10% below nominal.

For the actual input signal, C1, R1, R2, and A1 form an integrator (non-inverting input is constant). With the control voltage applied across R2 and the tachometer voltage applied across R1, integration forces the motor speed to be proportional to the input voltage. The value of C1 must be selected for proper damping of the total system which includes the mechanical characteristics of the drive train.

Resistors R4 and R6 set current limits of A1 to 7.5A. When A1 current limits, A2 will reduce its output voltage equal to the voltage change of A1. By insuring A1 will limit prior to A2, power stress levels of the two amplifiers are equalized. In addition to amplifier protection, this programmability is being utilized to limit the temperature rise in the motor, thereby increasing expected life of the system. Maximum continuous load rating of the motor shown is 10A and locked rotor (stall) current is 20A. Since locked rotor ratings generally refer to abnormal conditions, the motor is being used near capacity while maintaining a comfortable safety margin for motor and drive circuit.

The key to accuracy of this circuit lies in matching the division ratios from the reference voltage to ground for both the inverting and non-inverting inputs of A1. The inverting side division ratio is affected by the impedances of the control signal and tachometer. Normally, the impedance of a voltage output DAC and the winding impedance of the tachometer are negligible. This allows use of cost effective 1% resistors and requires only trimpot RV1 to provide precision adjustment.

Ratio match errors will appear as tachometer output errors. These errors will be of a size equal to the ratio of mismatch times the reference voltage.

The second major accuracy consideration of this circuit is the voltage offset of A1. As this error will appear at the tachometer at a gain of three, the PA12A was selected for its improved specification of 3mV compared to 6mV for the regular PA12.

Changes of input voltage range, RPM range or tachometer output ratings are easily accommodated. Lowering the values of R1 and R12 (ratio match still required) will re-scale smaller tachometer voltage spans or lower RPM ranges to the ±5V input level. While increased input signal levels could be re-scaled in the same manner, increasing R2 and R11 provides the required re-scaling with the added benefit of lowering control signal drive requirements.

Higher voltage tachometer voltage spans require a different approach to re-scaling due to the CMV limitations at the inputs of A1. Figure 2 illustrates a technique using a 25V tachometer which will maintain adequate CMV for A1 with supply voltages down to 20V. Calculations for the divide by five network at the tachometer includes winding impedance to achieve accurate scaling to the ±5 input signal. For error budgets, this factor of five must be applied to both the ratio mismatch errors and voltage offset errors as above. Total gain for calculating offset errors will be 10.

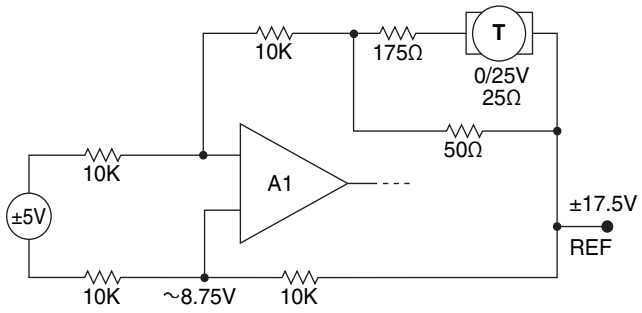


FIGURE 2. HIGH OUTPUT TACHOMETER

ELECTROSTATIC DEFLECTION

The cathode ray tube (CRT) shown in Figure 3 requires 500Vpp nominal drive. Allowing for a ±5% gain error plus a 10% (of full scale) centering voltage tolerance, brings the desired deflection voltage swing to 575Vpp. Two PA84 high voltage power op amps provide this differential voltage swing. Slew rates of 400 volts per microsecond at the CRT enable the beam to traverse the face plate in less than 1.5 microseconds.

The gain of A1 is set by (R3+RV1)/R1 at 100. The circuit provides for both gain adjustment (RV1) and beam centering (RV2). For proper scaling, R4 and R6 reduce the centering control voltage of trimpot RV2 to ±250mV. C2 provides the desired low AC impedance to ground to enhance stability and eliminate noise pickup. A2 inverts the output of A1 at unity gain (set by R8/R5), to yield an overall gain of 200 for single ended input signals measured at the differential output. R9 and C4 constitute a second input to A2 with an AC gain of 100 (R9/R8). Using ground as an input has no direct signal contribution, but it does allow both amplifiers to use the phase compensation recommended at a gain of 100 (20K, 50pF), thereby achieving a large power bandwidth of 250kHz.

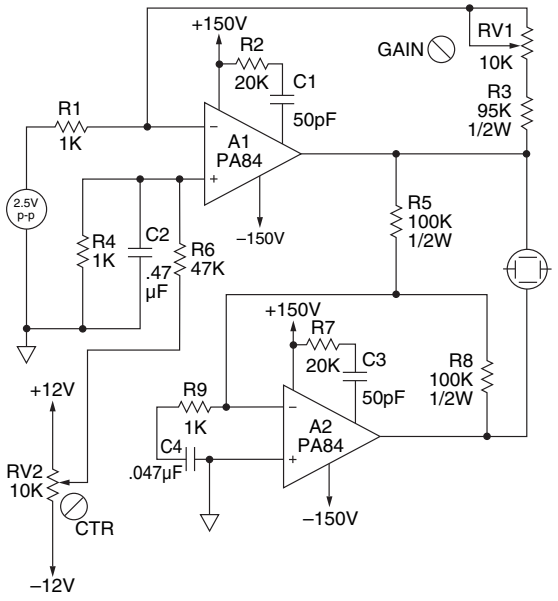


FIGURE 3. ELECTROSTATIC DEFLECTION AMPLIFIER

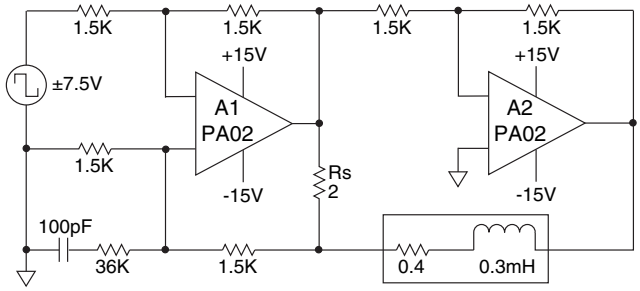


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

TRANSIMPEDANCE BRIDGE FOR MAGNETIC DEFLECTION

The circuit shown in Figure 4 drives the electro-magnetic deflection yoke of a precision x-y display. Two factors constitute the design challenge of this circuit:

1. Greater than 15V drive levels are required to change current magnitude and polarity to achieve fast endpoint-to-endpoint display transition times.
2. Only ±15V power supplies are available in the system.

The bridge circuit can drive almost double the single power supply voltage, thereby eliminating the need of separate supplies solely for CRT deflection. The maximum transition time between any two points is 100µs for display ratings of:

Yoke inductance = 0.3mH
Full scale current = ±3.75A
DC coil resistance = 0.4 ohms

The voltage required to change the current in an inductor is proportional to current change and inductance, but inversely proportional to transition time.

V = di*L/dt
V = 7.5A*0.3mH/100µs = 22.5V

The Apex Precision Power low voltage power op amp PA02 is an ideal choice for this circuit due to its high slew rate and ability to drive the load close to the supply rail. A1 in Figure 4

is configured as a Howland Current Pump. Voltage on the bottom of the sense resistor is applied directly to the load; voltage at the top is the applied voltage plus a voltage proportional to load current. With both these points for feedback, the amplifier sees a common function of load voltage on both inputs which it can reject (CMR), but sees a function of load current differentially. In this arrangement, A1 drives the load anywhere required (with in saturation limits) to achieve load current commanded by the input signal. As ratio match between the two feedback paths around A1 is critical, these four resistors are often implemented with a resistor network to achieve both precision match and tracking over temperature. A2 provides a gain of -1 to drive the opposite terminal of the coil. Gain setting resistors for A2 are not nearly as critical, a mismatch here simply means one amplifier works a little harder than the other. Starting values for the R-C compensation network come from the Apex Precision Power Power Design tool and are fine tuned with bench measurements.

A first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

In the middle graph of Figure 5, we find the large sense resistor does not destroy the circuit drive capability. The main portion of the transition is complete in about 80µs and settles nicely.

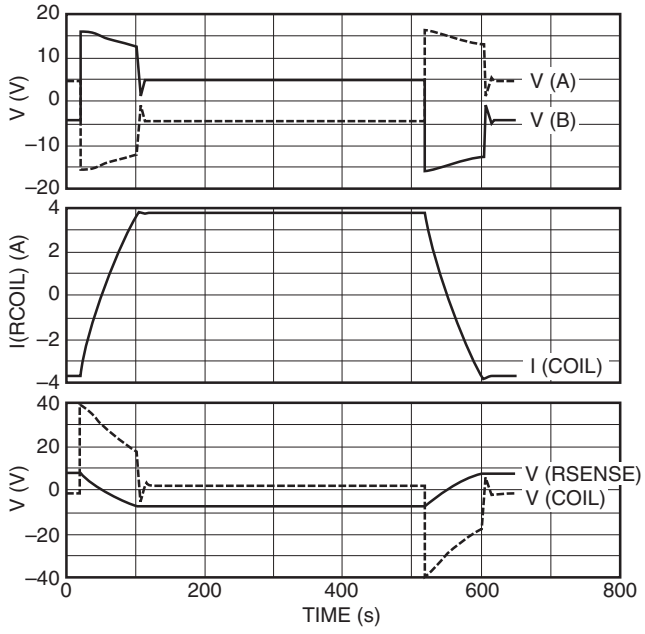


FIGURE 5. MAGNETIC DEFLECTION VOLTAGE AND CURRENT WAVEFORMS

In the top graph, we find a surprise; both amplifiers are actually swinging OUTSIDE their supply rails. The "upside down" topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

In the bottom graph, we find stored energy in the inductor develops voltage across the sense resistor, which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

EFFICIENT USE OF POWER SUPPLIES

To illustrate the advantages of the bridge circuit, Figures 6 and 7 show two high performance audio amplifier designs with equal output power, but substantially different supply requirements. In the circuit of Figure 6, the instantaneous load current will appear on only one supply rail. This means each supply rail must support the total wattage requirement and utilization is only 50% at peak outputs. In contrast, the equal and opposite drive characteristic of the bridge circuit shown in Figure 7 loads both positive and negative supply rails equally during each half cycle of the signal. This improved utilization reduces size, weight and cost of the power supply for the circuit in Figure 7 even though input and output power ratings are essentially equal.

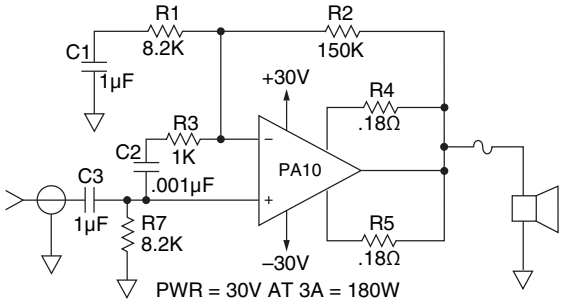


FIGURE 6. STANDARD AUDIO AMPLIFIER

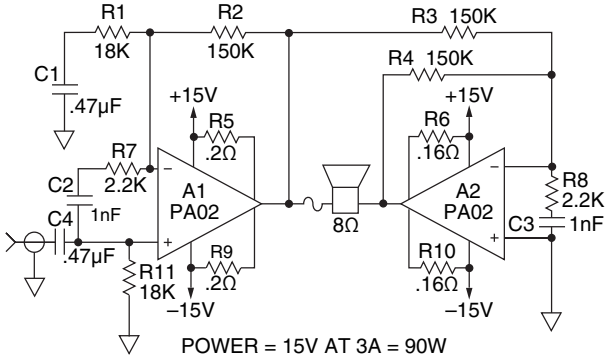


FIGURE 7. BRIDGE AUDIO AMPLIFIER

CONCLUSION

Bridge circuits can make the difference when performance requirements exceed voltage limitations of either the available power supplies or the power op amps. The input section of these circuits consists of a standard amplifier circuit for driving a single ended load. The added amplifier serves merely as an inverter. It doubles drive voltage by providing an equal and opposite output, thereby making the output fully differential. The performance increases usually outweigh the increased cost and complexity.

Precision Magnetic Deflection

INTRODUCTION

Closed loop power op amp circuits offer distinct advantages in current control over open loop systems. Using a power op amp in the conventional voltage to current conversion circuit, the negative feedback forces the coil current to stay exactly proportional to the control voltage. The resulting accuracy makes many new applications feasible. For example, by placing the non-linear impedance of the deflection yoke inside the feedback loop, steady state positioning, which is difficult, if not impossible, to achieve with open loop circuits, can easily be implemented with a power op amp. In addition, sweep systems with substantially improved linearity can be designed using power op amps.

Typical applications include: heads-up displays, which require random beam positioning or E-beam lithography; and other complex data displays which can achieve the needed accuracy with a power op amp. Moreover, the versatility and ease of use of power op amps will help speed up the design process while at the same time reducing development cost. The final result will be a more accurate and reliable display using fewer parts.

HIGH RESOLUTION AND HIGH EFFICIENCY

The vertical deflection circuit of Figure 1 was designed to drive a high efficiency RCA CODY II tube. The PA02 was selected for this configuration because of its exceptional linearity and other advantages such as high slew rate, fast settling time, low crossover distortion, and low internal losses. All of these advantages contribute to a superior resolution display.

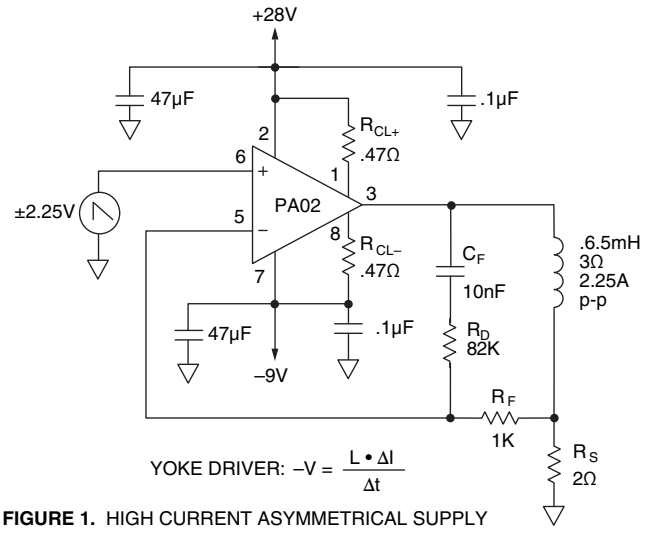


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

The key to this circuit is the sense resistor (R_S) which converts the yoke current to a voltage for op amp feedback. With the feedback applied to the inverting input and the position control voltage applied to the non-inverting input, the summing junction's virtual ground characteristic assures the voltage across R_S is equal to the input voltage. Thus, the highly linear control of the voltage across R_S insures accurate beam positioning.

The value assigned to R_S has significant impact on the circuit performance. All op amp input errors such as voltage offset, imperfect common mode rejection, offset drift, etc., will appear across the sense resistor, producing current errors. While it is easy to see large sense resistors minimize DC errors, it takes a little more study to realize they help dynamic response also. The R_S value is a major player in setting the loop gain of the circuit. Larger feedback voltages will result in noticeable improvements in power bandwidth and settling time. The limiting factors on raising R_S values are brought on by the fact that load current flows through them; voltage drive capability decreases; and power dissipation in this resistor increases.

Weighing these trade-offs between errors, bandwidth, and efficiency in the selection of R_S value will produce the optimum choice for each application. The voltage drive requirements will then be defined by inductance, transition times and current. This display must operate at 50Hz or 60Hz with retrace times of 730µs and coil currents of $2.25A_{P-P}$.

The drive voltage required to change the current in an inductor is proportional to both current change and inductance, but inversely proportional to transition time.

$$V_{DRIVE} = \Delta I * L/\Delta t \quad (1)$$
$$V_{DRIVE} = 2.25A_{P-P} * 6.5mH/15.93ms = .918V \quad (2)$$
$$V_{DRIVE} = 2.25A_{P-P} * 6.5mH/730\mu s = 20.03V \quad (3)$$

To determine the power supply levels, add the supply-to-output differential rating of the power op amp (from the Amplifier Data Sheet) and the voltage dropped across the combined values of the sense resistor plus the coil resistance, to these drive requirements to arrive at +28V and -9V as follows:

$$V_{DROP} = I_{PK} * (R_S + R_L) \quad (4)$$
$$V_{DROP} = 1.125A_{PK} * (2\Omega + 3\Omega) = 5.625V \quad (5)$$
$$V_S = V_{DRIVE} + (V_S - V_O) + V_{DROP} \quad (6)$$
$$V_S = .918V + 2V + 5.625V \cong 8.6V \quad \text{(sweep)} \quad (7)$$
$$V_S = 20.03V + 2V + 5.625V \cong 27.7V \quad \text{(retrace)} \quad (8)$$

Caution should be exercised when using asymmetric power supplies, because the inductive load has the potential to store energy from the higher supply. This could be initiated by an abnormal condition causing the high output voltage to remain on the yoke longer than the normal retrace time. After such an occurrence, the collapsing magnetic field would discharge the stored energy into the lower voltage supply via the inductive kickback protection diodes in the power op amp. This will produce a voltage transient on the supply rail with its amplitude a function of stored energy and the transient impedance of the power supply. If this transient added to the supply voltage exceeds the rail-to-rail voltage rating of the amplifier, the result will be destructive. In such cases, a zener clamp on the amplifier output should be used.

A note of caution when using modular construction. Instruction manuals always specify, **"power down first, then remove the module."** However, because this doesn't always happen, protective action should be taken. The mechanical break of the connection to any inductance, coil or wire, causes high voltage flyback pulses. The stored energy must be absorbed somewhere. It's much better to use the zener clamp than to risk the op amp.

STABILITY CONCERNS

Since the current control capabilities of this circuit rely on feedback from the current-to-voltage conversion sense resistor, phase shift due to the inductance of the yoke will be evident in the feedback signal. Because the phase shift approaches 90° on a perfect inductor and the phase margin of an op amp is always less than 90°, design adaptations are required to prevent oscillation.

The network consisting of R_D, R_F and C_F, serves to shift from a current feedback via R_S to a direct voltage feedback at the upper frequencies. This bypasses the extra phase shift caused by the inductor. In selecting component values for this network, R_F should be much larger than R_S, but should not exceed 1KΩ for the PA02, because the input capacitance of the op amp would otherwise add phase shift. In selecting values of R_D and C_F, start with values prescribed by the Apex Precision Power Power Design tool which will yield a stable circuit. Spice analysis and bench measurements will usually allow impedance of both these components to increase and speed up the circuit.

For an even more powerful version of this circuit, the PA10 power op amp can be used, as shown in Figure 2. With this device, a 7.8mH 4Ω coil can be driven at $5A_{P-P}$ with the same timing requirements. Calculations for this design are:

$$V_{DRIVE} = 5A_{P-P} * 7.8mH/15.93ms = 2.45V \quad (9)$$

$$V_{DRIVE} = 5A_{P-P} * 7.8mH/730\mu s = 53.43V \quad (10)$$

$$V_{DROP} = 2.5APK * (1\Omega + 4\Omega) = 12.5V \quad (11)$$

$$V_S = 2.45V + 6.5V + 12.5V \cong 21.5V \quad (sweep) \quad (12)$$

$$V_S = 53.43V + 6.5V + 12.5V \cong 72.5V \quad (retrace) \quad (13)$$

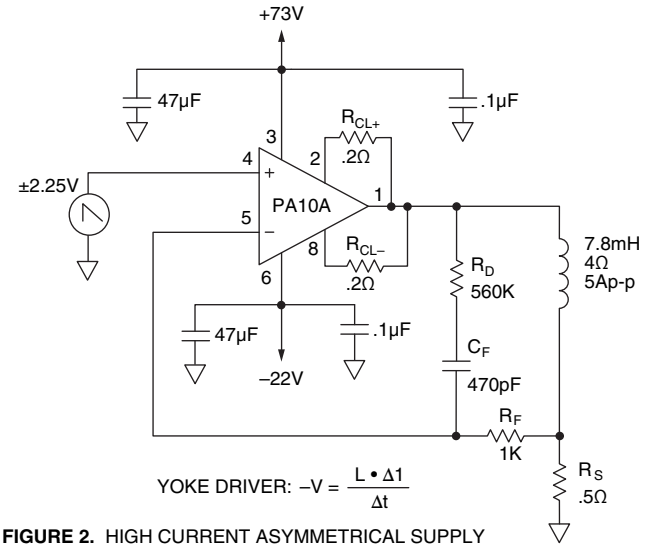


FIGURE 2. HIGH CURRENT ASYMMETRICAL SUPPLY

Both of the circuits illustrated have a 730µs retrace time requirement, met easily by the op amp's slew rate and settling time which is substantially faster.

To better understand this and other applications, Figure 3 illustrates input and output waveforms. Traces prior to time A, are the end of the sweep portion where current is changing at a relatively slow rate. The peak output voltage at time A is roughly the sum of equations 9 and 11.

Retracing begins at time A; the electron beam is turned off; and the amplifier starts running open loop because output current is not keeping up with the input command. Circuit slew rate is displayed between time A and time B where the output saturates. This slew rate is usually somewhat less than

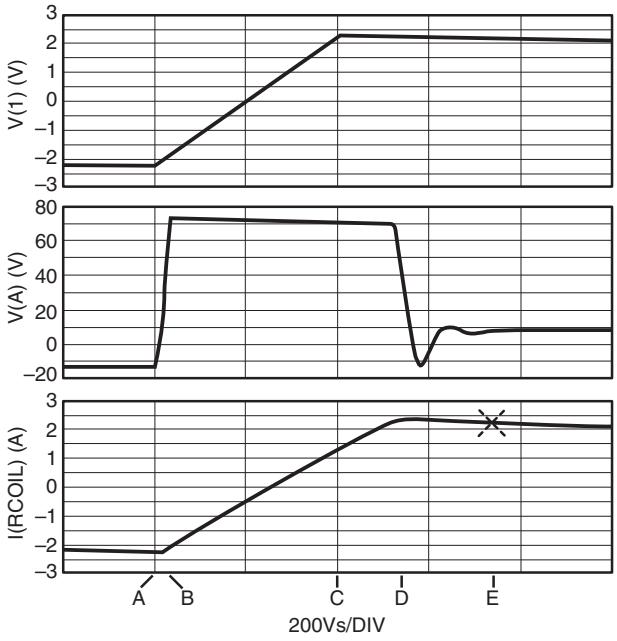


FIGURE 3. RETRACE WAVEFORMS

the amplifier rating because overdrive is small and the R_D/C_F network is a feedback path at the equivalent high frequency signal. At time C, the output current has caught up with the command signal, so the op amp begins closing the loop and settling. Time D is the end of the allotted retrace time and the electron beam is turned back on. Note the non-linearity of the current waveform between times C and D will not cause problems because of this timing.

Note that we calculated a supply voltage requirement of about 73V to change current 5A in 730µs, but most of this change takes place in about 550µs. The first thing making this possible is shown in the amplifier output voltage trace of Figure 3, where saturation voltage of the amplifier is much better than the 6.5V level of the calculations. At time B, current is still flowing through the negative side output transistor, NOT the positive side. The stored energy in the inductor is actually helping the op amp swing closer to the rail. A second factor helping reduce current slew time is again related to stored energy. From time B until current reaches zero, voltage developed across the sense resistor adds to the op amp voltage rather than subtracting from it. Spice analysis indicates peak voltage across the coil at time B is 74.6V.

If a circuit does not include offset and amplitude adjustment capability, the positive peak of the input signal needs to be increased by an amount equal to the normal current change between the actual input peak and time D. From Figure 3 this would be about 5A/15.93ms * .32ms ≅ 0.1A, or 2.35_{VPK} input.

When evaluating slew rates of potential amplifiers for these circuits, note that the amplifier is required to swing nearly twice the peak-to-peak output in a small fraction of the total retrace time. In this example, voltage slewing time was about 10% of the retrace time.

Both the PA02 used in Figure 1, and the PA10 used in Figure 2, have raised accuracy levels by placing the non-linear inductive element inside the op amp feedback loop. The very high gain of the op amp and the use of negative feedback produces superior linearity.

RAPID TRANSITION FOR HEADS-UP DISPLAY

Heads-up displays demand swift transition between any two points on the screen. The waveforms of Figure 4 depict the input drive voltage and required current to the yoke to achieve a single full-scale step in beam position for the circuit in Figure 5. The 3V levels sustain the steady state current through the coil resistance and the sense resistors. The 29V level corresponds to the peak output voltage required for a position change.

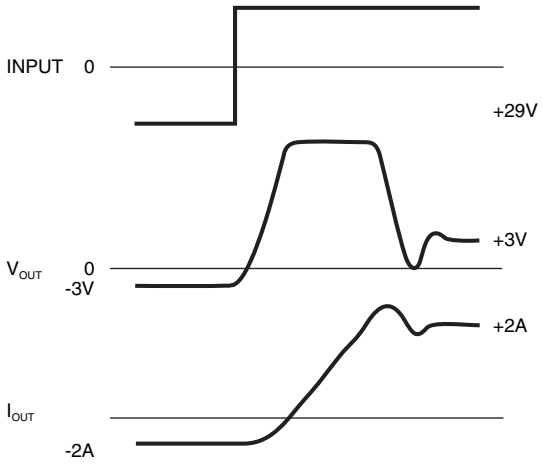


FIGURE 4. FULL SCALE STEP FUNCTION WAVEFORMS

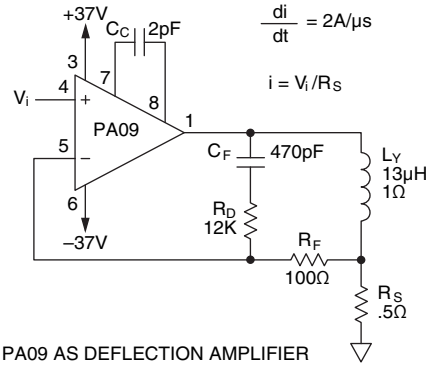


FIGURE 5. PA09 AS DEFLECTION AMPLIFIER

Starting with amplifier slew rates and settling times from the data sheet, it is determined what percentage of the total transition time will be required for slewing and settling. A reasonable starting point would be to allow 50% of the total transition time.

This circuit was designed for a maximum transition time of 4µs when delivering $2A_{PK}$ currents to the 13µH coil. While the fundamentals of this circuit are the same as previously detailed, there are differences due to the higher speed. To achieve rapid transitions, amplifier slew rates must be optimized. As a rule of thumb, compensation for this type circuit should not be lighter than that specified for a gain of 100. Again, the Power Design tool will help selecting values for R_D and C_F. With high speed circuits, it is even more important to analyze performance on the bench to insure parasitics don't spoil the circuit.

If 50% of the total transition time is allowed for slewing and settling, 2µs will remain to change the yoke current with full voltage applied to the coil. Voltage requirements are calculated as follows:

$$V = di^* L/dt \quad (14)$$
$$V = 4A^*13\mu H/2\mu s = 26V \quad (15)$$
$$V_{DROP} = 2A^* (.5\Omega + 1\Omega) = 3V \quad (16)$$
$$V_{DRIVE} = 26V + 3V = 29V \quad (17)$$
$$V_S = 29V + 8V = 37V \quad (18)$$

With the external compensation selected, the PA09 Data Sheet indicates the amplifier slew rate will be 400V per microsecond. For a calculated swing of 58V, the required voltage slewing time is 145 nanoseconds. Adding the settling time to 0.01% of 1.2µs, the total is comfortably below the 50% allotment of 2 microseconds.

When the circuit was tested, values were further optimized for best performance. The value of R_D had a considerable effect on damping of the circuit. This could be predicted because R_D affects the corner frequency where the roll off slope must be flattened near the unity gain point. The value of C_F was not critical; however, a compensation capacitor of 2pF, as opposed to the data sheet recommendation of 5pF, helped to increase the slew rate without significant affect on stability.

Due to the high speed of PA09, specific precautions are recommended to insure that optimum stability and accuracy are maintained:

1. To help prevent current feedback, use single point grounding for the entire circuit or utilize a solid ground plane.
2. To insure adequate decoupling at high frequency, bypass each power supply with a tantalum capacitor of at least 10µF per ampere of load current, plus a .47µF ceramic capacitor connected in parallel. The ceramic capacitors should be connected directly between each of the two amplifier supply pins and the ground plane. The larger capacitors should be situated as close as possible.
3. Use short leads to minimize trace capacitance at the input pins. Input impedances of 500Ω or less combined with the PA09 input capacitance of approximately 6pF will maintain low phase shift and promote stability and accuracy.
4. The output leads should also be kept as short as possible. In the video frequency range, even a few inches of wire have significant inductance, thereby raising the interconnection impedance and limiting the output slew rate. Also, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.
5. The amplifier case must be connected to an AC ground (signal common). Even though it is isolated, it can act as an antenna in the video frequency range and cause errors or even oscillation.

TRANSIMPEDANCE BRIDGE FOR HIGHER DRIVE VOLTAGE

The circuit illustrated in Figure 6 drives the deflection yoke of a precision x-y display from an available ±15V supply. Only the bridge configuration can provide the high voltage drive levels required with the power supplies available. This enables the system to drive double the single amplifier output voltage. Consequently, the need for separate power supplies solely for CRT deflection is eliminated.

A1 in Figure 6 (next page) is configured as a Howland Current Pump. Voltage on the bottom of the sense resistor is applied directly to the load; voltage at the top is the applied voltage plus a voltage proportional to load current. With both these points for feedback, the amplifier sees a common

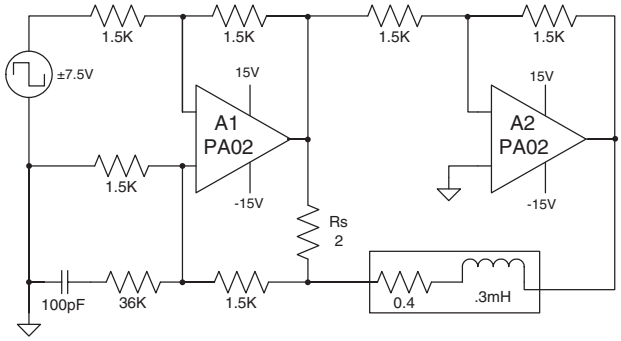


FIGURE 6. CURRENT-OUT BRIDGE DRIVE

function of load voltage on both inputs which it can reject (CMR), but sees a function of load current differentially. In this arrangement, A1 drives the load anywhere required (with in saturation limits) to achieve load current commanded by the input signal. As ratio match between the two feedback paths around A1 is critical, these four resistors are often implemented with a resistor network to achieve both precision match and tracking over temperature. A2 provides a gain of -1 to drive the opposite terminal of the coil. Gain setting resistors for A2 are not nearly as critical, a mismatch here simply means one amplifier works a little harder than the other. The PA02 brings a unique combination of high slew rate and low saturation voltage to this circuit. Starting values for the R-C compensation network come from Power Design and are fine tuned with bench measurements.

At first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.

Voltage across the inductor required to move the beam is given by:

$$V_L = 300\mu H * 7.5A / 100\mu s = 22.5V \quad (19)$$

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

In the middle graph of Figure 7, we find the large sense resistor does not destroy the circuit drive capability. The main portion of the transition is complete in about 80µs and settles nicely.

In the top graph, we find a surprise; both amplifiers are actually swinging OUTSIDE their supply rails. The "upside down" topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

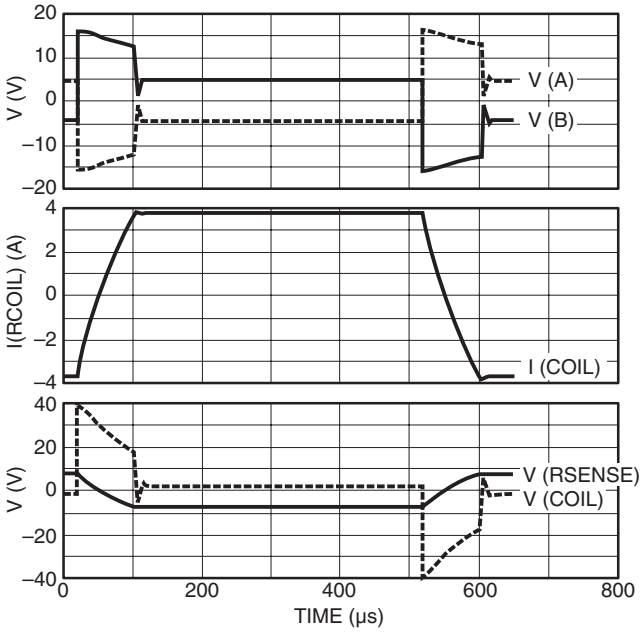


FIGURE 7. BRIDGE DRIVE CURRENTS AND VOLTAGES

In the bottom graph, we find stored energy in the inductor develops voltage across the sense resistor, which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

CONCLUSION

The capabilities of the power op amp provide higher accuracy levels, the ability to position beams in any desired position and to retain a steady state position. Having both the power and signals stage in one compact package offers space/weight advantages. The lower parts count increase reliability.

Power op amps are comparatively inexpensive and easy to use. They represent the most efficient solution to reducing development costs and decreasing design time.

Applying The Super Power PA03

INTRODUCTION

The super power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal op amps. Thus, this new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or in bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits, are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (Apex Precision Power PA12), while available monolithic IC's handle less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output: (1) parallel or bridge operation of two or more power op amps; (2) external booster transistors; (3) modular or rack mount power op amps.

While these options extend power capabilities, they can have major drawbacks in increased cost, excessive weight and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable power op amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the super power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful op amp (Apex Precision Power PA12) by a factor of four, and one PA03 is more cost effective and far more reliable than four less powerful op amps. Its thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. Moreover, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for power op amps. The common collector complementary output stage allows the output to swing within 4V of the supply rail at 12A and within 6V at 30A and has full shut-down control. This gives the designer a tool to protect sensitive loads or to minimize power consumption under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

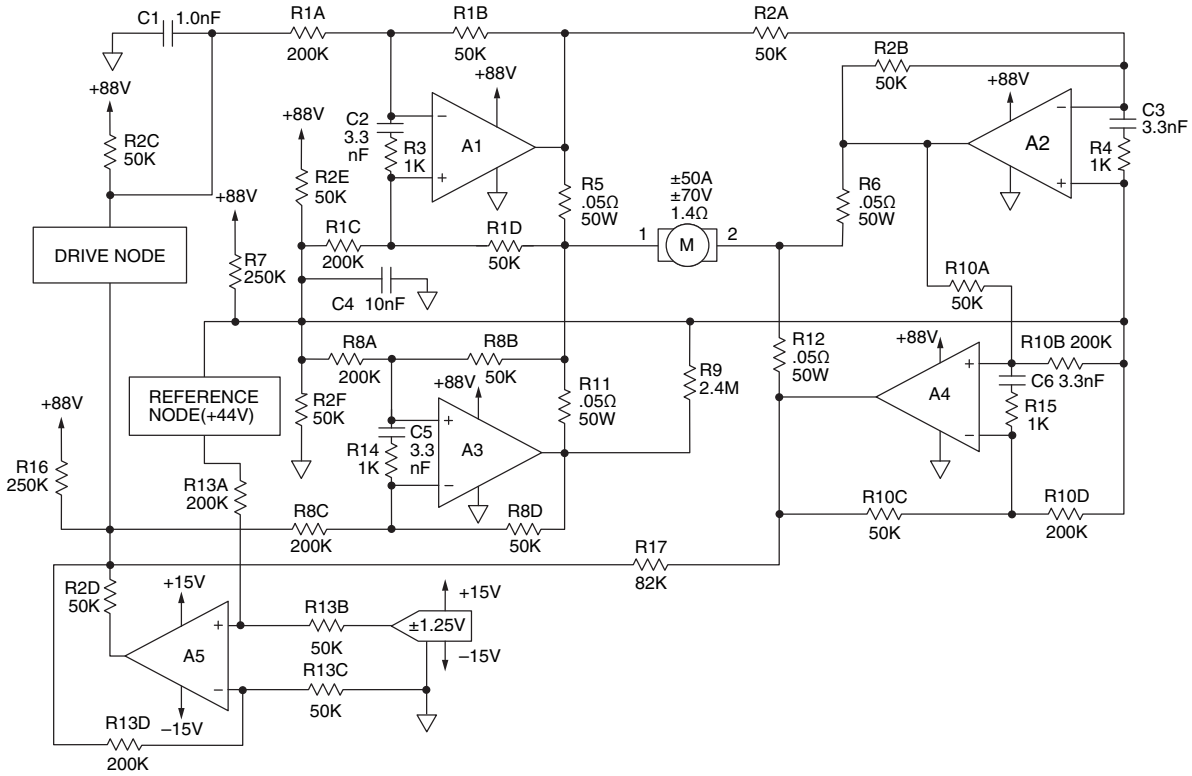


FIGURE 1. APPLYING THE SUPER POWER PA03

An external balance control option allows the already low offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes; to build long time period integrators; or to design 12 bit and better resolution programmable power supplies.

The super power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity, and three times the area of the conventional steel TO-3 package.

A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power levels again by increasing the current drive capability. Delete A3 and A4, and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

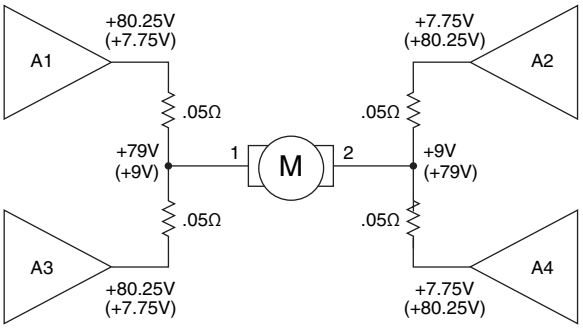


FIGURE 2. FULL SCALE DRIVE VOLTAGES

A5 (Figure 1) configured as a level shifter at a gain of 4, takes the 1.25V input from the DAC and swings the drive node to ±5V with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a ±25A output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share the total 50A current equally.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks, but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and R13B will match the current through R7. The voltages applied to R1, R8, R9, and R10 will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and R13B to the +1.25V DAC input. R10A, R10B, R10C, and R10D current will nearly match the currents of R1C and R1D plus R8A and R8B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

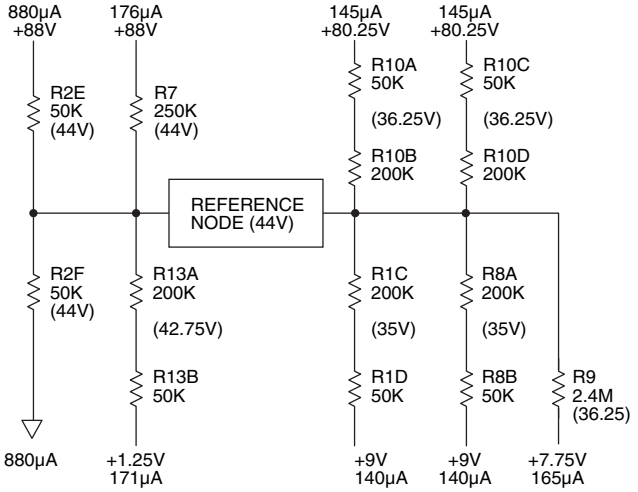


FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE

Figure 4 illustrates currents associated with the drive node where R2C and R2D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1 and R8, and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and R2D balance. The currents in R16 balance the currents of R13C and R13D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16, R13C and R13D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and R1B, plus R8C and R8D, make the node even less balanced. R17 was selected to slightly over compensate the current imbalance. Since the differential circuit of A5 (Figure 1)

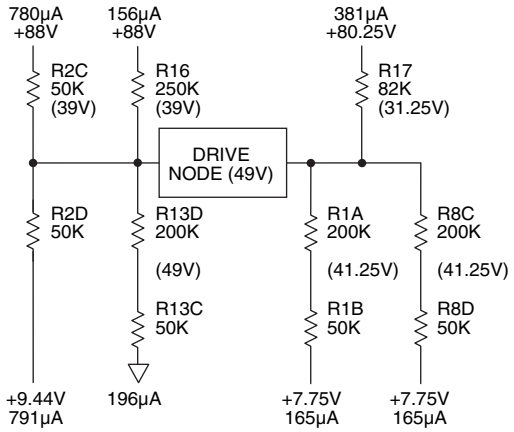


FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE

controls drive node voltage, its nominal swing will be a 9.44V, correcting the overall current imbalance of 12µA. Thus the overcompensation of R17 insures A5 will not be required to swing beyond its rated 10V due to component tolerances.

There are a lot of resistor networks in the circuit, but each has a critical task. The ratios are most important to insure gain accuracy. In addition, ratio matching provides common mode rejection and differential voltage amplification. Specifically, the R13 quad around A5 sets drive node swing to +5V with respect to the reference voltage even though the reference changes with supply variations. Similarly, the R1 quad and the R8 quad set the full scale voltage across sense resistors R5 and R11 at ±1.25V. The ±35V output swings across the impedance of the torque motor are rejected as a common mode signal to maintain the programmed voltage to current transfer function. Thus impedance variations of the motor winding and the associated connections do not affect accuracy. R10 fixes the gain of A4 to unity while keeping its input pins about 4V closer to the reference than the amplifier's output voltage. With the output swinging to within nearly 7V of the supply rails, the common mode voltage requirement of ±Vs –10V is satisfied.

A PROGRAMMABLE POWER SUPPLY USING THE PA03

Figure 5 shows the PA03 in a simple, reliable programmable power supply which utilizes the PA03's shutdown features. It requires little calibration because the current to voltage conversion of the D to A converter output is done by the power op amp itself, and the 12 bit DAC80 provides accuracy levels high enough to eliminate the need for adjustments.

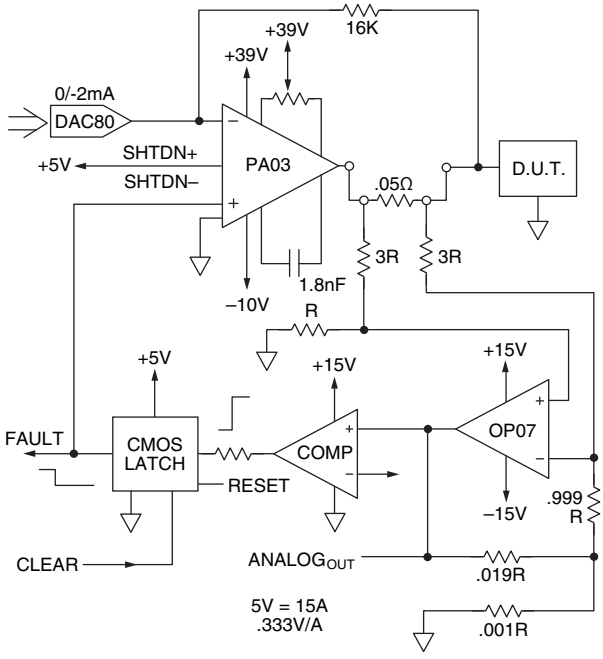


FIGURE 5. HI-POWER PROGRAMMABLE POWER SUPPLY APPLICATION

The programmable power supply is designed to test DC-to-DC converter modules drawing up to 15A. The majority of tests are performed at 28V. High and low limits of 18.5V and 32V will be applied for 500ms. The outputs must be accurate to within 0.5% and survive an occasional short circuit to ground.

The OP07 differential amplifier circuit senses the D.U.T. current on the four-terminal shunt resistor, and provides a signal of 0.333V/A to the comparator. The comparator will trip at a current of 18A, setting the latch, and the latch then shuts down the PA03 until the fault is cleared and the latch is reset. This safety circuit limits arcing hazards in the test socket.

The feedback resistor of 16KΩ yields the required 32V full-scale output when the DAC output is 2mA. The 0.05Ω current sense resistor develops a 0.75V signal at the full-scale output current of 15A. This amplitude is a compromise between monitoring the current accurately without imposing an excessively high power rating on the sense resistor. However, the sense resistor still must be mounted on a heatsink due to 11.25W dissipation at 15A and the possible 88W at the built-in maximum current limit of 42A.

To derive the power supply voltage needed, the 0.75V drop on the sense resistor must be added to the headroom (supply-to-output differential) required by the op amp. From the PA03 specifications (a drop of 7V at 30A and 5V at 12A), a maximum drop of 6V at 15A can safely be assumed. Selecting a positive voltage of 39V leaves a margin of 0.25V. Without remote sensing, such a conservative approach is best due to potential IR drops in the high current leads. For the negative supply, a minimum operating voltage of 10V is required to satisfy the input common mode voltage specifications.

Four power levels must be examined to determine the worst case maximum power dissipation of the power op amp. The first three are the output voltage levels for the devices under test at the maximum current of 15A. Calculating all three shows the 18.5V output to be the worst case scenario. The 18.5V output plus the 0.75V drop across the sense resistor leaves a voltage of 19.75V across the output stage of the PA03. At 15A, this produces an internal power dissipation (including quiescent power of 9.8W) of 306W and a junction to case temperature rise of 92°C (PA03 =0.3°C/W).

Because the worst case power demand exists only for 500ms, an examination of average power and thermal time constants will help to reduce the heatsink size. Figure 6 shows the general test plan and the specific testing sequence with the resulting power dissipation levels demanded of the PA03. The 32V output level requires 103.6W (39V supply less 32V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for 500ms. The 28V level amounts to 163.6W (39V supply less 28V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for another 500ms.

For the balance of the test of 4.5s, the maximum current of

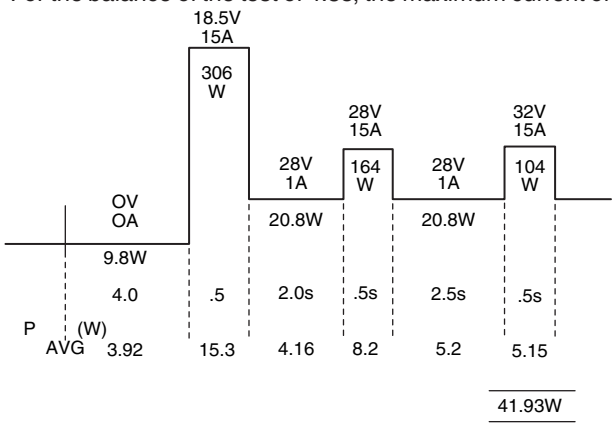


FIGURE 6. PROGRAMMABLE POWER SUPPLY INTERNAL POWER DISSIPATION

1A amounts to 20.8W. During the minimum removal/insertion time of 4s, the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C– 38°C– 92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The Apex Precision Power HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor (R_S) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms second breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the power op amp for the time required to eliminate the short.

REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a 40 Ft dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittent operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the noninverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions. R2 acts as a damping element limiting the integration time constant to minimize overshoot.

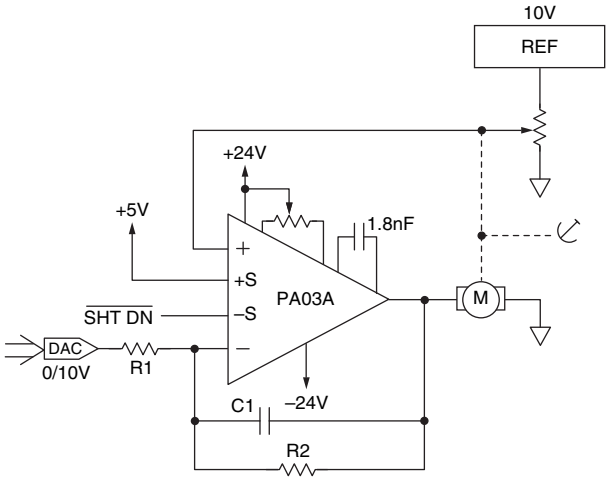


FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for 54 seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions, up to 17A may be drawn. In this application, the amplifier output will be decaying pulse; thus driving the motor to a new position once a minute. Because the amplifier is at maximum output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail) dissipation of 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45°C and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink as follows:

Q_{HS}= 95/103.1– 0.3 = 0.62°/W.

The Apex Precision Power HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

P_{AV} = 0.1 (24*8+48*0.2) +0.9 (48 *0.040) = 22W

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as ±75V and asymmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltage due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°C/W is often required such as: very large surfaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring of electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must

be bypassed with a ceramic capacitor of 0.47µF or greater, in parallel with a 10µF per ampere of peak output current (up to 300µF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

WATCH THE POWER DISSIPATION

The internal power dissipation (P) in a DC circuit is:

$$P = (V_S - V_O)\, I_O + (|+V_S| + |-V_S|)\, I_Q$$

where: I_O: OUTPUT CURRENT
I_Q: QUIESCENT CURRENT
V_O: OUTPUT VOLTAGE
V_S: SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage (V_S) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the power dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct power dissipation (P):

$$P = P_I - P_O$$

where: P_I = POWER DRAWN FROM THE POWER SUPPLY
P_O = POWER DELIVERED TO THE LOAD

Keep in mind that using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

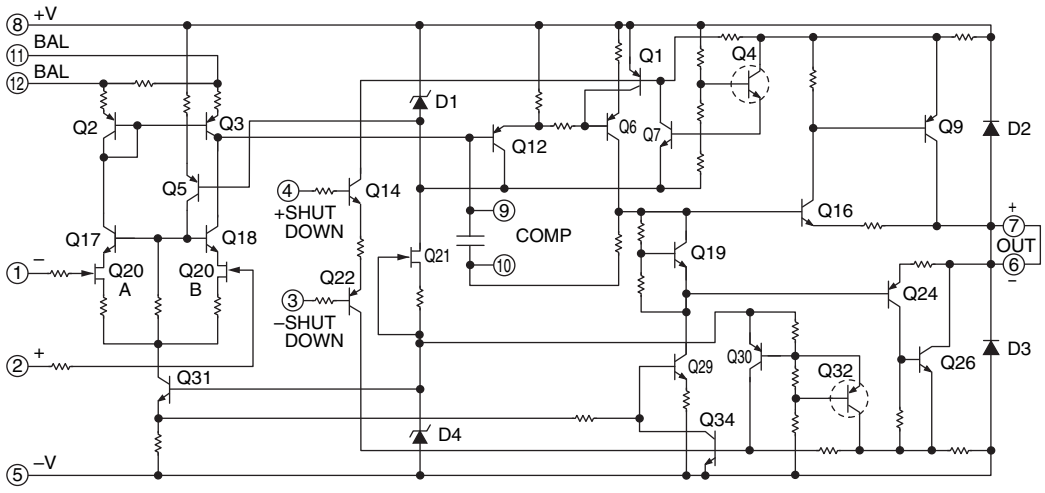


FIGURE 8. PA03 EQUIVALENT SCHEMATIC

JUNCTION TEMPERATURES

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure. This assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature (T_A) of the application known, the operating temperatures of both case (T_C) and junction (T_J) of the power transistors can be determined:

$$T_C = T_A + P \bullet \Theta_{HS}$$

where: Θ_{HS} = THERMAL RESISTANCE FROM THE HEATSINK MOUNTING SURFACE TO AMBIENT AIR
Θ_{JS} = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum internal power dissipation (P).
2. Determine the maximum junction temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. Apex Precision Power recommends 150°C or less.
3. Calculate $T_J - T_A$, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink:

$$\Theta_{HS} = (T_J - T_A)/P - \Theta_{JC}$$

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

$$\Theta_{HS} = (150 - 30)/300 - 0.3 = 0.1°C/W$$

HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most Apex Precision Power FET input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and Q20B (the FET input pair), Q17 and Q18 (the cascode transistors), and Q2 and Q3 (the half dynamic load). The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24, and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close to the supply rails. Inverters Q16 and Q24, form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The V_{BE} multiplier Q19, provides DC bias for the output transistors via Q16 and Q24, and is thermally coupled to the power dissipating transistors in the output stage. In addition, the V_{BE} multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A/B stage provides low crossover distortion, as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts, thereby turning on Q1 or Q34. In turn, these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

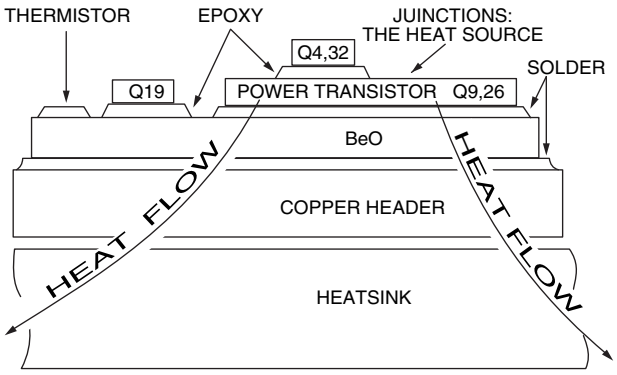


FIGURE 9. THERMO-MECHANICAL DESIGN

CONCLUSION

The PA03 is a versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Programmable Power Supplies

INTRODUCTION

The programmable power supply (PPS) is not only a key element in automated test equipment, but it is also used in fields as diverse as industrial controls, scientific research and vehicular controls. When coupled to a computer, it bridges the gap from the software to the control task at hand. This application note examines the basic operation of the PPS, the multitude of possible configurations and the key accuracy considerations.

VOLTAGE OUTPUT VERSIONS

The most basic and often most accurate version of the PPS requires only a current output Digital to Analog Converter (DAC), a power op amp and a feedback resistor as illustrated in Figure 1. According to op amp theory, the voltage at the inverting input (summing junction) will be zero and op amp input current will be zero. As a result, all current from the DAC flows through the feedback resistor R_F. Ohm's law then causes the circuit to provide a precise output voltage as function of DAC output current. Given a perfect DAC and feedback resistor, only two op amp parameters contribute significantly to the output voltage errors. These are voltage offset (V_{OS}), modeled by the battery, and bias current (I_B), represented by the current source. Due to the high output impedance of the current output DAC in relation to R_F, V_{OS} errors appear at the output without gain.

For a 10V output and op amp offset of 5mV, this error contributes only 0.05%. For a 100V output, a 0.5mV offset

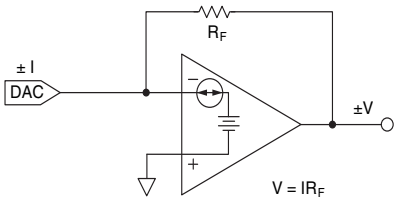


FIGURE 1. CURRENT TO VOLT CONVERSION

contributes an error of only 5ppm. Clearly, the DAC can easily be the major error source.

Op amp bias currents add to the DAC output current. The majority of available DAC's have full scale currents of ±1mA or 0/2mA. Most of today's bipolar input power op amps feature bias currents of less than 50nA. This results in errors of only 25 ppm maximum of the full scale range (FSR). FET input bias currents at 25°C are seldom over 100 pA and are specified as low as 10pA. These errors translate to 0.05ppm and 0.005 ppm. Since FET bias currents are generally characterized as doubling every 10°C, the bias current of the two examples could become 100nA and 10nA at 125°C, producing errors of 50ppm and 5.4ppm, respectively. Again,the DAC is the critical error source.

To determine the significance of the error contribution of a specific power op amp to the performance of various systems, refer to Table 1, next page. The least significant bit (LSB) is the value of the smallest step change of output. Comparing the calculated errors to the LSB values reveals system compatibility. For current output, DACs op amp bias currents compare directly with the DAC current LSB and V_{OS} errors compare directly with the full scale output voltage. Thus, the importance of low bias currents is dependent solely on system resolution. However, the significance of voltage offset specifications varies with both resolution and full scale voltage range.

USING VOLTAGE OUTPUT DACS

When using a voltage output DAC, the power op amp can be added with either inverting or non-inverting gain to form the PPS. It usually costs more than implementation with a current output DAC, and has less accuracy. However, system or logistic factors may dictate the use of the voltage output DAC.

Figure 2 illustrates the basic inverting gain version and Figure 3 shows a non-inverting setup. Error calculations are still simple even though some new variables have been added. Voltage offset errors appear at the output multiplied by the gain of the circuit (A_V+1 for inverting circuits). To maximize accuracy, the highest output DAC's should be used with minimum voltage gains in the op amp configuration. When using ±10V DAC's, a direct Vos to LSB comparison can be made using the 20V FSR values listed in Table 1. Also, bias currents flow through the feedback resistor producing output voltage errors; thus, values of R_F and R_{IN} are usually kept as low as possible.

A CASE FOR REMOTE SENSING

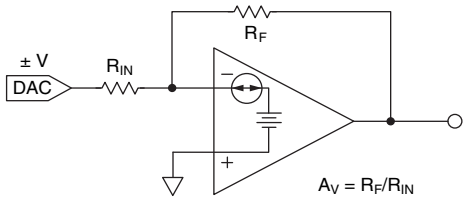


FIGURE 2. INVERTING VOLTAGE GAIN

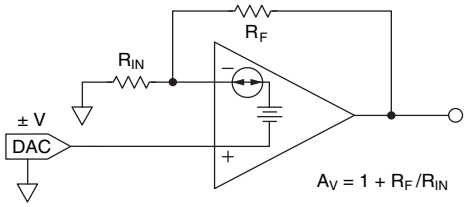


FIGURE 3. NON-INVERTING VOLTAGE GAIN

The circuit of Figure 4 shows the wire resistance (R_W) from the power op amp to the load and back to the local ground via the power return line. A 5A load current across only 0.05Ω

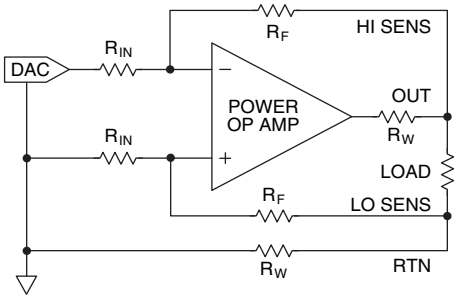


FIGURE 4. REMOTE SENSING PROGRAMMABLE POWER SUPPLY

in each line would produce a 0.5V IR drop. Without remote sensing, this would become an error at the load. With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop; therefore, as long as the power op amp has the voltage drive capability to overcome the IR losses, accuracy remains high.

CURRENT OUTPUT VERSIONS

A current output PPS using a current output DAC can be implemented as shown in Figure 5. Another version of the current output PPS is shown in Figure 6. This allows the load to be grounded, but is more complex and has additional errors. Especially if the output currents are relatively low, the current through the lower R_F/R_{IN} pair may become significant because it is also sensed by R_S. Major errors can be caused by ratio mismatching between the R_F/R_{IN} pairs. The resulting voltage errors across the sense resistor equal the output voltage times the ratio mismatch. For example, consider a 0.2Ω sense resistor, a 5A output requiring a 20V drive and a ratio mismatch of only 0.1% causes an error of 2%. Even an 8-bit LSB is only 0.39%!

In all of the current output circuits discussed, errors due to voltage offset appear across the sense resistor at a gain

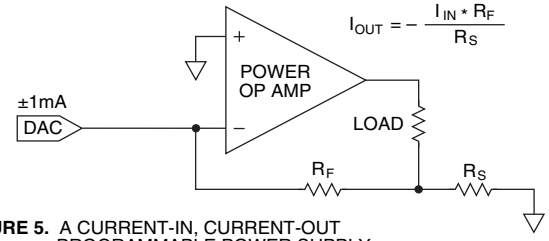


FIGURE 5. A CURRENT-IN, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

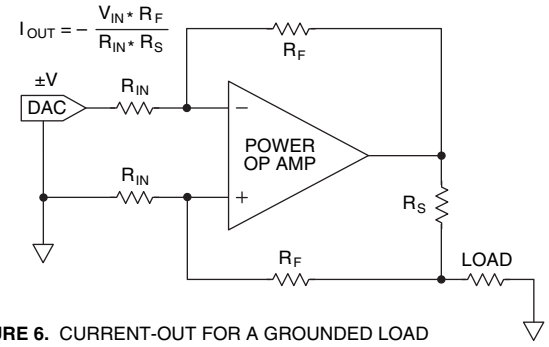


FIGURE 6. CURRENT-OUT FOR A GROUNDED LOAD

of one or more. This means higher sense resistor values will minimize output current errors at the expense of increased power dissipation in R_S, the power op amp and system power supplies. One other word of caution, if the load contains inductive elements, refer to Applications Note 5 which discusses maintaining stability in precision current output circuits having reactive loads such as deflection coils. A current output PPS using a voltage output DAC is shown in Figure 7. The power op amp drives current through the load until voltage on the sense resistor (R_S) equals the input voltage. To achieve high efficiency (low voltage across R_S compared to the load voltage), this circuit requires a low voltage DAC or a high voltage op amp. If neither is possible, the circuit of Figure 8 allows the sense resistor voltage drop to be lower than the input voltage.

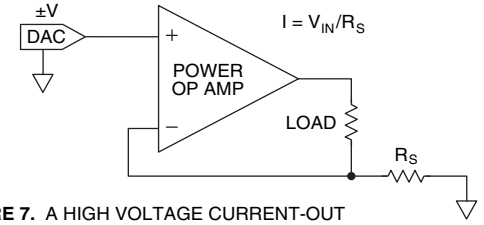


FIGURE 7. A HIGH VOLTAGE CURRENT-OUT PROGRAMMABLE SUPPLY

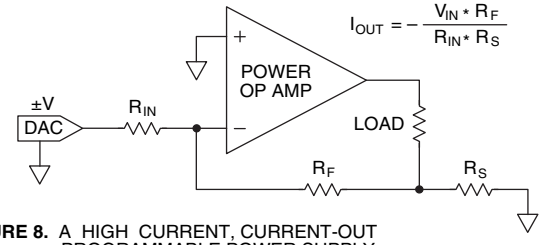


FIGURE 8. A HIGH CURRENT, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

PROGRAMMABLE ACTIVE LOADS

To obtain the V-I characteristics of a power source, it may be desirable to control the output voltage and measure the output current or visa versa. The current output circuits shown are suitable as active current loads. The circuit of Figure 9 performs voltage loading of a solar cell panel. The power op amp forces the DAC voltage to appear across the panel and also performs an I to V conversion providing the data to plot V-I characteristics.

Due to its flexibility, accuracy and ease of use, the power op

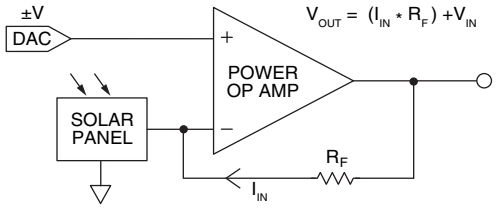


FIGURE 9. SOLAR PANEL TESTER

amp is the leading choice when programmable power supplies are called for. They greatly simplify circuits requiring unipolar outputs and are very cost effective when designing bipolar power supplies. The only remaining question is whether to buy the power op amp or to make one in discrete form. For low quantity production runs, the required design effort renders the "make" option too expensive. For high volume runs, the question is more involved. In many applications, the smaller size and lower weight plus high reliability, make the "buy" decision the only reasonable choice. (See "The Advantages of IC power op amps.") In all applications, the hybrid power op amp enhances design quality, speeds assembly and reduces overhead costs.

FULL SCALE RANGE					
BITS	PPM	2mA	20V	50V	200V
8	3906	7.8µA	78mV	195mV	.78V
10	977	1.95µA	19.5mV	48.8mV	195mV
12	244	488nA	4.88mV	12.2mV	48.8mV
14	61	122nA	1.22mV	3.05mV	12.2mV
16	15.3	30.5nA	305µV	.763mV	3.05mV

TABLE 1. LSB VALUES FOR VARIOUS OUTPUT LEVELS

Optimizing Output Power

THE MODERN POWER OP AMP

Power op amps are attractive because they reduce circuit design time enormously. Assembly costs of the power op amp design amount to a fraction of the discrete counterpart due to vastly reduced parts count. Careful attention to the power aspects of a circuit is required, as the well known op amp design rules based on low power devices. The objectives are to maximize reliability plus optimize output power and system efficiency. This application note points out some optimizing techniques and some areas to be especially watchful.

INTERPRETING SPECIFICATIONS

The first step in achieving high power levels is to operate within specifications. This means check the data sheet first. Apex Precision Power data sheets are divided into product description, absolute maximum ratings, specification table, typical performance graphs, and application hints. Each section should be checked for relevant information.

Absolute maximum ratings are stress levels which, when applied to the amplifier one at a time, will not cause permanent damage. However, proper operation is only guaranteed over the ranges listed in the specifications table. For example, most amplifiers have an absolute maximum case temperature range of –55°C to 125°C. If the specified operating temperature range is less, i.e. –25°C to 85°C, an amplifier may latch to one of its supply rails when operating above that temperature (+85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area. Simultaneous application of two or more of these maximum stress levels, such as maximum power and temperature, may induce permanent damage to the amplifier.

The generally accepted industry method of specifying absolute maximum power dissipation assumes the case temperature is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick to compare ratings of various manufacturers. However, it is not a reliable operating point. An ideal heatsink is required, and even with the best heatsink, it would still result in reduced product life due to operation at extreme temperatures. Apex Precision Power recommends maximum junction temperature of 150° or less.

The specifications table should be the prime working document while designing the application. In addition to the minimum/maximum parameters (voltage offset, output capability, etc.), this table contains the guaranteed linear operating ranges: common mode voltage, temperature ranges, power supplies, etc.

Typical performance graphs are most useful in determining performance variation as operating conditions change. For example, all amplifiers are specified for a minimum voltage output at maximum current rating. If your application needs only 75% of this current, you might determine from the typical graph you will gain 0.5V at this level. A safe design will assume output capability of 0.5V better than the specification table, not the actual number on the typical graph. Bear in mind, if your design is based on the typical performance graphs, it will statistically work 50% of the time.

OPTIMIZING THE POWER SUPPLY

To deliver the most output power and achieve maximum efficiency, internal power dissipation must be minimized. This condition is met if the power supply voltage is selected for the minimum voltage necessary to produce the required output. Internal power dissipation is the sum of quiescent power *plus* the product of output current and the supply to output differential. Supply voltage is the only variable for the designer to optimize. Refer to the product data sheet's specified minimum supply to output differential voltage. Each extra volt here dissipates one more watt for every ampere of output current. Trade-offs in this area are not recommended. Deriving required outputs from existing system supplies reduces efficiency if the difference between supply and required output exceeds the supply to output differential of the op amp. Also, this supply vs. efficiency trade-off must be considered when contemplating the use of unregulated supplies. When using unregulated supplies, line and load variations must be taken into consideration along with the ripple content of the supply. The result is a voltage band above the minimum operating voltage required by the power op amp to produce the required output. Power in this band must be dissipated. Voltage above the minimum operating voltage decreases the power handling capability of the power op amp.

The choice is whether to dissipate the power in the power op amp or in a separate regulator. As current levels increase, the dollar per watt cost generally rises faster for the power op amp than it does for a DC regulator.

Usually, unregulated supplies are not economical because they lack transient protection. Power lines are notorious for being extremely noisy. They have high voltage, high speed spikes riding on the sine wave which pass right through the power transformer. Furthermore, the large electrolytic capacitors used for filtering often do not have low equivalent series resistances at those high frequencies. A 1K volt spike on the incoming line can result in an excessive voltage spike at the amplifier supply pin. Destruction of the op amp may be the result. Therefore, line filters and zener clamps are required to eliminate the voltage spikes; thus, the economy of unregulated supplies is reduced.

Once the minimum supply voltages above have been selected, steps need to be taken to minimize IR losses. Some of today's modern hybrid power op amps handle currents higher than most branch circuits in residential wiring. Losses can be kept to a minimum, especially as frequencies increase, if leads are as short as possible between supply and amplifier, as well as between the amplifier and the load. In the video frequency range, where even a few inches of wire have significant inductance, and the skin effect increases the resistance of heavy wires at high frequency, multi-strand litz wire is recommended.

SINGLE OR ASYMMETRIC SUPPLY OPERATION

Asymmetric output swings present another opportunity to optimize power supplies. Consider the circuit of Figure 1. If the symmetric power supplies were used, power dissipation would be substantially increased, a power op amp with a higher voltage rating would be necessary and output power would be reduced.

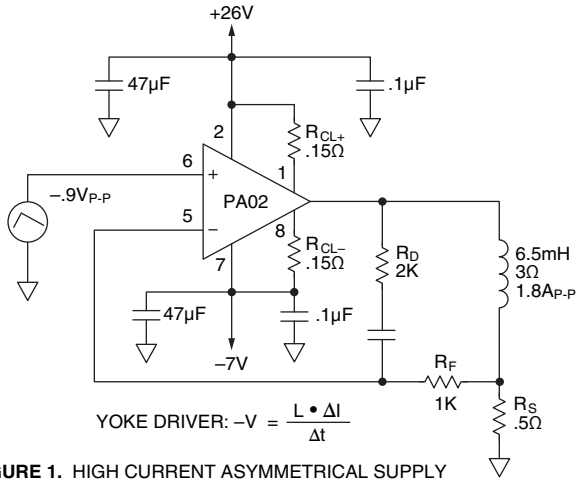


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

Fortunately, most power op amps are suitable for operation from a single supply voltage. The common mode operating requirements do, however, impose the limitation that the input voltages not approach closer than 5 to 10 volts to either supply rail (determined by the common mode voltage specification). Thus, single supply operation requires the input signals to be biased 5 to 10V from either supply rail. Figure 2A illustrates one bias technique to achieve this.

Figure 2A illustrates a very practical alternative to single supply operation, a second low voltage supply. This allows ground referenced input signals, but also maximizes the voltage swing of the unipolar output. The 12 volt supply in Figure 2B must usually supply only the quiescent current of the power op amp unless the load is reactive or EMF producing.

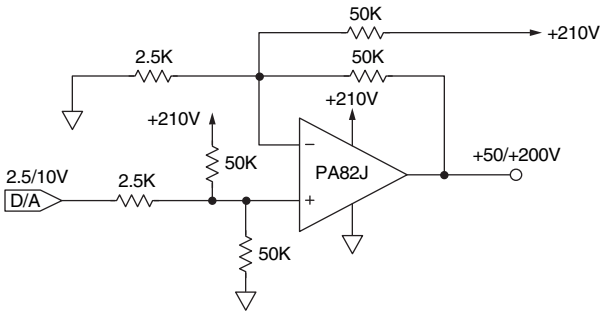


FIGURE 2A. TRUE SINGLE SUPPLY OPERATION

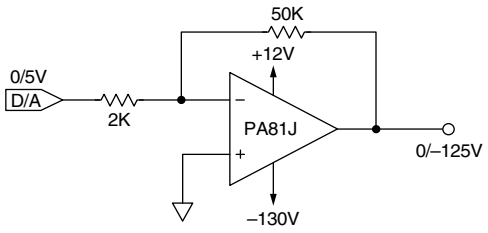
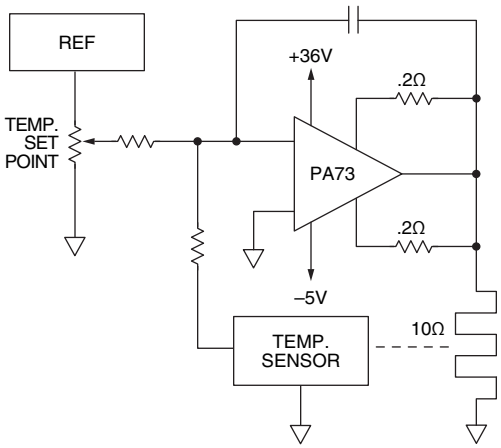


FIGURE 2B. ASYMMETRIC SUPPLIES

KNOW YOUR POWER DISSIPATION

Power requirements of the load are most often well known, but calculating the power dissipated inside the amplifier is not always simple.

For purely resistive loads, maximum internal power dissipation occurs when the output voltage equals half the supply voltage. This is the worst case to analyze if the amplifier does not have to withstand short circuits. An example of DC application is the temperature controller in Figure 3.



MAX INTERNAL POWER	MAX OUTPUT POWER
1/2 V_S = 18V	V_{OUT} = 28V
I_{OUT} = 1.8A	I_{OUT} = 2.8A
P_{OUT} = 32.4W	P_{OUT} = 78.4W
P_{INT} = 32.4W	P_{INT} = 22.4W

FIGURE 3. TEMPERATURE CONTROL CIRCUIT POWER LEVEL

Programmable power supplies (PPS) for automated test equipment must often tolerate short circuits in the device under test. For the PPS shown in Figure 4, the worst case dissipation will occur with a short to one of the 24V DUT supplies if the PPS is programmed to the opposite voltage. Assuming the current limit of the 24V supply is greater than the PPS limit, the PPS goes into current limit with considerably higher power levels than encountered under normal operation. Worst case for the amplifier could be its supply voltage plus the DUT supply voltage times the current limit.

AC OUTPUTS ALLOW HIGH POWER LEVELS

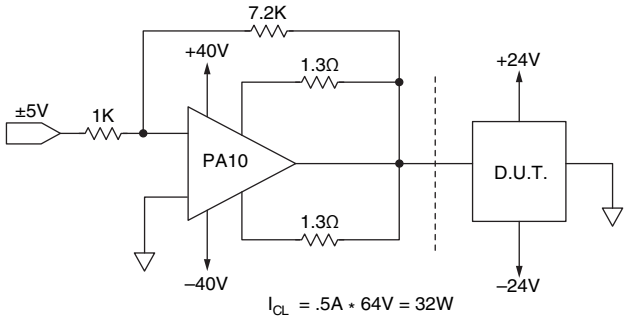


FIGURE 4. PPS POWER DISSIPATION CONSIDERATIONS

If an AC drive has a frequency of 60Hz or greater, the half-wave period of the power dissipating waveform is shorter than the thermal time constant of the power amplifier. The resultant power averaging between the output transistors results in a lower thermal resistance. This lower thermal resistance immediately increases the power handling capability of a given amplifier.

Apex Precision Power data sheets provide both AC and DC ratings of thermal resistance. Power levels specified on both the absolute maximum rating and the power derating typical performance graphs are based on DC thermal resistance. This means an AC only application is capable of delivering more power or running cooler (more reliably).

Sine wave circuits share a similarity with DC circuits. Maximum internal RMS power dissipation occurs when the peak output voltage swings to 63.7% of supply voltage. Maximum internal power may be calculated as follows:

$P = V_{SS}^2/(2\pi^2 * R_L)$

Where: V_{SS} = total rail-to-rail supply voltage
R_L = load resistance

REACTIVE LOADS INCREASE DISSIPATION

When driving reactive loads, more caution is required due to the phase difference between V_O and I_O. The actual power dissipation may be several times higher than the equivalent resistive loads. In such cases, It is best to use a totally different, but equally simple, approach to calculate power dissipation (P):

$P = P_1 - P_O$

Where: P_1 = Power drawn from the power supply
P_O = Real power delivered to the load

In calculating P1, use DC supply voltage and AVERAGE output current (RMS * .9003 [.9003 = AVG/RMS or $2/\pi \div \sqrt{0.5}$]). For example, a 1A RMS output, with supplies of ±15V, means .9003 * 1 * 15 = 13.5W plus quiescent current * 30V.

Driving purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier because the load power factor is reduced to zero.

DEALING WITH MOTOR DRIVES

Motor control applications often place brutal requirements on the driving circuit. Section A of Figure 5 shows two output transistors of a power amplifier and the motor with its ratings. It is important to recognize that the winding resistance and the voltage rating of the motor alone do not determine the running current. The back EMF of the motor must also be considered when calculating the running current. This EMF can be modeled as a battery whose voltage is proportional to instantaneous velocity as shown in Section B of Figure 5.

When the amplifier is given a reversal command, it changes its output very quickly while the actual speed and EMF can diminish only as fast as mechanical system inertia is dissipated. The initial result of the vastly different response times between the electronics and the mechanics is shown in Section C of Figure 5. The amplifier has responded to its new drive command, but the EMF has not yet had time to change.

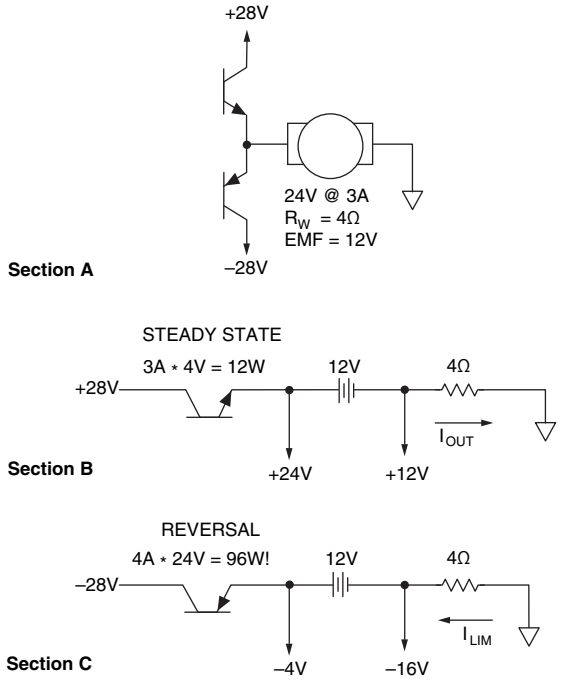


FIGURE 5. POWER DISSIPATION IN MOTOR DRIVES

The model shows that if the amplifier could produce the programmed output level of –24V, a total of 36V would be applied across the winding resistance developing a current on 9A. In this situation, the output voltage is determined by the current limit of the amplifier rather than the control voltage. The programmed limit of 4A through the winding resistance produces 16V. Adding the initial 12V EMF places the amplifier output voltage at -4V. With 24V across the conducting transistor, the internal power dissipation is eight times the level encountered in steady state operation. Failure to analyze this situation has taken the lives of many power op amps.

A useful technique to maximize available power for steady state running requirements is to limit the rate of change of the drive voltage to approximately the same limitation imposed by the inertia of the mechanical system. In this manner, the extremely high power levels described can be avoided. In other words, fast reversal times can be traded off for high levels of running torque.

CIRCUIT DESIGNS TO INCREASE OUTPUT POWER

Two power op amps configured in a bridge circuit can double power levels. To illustrate the advantages of the bridge circuit, Figure 6 shows a composite where alternate connections transform the circuit from single ended to a bridge. A1 is a standard single ended power op amp which would drive the 4 ohm speaker. If A2 is added, it completes a bridge circuit. The resulting doubling of the voltage drive would be suitable for an 8 ohm speaker. With this trick, not only are power levels doubled, but the same supply is capable of powering either circuit. This is possible because the single ended circuit peak current demand utilizes only 50% of the supply capability. In contrast, the equal and opposite drive characteristics of the bridge circuit loads both positive and negative supply rails equally during each half cycle of the signal.

Parallel operation is often used to increase output current or

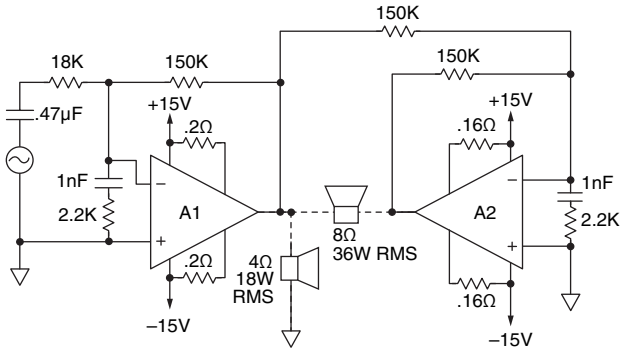


FIGURE 6. DOUBLING POWER WITH A BRIDGE

wattage. However, due to their low output impedance, power op amps cannot be connected in parallel without modifying the circuits. Figure 7 illustrates one method of doing this. This uncommitted *master* amplifier, configured as required to satisfy the circuit function, has a small sense resistor inside its feedback loop. The *slave* amplifier is a unity gain buffer. Thus, the output voltages of the two amplifiers are equal. If the two sense resistors connected to the load are equal, the amplifiers share current equally. More slaves may be added as desired.

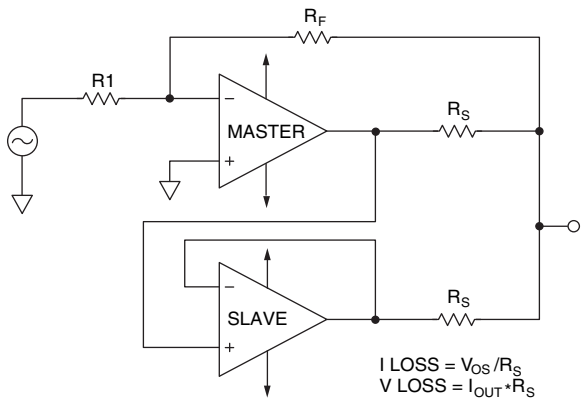


FIGURE 7. PARALLEL OPERATION

There are two factors to consider in the selection of the sense resistors. First, the output current will produce a voltage drop which adds to the supply requirements. Second, the voltage offset of the slave appears across the sum of the two sense resistors. Thus, a small current will circulate strictly between the two amplifiers. This wastes power. When this technique is used, it is recommended that inputs be limited in such a way that they demand only 50% of the typical slew rate of the amplifier. This prevents two amplifiers with different slew rates from generating large currents between each other during fast transitions.

PROPER HEATSINKS INCREASE OUTPUT POWER

With a given power op amp, the larger the heatsink is, the higher attainable output power can be. Furthermore, as power levels increase, it is more cost effective to use a larger heatsink.

To minimize space and weight, forced air cooling or even liquid cooling is often used with power amplifiers. While obviously easier to implement, forced air cooling gives a maximum improvement of only about 2:1. At higher power levels, liquid cooling becomes a more attractive option. Reasonable heatsink ratings, which can be achieved given an area 6 inches square and 2 inches tall, are 0.85°C per watt for free air cooling, 0.4°C per watt for forced air, and 0.05°C per watt for a liquid cooled system. See the Apex Precision Power application note on heatsinking for more information.

THERMAL SHUTDOWN CAN HELP

Internal thermal protection can increase output power under nominal operating conditions because the amplifier shuts off when the substrate temperature exceeds safe limits. This allows the amplifier circuit design to be based solely on normal conditions but prevents excessive temperature during abnormally high power conditions.

The thermal shutdown feature is especially valuable in circuits such as programmable power supplies (PPS). Here the output voltage is the normal operating voltage of the unit under test. Occasionally the unit under test will be defective which may short the output of the PPS to ground; thus, power levels increase substantially. Thermal shutdown will simply shut the device off rather than lead to destruction. Thermal shutdown is not a panacea for all problems. It does not mean to disregard the second breakdown curves of the safe operating area. Assume the time constant for operation of the thermal shutdown is 250-500ms. This means the worst case power levels should not exceed the steady state second breakdown line of the SOA curve.

OPTIMIZING IS A TEAM EFFORT

Apex Precision Power power op amps employ unique thermistor circuits that provide superior control of internal currents and offer exceptional specifications plus a superb quality record. With careful attention to design of the application, the end result will be advanced products of greater value.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Current Limiting

INTRODUCTION

Power op amp circuits without suitable current limiting can be compared to putting a gun in the hands of a child – you may get away with it but disaster is waiting to strike. While elaborate circuits have been used, most power op amps use a simple and cost effective circuit which still requires engineering homework to be safe. The objective is delivering desired power to the load without violating the SOA.

BASIC CURRENT LIMITING

Current limiting circuits in power op amps are local to only the output stage so they can very quickly (sub microsecond) reduce output current to a predetermined level. There are at least four reasons to incorporate such a limit:

1. The output transistors of the amplifiers are almost always capable of delivering more current than the ABSOLUTE MAXIMUM RATING of the amplifier. Exceeding this limit can destroy metal, usually a wire bond to the supply or the output pin fuses. A common mistake is to rely on the power supply current limit for this protection. Do NOT fall into this trap. Filter capacitors (both inside the supply and local to the op amp) often store plenty of energy to vaporize a wire bond.
2. Loads with variable impedance may need protection against possible fault conditions. A mechanical jam on a motor drive is a good example.
3. Current limit can prevent overloading power supplies. This may be critical if other circuits share the same supply.
4. Observing the Safe Operating Area (SOA) of the power amplifier keeps junction temperatures to a reasonable level. Output current is one term of the power equation.

A fixed current limit is usually adequate for the first three reasons. A simple and cost effective approach to current limiting is shown in Figure 1. Current through the output transistor Q1 is converted to a voltage by the sense resistor Rcl. When this voltage exceeds the Vbe of the current limit transistor Q2, drive current from the preceding stage is diverted to the output to shut down Q1. In addition to being an amplifier, Q2 serves as an imperfect voltage reference for the current limit set point. At room temperature the typical value is around 0.65V. Rb along with the capacitance of Q2 slow the circuit just enough to prevent oscillation. In equation form:

$$Icl = 0.65/Rcl \quad (1)$$

or

$$Rcl = 0.65/Icl \quad (2)$$

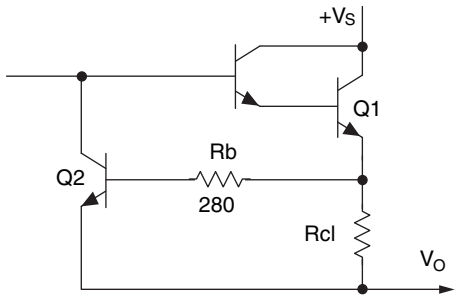


FIGURE 1. CLASSIC CURRENT LIMIT CIRCUIT

where Icl is the current limit in amperes and Rcl is the current limit resistor in ohms.

The fourth reason is more complex. Figures 2 and 3 illustrate the challenge of meeting SOA limitations with fixed current limit. First, note that the X axis labeling of the PA10 SOA graph is NOT output voltage but the stress voltage across the conducting transistor. Assume DC signals and a case temperature of 25°C for the following. The resistive load implies stress voltage is limited to single supply voltage and that maximum heat in the output transistor occurs at an output of 50% of supply. At 25V the SOA graph tells us maximum current is 2.7A. This implies a minimum load of about 9.3 ohms will limit current to safe levels at any output voltage. Maximum current will be 4.75A (44V/9.3 ohms) and maximum output power will be 209W. Note: The voltage swing specification of the PA10A is Vs-6V at 5A. However, if the application must survive a shorted component or cable on the output, the stress voltage jumps to 50 and maximum safe current is only 1.05A. Once this current limit is set output power is limited to 46W peak into 44 ohms. For energy storing loads, assume an initial voltage of nearly -50V and a positive going signal. Initial supply to output stress is nearly 100V and maximum safe current is less than .3A.

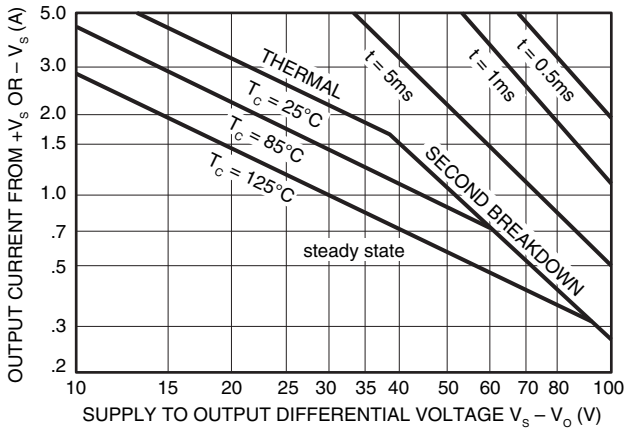


FIGURE 2. SOA GRAPH OF PA10

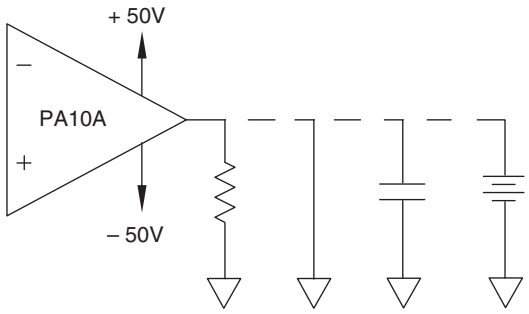


FIGURE 3. DIFFICULT LOADS OR POSSIBLE FAULT CONDITIONS

CURRENT LIMIT IS A MOVING TARGET

The largest variable of the current limit circuit is the temperature coefficient of the imperfect reference voltage, the Vbe of Q2. It decreases approximately 2.2mV for each degree C

increase in case temperature. Thus the 0.65 term ranges from 0.826 at -55°C to 0.43 at 125°C. From an steady state power dissipation point of view, this slope is in the right direction but it is still possible to get in trouble. Comparing this slope to our initial reasons to limit current:

1. The reason does not vary with temperature.
2. The reason is load dependent.
3. The reason is supply dependent.
4. The reason does not vary with temperature.

It is best to plot the limit on the SOA graph and compare to other requirements of the system. To this end, visit the Apex Precision Power web site at www.Cirrus.com or contact Apex Precision Power applications engineering for software to automate the task.

Looking again at Figure 1, we can find several reasons actual current limit varies from the equations presented. When in the limiting mode, Q2 is shunting drive stage current away from Q1 directly to the output. This means actual current limit can not be less than drive stage capability. Some data sheets give a minimum practical current limit. Operation in this region is unusual because drive stage current is so much less than output capability that being in this region implies amplifier capability is likely an overkill for the application.

Now consider that when Q2 is conducting there will be base current flowing through Rb which effectively increases the reference voltage. On some amplifiers this effect is large enough that the specific data sheet will give a unique value greater than 0.65 to use in the equations.

Although it is not immediately obvious looking at figure 1, resistance of internal wire bonds, solder joints, wiring traces and the leads of Rcl all add to the rated value of Rcl unless pins are provided to implement four wire current sensing. In high current applications, measurements of prototype circuits may be the best way to finalize the design.

We now have a very wide range of "safe" currents depending on loads or fault conditions which must be tolerated. We have also seen that while simple and cost effective, these limiting circuits are not reference standards; think in the area of +/-20%. The sad part is that the fixed current limit set to protect for worst case fault condition also limits current for the non-fault condition. It is also interesting to note that we assumed an unrealistic heatsink and safe currents are still only a fraction of the absolute maximum for the amplifier. This shows the importance of both heatsinking and current limiting. An ideal solution for SOA protection might be the addition of a stress voltage sensor and multiplier for each output transistor such that limiting could be based on watts. If all this circuitry is fast enough, SOA concerns would be no more. This approach is quite rare because the cost measured in components, design time and space is almost always more than that of using a larger amplifier. Clearly, an affordable improvement in current limit technique is called for.

FOLDOVER CURRENT LIMIT BASICS

Apex Precision Power models PA04, PA05, PA10 and PA12 can take advantage of foldover current limiting. Adding only one resistor to the classic current limiting circuit (Figure 4) provides dynamic response to output voltage swing. Realizing that Rcl is typically three orders of magnitude below Rb, it is reasonable to ignore Rcl and say Rb and Rfo form a voltage divider between ground and the output voltage. With Rfo typically being a couple orders of magnitude larger than Rb, the divider adds a very small portion of the output voltage in series with the base of Q2. With a 0V output, current limit will be the same as the classic circuit. However, as the output goes positive, the addition of the divider voltage effectively increases the reference voltage (Vbe of Q2) allowing more current to flow. For negative output voltages (Q1 is still conducting), the very small fraction of the negative output added reduces current flow. Another way to view this would be state we have added a term to the current limit equation based on output voltage but modifying current limit in an inversely proportional manner to voltage stress on the conducting transistor. While this is still a long way from the ideal of a multiplier calculating watts, and it does nothing in the case of variable supplies, it does add a desirable slope to the current limit function. In equation form:

$$I_{CL} = \frac{0.65 + V_O \bullet \left(\frac{Rb}{R_{FO} + R_B} \right)}{R_{CL}} \qquad (3)$$

$$R_{CL} = \frac{0.65 + V_O \bullet \left(\frac{Rb}{R_{FO} + R_B} \right)}{I_{CL}} \qquad (4)$$

where Vo is output voltage in volts and resistors are from Figure 4 and in ohms.

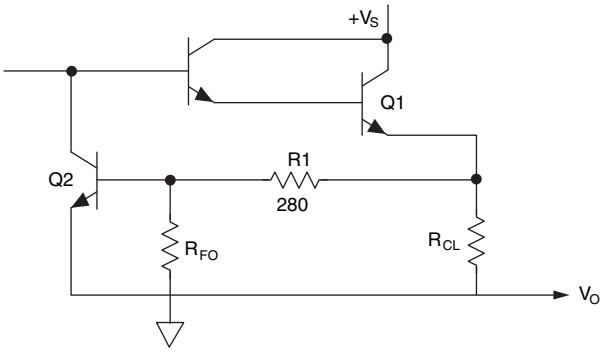


FIGURE 4. BASIC FOLDOVER CURRENT LIMIT CIRCUIT

Looking again at the case of the resistive load driver which must tolerate a short on the output, let us further assume the objective is to drive 22 ohms to 88W peak (44Wrms, 44V pk and 2A pk). Start with an Rb of 280 ohms and Rfo of 20Kohms and use Equation 4 to calculate Rcl = 0.629 ohms for peak current at peak voltage. Use a 0.62 ohm resistor. Equation 1 now shows us current during the short fault condition is limited to 1.05A. Plotting the current limit on the SOA graph as shown in Figure 5 reveals that this current limit is safe for any output voltage from zero to supply. Using foldover instead of fixed current limit has nearly doubled the power delivery capability.

In the case of the energy storing load, Equation 3 shows us this foldover circuit current limit crosses zero and turns negative within the swing capability of the amplifier at all temperatures above 25°C. This can cause amplifier latch-up and MUST be avoided. A lower supply voltage or a larger foldover resistor will solve this problem.

Even though we know the current limit is safe for a short to ground and for the full 100V stress level, Figure 5 shows that at 25°C and colder allowable current crosses above the SOA line in between these points. Increasing Rcl will lower current limit at all output voltages and solve this problem.

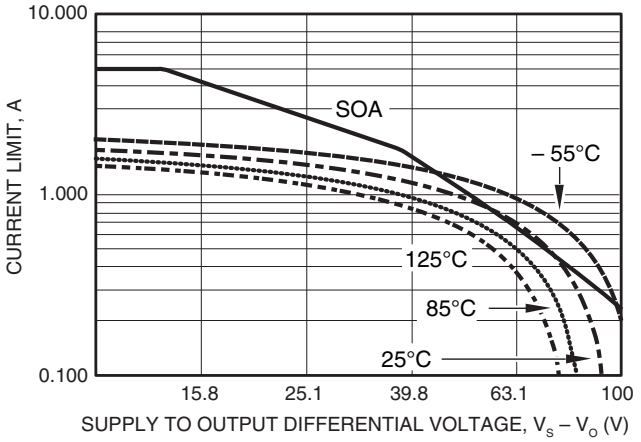


FIGURE 5. FOLDOVER ILIMIT VS. VOUT

TWO TYPES OF FOLDOVER

The PA10 and PA12 have an internal Rb of 280 ohms and internal Rfo of 20K for both the positive and negative current limit transistors. The two 20K resistors tie together at pin 7 where the user may ground the pin for maximum foldover slope or add an additional resistor in series from pin 7 to ground for less foldover action. Since both 280 ohm resistors tie essentially to Vo and the two series networks of 0.28K + 20K are essentially in parallel, the equations specific to the PA10 and PA12 are more complex than the previous example:

$$I_{CL} = \frac{0.65 + V_O \bullet \left(\frac{10.14}{10.14 + R_{FO}}\right) \bullet \left(\frac{.28}{20.28}\right)}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + V_O \bullet \left(\frac{10.14}{10.14 + R_{FO}}\right) \bullet \left(\frac{.28}{20.28}\right)}{I_{CL}} \quad (6)$$

where Icl is in amperes, Vo is in volts Rcl is in ohms and Rfo is the PA10 or PA12 external foldover resistor and is in Kohms.

Foldover connections for the PA04 or PA05 are shown in Figure 6. Use 270 ohms for Rb and use equations 3 and 4. Beware that even momentary shorts directly at pin 10 can destroy the amplifier now that pin 10 is isolated from the output by the 270 ohms.

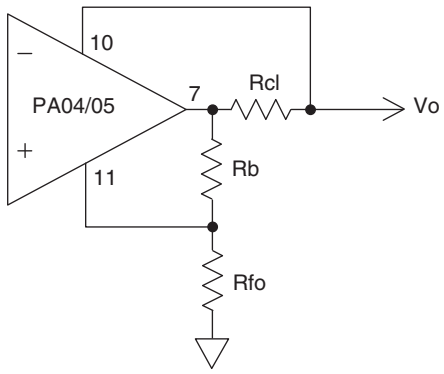


FIGURE 6. FOLDOVER CIRCUIT FOR PA04 OR PA05

CONCLUSION

Current limit is to the power op amp as survival instinct is to an animal; a REALLY good thing to have. While basic current limiting is simple, adding temperature variations and circuit options such as foldover make the job of checking all the points of possible danger quite a chore. First comes the math, then data plotting on the SOA graph with those log scales we all love so well. This drudgery has become history with the spreadsheet automation. Get your copy from the Apex Precision Power web site at www.Cirrus.com or call Apex Precision Power applications.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
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Power Amp Output Impedance

INTRODUCTION

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Current control circuits, or current sources, include the load as a series element in the feedback loop with a sense resistor developing a voltage proportional to load current. Figure 1 shows a generalized example of just such a circuit. The load often consists of an inductive element such as a deflection yoke which can have up to 90° of phase shift at higher frequencies. Totally accurate prediction of phase in the feedback loop might at first seem to involve the series equivalent of output impedance and yoke impedance. In reality, it's because the feedback the op amp is operating as a true current source with an impedance approaching infinity. A realistic approach to stabilizing the circuit merely involves an auxiliary feedback whose effect dominates before the combination of yoke feedback and amplifier phase approaches 180°. Output impedance is not necessary to determine stability.

It is also important to realize that output impedance of a power op amp is not related in any way to power delivery capability or internal losses. A model of a power amp with the output resistance in series with the output will develop inordinate losses which are not observed in real world op amps.

Output impedance is dependent on several variables such as frequency, loading and output level. Often, the impedance will rise at higher frequencies. A class C amplifier, such as PA51 or PA61, will exhibit higher impedances at lower levels due to bulk emitter resistance effects in the emitter follower outputs.

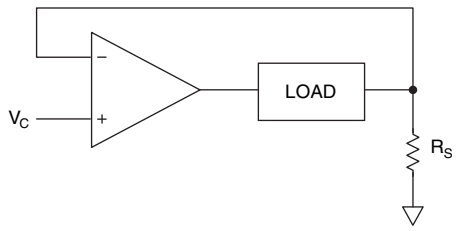


FIGURE 1. GENERALIZED CURRENT CONTROL CIRCUIT

OUTPUT IMPEDANCE MEASUREMENT

Several methods are available to measure output impedance. The simplest method is to measure open loop gain in loaded and unloaded conditions. This method measures the dynamic impedance in series with a perfect voltage source. Variations in output with loading are due to this impedance.

A more direct method is to generate a signal which is impressed into the output of an amplifier operating under open loop conditions. A measurement of current will determine the effective impedance that this signal is looking into.

ACTUAL IMPEDANCE VALUES

Several Apex Precision Power power amplifiers were measured using the gain variation with loading method. The test circuit of Figure 2 was loaded with 10 ohms. To establish uniformity of measurement, the smallest possible amplitude at 10Hz was used. Where a range of values is shown, it represents a range observed for several devices.

PA02: 10-15 ohms
PA07: 1.5-3 ohms
PA08: 1500-1900 ohms (high voltage amplifier)
PA09: 15-19 ohms
PA10: 2.5-8 ohms
PA12: 2.5-8 ohms
PA19: 30-40 ohms
PA51: 1.5-8 ohms
PA61: 1.5-8 ohms
PA84: 1400-1800 ohms (high voltage amplifier)

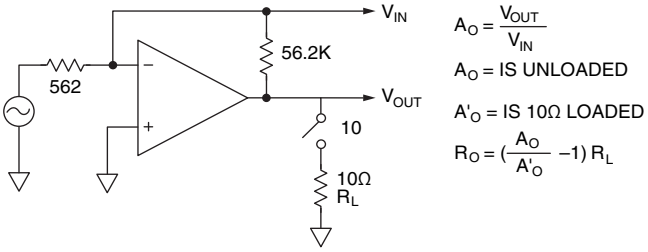


FIGURE 2. OUTPUT IMPEDANCE MEASUREMENT CIRCUIT

The high voltage amplifiers are much lower in current capability than the high current amplifiers. As a result, the higher impedance is to be expected.

The high impedance shown for PA19 is a result of the drain output MOSFET circuit without local feedback at the output stage. This is an example of how this parameter can be misleading. If 30 to 40 ohms of resistance were in series with the output, then the PA19 would never be capable of greater than 1 amp of output current. Under closed loop conditions, the output impedance is reduced to milliohm levels like any other power amplifier. Keep in mind the output impedance is an abstract term as far as output voltage and current capability are concerned.

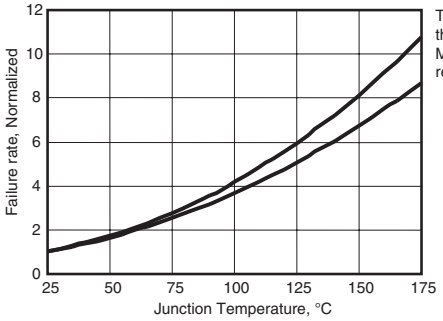
To demonstrate the effect of output impedance when modeling, use the highest and lowest expected values. The results will verify that output impedance plays an insignificant role in power amp performance.

Thermal Techniques

THERMAL MANAGEMENT

As power op amps shrink in size and become more powerful, the importance of a good thermal design is more critical than ever. Most importantly, reliability is a direct function of internal component temperatures and dissipated power. Furthermore, as the amplifier case rises above 25°C, derating factors do not just reduce the allowable power level. Voltage and current offsets drift, current limits change and, sometimes even dynamic performance is affected. This application note discusses thermal management starting with actual dissipation vs. allowable dissipation, the common cooling options, how to achieve maximum performance with sound mounting techniques, as well as the benefits of thermal capacity.

Thermal management techniques must be applied to remove as much heat as possible from the semiconductor junction, thereby maintaining minimum operating temperatures and maximum reliability. A further goal is to minimize the effects of the removed heat on other devices. Figure 1 shows the average of bipolar and MOSFET power transistor failure rates at elevated temperatures relative to operation at 25°C. All electronic components encounter similar increased failure rates.



This data was extracted from the base failure rate tables of MIL-HDBK-217F, Notice 2, revision of 28 February, 1995.

FIGURE 1. MTBF vs. Temperature.

MAXIMUM POWER RATING

Your new home stereo system boasts 200W. Industrial amplifier #1 claims 100W audio output. Industrial amplifier #2 claims 67W internal dissipation.

Your challenge is to determine which of these is the most powerful. With a 115V input current rating of only 0.4A, we can dismiss the stereo. Analysis of the industrial amplifiers requires we either find internal dissipation for amplifier #1 or find maximum audio output for amplifier #2. Power Design is the tool for this work once circuit details become known (load impedance, supplies and a few other amplifier specifications). Figure 2 illustrates the general concept that there could be almost a 2:1 ratio between output power and internal power for AC signals and about 3:1 for DC signals (even assuming a purely resistive load).

	Pint	Pout	Vout	Iout	Tcase	Tjunction
AC (rms)	59W	100W	20V	5A	85°C	138°C
DC (peak)	72W	200W	28.3V	7.07A	98°C	200°C

With internal dissipation of industrial amplifier #1 being only 59W when delivering its maximum output of 100W, #2 is the power champion because at 100W output it still has

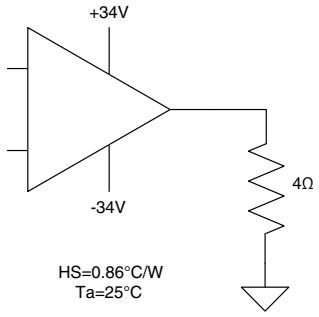


FIGURE 2. What Wattage Number Should be Applied to This Circuit?

8W reserve as far as internal dissipation is concerned. The second concept to note in Figure 2 is that DC signals result in higher temperatures than AC signals. This is because with AC signals, each power transistor has a half cycle to cool while the opposite polarity transistor does the work. The bottom line on power ratings: All of the four wattage numbers above accurately describe the circuit, but the actual number can vary better than 3:1, depending on definitions.

Θ_{JC} is the thermal resistance from junction to case. With these ratings (one for DC and a more advantageous one for AC) output power capability for any type circuit can be easily determined. A great deal of effort has been put into minimizing this thermal resistance. It is the major specification affecting power handling capability. When allowing for a case temperature of 25°C and maximum junction temperature, the maximum internal dissipation rating is developed.

$$P_{MAX} = (T_{JMAX} — 25°C) / \Theta_{JC} \qquad (1)$$

This rating is consistent with rating methods of most transistor manufacturers and should not be confused with advertised output power which is highly application dependent. Before using this rating, check for factors which might degrade the rating such as actual ambient temperature (T_R), heatsink thermal resistance (Θ_{HS}) mounting, and in some cases, an isolation washer.

$$P_{MAX} = (T_{JMAX} — T_A)/(\Theta_{JC} + \Theta_{HS} + \Theta_{HSC}) \qquad (2)$$

Equation 2 gets back to the real world where a real heatsink is used, the interface between amplifier and heatsink is not prefect, ambient temperature may not be ideal, and reliability requirements may not allow junction temperatures up to data sheet maximums. Read the heatsink data sheet carefully. There are multiple thermal ratings for heatsinks because they vary with power level, sometimes with orientation and always with flow rate (air or liquid). Thermal interface rating between cases and heatsinks are built into Power Design and can be found on the Apex Precision Power Accessories Information data sheet.

WASHERS AND WASHERS

The most common is the thermal washer mounted between the amplifier and the heatsink. It's prime objective is to enhance thermal conduction compared to a bare joint. This is

the washer which MUST NOT BE COMPRESSIBLE. Using a compressible washer on a metal can type package VOIDS THE WARRANTY. The most common of these washers is an aluminum substrate with a thermal coating on each side. Thermal performance of these washers is at least as good as a joint with properly applied thermal grease. Advantages over grease include removal of operator variables on performance (too thick, too thin, missing coverage), and not being messy. When electrical isolation is required, similar washers with a Kapton substrate provide isolation at the expense of additional thermal resistance on the order of 2x. These washers are not reusable. When replacing an amplifier, the old coating residue should be removed from the heatsink to avoid buildup and possible amplifier damage.

The second washer type used in mounting power devices is the compression washer used under the head or nut of the mounting screw. These may be (in order of effectiveness) Belleville washers, split lock washers or tooth lock washers. One of these washers should be considered when the equipment would be regularly subjected to temperatures where humans would require protective clothing.

SYSTEM LAYOUT

Thermal management starts with determination of actual dissipation and should result in a layout of an optimized thermal system to convey the heat to the ambient environment. In systems using natural convection, heat sources should be separated as widely as possible. In contrast, systems using high velocity air or liquid cooling perform optimally when localizing these devices. Understanding convection and radiation may help avoid layout related problems. Since convected heat rises, it is best to place the heat sources near the top of the enclosure and avoid having temperature sensitive circuits above or near the heat sources. The hot air should flow in its natural vertical direction using vertical board and fin orientation. Heatsinks should be oriented so air can pass freely over all the fins.

MOUNTING THE AMPLIFIER

The design of the amplifier mounting must:

1. Provide the required thermal path from amplifier to ambient.
2. Maintain intimate contact between amplifier and heatsink surfaces.
3. Maintain amplifier lead positions with respect to a PCB, socket or wire.

Occasionally, an Apex Precision Power amplifier will not require a heatsink. If this appears to be the case, double check the thermal calculations, and then proceed to use cage jacks, socket or soldering leads directly on the pins to finish the design.

Figure 3 shows common mounting layouts for metal can type packages. While the PC board example shows the use of cage jacks, this is drawing would also apply when soldering the pins directly to the PCB. Note that in this example, either the heatsink is supporting the PCB or the PCB is supporting the heatsink. In this latter case, if the heatsink is more than four square inches (in the same plane as the PCB), consider the configuration in Figure 4 where heatsink mass places less stress on the PCB in the immediate area of the amplifier when subjected to shock or vibration.

Figure 5 shows the preferred mounting method for the DIP10 products. Number 4 hardware is first used to mate the amplifier to the flat surface of the heatsink. Do not forget the thin layer of thermal grease spread evenly over this area. The heatsink/amplifier assembly can now be mounted to the PCB with (usually) #6 hardware. A spacer length of 0.25" plus a washer at least 0.02" (almost all washers are thicker than this) will insure amplifier components do not touch the PCB.

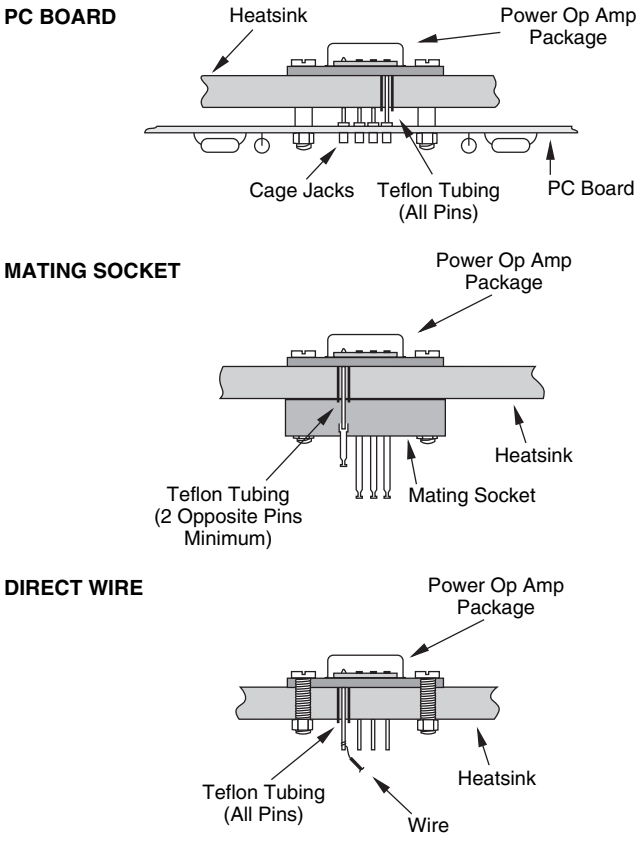


FIGURE 3. Mounting Techniques (Cross Section Views)

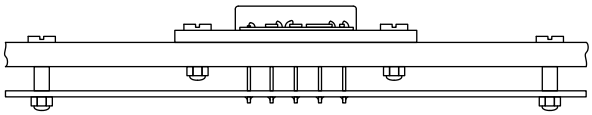


FIGURE 4. Large Heatsinks Need More Support.

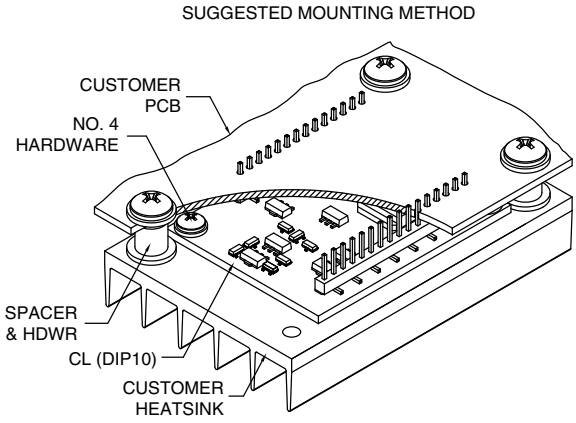


FIGURE 5. Preferred mounting for CL (DIP10) packages.

When DIP10 packages are mated with very small heatsinks (about the same size as the amplifier and fins of 1" or less, the method in Figure 6 may be used.

Generally, The BC series amplifiers are used in systems requiring large power delivery. As discussed in the previous

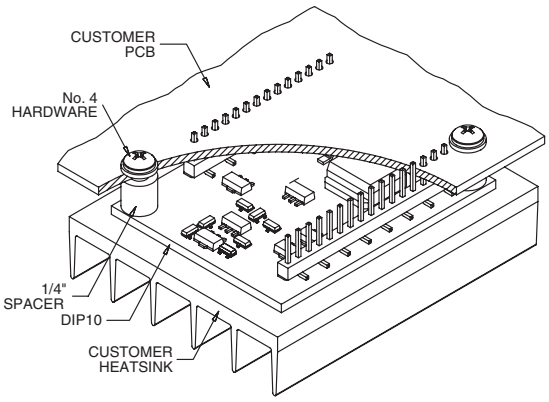


FIGURE 6. Mounting CL (DIP10) packages to very small heatsinks.

section, large heatsinks may often necessary to keep the amplifier cool while delivering significant power. The mechanical assembly of the printed circuit board, BC amplifier, and heatsink deserves some discussion.

The heatsink should be the main structural element that supports the amplifier and the PCB. The BC pins and most circuit card material are not strong enough to support a heatsink of any significant size. Failures are likely to arise by doing so - circuit traces may crack, pins may bend and lose contact with sockets, and solder joints may weaken and lose effectiveness. Figure 7 shows one acceptable arrangement where the PCB and heatsink are supported by standoffs to some structural element. The BC amplifier is attached to the heatsink with 2 screws. Cage jacks or solder connections may be used for the electrical connection to the pins. Half-inch standoffs provide stable support of the heatsink above the PCB.

Commercial heatsinks usually specify a surface finish of 63

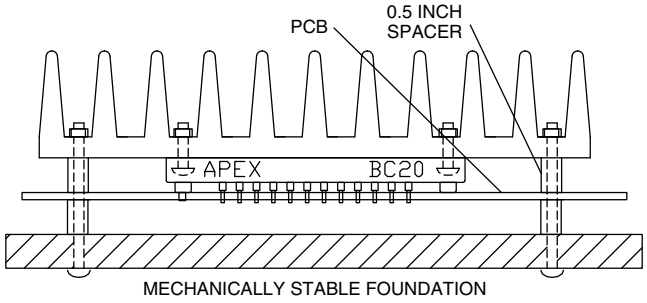


FIGURE 7. Heatsink is not mechanically supported by the PCB or the BC Amplifier.

micro inches, flatness of 4mils/inch in the direction of extrusion and 6mils/inch perpendicular to the direction of extrusion. This is marginal but generally considered acceptable for packages up to about 1 square inch. Apex Precision Power procures all heatsinks with flatness specified at 2mils/inch. This forces a machining operation on the mounting surface, resulting in less than 1mil/inch actual flatness. We recommend this approach when specifying a heatsink, whether it is a normally an off the shelf model, a custom designed heatsink or uses structural members of equipment as a heatsink. Do not forget to require deburring of all holes. When amplifier pins go through the heatsink, specify a hole for each pin of the amplifier. A single hole or cutout for all the pins will thermally isolate the amplifier from the heatsink.

Aging of this thermal interface has proven to be no problem, as long as the mechanical assembly is not disturbed. If disassembled, clean off grease or washer coating material from both amplifier and the heatsink, reapply and reassemble.

THERMAL CAPACITY

The power levels that can be achieved in the pulse mode of operation are elevated far above those of steady state operation. This is due to the thermal capacity of the heatsink. As heat is first applied, the rate at which the case temperature increases can be compared to its electrical equivalent, the voltage build up on a capacitor of a R-C network. Figure 8 displays this analogy.

Thermal capacity is the amount of heat needed to raise the

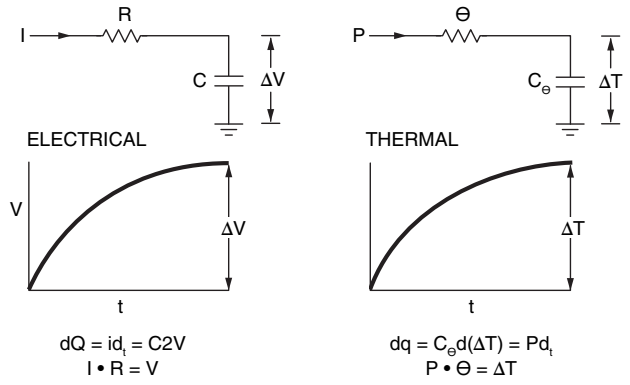


FIGURE 8. Electrical and Thermal Models.

temperature of the given object 1°C. The generally published parameter for materials is specific heat given in calories/gram, so multiplying by grams yields calories. Multiplying this by 4.186 will convert to watt-seconds, again for a 1°C change. The thermal time constant (Tau) is the product of the thermal capacity and the thermal resistance. This time constant defines the rate at which the material reaches thermal equilibrium. The time required to achieve 95% of the final temperature is three time constants.

To illustrate the principle, aluminum has a density of 2.7gr/cm³ and a specific heat of .22calorie/gram/°C (times 4.186 = 0.921watt-seconds/gram/°C). The Apex Precision Power HS05 heatsink weighs 18.3 ounces (518.8grams) and has a thermal resistance (free air) of 0.85°C/W. Thermal capacity of the heatsink is then 0.0921 • 515.8 or 478watt-seconds/°C. Finally, the time constant of the HS05 with a free air mounting will be 478 • 0.85, or 406 seconds.

Adding a fan to the application reduces thermal resistance, but thermal capacity remains constant, meaning the time constant will be proportional the thermal resistance. Graphs for the HS05 indicate 500 feet/minute linear air flow produces a thermal resistance of 0.3°C. The new time constant is 478 • 0.3, or 143 seconds.

If power is applied as a single pulse, the case temperature follows the curve in Figure 4. The Δ T in °C for both heating and cooling follow these equations :

$$\Delta T_{HEAT} = W * \Theta_{HS} (1 - e^{-t/tau}) \quad (3)$$

$$\Delta T_{COOL} = \Delta T_{HEAT} (e^{-t/tau}) \quad (4)$$

The Figure 9 (next page) curve indicates that thermal capacity plays a major role when the duty cycle is extremely low.

Figure 10 (next page) shows the initial response to application of repetitive pulses. The pulse train is repetitive when the duty cycle does not allow the circuit to return to its initial temperature between pulses. The following procedure will predict operating

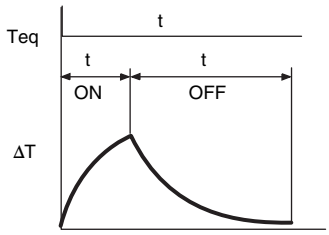


FIGURE 9. Single Pulse Response.

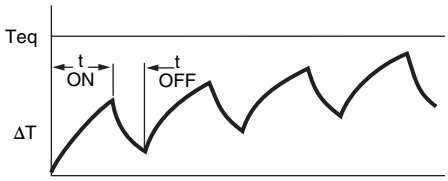


FIGURE 10. Repetitive Pulse Response.

temperatures after the heatsink has reached equilibrium. Peak power is multiplied by duty cycle to arrive at average power. The average temperature of the case will be $T_A + (P_{AVERAGE} \bullet \Theta_{HS})$. To determine the peak power, the pulse duration and time constant are substituted into equation 3 above. Then 1/2 Δ heating is added to average temperature to yield the maximum case temperature. This case temperature should be used in conjunction with the SOA curves to determine the maximum power available from the device.

CONCLUSION

Thermal management optimizes space, cost and size for your power levels and temperature range. When properly applied, it will get the heat out and keep your circuits cool; thereby, maintaining the highest possible reliability and performance.

For easy calculations of this information see the spreadsheet EE Friend at www.Cirrus.com.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Voltage to Current Conversion

VOLTAGE TO CURRENT CONVERSION

Voltage controlled current sources (or VCCS's) can be useful for applications such as active loads for use in component testing or torque control for motors. Torque control is simplified since torque is a direct function of current in a motor. Current drive in servo loops reduces the phase lag due to motor inductance and simplifies stabilizing of the loop.

VCCS's using power op amps will assume one of two basic forms, depending on whether or not the load needs to be grounded.

CURRENT SOURCE: FLOATING LOAD

Figure 1A illustrates the basic circuit of a VCCS for a floating load. The load is actually in the feedback path. R_S is a current sense resistor that develops a voltage proportional to load current.

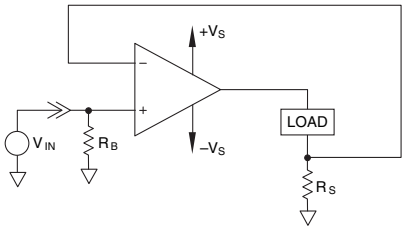


FIGURE 1A. BASIC VCCS FOR FLOATING LOAD

Note the inclusion of resistor R_B in Figure 1A and subsequent figures where non-inverting VCCS's are described. This resistor is present to prevent the non-inverting input from floating when the input voltage source is disconnected or goes to high impedance during the power on cycle. R_B provides a path for input bias current of the amplifier and commands the amplifier output current to zero in cases where V_{IN} is disconnected or goes to a high impedance. Figure 1B shows an implementation of a VCCS for a floating load. At low frequencies the added components Cf, Rd, and R_F have no effect and are included only to insure stability. Considerations for these components are discussed in the section on "Stabilizing the Floating Load VCCS" covered later in this application note.

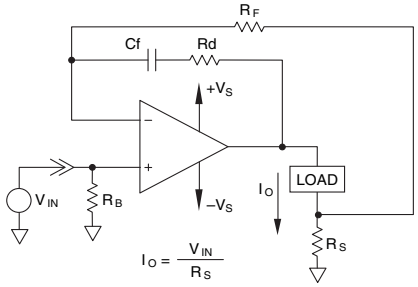


FIGURE 1B. VCCS FOR FLOATING LOAD WITH STABILITY COMPENSATION

The amplifier's loop gain will force the voltage across R_S to assume a value equal to the voltage applied to the non-inverting input, resulting in a transfer function of:

$$I_O = V_{IN}/R_S$$

Several variations are possible for this basic circuit. It is not necessary to have a direct feedback connection from R_S to the inverting input; components can be included to raise the gain of the circuit. Figure 2 shows a higher gain version with its equivalent transfer function. Higher gain circuits will lose some accuracy and bandwidth, but can be easier to stabilize.

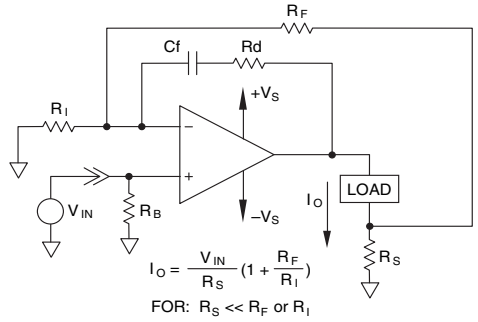


FIGURE 2. VCCS FOR FLOATING LOAD; INCREASED GAIN CONFIGURATION

Figure 3 shows an inverting VCCS. The input voltage results in an opposite polarity of current output. Just as in the case of inverting voltage amplifiers, the advantage of not having any common mode variation at the amplifier input is higher accuracy and lower distortion.

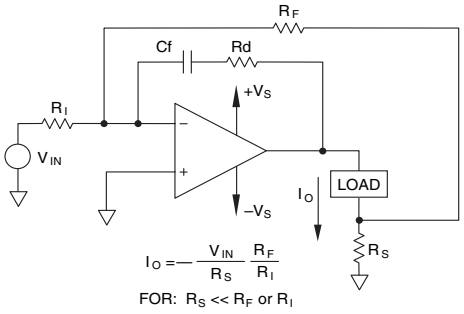


FIGURE 3. VCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

Figure 4 is a current input version which is actually a CCCS, or current controlled current source. This is truly a current amplifier. This circuit could be useful with current output Digital-to-Analog Converters (DAC's), or in any application where a current is available as an input.

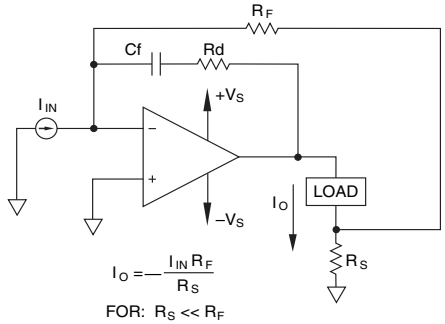


FIGURE 4. CCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

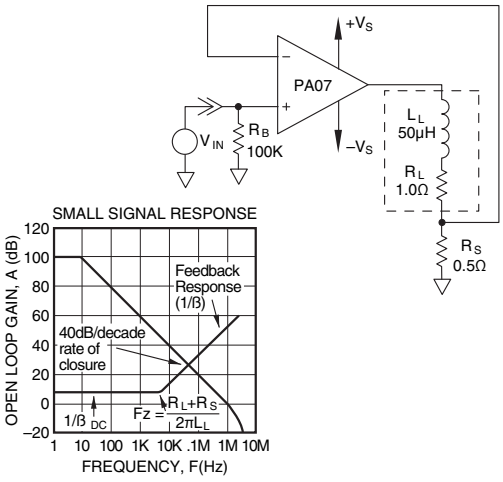
STABILIZING THE FLOATING LOAD VCCS

Because the load is in the feedback loop on all of these circuits, it will have a significant effect on stability. If the load was always purely resistive, the analysis would be simple and many circuits would not require any additional components (such as Cf and Rd) to insure stability. In the real world however, we usually find ourselves using these circuits to drive such complex loads as magnetic coils and motors.

Stability analysis is most easily accomplished using **"Rate of Closure"** techniques where the response of the the feedback is plotted against the amplifier open loop gain. This technique uses information easily obtained on any amplifier data sheet.

Rate-of-closure refers to how the response of the feedback and amplifier Aol intersect. If the slope of the combined intersection is not over 20 dB per decade, the circuit will be stable.

For an example, consider the amplifier of Figure 1A. Assume a PA07 amplifier with a 0.5 ohm current sense resistor will be used to drive a 50 µH coil with 1 ohm of series resistance. In Figure 5 we have superimposed on the Aol graph of the PA07 the response of the load and sense resistor.



$$ß_{DC} = \frac{.5}{1.5} = .333 \rightarrow 1/ß = 9.5dB \quad Fz = \frac{1.0 + .5}{2\ 50µH} = 4.77kHz$$

FIGURE 5. PLOTTING FEEDBACK RESPONSES

The intersection of the responses exhibits a combined slope of 40 dB per decade, leading to ringing or outright oscillation. Let's refer to that point as the "critical intersection frequency." Compensation for this circuit is best accomplished with an alternate feedback path; the response of which will dominate at the critical intersection frequency.

A good criteria for the response of the alternate feedback would be:

1. A response which dominates by at least an order of magnitude (20 dB) at the critical intersection frequency.
2. The alternate feedback response should have a corner occurring at a frequency an order of magnitude less than the critical intersection frequency.

To provide this response, the alternate feedback components have been selected to provide the compensating response illustrated in Figure 6. A_B in Figure 6 is the dominant feedback path the amplifier will see in its closed loop configuration. R_F merely acts as a ground leg return impedance for the alternate feedback loop, and should be a low value between 100 and 1000 ohms. Rd is then selected to provide the desired high frequency gain, and Cf is selected for the alternate feedback

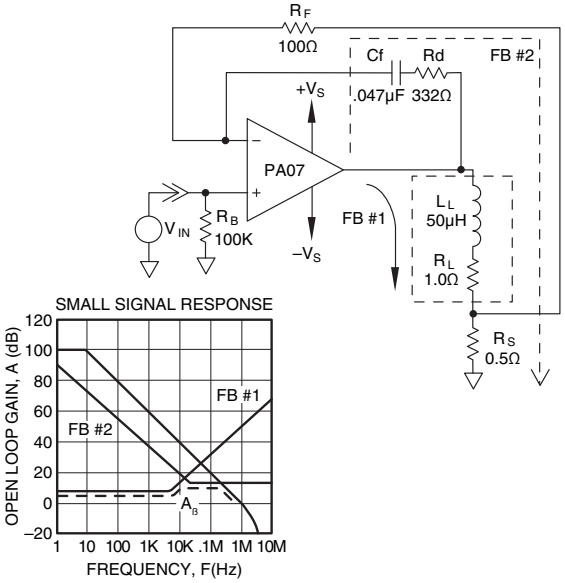


FIGURE 6. COMPENSATING THE AMPLIFIER

corner.

Note that these are similar to techniques used to stabilize magnetic deflection amplifiers described in Apex Precision Power AN05, **"Precision Magnetic Deflection."**

CURRENT OUTPUT FOR GROUNDED LOAD

The VCCS for a grounded load is sometimes referred to as the **"Improved Howland Current Pump."** It is actually a differential amplifier which senses both input signal and feedback differentially.

Figure 7 shows a general example for this VCCS with its associated transfer function.

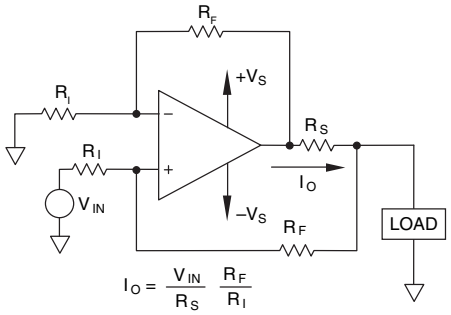


FIGURE 7. VCCS FOR A GROUNDED LOAD

First among the special considerations for this circuit is that the two input resistors (R_I), and the two feedback resistors (R_F), must be closely matched. Even slight mismatching will cause large errors in the transfer function and degrade the output impedance causing the circuit to become less of a true current source.

As an example of the matching requirement, consider the actual example using PA07 in Figure 8. Matching the resistors as closely as tolerances permitted produced an output impedance of 43 K ohms. A 1% mismatch reduced output impedance to 200 ohms and introduced nearly 20% error into the transfer function.

This suggests that matching to better than 0.1% is required which is probably best accomplished with prepackaged resis-

tor networks with excellent ratio match. The circuit of Figure 8 actually required a slight amount of mismatch in the two (R_F) resistors to compensate for mismatches elsewhere, suggesting that the inclusion of a trimpot may be necessary to obtain maximum performance.

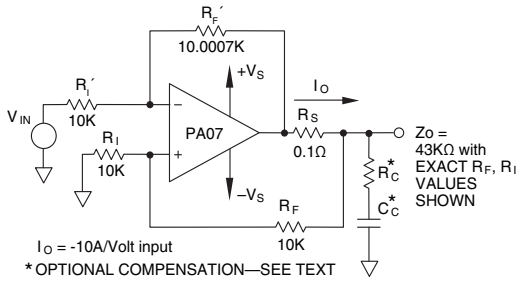


FIGURE 8. ACTUAL PA07 VCCS

STABILITY WITH THE GROUNDED LOAD CIRCUIT

The grounded load circuit is remarkably forgiving from a stability standpoint. Generally, no additional measures need to be taken to insure stability.

Any stability problems that do arise are likely to be a result of the output impedance of the circuit appearing capacitive. The equivalent capacitance can be expressed as follows:

$$Ceq = \frac{R_I + R_F}{2\pi foR_IR_S}$$

Where: fo = THE GAIN-BANDWIDTH PRODUCT OF THE AMPLIFIER

This capacitance can resonate with inductive loads, resulting most often in ringing problems with rapid transitions. The only effective compensation is a simple **"Q-snubber"** technique: determine the resonant frequency of the inductive load and output capacitance of the circuit. Then, select a resistor value one-tenth the reactance of the inductor at the resonant frequency. Add a series capacitor with a reactance at the resonant frequency equal to one-tenth of the resistor value. An alternate method would be to put a small inductor and damping resistor in series with R_S.

Also keep in mind that the equation favors larger values of R_I and R_S, and the use of op amps with better gain-bandwidth to reduce effective capacitance. In circuits where good high frequency performance is required, this will necessitate increasing either or both R_I and R_S with the upper limits being established where stray capacitance and amplifier input capacitance become significant.

An infrequent second cause of instability in this circuit is due to negative resistance in the output impedance characteristic of the circuit. This problem can be solved by trimming the feedback resistors to improve matching.

THE CURRENT MIRROR

The current mirror circuit is a handy device for generating a second current that is proportional to input current but opposite in direction.

The mirror in Figure 9 must be driven from a true current source in order to have flexible voltage compliance at the input. Any input current will attempt to develop a drop across R1 which will be matched by the drop across R2 causing the current through R2 to be ratioed to that in R1. For example, if R1 were 1.0 K ohm and R2 were 1 ohm, then 1 mA of input current will produce 1 Amp of output current.

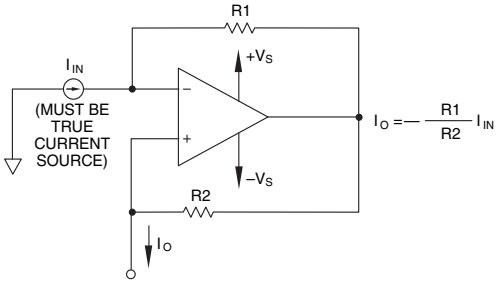


FIGURE 9. CURRENT MIRROR

RATE-OF-CLOSURE AND FEEDBACK RESPONSE

Rate-of-closure stability analysis techniques are a method of plotting feedback response against amplifier response to determine stability.

The closed loop gain of any feedback amplifier is given by:

$$Acl = Aol/(1-\beta Aol)$$

Where: Aol IS THE OPEN-LOOP GAIN OF THE AMPLIFIER, AND Acl IS THE RESULTANT CLOSED LOOP GAIN

ß is a term describing the attenuation from the output signal to the signal fed back to the input (see Figure 10). In other words, ß is the ratio of voltage fed back to the amplifier over the amplifier's output voltage. (Vfeedback=ßVout)

In the examples used in this application note, the plotting of ß versus amplifier response is facilitated by plotting an equivalent closed loop response (1/ß) of the amplifier circuit and superimposing this response on the amplifier open loop response. This **"equivalent closed loop response"** is also referred to as noise gain, Av (n).

In the example in Figure 5, the curve referred to as feedback response is actually representative of the closed loop noise gain response of the amplifier due to the feedback network consisting of yoke and sense resistor. In Figure 6, an additional feedback response for Cf, Rd, and R_F is plotted independently of all other responses. There are several important points to be noted in the use of these graphs:

1. In the case of multiple feedback networks such as in Figure 6, the response with the lowest noise gain at any given frequency will be the dominant feedback path. In Figure 6 this dominant feedback path is labelled $A_ß$.
2. Whenever the noise gain and open loop gain intersect with a combined slope, or rate of closure, exceeding 20 dB/decade, poor stability will result. 40 dB/decade will definitely oscillate since this represents 180 degrees of phase shift. An example of this is shown in Figure 5.

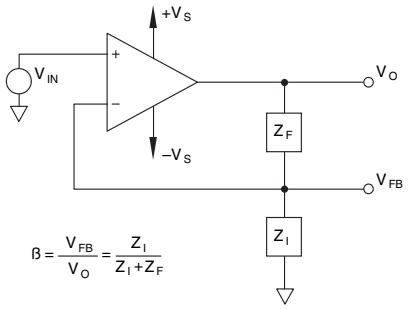


FIGURE 10. FEEDBACK FACTOR, ß

Power Booster Applications

The Apex Precision Power PB series of power booster amplifiers, PB50 and PB58, are high performance, yet economical and flexible, solutions to a wide variety of applications. Their voltage and current ratings of up to 200 volts at 2 amps for the PB50, and 300 volts at 1.5 amps for the PB58, satisfy most high voltage and high current requirements. In addition, the PB series is fast. The 100 V/µs slew rate these boosters offer is matched or exceeded by only a few expensive power or high voltage op amps. If accuracy, in the form of low offset, drift, and/or bias current, is the system requirement, the PB series, with the proper choice of driver amplifier, can deliver high voltage performance with accuracy equal to the best small-signal op amps available on the market, and do it economically.

DESIGNING WITH BOOSTER AMPLIFIERS:

BASIC CONNECTIONS

Power supply requirements for the PB50 dictate that the negative supply rail must be at least 30 Volts below the COMMON terminal (pin 5), setting the minimum supply voltage at +/-30 V. The PB58 can operate from supplies as low as +/-15 volts.

The INPUT terminal of the PB series devices is a low impedance input typically on the order of 50 KΩ. Maximum safe input voltage range must be limited to less than +/-15 volts. These power boosters will always have an offset of typically .75 volts as a result of the common base bipolar input stage. When used with a driver amplifier, this offset will subtract from the swing available from the driver. For example, a driver op amp that is required to swing 20 volts peak-to-peak will actually swing -10.75 and +9.25 volts. This offset has no effect on offset of the total driver and booster circuit since this offset is effectively reduced by the open loop gain of the driver amplifier. Remember that this offset will always be apparent when used without a driver amplifier.

The COMMON terminal provides a ground reference for the internal input and feedback circuitry. It might be noted that it is possible to use this “ground” terminal as an input; however, the PB series has not been characterized for such usage. The ground terminal would appear as a low impedance inverting input which must be driven from a low impedance source such as an op amp output.

The GAIN terminal allows the connection of additional resistance in series with the built-in feedback resistor of the PB series. The compensation capacitor connected to COMP, pin 8, is in parallel with the feedback resistor. Designers can predict the frequency response of the PB series amplifiers for any compensation by simply calculating the pole frequency of the parallel connection of feedback resistor, R_G, and compensation capacitor. The pole frequency is given by:

$$FP = \frac{1}{2\pi\,(R_G + 6.2K)\,C_C}$$

Where: R_G = EXTERNAL FEEDB ACK RESISTANCE
C_C = EXTERNAL COMPENSATION CAPACITOR

For example, a 22 pF compensation capacitor across the 6.2 K ohm feedback resistor results in a pole frequency of 1.2 MHz. This corresponds with the Closed Loop Small Signal Response graph on the PB50 data sheet. A gain of 10 will require placing a 22 K ohm resistor in series with the built-in 6.2 K ohm internal feedback for a total feedback resistance of approximately 28 K ohm. In this case a 22 pF compensation capacitor produces a rolloff at 260 kHz, again corresponding to the PB50 small signal response graph.

COMPOSITE AMPLIFIER STABILITY CONSIDERATIONS

The PB series data sheets provide 4 guidelines for insuring the stability of circuits designed with these boosters. Use of these guidelines can be complemented by the use of standard techniques such as plotting the overall gain response of the driver/booster combination and superimposing the feedback network response.

An example for determining the Aol (open loop gain) response of the composite amplifier is illustrated in Figure 1. At any given point on the frequency response, the overall gain is the sum of the gains (in dB) of the two amplifiers.

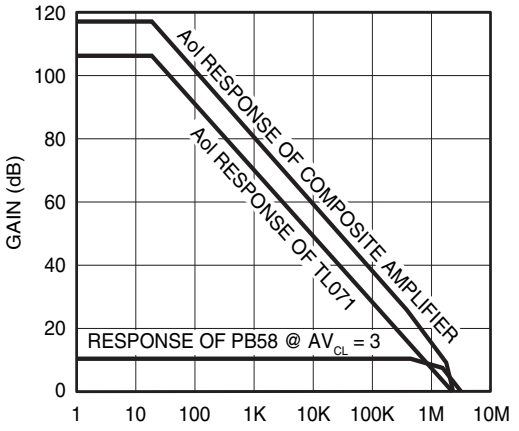


FIGURE 1. PLOTTING Aol FOR THE COMPOSITE AMPLIFIER

Figure 2 shows an example of such a plot for the deflection amplifier described in this application note. As a general rule, the intersection of the feedback response and open loop response should equate to a slope of no greater than 20 dB/decade to insure stability.

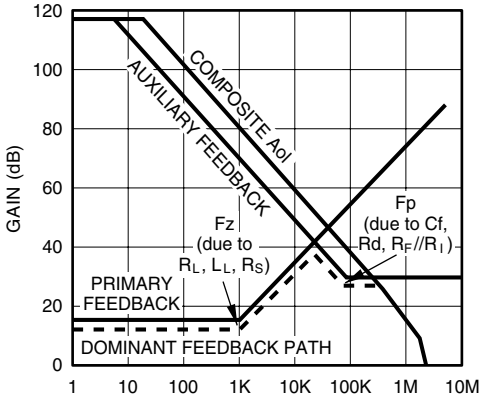


FIGURE 2. DEFLECTION AMPLIFIER FEEDBACK (I/ß)

The particular deflection amplifier described in this application note is a testament to the ease with which the PB series

devices can be designed into circuits where stability is usually a problem. The magnetic deflection circuit, which is a current source with an inductive load inside the feedback loop, is inherently unstable. The composite amplifier responded quite well to standard techniques used to stabilize deflection amplifiers (see AN #5, **"Precision Magnetic Deflection"**) and presented no special stability problems.

The designer who may be apprehensive about using a booster (buffer with gain) need have no reservations when using PB50 or PB58.

APPLICATION EXAMPLES: PROGRAMMABLE POWER SUPPLIES

The programmable power supply (PPS) application is useful to demonstrate the versatility of the PB series boosters. Along with the need to supply high voltages and currents, programmable power supplies often need high accuracy and low drift, while at other times they may need to be fast-responding. The PB series allows the designer to optimize the circuit for these choices. Figure 3 is an example of a high accuracy PPS. An AD707 is selected as the driver amplifier to provide the extremely low offset required to obtain best possible performance from a high accuracy 18-bit DAC. The divider network on the output, R1 and R2, scale the output swing down to the full-scale range of the DAC. Accuracy will be affected by this divider, necessitating the use of high quality, low temperature coefficient (TC) resistors. If a packaged network can be used, then absolute TC is not nearly as important as TC ratio between R1 and R2. The use of this divider is preferable to the alternative technique of using an external DAC feedback resistor, since using the internal DAC feedback resistor insures the best possible temperature drift performance of the DAC itself. Most DAC's can exhibit up to 300 ppm/°C drift with external feedback resistors.

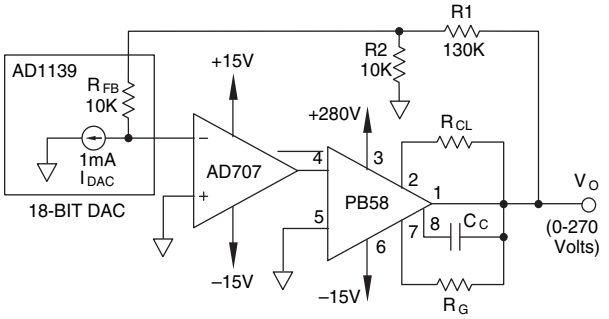


FIGURE 3. HIGH ACCURACY PPS

APPLICATIONS AT LESS THAN FULL VOLTAGE AND CURRENT

The PB series do not have to be used at high voltages to realize all their performance benefits. Presently, only a few expensive IC power amplifiers can match these parts for slew rate and power bandwidth. Magnetic deflection applications require amplifiers with good speed performance at current levels often within those that the PB series can supply. While these applications don't always require high supply voltages, the high voltage capability of the PB series is useful when fast transitions are required with high inductance yokes, necessitating high supply voltages as a result of the yoke energy requirement:

The basic techniques of magnetic deflection amplifier design

$$V = L \frac{dI}{dt}$$

are detailed in AN#5, **"Precision Magnetic Deflection."** Figure 4 is an example of these techniques put to use in the design of a magnetic deflection amplifier using the PB58. This circuit forces a yoke current proportional to input voltage by including the yoke within a current sensing feedback loop. In this example, the feedback resistors R_F and R_I are configured for a minimum gain of 5 to compensate for the added booster gain, thereby easing stability considerations. The auxiliary feedback network Cf and Rd act to bypass the 90° phase shift of the yoke/sense resistor feedback at higher frequencies ensuring stability with best transition times. The fastest transition time in any magnetic deflection amplifier is determined by the available voltage swing and yoke inductance. In the circuit of Figure 4, nearly 140 volts could be made available for the 200 microhenry yoke, resulting in a minimum possible transition time of 2 microseconds. The TL071 and PB58 combination can slew at 40 V/microsecond which means the amplifier requires an additional 4 microseconds to provide full voltage swing. The end result is a circuit that can deliver total transition times of less than 6 microseconds, equating to sweep speeds of 83 kHz.

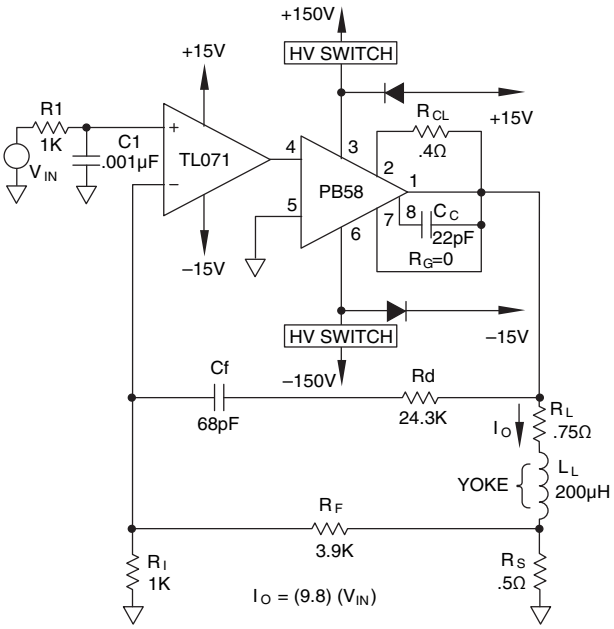


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

An important advantage of a separate booster amplifier in deflection applications is the ability to swing the output stage supply rails to improve efficiency. Slower sweep speeds can use lower power supply voltages than higher speeds. In addition, during a high speed sweep the high voltage is only needed for a short period of time until yoke current builds and can then be switched to a lower value. Using the lower supply voltages whenever possible improves efficiency and reduces dissipation. In applications where the supply rails will be "flexed" in this manner, only the rails connected to the power booster need to be flexed. The constant supply available at the driver amplifier enhances the driver amplifier's ability to maintain overall loop control by preventing the coupling of supply switching transients into the input section of the amplifier.

Figure 4 provides a general idea of the circuitry involved

in switching the supply rails. The actual implementation could take on many forms that are beyond the scope of this application note.

A final performance consideration in magnetic deflection amplifiers is avoidance of slew rate overload (or any condition which could result in input overload). This problem actually occurs during the rapid retrace transition, but shows up during the trace interval. The evidence of input overload is ringing during the trace interval. To eliminate this problem, reduce the transition time of the retrace portion of the input waveform to a rate which is within the slew rate specification of the amplifier. Slower transition times do not necessarily reduce circuit performance since the amplifier was overloaded to begin with, and eliminating ringing is actually an improvement on settling time when returning to the trace interval. Controlling input slew rate can be accomplished in many ways. If the actual risetime of the input signal itself cannot be controlled, a simple low-pass R-C filter at the input of the amplifier will suffice. In the example shown in Figure 4., R1 and C1 provide a filter which limits the slew rate of any input signal rise time to within the amplifier's slew rate.

Selection of the correct filter time constant takes into account both amplifier slew rate and gain of the circuit. In the case of a magnetic deflection amplifier, the appropriate value for gain would be the effective gain of the alternate feedback path Cf and Rd.

$$t = \frac{V_{IN}Av}{SR}$$

Where: V_{IN} = PEAK TO PEAK INPUT VOLTAGE
Av = COMPOSITE AMPLIFIER CLOSED LOOP GAIN
SR = RATED SLEW RATE OF THE AMPLIFIER

BOOSTER WITH NO DRIVER

It is entirely possible to use power boosters without an external driver. This could be done for simplicity or economy. It also provides the best slew rate and bandwidth performance possible with the PB series. All of this is made possible due to the boosters' self-contained internal feedback loop.

When used without a driver, the PB50 will have an inherent offset of typically 750 millivolts. Harmonic distortion remains under 0.5% at up to 30 kHz. Input impedance will be 25 K ohms minimum. Power bandwidth will typically be the full 320 kHz at the 100 Volts P-P output the PB50 is capable of.

The ground terminal on pin 5 of the PB50 presents possibilities as an additional input. Some improvement in bandwidth would be noted if this terminal were used as an input with the actual input terminal grounded. This forces the input transistor into a cascode connection. It is possible to utilize the booster as if it had true op amp type inverting and non-inverting inputs.

SOA Advantages of MOSFETs

NEW MOSFET POWER OP AMPS EASE SAFE OPERATING AREA LIMITATIONS

Hybrid power op amps continue to provide higher levels of performance and power handling than their monolithic counterparts. Power MOSFET's promise to continue the dominance of the hybrid power op amp in terms of power delivery and Safe Operating Area (SOA).

Protection issues must not be neglected regardless of amplifier choice, but the compromises required to protect the amplifier are eased with MOSFET designs. Protection of an amplifier is a matter of keeping it within its SOA under all expected conditions including faults such as short circuits.

An example of a common mistake in selecting an amplifier for a motor drive application is to use a 5A rated amplifier to drive a 1A motor. Specifying an amplifier for a motor drive application is not that simple, and stall or reversal conditions could overstress the amplifier.

Here is an illustration using a motor with the following specifications:

Winding resistance: 1.24 ohms
Voltage constant: 7.41V/K RPM
Torque constant: 10oz/in/A

The actual running current depends on the required torque. Of most concern is the worst-case current requirements that occur under stall and acceleration conditions. Under stall conditions, the amplifier is presented with a load equal to the winding resistance of the motor. This condition must be within the SOA of the amplifier.

The motor's speed determines the applied voltage. If there are sudden reversals, the motor back EMF could theoretically reach a value equal to the full applied voltage or equal to the amplifiers supply rails. This would be equivalent to shorting the amplifier output to one of its supply rails with only the motor winding resistance in series.

While the MOSFET power op amps are often featured for their high speeds, motor drive applications can take advantage of the MOSFET SOA that is free from second breakdown. Second breakdown is a limitation of all bipolar output power op amps. Second breakdown severely limits an op amp's current capacity under conditions of high voltage stress. The MOSFET on the other hand is strictly limited by its power dissipation, or thermal limits. Figure 1 compares the 25°C SOA of the PA04 MOSFET amplifier with the bipolar PA03. While the PA03 is rated for higher currents and dissipation, the PA04 has greater current capacity when there is more than 110V stress on the output devices.

For 25°C SOA calculations with a MOSFET amplifier an SOA graph is not even necessary. As long as the product of voltage and current stress is within the power dissipation rating, the amplifier is safe. MOSFET's, to reiterate, are strictly power limited.

Proper selection of current limit will determine if an amplifier is safe under fault conditions. One way of viewing this limitation is to draw a graph of output voltage and current, and superimpose SOA limits as shown in Figure 2. This graph (PA04 and ±50V supplies shown) illustrates how greater currents are available

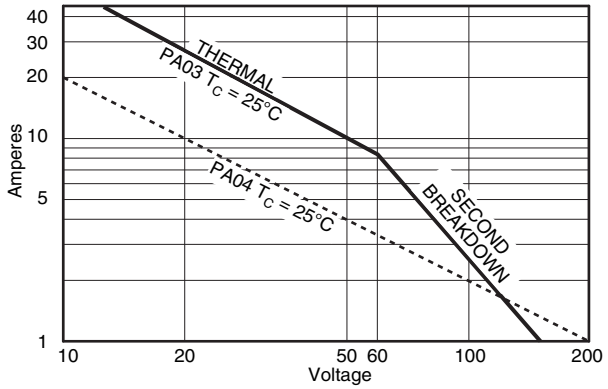


FIGURE 1. COMPARISON OF SOA FOR BIPOLAR (PA03) AND POWER MOSFET (PA04) POWER OP AMPS

when the output voltage swings closest to the rail supplying the current. The tradeoff occurs when setting current limits, usually for either of two fault conditions: shorts to ground or shorts to either supply rail. A stalled motor is equivalent to a short to ground through the motor winding resistance, while a reversal could assume the stresses of a short to either rail.

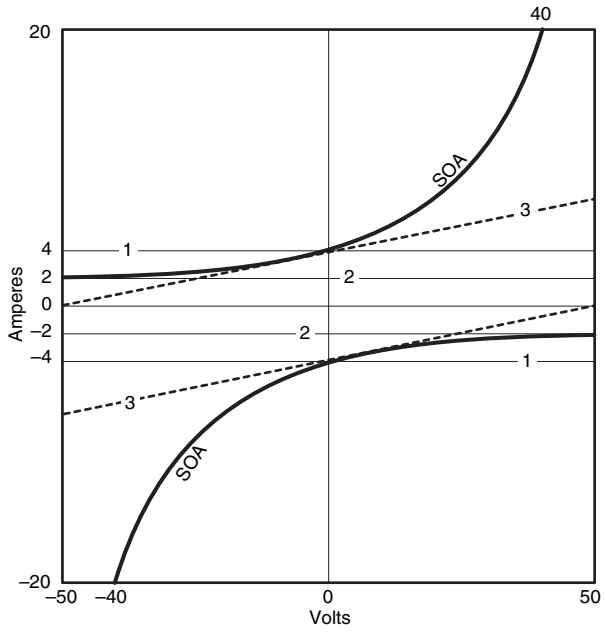


FIGURE 2. PLOT OF OUTPUT VOLTAGE AND CURRENT WITH SOA SUPERIMPOSED

From Figure 2, line 1, a limit safe for shorts to ground would be 4A (4A*50V=200W). This is well below the amplifier's full 20A capability. Even more stringent is the current limit for a short to either rail of 2A indicated by line 2 of Figure 2. A 2A limit, combined with external flyback diodes, would result in an amplifier tolerant of virtually any short or voltage kickback stress on its output. Keep in mind that this brief example uses as its basis, the 25°C SOA limits. In reality, internal dissipation and heatsinking limitations elevate temperatures, further reducing safe current levels.

FOLDOVER CURRENT LIMITING

The PA04 features four-wire current limit to overcome sensing errors occurring when working with such low resistances. While this four-wire current limit is useful in improving accuracy of current limit, it also facilitates implementing foldover current limiting. This limiting is known as load line limiting.

Foldover current limit allows more amplifier current as the output swings closer to the rail supplying the current shown by line 3 in Figure 2. Figure 3 shows the circuit to implement foldover current limiting. Rb and Rf configure a voltage divider that reduces the signal to the current limit transistors as the output swings closer to the current-supplying rail. Rf determines the slope of the foldover function. The value selected for Rb corresponds to the similar resistor internal to PA12 (actually 280 ohms) so that equations and methods developed for use with PA12 foldover limiting would be easily applied to PA04 external foldover limiting. The capacitor across Rb prevents stability problems while in current limit.

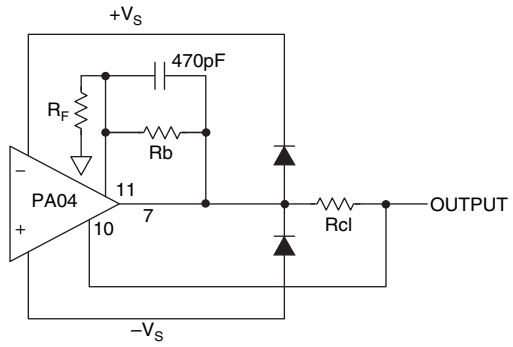


FIGURE 3. FOLDOVER CURRENT LIMITING CIRCUIT

The foldover slope must not be too steep, or latching may occur. This sets a limit to the value of Rf equal to V_S/.0025 which results in a foldover characteristic where current available when the voltage output has swung fully to the rail opposite to the one supplying current is zero. The current available when the output is closest to the rail supplying current is twice that available when the output is at zero volts. When using PA12 equations, substitute this value of Rf, in Kohms.

A PA04 incorporating foldover limiting at ±50V and requiring safety for a short to ground, would have R_{CL} selected for a 4A limit (this presumes the amplifier case can be maintained at 25°C for the duration of the short, otherwise it would have to be reduced further to stay within temperature limitations). The foldover limiting would then allow 8A at full output swing, or near zero current when delivering current from the rail opposite the output voltage polarity. A bipolar amplifier such as PA12 would be limited to 3.2A under the same criteria. The most powerful monolithic would be limited to 300mA because it is configured only for simple single resistor current limiting.

SATURATION VOLTAGE AND BOOST PINS

In motor drive applications at lower voltages, the saturation voltage, described on the data sheet as *voltage swing*, the PA04 could result in considerable power dissipation. At 15A, the PA04 output can only swing to within 8.8 volts of the rail resulting in 132W of dissipation. Boost pins are provided on the PA04 to power the front-end of the amplifier on voltages higher than the output stage, thus improving saturation. Using these terminals reduces the swing-to-rail to 5.3V at 20A for 106W dissipation. At 15A it is 4.7V for 60.5W dissipation.

Several methods can be used to supply the higher voltage required by the front-end. Additional power transformers, or additional taps on existing power transformers, or additional regulated supplies are obvious options. Modern voltage converter IC's make it inexpensive to develop these voltages under almost any condition. In Figure 4, zener regulated voltages are referred to each rail and provide power to Maxim voltage converter IC's to develop the boost potentials.

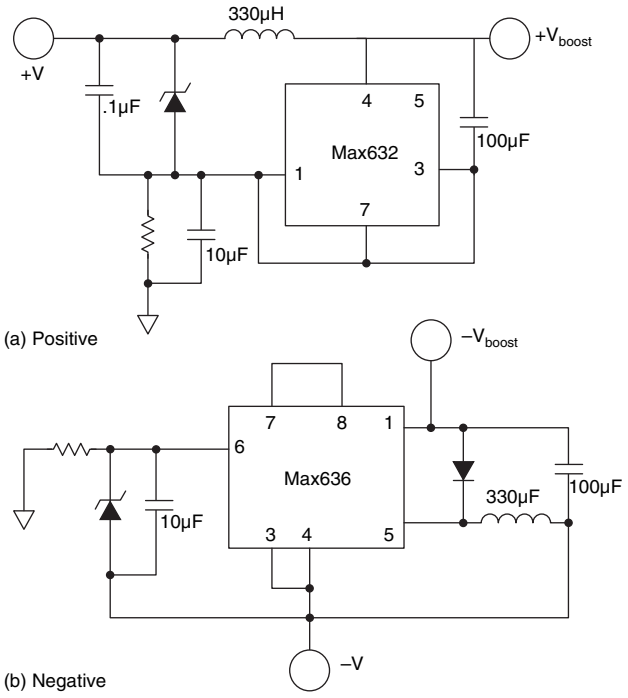


FIGURE 4. VOLTAGE BOOST CIRCUITS

MOSFET ADVANTAGES AT HIGHER VOLTAGES

The PA04 is rated at ±100V or 200V rail-to-rail. This is twice the rating of any bipolar hybrid power op amp other than PA03, and 2.5 times the rating of any monolithic power op amp.

MOSFET's have made possible this increase in voltage ratings and this can be useful in motor drive applications at high voltages. Surprisingly, some DC motors require voltages around 100 volts. The PB50 power booster is a low-cost hybrid *buffer with gain* that gives the same ±100 volt capability of PA04 with a maximum current of 2A. Because the PB50 is a MOSFET device, it can still provide 200mA at a full 200V stress.

An upgrade to the PB50 is the PB58 providing voltage capability up to ±150 volts. While PB58 is rated 1.5A, the premium PB58A is specified up to 2A. A key advantage of PB58, especially for motor drives, is its 87W dissipation. Operated at ±100V, the PB58 can provide 435mA with complete safety. At ±50V, PB58 can deliver up to 870mA. This is well over twice what could be tolerated from an amplifier such as the PA12 under the same conditions, much less from monolithic power op amps.

Both PB50 and PB58 are power booster amplifiers, not stand alone op amps. Refer to PB50 and PB58 data sheets for typical examples of actual composite amplifier circuits.

Several alternatives are given. They range from low speed, high accuracy circuits, to high speed circuits.

ADVANCED AMPLIFIER PROTECTION

The PA04's adaptability to foldover current limiting is important but not the last word in protection. Prior efforts at SOA protection have been based on bipolar transistor designs sensing output transistor temperature combined with current limiting. These techniques have shortcomings when overstress occurs while operating in the second breakdown region of bipolar power devices. The isolated hot spot occurring during second breakdown can escape sensing by the temperature sensor.

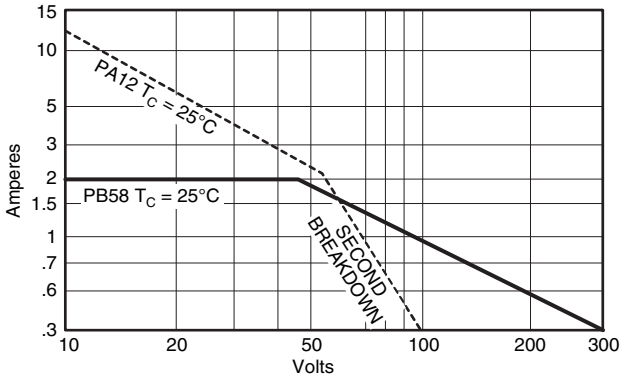


FIGURE 5. COMPARISON OF SOA FOR PA12 AND PB58

For example, PA03 senses power transistor temperature to provide a high degree of protection. But at total rail-to-rail voltages in excess of 60V (±30V), second breakdown still makes the amplifier prone to failure in extreme stresses.

In a MOSFET power output device, if a local hot spot occurs, the local transconductance decreases along with an increase in Rds at the hot spot. This facilitates thermal spreading rather than concentrating heat. As a result thermal sensing should prove extremely effective with power MOSFET's. Apex Precision Power is developing such amplifiers and early testing has shown that this may be the key to ultimate amplifier protection.

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Wideband, Low Distortion Techniques

WIDEBAND, LOW DISTORTION TECHNIQUES FOR MOSFET POWER AMPS

Shake table systems, function generators and acoustic instruments all have requirements similar to quality audio amplifiers: wide bandwidths along with low distortion. In the past, industrial grade power op amps have traded off bandwidth to insure unity gain stability, and the bipolar designs have not always met the linearity requirements of demanding applications. The PA04 changes all this with a MOSFET based architecture that sets new standards for bandwidth and linearity of integrated circuit power amplifiers.

The development of the PA04 was driven by sonar application requirements for a highly linear, high power amplifier with a power bandwidth in excess of 100 kHz. MOSFET's are the optimum choice power device to provide this performance, and in the PA04 Apex Precision Power goes several steps further in using MOSFET's in all active gain stages. While this application note will focus on getting best bandwidth and linearity from the PA04, the techniques described apply to any power op amp.

Op amps depend on negative feedback to improve performance in all ways including accuracy, linearity and bandwidth. The ideal condition is to use feedback around a design which has inherently good open loop characteristics. Evaluation of prospective amplifiers under open loop conditions quickly reveals linearity and bandwidth deficiencies. Even a simple distortion measurement under open loop conditions will give rapid comparative evaluation. Alternatively, an X-Y comparison using an oscilloscope and the circuit of Figure1, which multiplies summing node error by 100, will give a visual display of amplifier linearity. The circuit of Figure 1 will reveal that PA04 has an inherently linear characteristic while even the best bipolar designs such as PA07 have quite a bit of curvature in their open loop linearity. This is traceable to the better inherent linearity of MOSFET devices in comparison to bipolar transistors.

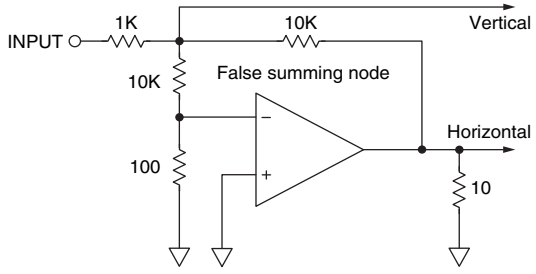


FIGURE 1. SIMPLE TEST CIRCUIT

CIRCUIT CONSIDERATIONS

The design considerations desirable for wideband, low distortion designs can be summed up with four guidelines:

1. Lowest possible closed loop gain.
2. Inverting configuration.
3. External phase compensation.
4. Input slew-rate limiting.

Distortion reduction in an op amp circuit is proportional to the amount of feedback, and this corresponds to lower gain circuits having reduced distortion. Distortion reduction is described mathematically as:

$$Df = D\left(\frac{Af}{A}\right)$$

Where: Df = % DISTORTION WITH FEEDBACK
D = % DISTORTION OPEN LOOP
A = OPEN LOOP GAIN
Af = CLOSED LOOP GAIN

It is obvious that open loop distortion is an important criteria in amplifier selection. A high open loop gain is also desirable, but op amps with high open loop gains most often have a severe tradeoff in gain-bandwidth.

The minimum useful closed loop gain is determined by the amplitude of the drive signal available to the power op amp circuit. Most often this drive is likely to come from a small signal op amp with the customary ±10 V peak drive capability. If for example a PA04 power op amp is being designed which operates at the full ±100 V supply rail limit of the PA04, this will require a minimum gain of 10.

In the event the drive signal is not a full ±10V peak, a tradeoff must be made as to whether the power op amp should be operated at a higher gain, or an additional small signal op amp be included for additional gain. Consider that the additional small signal op amp will result in insignificant contributions to distortion as long as its gain is low (<30). The light loading of the power amp circuit further minimizes distortion from the small signal op amp. These considerations favor this multiple op amp approach with a lower gain power op amp compared to a single high gain power op amp.

Low closed loop gain in the power op amp equates to increased amounts of negative feedback. This condition occasionally meets with unfounded objections when the requirement is low distortion, especially under transient conditions. However, this is dealt with by slew rate limiting to be discussed later.

The inverting amplifier configuration forces common mode potentials to zero. By doing so, non-linearities due to common-mode effects are also reduced to zero. The main advantage a non-inverting configuration would have is greater freedom of design regarding input impedance of the power op amp circuit along with the obvious lack of inversion.

Although the inverting configuration reduces input impedance, the two amplifier approach insures that the power amp circuit is driven by a source adequate to handle the resultant impedance. The cascade of two inverting amplifiers yields a non-inverting circuit. A further possible useful feature of the inverting power amp circuit is that the summing node can be monitored and any voltage detected used to indicate fault or non-linear conditions.

EXTERNAL PHASE COMPENSATION

Many power op amps are internally compensated for unity gain stability. However, this trades off gain-bandwidth product for stability under all operating conditions. Since distortion reduction is proportional to the ratio of open loop to closed loop gain, it is desirable to have as high as possible open-loop gain at high frequencies. Since it is unlikely that the power op amp will be configured for unity gain, the external phase compensation allows for a reduced compensation, yielding improved distortion and slew performance.

The small signal response curve for PA04 shown in Figure 2 helps to illustrate the comparative advantage of external phase compensation. The straight line at 20dB represents a gain of 10 amplifier which if the PA04 were compensated for unity gain would provide a 200 kHz rolloff. Decompensation for a gain of 10 results in a 700 kHz rolloff. In addition, note that loop gain for the unity-gain compensation is only 22 dB at 20 kHz, while it is 30 dB for the gain of 10 compensation. This increase in loop gain results in 2.5 times less distortion at 20 kHz.

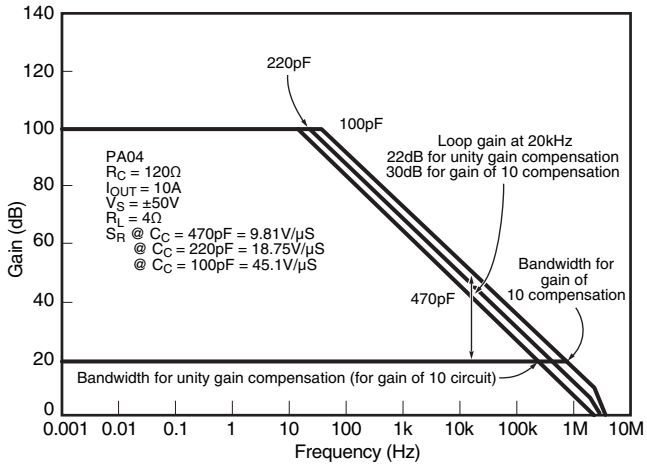


FIGURE 2. THE SMALL SIGNAL RESPONSE FOR THE PA04

The large amount of feedback at low gains obviously reduces distortion. Problems can occur however under transient conditions. If a step function is applied to the input of the amplifier circuit, the output can only change as fast as the amplifier slew rate allows. During this slew interval the input summing node will develop a large differential voltage. This nonlinear condition and input overload can cause a host of difficulties including a slow and poorly behaved recovery from this overload.

Restriction of the input slew rate can avoid these transient distortion problems. The input should never be allowed to slew faster than the amplifier output can follow. If the actual slew rate of the source cannot be predicted or controlled, then simple low pass filtering at the amplifier input will prevent transient distortion.

The filter time constant is a function of amplifier slew rate. The maximum acceptable rate-of-change on the input signal is limited to a value less than the amplifier slew rate divided by the amplifier gain. With a known maximum step function input, the maximum rate-of-change at the low pass filters output occurs at t=0 and is determined by:

$dv/dt = (V/R)/C$

The RC time constant trc required at the amplifier input is:

$trc = (V_{IN}A_V)/S_R$

Where: V_{IN} = PEAK-TO-PEAK INPUT VOLTAGE
A_V = CLOSED LOOP GAIN
S_R = SPECIFIED AMPLIFIER SLEW RATE

Note that there is some reduction in bandwidth with this filter. However, with the PA04 this still permits a 40 kHz bandwidth. This limitation again favors the use of the fastest possible power amplifiers. Keep in mind that transient behavior is actually enhanced by the addition of the input filter.

STABILITY CONSIDERATIONS

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive load creates an additional pole and attendant phase shift in amplifier response (Figure 3). Inductive loads can result in stability problems due to rising impedances at high frequencies. Most follower type output stages are immune to the effects of inductive loads, but collector output, drain output and quasi-complementary output stages with local feedback loops are susceptible to parasitic oscillations driving inductive loads.

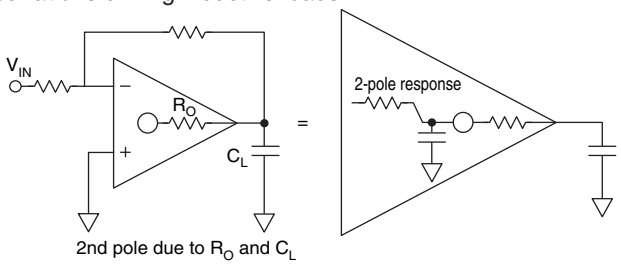


FIGURE 3. CAPACITIVE OP AMP LOADS

Figure 4 shows several measures are available to improve stability, each with some advantage and disadvantage: (a.) Capacitor across feedback resistor. This provides a compensating phase lead in the feedback path to counteract the effects of additional poles. This technique generally requires a unity-gain stable amplifier. (b.) Parallel inductor-resistor combination in

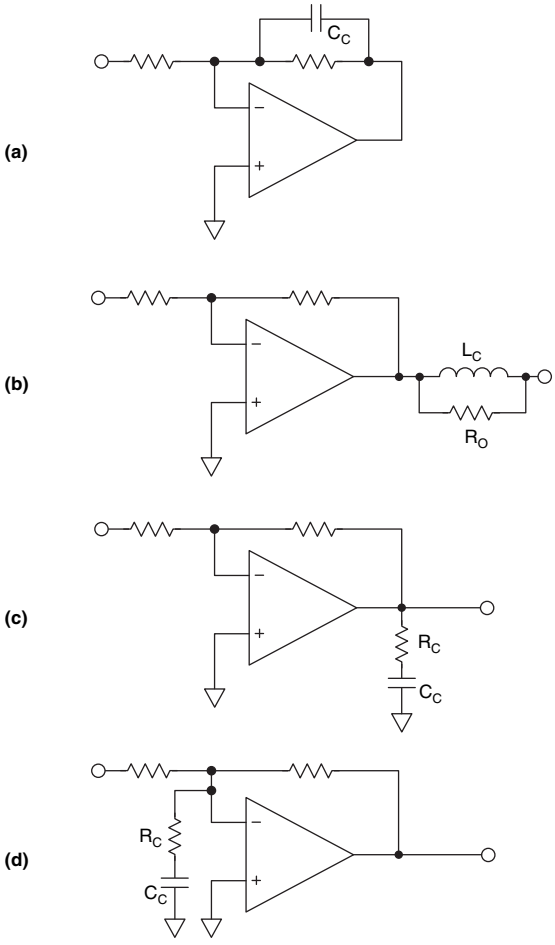


FIGURE 4. STABILITY ENHANCING TECHNIQUES

series with amplifier output. Feedback must be taken directly at output of amplifier so that inductor-resistor has the effect of isolating the amplifier and feedback network from the capacitive load. (c.) Series resistor and capacitor from amplifier output to ground, often referred to as a snubber. Used only in situations where amplifiers are sensitive to inductive loads. Insures a low, resistive load impedance at high frequencies. (d.) Series R-C network across op amp inputs, often referred to as noise-gain compensation. Simply described, this technique reduces feedback at high frequencies to the point where stability is not a problem.

Methods a and b offer the best overall bandwidth performance and transient behavior. Method a has been mentioned already as having the tradeoff of requiring a unity gain stable amplifier. However, with proper attention to design, it is possible to incorporate method a with any amplifier to help control overshoot and ringing behavior.

Method d, the noise gain compensation, will have the effect of reducing the closed loop bandwidth of the resultant circuit to the same effective closed loop bandwidth corresponding to the noise gain. To illustrate, consider a gain of 10 amplifier with a network across the inputs configured for a high frequency noise gain of 100. If the gain of 10 amplifier had an uncompensated bandwidth of 100 kHz, with the noise gain compensation, the bandwidth would be reduced to 10 kHz. In addition, the response curve peaks near the high frequency limit resulting in overshoots in the square wave response.

All amplifiers vary in their ability to tolerate capacitive loading before stability problems occur. PA04 is especially good in this regard tolerating well over 1 uF while operating at a gain of 10. In the case of PA04, no additional stability enhancement measures are required and this is the ideal case for best frequency response.

TYPICAL DESIGN EXAMPLE

A design utilizing all of the guidelines described here would be constructed around a PA04 in an inverting gain of 10 configuration as shown in Figure 5. For additional gain the PA04 is preceded by a small signal op amp also operating at an inverting gain of 10. Many choices are available for this op amp such as the 5534 or OP37. The PA04's tolerance of reactive loads negates the need for additional stability enhancement components.

With an 8 ohm load this circuit can supply over 300W at up to 150 kHz with the input slew rate filter bypassed. With the filter in place, gain begins to rolloff at 40kHz, although full output swing is available up to 150kHz. Distortion never exceeds 0.02% THD. Power supplies will need to be capable of at least 7A to support 8 ohm loads in ac coupled applications. Regulated supplies aren't necessary but are desirable from a reliability standpoint.

When designing for low distortion with PA04, the impedance of the feedback and input networks around the op amp should be kept as low as possible. The input MOSFET's of the PA04 cause it to have a large input capacitance which is nonlinear with variations in input signal. Excessive impedances will increase distortion due to these higher order capacitance effects. The 2K ohm input resistor of Figure 5 is high enough to avoid excessive loading of the small signal op amp and low enough to avoid distortion effects with the PA04.

Several basic practices are important to implement when using PA04. Power supply bypassing consisting of good high frequency capacitors, generally ceramic, must be connected from each supply rail to ground. Unless these capacitors are physically close to the amplifier, parasitic oscillations may occur. Even an inch away from the socket pins is too far. Be sure to read and observe all ESD precautions on the PA04 data sheet, and those shipped with PA04.

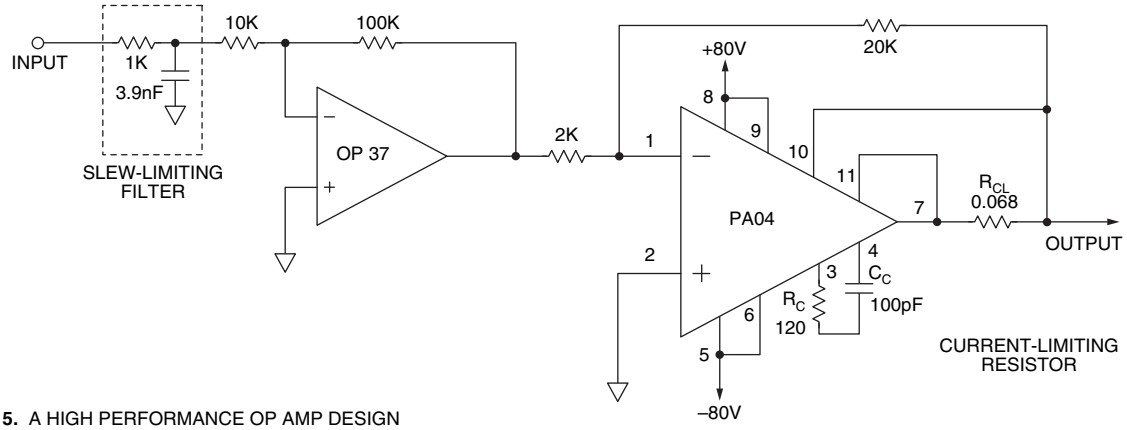


FIGURE 5. A HIGH PERFORMANCE OP AMP DESIGN

Stability for Power Operational Amplifiers

1.0 LOOP STABILITY VS NON-LOOP STABILITY

There are two major categories for stability considerations — Non-Loop Stability and Loop Stability.

Non-Loop Stability covers design areas not related to feedback around the op amp that can cause oscillations in power op amp circuits such as layout, power supply bypassing, and proper grounding.

Loop Stability is concerned with using negative feedback around the amplifier and ensuring that the voltage fed back to the amplifier is less than an additional –180 phase shifted from the input voltage.

The two key factors to troubleshooting an oscillation problem are:

1) What is the frequency of oscillation? (refer to Figure 1 for definitions of UGBW (Unity Gain Bandwidth) and CLBW (Closed Loop Bandwidth) to be used throughout this text)
2) When does the oscillation occur?

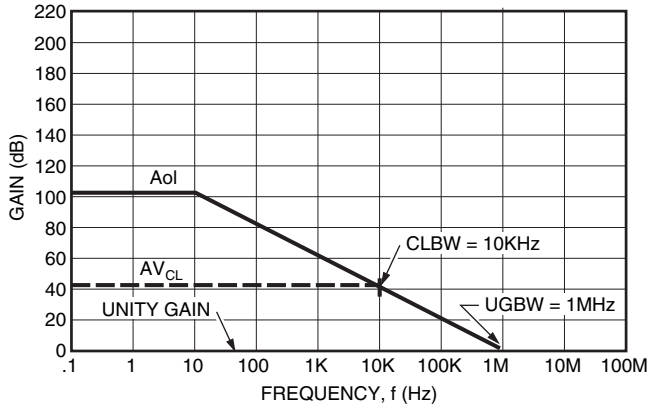


FIGURE 1. DEFINITION OF CLBW & UGBW

The answers to these two questions, along with the sections that follow, should enable you to identify and solve most power op amp stability problems. More importantly, by applying the recommendations in the following sections, you can design power op amp circuits free of oscillation.

2.0 NON-LOOP STABILITY

2.1 CASE GROUNDING

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Ungrounded cases of power op amps can cause oscillations, especially with faster amplifiers. The cases of all Apex Precision Power amplifiers are electrically isolated to allow for mounting flexibility. Because the case is in close proximity to all the internal nodes of the amplifier, it can act as an antenna. Providing a connection from case to ground forms a Faraday shield around the power op amp's internal circuitry that prevents noise pickup and cross coupling or positive feedback.

2.2 RB+ BIAS RESISTOR

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Figure 2 is a standard inverting op amp circuit which includes an input bias current matching resistor on the noninverting input. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. RB+ can form a high impedance node on the noninverting input which will act as an antenna receiving unwanted positive feedback.

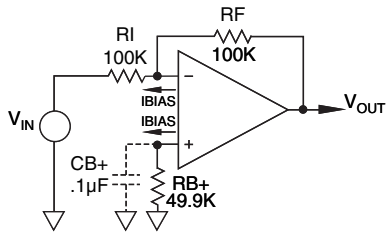


FIGURE 2. RB+

Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of RB+. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave RB+ out, grounding the + input, if possible. If the resistor is required, bypass it with a .1 uF capacitor in parallel with RB+ as shown in Figure 2.

2.3 POWER SUPPLY BYPASSING

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—may or may not

Supply loops are a common source of oscillation problems. Figure 3 shows a case where the load current flows through the supply source resistance and parasitic wiring or trace resistance. This causes a modulated supply voltage to be seen at the power supply pin of the op amp. This modulated signal is then coupled back into a gain stage of the op amp via the compensation capacitor. The compensation capacitor is usually referred to one of the supply lines as an AC ground.

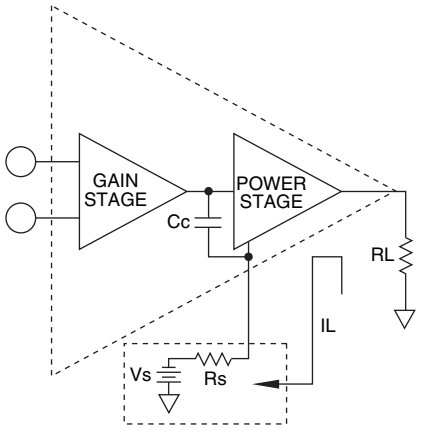


FIGURE 3. IL MODULATION

Figure 4 shows a second case for supply loop oscillation problems. Power supply lead inductance interacts with a capacitive load forming an oscillatory LC, high Q, tank circuit.

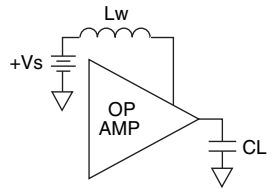
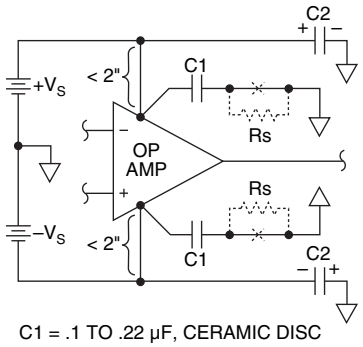


FIGURE 4. LC OSCILLATION

Fortunately, both of the above supply line related problems can be eliminated through the use of proper power supply bypass techniques. Each supply pin must be bypassed to common with a "high frequency bypass" .1uF to .22uF ceramic capacitor. These capacitors must be located directly at the power op amp supply pins. In rare cases where power supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the high frequency bypass capacitor to dampen the Q of the resultant LC tank circuit. This additional resistor will probably only be necessary when using a wideband amplifier since amplifiers of 5 MHz unity gain bandwidth or less will not respond to the high frequency oscillation caused by line inductance interacting with the high frequency bypass capacitor. Refer to Figure 5.



C1 = .1 TO .22 µF, CERAMIC DISC
C2 = 10 µF/AMP OUT (PEAK), ELECTROLYTIC
Rs = 3 –10Ω (PROVISIONAL–
HIGHLY INDUCTIVE P.S. LINES)

FIGURE 5. POWER SUPPLY BYPASSING

In addition, a "low frequency bypass" capacitor, minimum value of 10uF per Ampere of peak output current, should be added in parallel with the high frequency bypass capacitors from each supply rail to common. Tantalum capacitors should be used when possible due to their low leakage, low ESR and good thermal characteristics. Aluminum Electrolytic capacitors are acceptable for operating temperatures above 0°C. These capacitors should be located within 2" of the power op amp supply pins. Refer to Figure 5.

2.4 MULTIPLE AMPLIFIER BOARDS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} =0?—yes

A prototype circuit is built and bench tested to confirm desired performance. Several channels of the same circuit are used on a printed circuit board layout. Much to the dismay of the design engineer, the amplifier circuits on the printed circuit board oscillate. Cross coupling through the power supply lines can be a major problem on multiple amplifier printed circuit boards. Ground the case of each amplifier and ensure each amplifier has its own power supply bypassing per Section 2.3.

2.5 OUTPUT STAGE OSCILLATIONS / OUTPUT R-C SNUBBER

* fosc > UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?— no, only oscillates over a portion of the output cycle

Sometimes output stages of power op amps can contain local feedback loops that give rise to oscillations. The first type of output stage instability problem arises from a tendency of emitter followers to appear inductive when looking back into their emitter. This occurs if they are driven from a low impedance source and can create output stage oscillations if capacitance is present on the amplifier's output. Refer to Figure 6. This type of instability is rare and usually only shows up when driving load capacitances within a limited range of values.

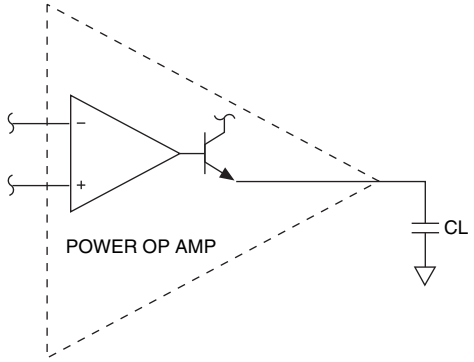


FIGURE 6. EMITTER FOLLOWER WITH C LOAD

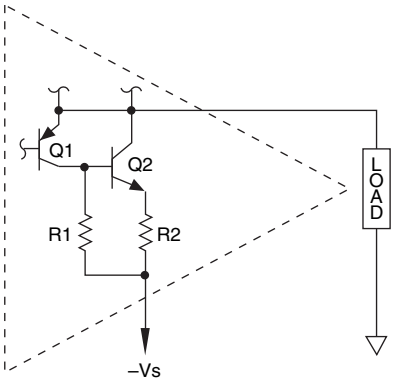


FIGURE 7. COMPOSITE OUTPUT STAGE

The second, more common type of output stage oscillation is due to non-emitter follower output type stages. These stages have heavy local feedback paths. Refer to Figure 7 which is an

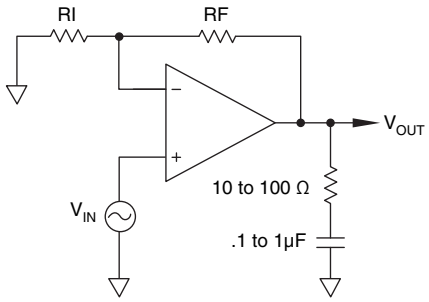


FIGURE 8. OUTPUT R–C SNUBBER

example of a composite PNP type output stage. This stage is typical of monolithic power op amps where high current PNP transistors are not readily available. The local feedback in the Q1, Q2 loop will cause output stage oscillations when the output swings negative under reactive loading.

Both of these output stage problems can be fixed by using an R-C Snubber on the output of the op amp to ground or the negative supply rail. This is provided the negative supply rail is properly bypassed per Section 2.3. The Snubber network consists of a 10 to 100 ohm resistor in series with a capacitor of .1 to 1 µF (refer to Figure 8). This network lowers the high frequency gain of the output stage preventing unwanted high frequency oscillations.

2.6 GROUND LOOPS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

Ground loops come about from load current flowing through parasitic layout resistances and wiring. If the phase of the output signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (RR in Figure 9) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a “star ground” approach. Refer to Figure 9. The star ground is a point that all grounds are referenced to. It is a common point for load ground, amplifier ground, signal ground and power supply ground.

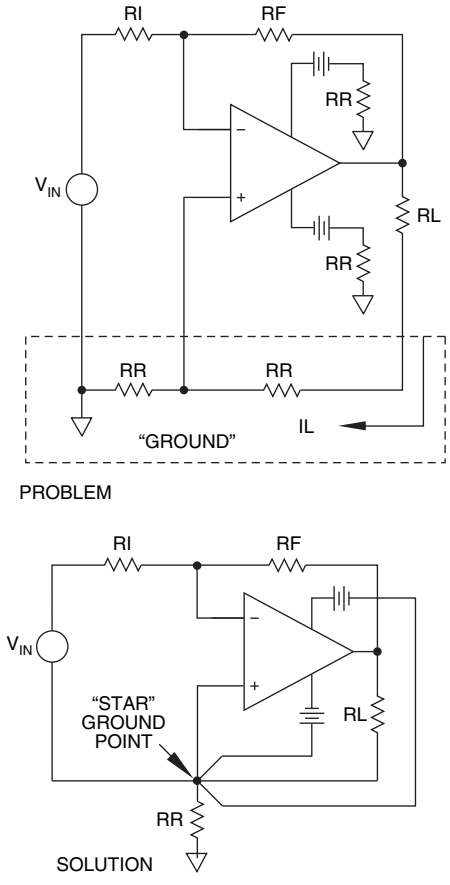


FIGURE 9. GROUND LOOPS

2.7 PRINTED CIRCUIT BOARD LAYOUT

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—no

High current output traces routed near input traces can cause oscillations. This is especially true when the output is adjacent to the positive input, giving undesirable positive feedback through capacitive coupling between the adjacent traces. Feedback, input, and bypass components, along with current limit sense resistors, should be located in close proximity to the amplifier.

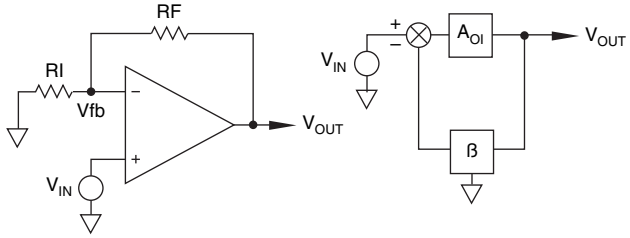
If a printed circuit board has both a high current output trace and a return trace for that high current, then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form a twisted pair type of layout. This will help cancel EMI generated outside from feeding back into the amplifier circuit.

3.0 LOOP STABILITY

3.1 BETA SS - FEEDBACK FACTOR

Control theory is applicable to closing the loop around a power op amp. The block diagram in Figure 10 consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the ß represents the feedback network. The value of ß is defined as the fraction of the output voltage that is fed back to the input; therefore, ß can range from 0 (no feedback) to 1 (100% feedback).

The term Aol ß that appears in the V_{OUT}/V_{IN} equation in Figure 10, has been called “loop gain” because this can be thought of as a signal propagating around the loop that consists of the Aol and ß networks. If Aol ß is large, there is a lot of feedback. If Aol ß is small, there is not much feedback.



$$Vfb = \frac{V_{OUT}\ RI}{RI + RF}$$

$$Vfb = ß\ V_{OUT}$$

$$ß = \frac{RI}{RI + RF}$$

$$V_{OUT} = V_{IN}\ Aol - Aol\ ß\ V_{OUT}$$

$$\frac{V_{OUT} + Aol\ ß\ V_{OUT}}{V_{IN}} = Aol$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Aol}{1 + Aol\ ß} = \frac{1}{ß}$$

(FOR: Aol b >> 1)

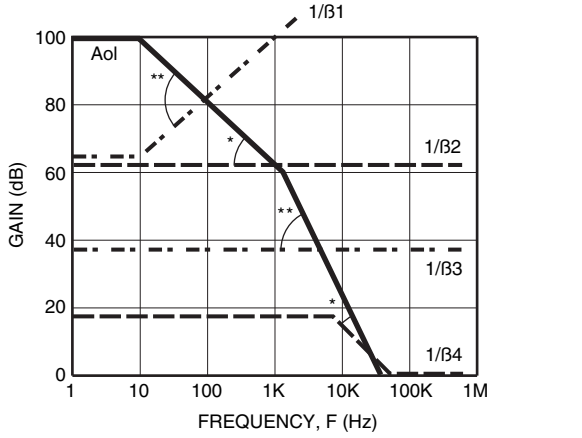
FIGURE 10. BETA (ß) – FEEDBACK FACTOR

3.2 RATE OF CLOSURE & STABILITY

Refer to Figure 11. Aol is the amplifier’s open loop gain curve. 1/ß is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/ß curve is the “loop gain”. Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure when loop gain goes to zero, open loop phase shift must be less than 180 degrees where the 1/ß curve intersects the Aol curve. Another way of viewing that same criteria is to say at the intersection

of the 1/ß curve and the Aol curve the difference in the slopes of the two curves, or the RATE OF CLOSURE, is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.



* 20 dB/ DECADE RATE OF CLOSURE → "STABILITY"
** 40 dB/ DECADE RATE OF CLOSURE → "MARGINAL STABILITY"

FIGURE 11. RATE OF CLOSURE & STABILITY

A 40 dB per decade RATE OF CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Figure 11 contains several examples of both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

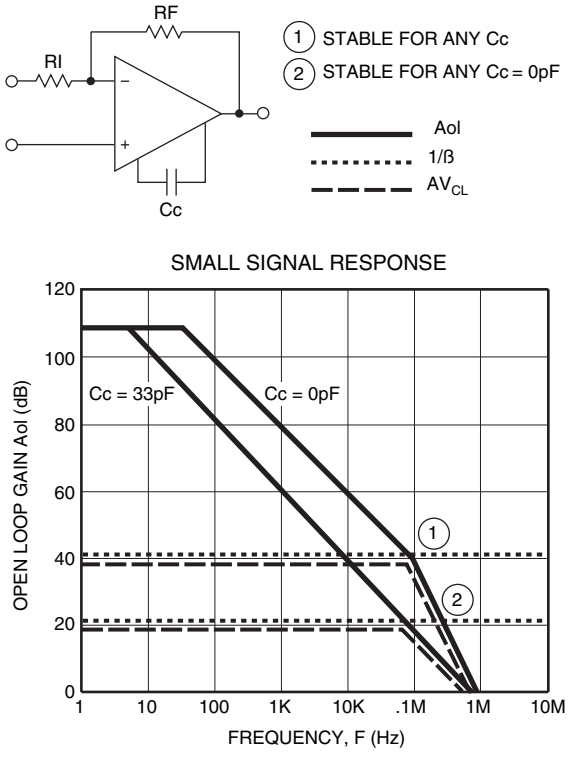


FIGURE 12. EXTERNAL PHASE COMPENSATION

3.3 EXTERNAL PHASE COMPENSATION

External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the op amp. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I = CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In Figure 12 we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc = 33pF, to a two pole response with Cc = 0pF. Curve 1 illustrates that for 1/ß of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc = 33pF or Cc = 0pF). Notice that 1/ß curve continues on past the intersection of the Aol curve. At the intersection of 1/ß and Aol, the AV_{CL} closed loop gain curve, or V_{OUT}/V_{IN} gain begins to roll off and follow the Aol curve. This is because there is no loop gain left to keep the closed loop gain flat at higher frequencies.

Curve 2 illustrates that for 1/ß of 20 dB and Cc = 0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc = 0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

3.4 STABILITY - RATE OF CLOSURE

Figure 13 shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional V_{NOISE}

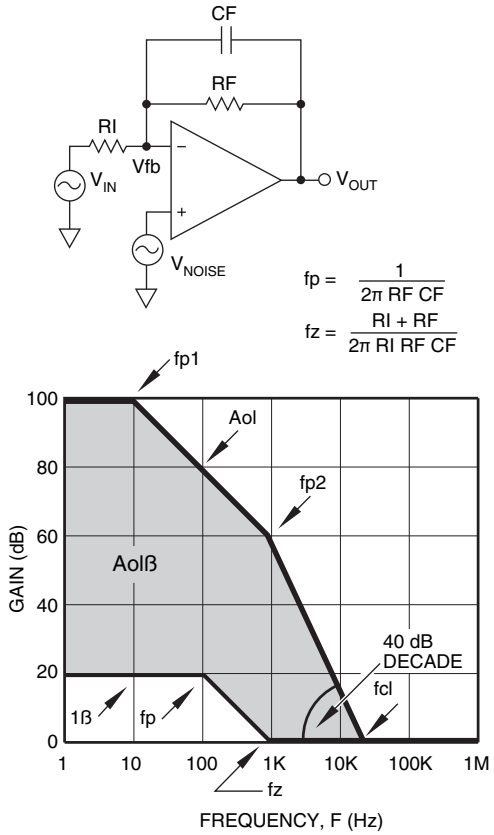


FIGURE 13. STABILITY– RATE OF CLOSURE

voltage source shown at the +input of the op amp. This is shown to aid in conceptually viewing the 1/ß plot.

An inverting amplifier with its +input grounded, will always have potential for a noise source to be present on the +input . Therefore, when one computes the 1/ß plot, the amplifier will appear to run in a gain of 1 + RF/RI for small signal AC. The V_{OUT}/V_{IN} relationship will still be –RF/RI. This is also why an amplifier can never run at a gain of less than one for small signal AC stability considerations.

The plot in Figure 13 shows the open loop poles from the amplifier's Aol curve, as well as the poles and zeroes from the 1/ß curve. The locations of fp and fz are important to note as we will see that poles in the 1/ß plot will become zeroes and zeroes in the 1/ß plot will become poles in the open loop stability check.

Notice that at fcl the RATE OF CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/ß curve is labelled Aol ß which is also known as loop gain.

3.5 STABILITY - OPEN LOOP

Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. Refer to Figure 14. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure the open loop phase does not dip to –180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180, the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice in Figure 14 this open loop plot is really a plot of Aol ß. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/ß plot in Figure 13 became a pole in the open loop plot in Figure 14 and likewise the pole from the 1/ß plot in Figure 13 became a zero in the open loop plot of Figure 14. We will use this knowledge to plot the open loop phase plot to check for stability. This plot of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/ß curve and the Aol curve.

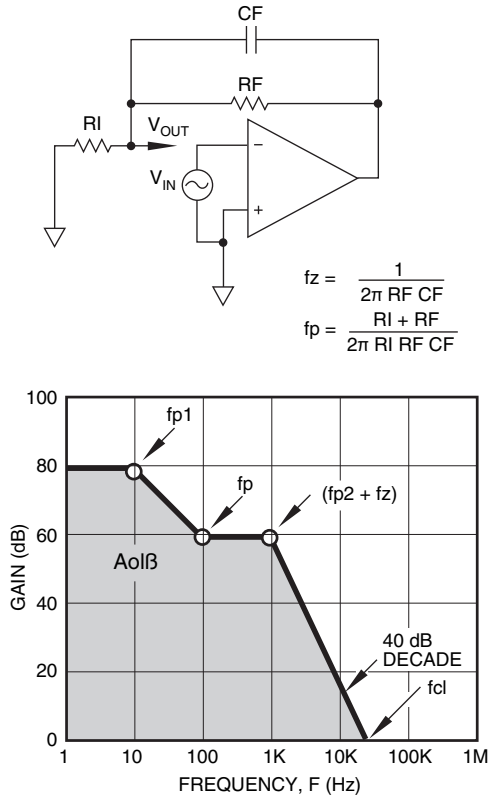


FIGURE 14. STABILITY– OPEN LOOP

4.0 STABILITY & THE INPUT POLE / INPUT & FEEDBACK IMPEDANCE

* fosc < CLBW
* oscillates unloaded?—yes
* oscillates with V_{IN} = 0?—yes

All op amps have some input capacitance, typically 6-10 pF. Printed circuit layout and component leads can introduce additional input stray capacitances. When high values of feedback and input resistors are used, this input capacitance will contribute an additional pole to the loop gain response (a zero in the 1/ß plot, a pole in the open loop phase check for stability, or a pole in the Aol ß, loop gain, plot).

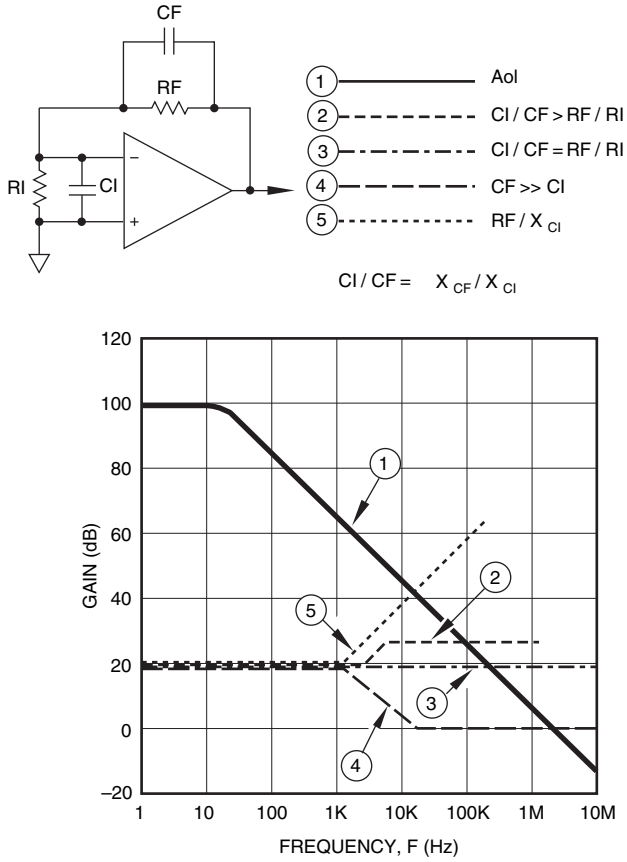


FIGURE 15. THE INPUT POLE

We will refer to Figure 15 for a detailed look at the input pole and stability. Remember, our first order criteria for stability is a

Rate Of Closure of 20dB per decade or less. Curve 1 is the op amp's AoI plot. Curve 5 shows the effect of input capacitance with no CF feedback capacitor. We see the rate of closure is 40 dB per decade and marginal stability exists. With just CI present, as frequency increases, the impedance from the -input of the op amp decreases, thereby causing the 1/ß plot to increase (remember $X_{CI} = 1/2\pi fCI$). If we now add some small value of CF as in Curve 2 we see the 1/ß plot flatten out to intersect the AoI at a rate of closure 20 dB per decade implying stability. If we further increase CF, as in Curve 3, such that both breakpoints are the same frequency, we will have ZF/ZI constant over frequency and the 1/ß plot will be flat with frequency. This yields the ever-stable 20 dB per decade rate of closure. If we then continue to increase CF as in Curve 4, we will see CFdominate as frequency increases and the net result is a low pass filter frequency roll-off. For this case the op amp must be unity gain stable, since the op amp operates at a gain of one for frequencies above 10KHz.

Often you will see CF recommended to be used to decrease overshoot and improve settling time for a transient input into a given op amp circuit. In the AC small signal domain, we are merely optimizing the circuit for stability.

Minimize values of feedback and input resistor values. This will reduce the effect of the input pole as well as help reduce DC errors by keeping voltage drops due to bias currents low. A summing node of an op amp can pick up unwanted AC signals and amplify them if that node is high impedance. Keeping the feedback and input resistance values low will reduce the impedance at the summing nodes and minimize stray signal pick up. Practical values for feedback and input resistance values are from 100 ohms to 1 megaohm.

5.0 LOOP STABILITY EXAMPLES

5.1 VOLTAGE TO CURRENT CONVERSION— FLOATING LOAD

* fosc < CLBW
* oscillates unloaded ? — yes
* oscillates with $V_{IN} = 0$? — yes

Figure 16 illustrates a common voltage to current conversion circuit. The input command voltage of +/-10V is scaled to control -/+1.67A of output current through the load.

This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

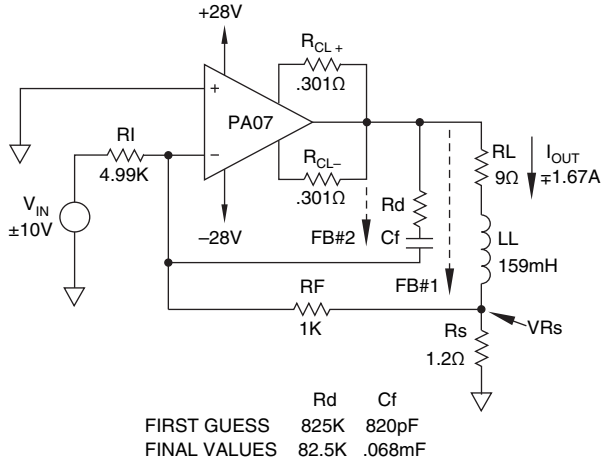


FIGURE 16. V-I CIRCUIT AND STABILITY

The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply -RF/RI which translates to (–1K/4.99K = -.2004). The Iout/Vin relationship is then VRs/Rs or Iout = - Vin (RF/RI)/Rs which for this circuit is (Iout = -.167 Vin). We will use our knowledge of 1/ß, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

STABILITY SOLUTION FOR V-I CIRCUIT

STEP 1: On Figure 17 plot the op amp's AoI curve as given by the manufacturer.

STEP 2: On Figure 17 plot FB#1. Refer to Figure 18 for calculation of FB#1. At DC, LL is a short and so ß is a voltage divider through resistors as shown in Figure 18. As we go to higher frequencies, the reactance of LL will increase (XL = 2πfL). This will increase the net load impedance which will cause ß to decrease and 1/ß to increase as frequency increases. Since we are working with a single reactive element the increase of that gain will be 20 dB per decade. Figure 18 details the breakpoint fz where this increase begins. We see that at the intersection of FB#1

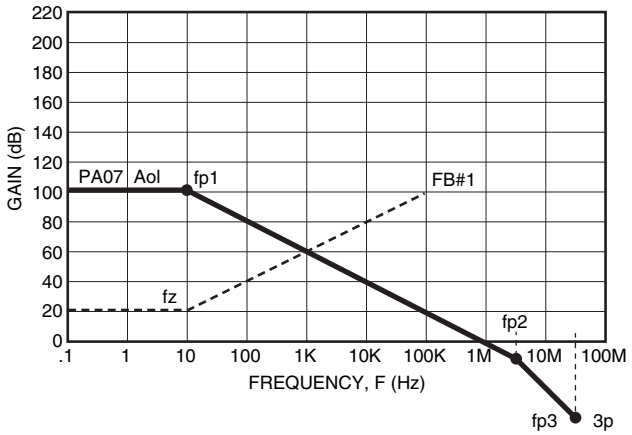


FIGURE 17. AoI AND FB # 1 – MAGNITUDE PLOT FOR STABILITY

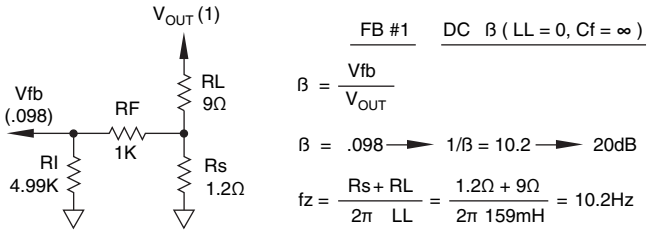


FIGURE 18. FEEDBACK NO.1 (FB #1)

and the PA07 AoI curves the rate of closure is 40 dB per decade indicating marginal stability.

STEP 3: Refer to Figure 19 which repeats PA07 AoI and FB#1. We will add FB #2 to force the high frequency part of the 1/ß curve to flatten out and intersect the PA07 AoI curve at 20 dB per decade. FB #2 will dominate at frequencies above 1 KHz. Although our V-I circuit has two feedback paths, the op amp will follow whichever feedback path is dominant. This means the larger ß is, the more voltage is fed back from the output to the -input as negative feedback (Remember $ß = Vfb/V_{OUT}$). With a larger ß, 1/ß will

become smaller; therefore, the dominant feedback path out of FB#1 and FB#2 will be the lowest gain path.

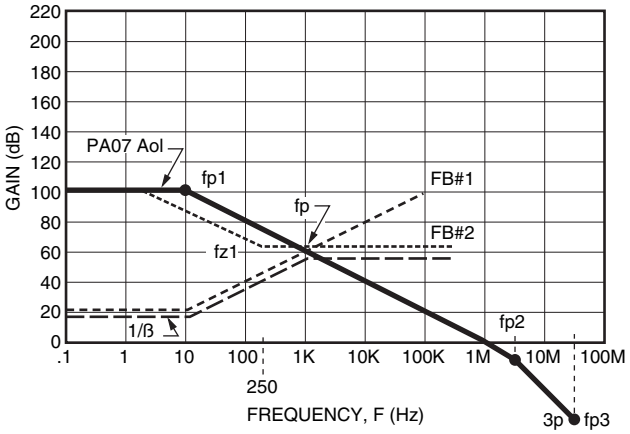


FIGURE 19. FIRST GUESS MAGNITUDE PLOT FOR STABILITY

Plot a desired feedback path for FB#2. At high frequencies, FB#2 will be a flat line since Cf will be a short leaving a pure resistive divider for ß. At DC, FB#2 will be infinite since Cf is an open. This will be limited by the PA07 Aol curve. Since we only have one reactive element in FB#2, we will have a 20 dB per decade slope from low to high frequency. Set fz1 one half to one decade below the intersection of FB#1 and FB#2. This "Decade" rule of thumb ensures that as component values and Aol curves vary we will not get into stability trouble—more about this later.

STEP 4: In Figure 19 the long-dashed line represents the 1/ß feedback path that the PA07 operates in for small signal AC. According to our first order check for stability we see a 20 dB per decade rate of closure indicating a stable design. But let's do our complete stability check by using the 1/ß curve and PA07 Aol curve to plot the open loop phase plot. Remember the following rules when plotting open loop phase plots for stability checks.

RULES FOR PLOTTING OPEN LOOP PHASE PLOTS

1) Poles in 1/ß plot become zeroes in the open loop stability check.
2) Zeroes in 1/ß plot become poles in the open loop stability check.
3) Poles and zeroes in the Aol curve of the op amp remain respectively poles and zeroes in the open loop stability check since the op amp Aol curve is an open loop curve already.
4) Phase for poles is represented by a -45 degree phase shift at the frequency of the pole with a -45 degree per decade slope, extending this line with 0 degree and -90 degree horizontal lines.
5) Phase for zeroes is represented by a +45 degree phase shift at the frequency of the zero with a +45 degree per

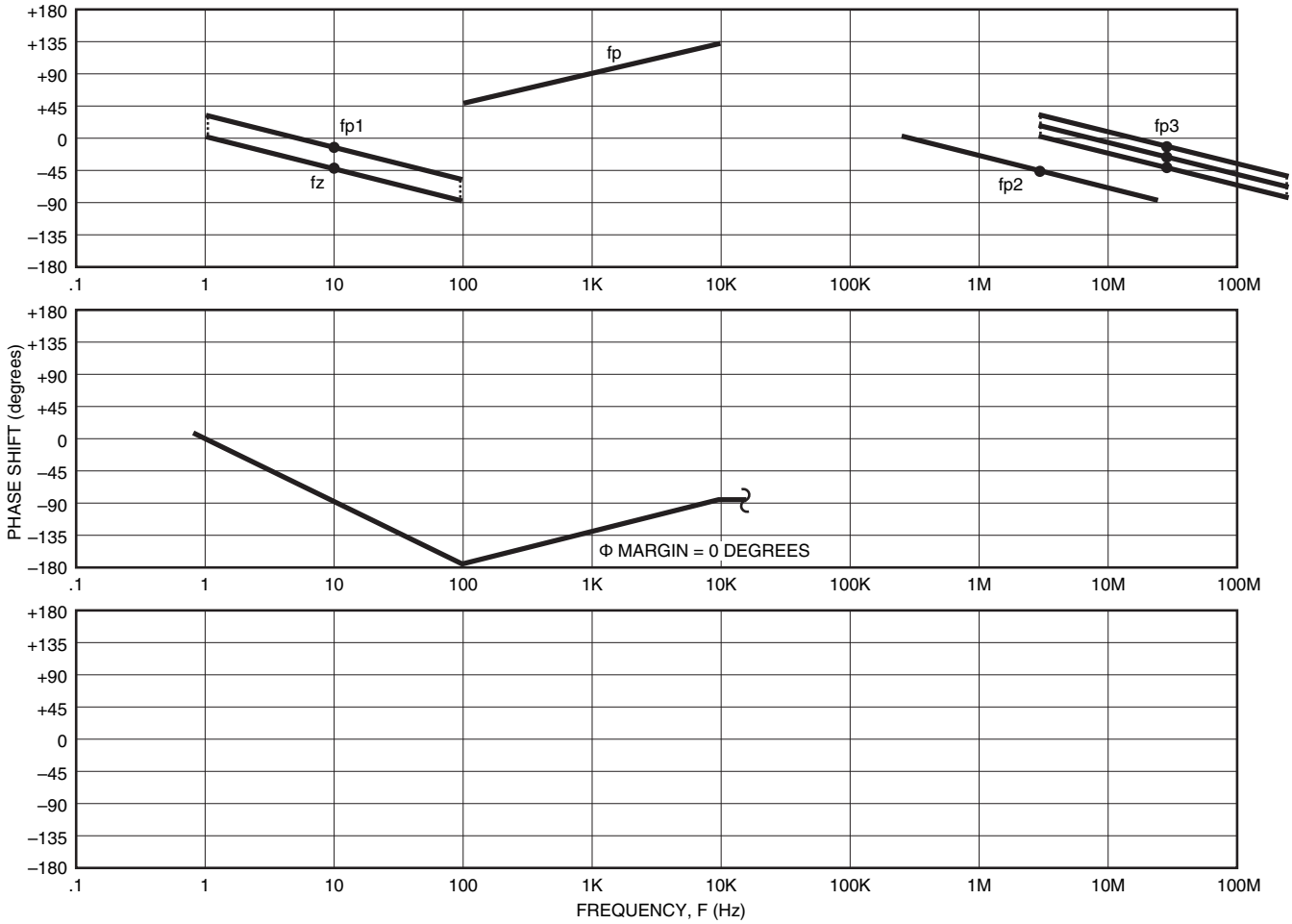


FIGURE 20. FIRST GUESS OPEN LOOP PHASE PLOT FOR STABILITY

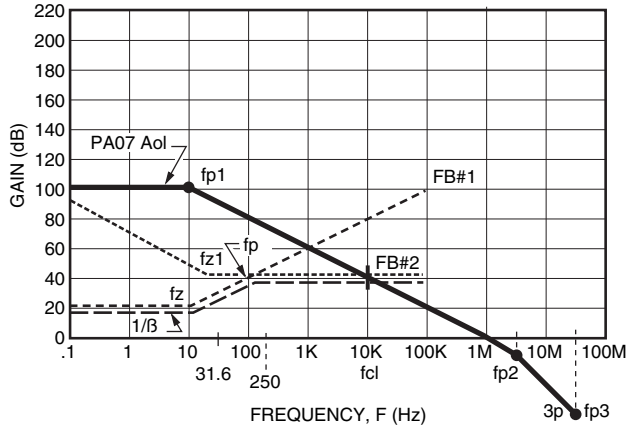


FIGURE 21. FINAL VALUE MAGNITUDE PLOT FOR STABILITY

decade slope, extending this line with 0 degree and +90 degree horizontal lines.

Figure 20 is the resultant open loop phase plot using the information from Figure 19. After plotting individual open loop poles and zeroes, and drawing the appropriate slopes, we graphically add the slopes to yield a resultant open loop phase as shown in Figure 20. Notice fp3 in Figure 20 is a triple pole. It is easier to plot this as shown in Figure 20 as three poles "on top" of each other. This makes it easier to add graphically for a resultant open loop phase plot. As shown in Figure 20, our open loop phase dips to -180 at 100Hz. Our first attempt at compensation was not successful since we desire at least 45 degrees of phase margin (open loop phase should not dip to less than -135 degrees).

STEP 5: We need to revisit FB#2 to make this V-I circuit stable. Figure 21 shows a new FB#2 and the resultant 1/ß plot. Before we look at the open loop phase plot, let's discuss Figure 21. We see that in the PA07 Aol curve there is a pole at fp1, 10Hz, which will be a pole in our open loop phase plot. We also see a zero at fz, 10Hz, in the 1/ß plot, which will become a pole in our open loop phase plot. Now we have two poles at 10Hz in our open loop phase plot. To keep the open loop phase from reaching -180, we must add a zero at 100Hz to get 45 degrees of phase margin. Poles and zeroes a decade beyond fcl, the intersection of 1/ß and PA07 Aol, are of no concern for stability since at fcl the loop gain is zero. The reason we must look a decade beyond fcl on the magnitude plot is that poles and zeroes have an effect on phase plus or minus a decade away from their physical location on the magnitude plot.

Viewing the magnitude plot in this way can help us save iterative steps in compensating to guarantee good stability. Refer to Figure 22 for final open loop phase plot stability.

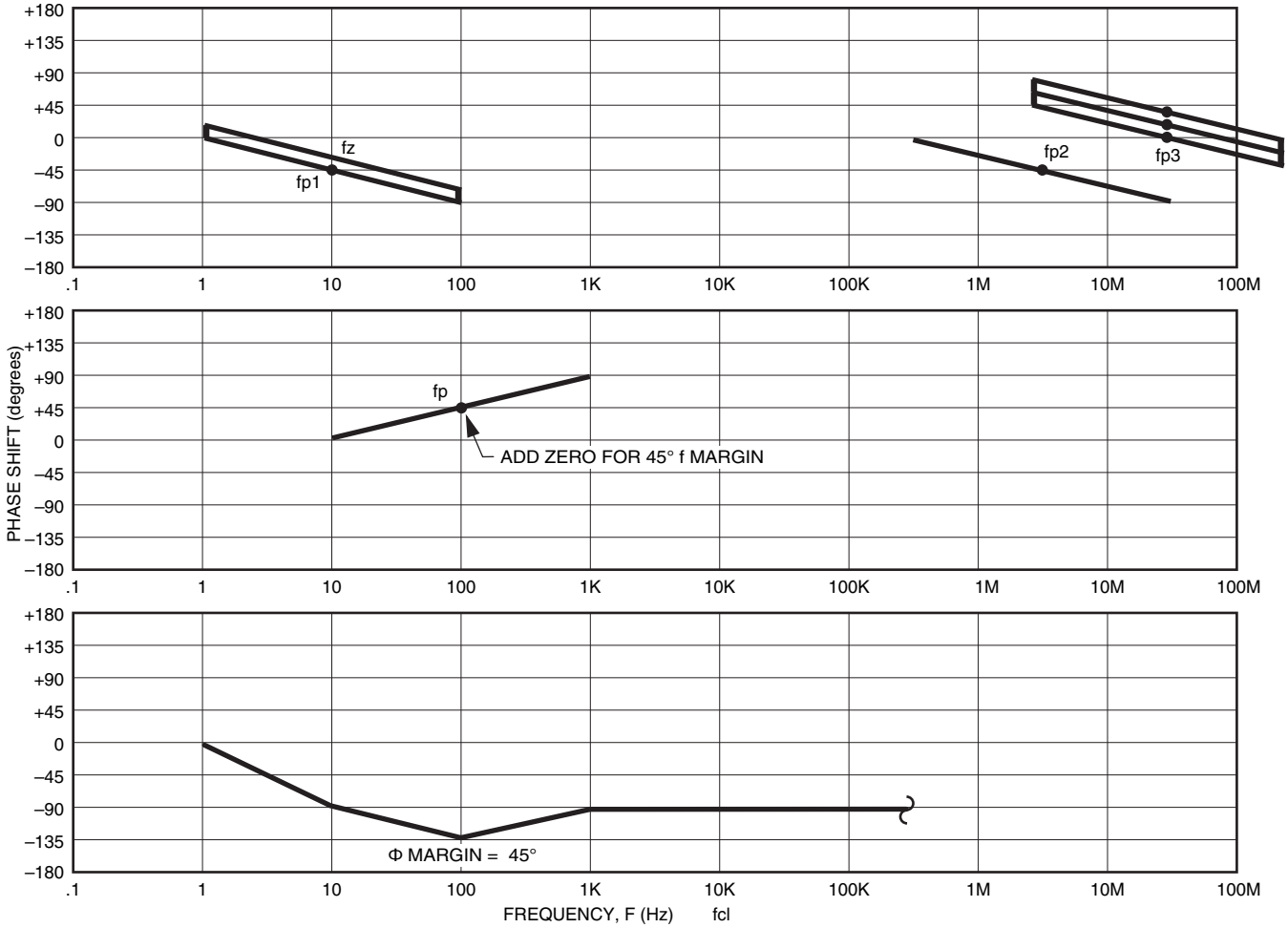


FIGURE 22. FINAL VALUE OPEN LOOP PHASE PLOT FOR STABILITY

Once the open loop phase plot verifies stability, it is time to compute final values for FB#2 components Rd and Cf. Figure 23 (next page) details these calculations. Notice in Figure 23 that to work with ß it is easiest to set Vout to 1 which then allows us to easily use voltage dividers and currents to calculate values for Rd. Cf is computed as given by the formula in Figure 23.

OPEN LOOP PHASE PLOTS FOR STABILITY — FINAL NOTE:

This hand plotting technique is a linear graphical method. Actual magnitude plots run on such analog circuit simulations as SPICE will be 3 dB different and actual phase plots will be 6 degrees different.

5.2 CAPACITIVE LOADING & STABILITY

* fosc < CLBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

5.2.1 CAPACITIVE LOADING - GENERAL

Refer to Figure 24 (next page) for discussion of power op amps and capacitive loading. The output impedance of a power op amp, Ro, can interact with capacitive loads and form an additional high frequency pole in the op amp's Aol curve. This modified Aol curve is what we must look at for stability checks. In Figure 24, we see a modified Aol curve whose slope changes from 20 dB per decade to 40 dB per decade at 10 kHz. Note that the rate of closure for this circuit is 40 dB per decade indicating marginal stability.

5.2.2 CABLE AND CAPACITIVE LOADING

Beware of coaxial cables which can appear capacitive. A coaxial cable appears capacitive, instead of its characteristic impedance, resistive, if the length of the cable is less than one-fortieth of the wavelength in the cable at the frequency of interest, f. This length, l, is given by:

$$l \leq \frac{1}{40}\,\frac{Kc}{f}\ \text{meters}$$

where K is a propagation constant that is sometimes called the velocity factor (0.66 for coaxial cable) and c is the velocity of light (3.00 X10^8 m/s).

EXAMPLE: If f = 10KHz:

$$l \leq \frac{1}{40}\,\frac{(0.66)\ (3\text{x}10^8)}{10^4} = 495\ \text{meters (1624 feet)}$$

Cables less than 495 meters will appear capacitive for 10 kHz signals at the rate of 95 pF/meter (29 pF/foot) for RG-58A/U, a commonly used coaxial cable.

5.2.3 AMPLIFIER OUTPUT IMPEDANCE, RO AND CAPACITIVE LOADING

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp.

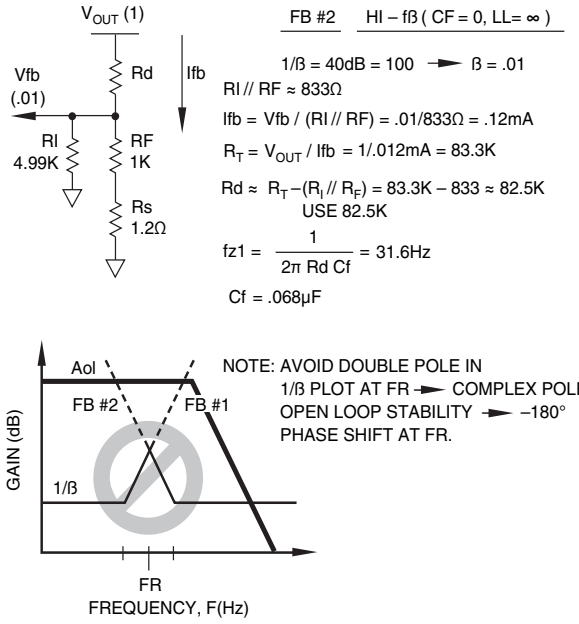
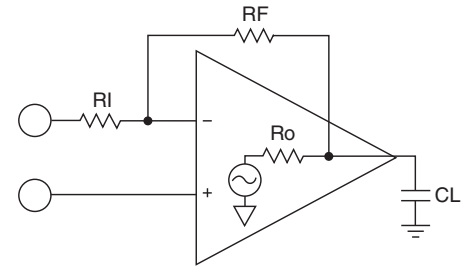


FIGURE 23. FEEDBACK NO. 2 (FB #2) FINAL VALUE CALCULATIONS



UNITY GAIN STABLE AMPLIFIER
BUT: UNSTABLE 40 dB/DECADE WITH CL

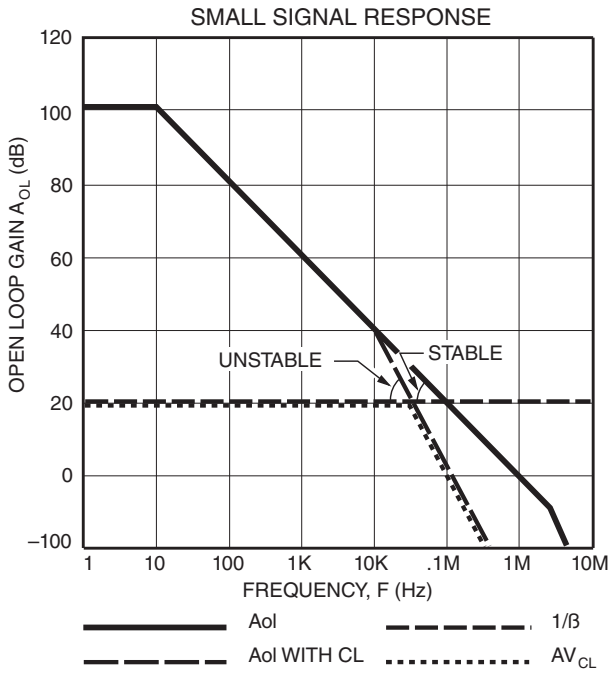


FIGURE 24. CAPACITIVE LOADING

Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Within the bandwidth of the amplifier the output impedance of most Apex Precision Power power op amps appears predominantly resistive. As an output stage drives higher currents, its output impedance changes when compared to the low current or unloaded output impedance. In general, this impedance reduces as current is driven through the output stage.

When compensating circuits with capacitive loading we will use the low current or unloaded output impedance for Ro. This will be the highest value of Ro causing the lowest frequency additional pole which modifies an amplifier's Aol curve when driving a capacitive load. Many designs in the past have verified that compensating for this condition will give the best stability for all conditions when driving capacitive loads.

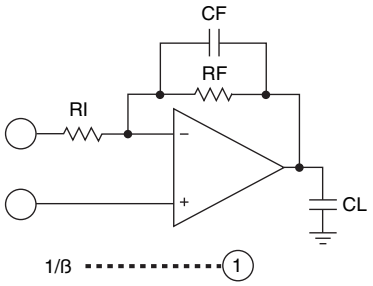
The following is a list of output impedances for Apex Precision Power power op amps and boosters.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA01	2.5-8.0 ohms
PA02	10-15 ohms
PA03	25 ohms
PA04	2.0 ohms
PA05	5 ohms
PA07	1.5-3.0 ohms
PA08	1.5K-1.9K ohms
PA09	15-19 ohms
PA10	2.5-8.0 ohms
PA12	2.5-8.0 ohms
PA19	30-40 ohms
PA51	1.5-1.8 ohms
PA61	1.5-1.8 ohms
PA73	1.5-1.8 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8K ohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

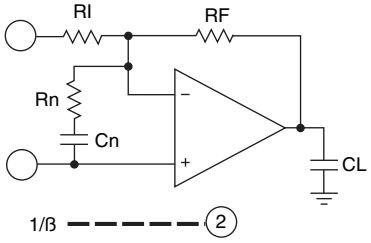
5.2.4 COMPENSATING CAPACITIVE LOADS

There are two main ways to compensate for capacitive loads or two pole Aol curves. The "Feedback Zero" and "Noise Gain" or "Input R-C Network" compensation techniques for capacitive loads will both be discussed.

The "Feedback Zero" technique uses a pole in the 1/ß plot (a zero in the open loop phase check for stability or a zero in the Aol ß, loop gain, plot) to compensate for the additional pole due to capacitive loading in the amplifier's modified Aol curve. Refer to Figure 25. Note that in Curve 1 there is both a pole and zero in this 1/ß plot. The pole is due to the interaction of Rf and Cf. The zero can be found by graphically extending the 1/ß plot to zero dB. Remember from previous discussion that an op amp cannot operate at a gain of less than 1 for small signal AC.



FEEDBACK ZERO COMPENSATION



NOISE GAIN COMPENSATION

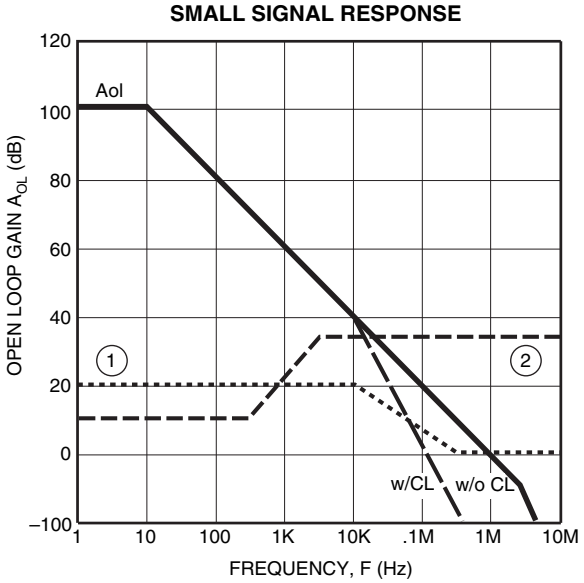


FIGURE 25. CAPACITIVE LOAD COMPENSATION

The "Noise Gain" compensation technique raises the small signal AC gain of the amplifier to run at a gain that is high enough to ignore the additional high frequency pole in the Aol curve due to capacitive loading. Refer to Figure 25. Curve 2 shows the 1/ß plot for noise gain compensation.

Notice in Figure 25 that both Curve 1 and Curve 2 yield a 20 dB per decade rate of closure implying stability; whereas, with just resistive feedback at the given gains the circuits would be unstable with a 40 dB per decade rate of closure.

5.2.4.1 FEEDBACK ZERO COMPENSATION

Figure 26 illustrates a circuit utilizing Feedback Zero Compensation for stability when driving a capacitive load. Figure 27 is our magnitude plot to work with for stability. The following procedure will ensure a logical approach to optimize stability:

$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10\ kHz$$

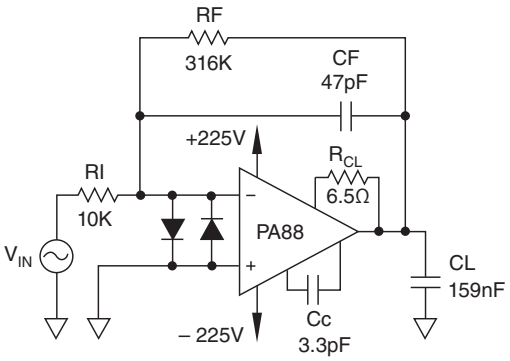


FIGURE 26. FEDBACK ZERO COMPENSATION FOR CL

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms.
The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 26.

STEP 2: Calculate DC ß for circuit.
DC ß = RI/(RF + RI) = 10K/(316K+10K) = .030674846
DC 1/ß = 20 Log (1/.030674846) = 30.26 dB

STEP 3: Plot DC 1/ß. Add pole in 1/ß plot to compensate for fp2. Ensure fp5 is one-half to one decade away from

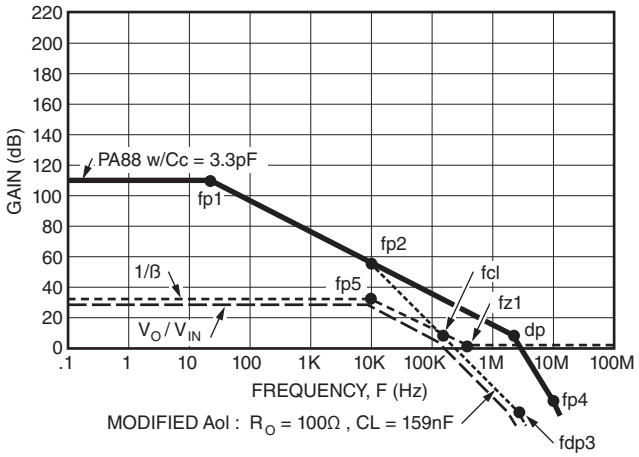


FIGURE 27. FEEDBACK ZERO COMPENSATION FOR CL MAGNITUDE PLOT FOR STABILITY

fcl such that if the modified Aol plot in the real world moves to the left towards lower frequency we will not be back at a 40 dB per decade rate of closure. Note in Figure 27 that the 1/ß plot has fp5 and fz1. The feedback network continues to feed back output voltage beyond fcl until we reach 0 dB. Then the 1/ß plot flattens out at 0 dB. It is important to include fz1 since it will be a pole in our open loop phase check

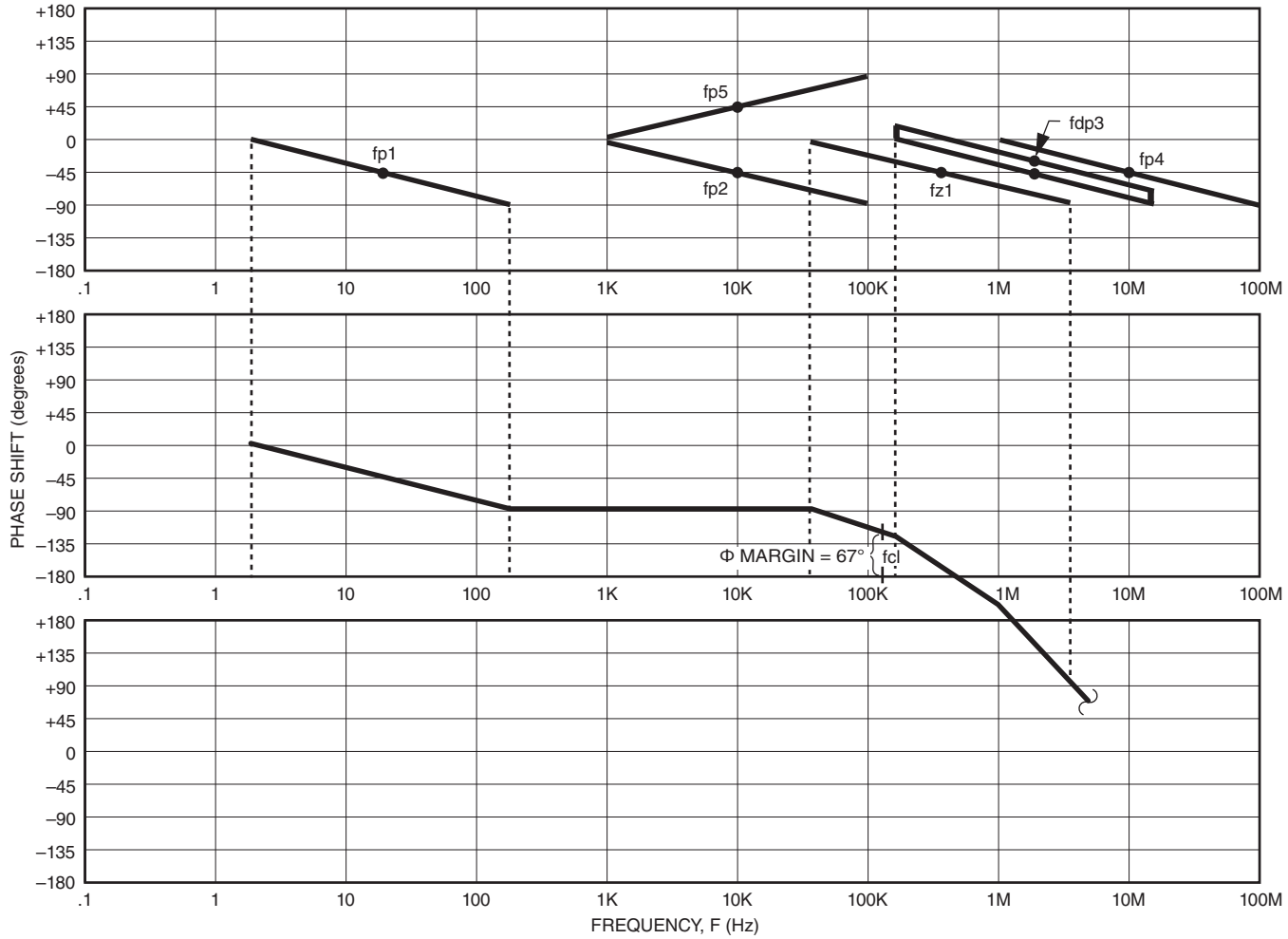


FIGURE 28. FEEDBACK ZERO COMPENSATION FOR CL OPEN LOOP PHASE PLOT FOR STABILITY

and will affect phase at frequencies lower than fcl. At fcl loop gain is zero and beyond fcl we are not concerned with phase shift to guarantee stability. Note that the V_O/V_{IN} plot follows the 1/ß plot until at which point there is no loop gain and V_O/V_{IN} will follow the Aol curve on down in gain.

STEP 4: Plot open loop phase as in Figure 28. We see we have 67 degrees of phase margin and therefore guaranteed stability.

STEP 5: Once you have chosen CF to get the fp5 you want you automatically set fz1. fz1 can be gotten graphically from the 1/ß plot. For those of you who want exact breakpoints, here are the formulae for the 1/ß plot in Figure 27.

$$fp5 = \frac{1}{2\pi\ RF\ CF}$$

$$fz1 = \frac{RI + RF}{2\pi\ CF\ RI\ RF}$$

5.2.4.2 NOISE GAIN COMPENSATION

Figure 29 illustrates how Noise Gain compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, V_O/V_{IN} will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/ß plot of the feedback as when Cn becomes a short and if Rn << RI the gain will be set by RF/Rn. Figure 29 shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in Figure 29 that the V_O/V_{IN} relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the V_O/V_{IN} curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/ß plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency flat part of the noise gain no higher in magnitude than 20 dB greater than the low frequency gain. This will force fp and fz in Figure 29 to be no more than a decade apart. This will also keep the phase from dipping to -135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional -90 degrees in the open loop phase plot. Keep fp one half to one decade below fcl to prevent a rate of closure of 40 dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world.

Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/ß plot. Once again for completeness, here are the formulae for noise gain poles and zeroes:

$$fp = \frac{1}{2\pi\ Rn\ Cn} \qquad fz = \frac{RF + RI}{(2\pi)\ (Cn)\ (RFRI + RFRn + RIRn)}$$

$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10KHz$$

Figure 30 illustrates a circuit utilizing noise gain compensation for stability when driving a capacitive load. Figure 31 is our magnitude plot to work with for stability.

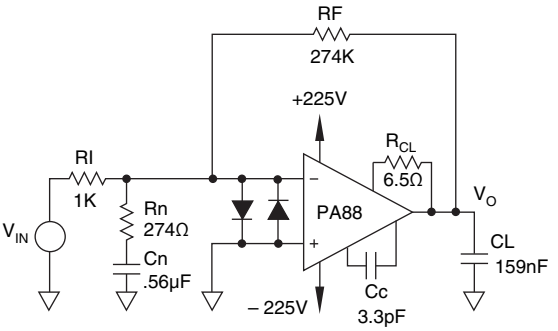


FIGURE 30. NOISE GAIN COMPENSATION FOR CL

The following procedure will ensure a logical approach to optimize stability:

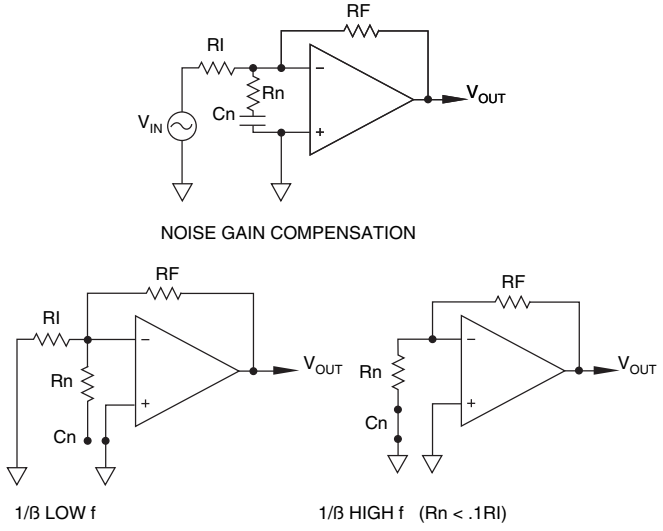
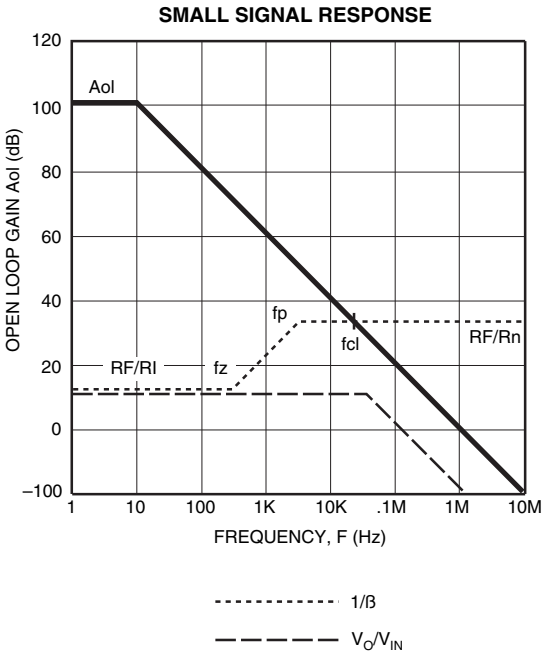


FIGURE 29. NOISE-GAIN COMPENSATION



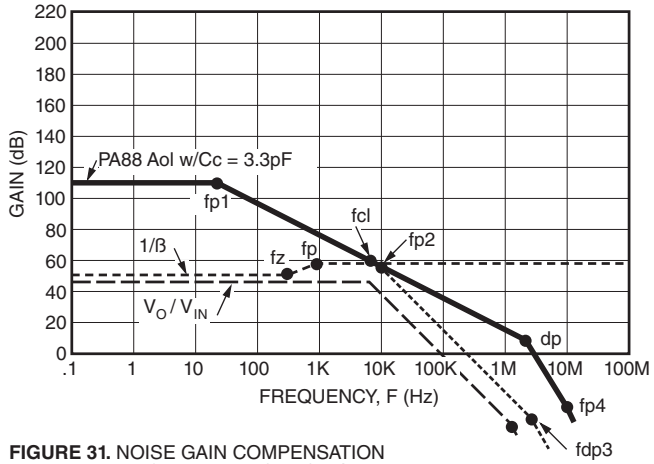


FIGURE 31. NOISE GAIN COMPENSATION MAGNITUDE PLOT FOR STABILITY

STEP 1: Modify the PA88 AoI due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms. The higher frequency poles of the unmodified PA88 AoI must be added into the modified AoI as shown in Figure 31.

STEP 2: Calculate DC ß for circuit, Cn is an open for DC.

DC ß = RI/(RF+RI) = 1K/(274K+1K) = .003636363
DC 1/ß = 20 Log (1/.03636363) = 48.79 dB

STEP 3: Plot DC 1/ß. Add noise gain compensation using the hints given above. Things look okay. We have 20 dB per decade rate of closure. fp is a decade away from fcl. High frequency 1/ß is less than 20 dB greater than low frequency 1/ß, and fz is less than a decade spaced from fp.

STEP 4: Plot open loop phase plot as in Figure 32 from the information given in Figure 31. We see from this plot we have 45 degrees of phase margin.

5.3 COMPOSITE AMPLIFIER & STABILITY

There are design cases where the input characteristics of a power op amp may not be sufficient to meet required specifications. In these cases one can still have the advantages of using the power op amp for linear analog control, but can optimize the front end of the circuit to meet the required specifications. A composite amplifier such as Figure 33 (see following page) will provide a highly accurate 75uV input offset voltage versus the 40 mV input offset voltage of the PA241. In the composite amplifier, the PA241 acts as a booster running in a closed loop gain of 11. The PA241 "booster"" and the OP07 form a new composite amplifier with the feedback from output all the way back to the input of the OP07.

The application in Figure 33 (next page) provides an excellent opportunity for us to utilize our knowledge of stabilizing circuits with capacitive loads, as well as acquire new techniques for dealing with stability and composite amplifiers.

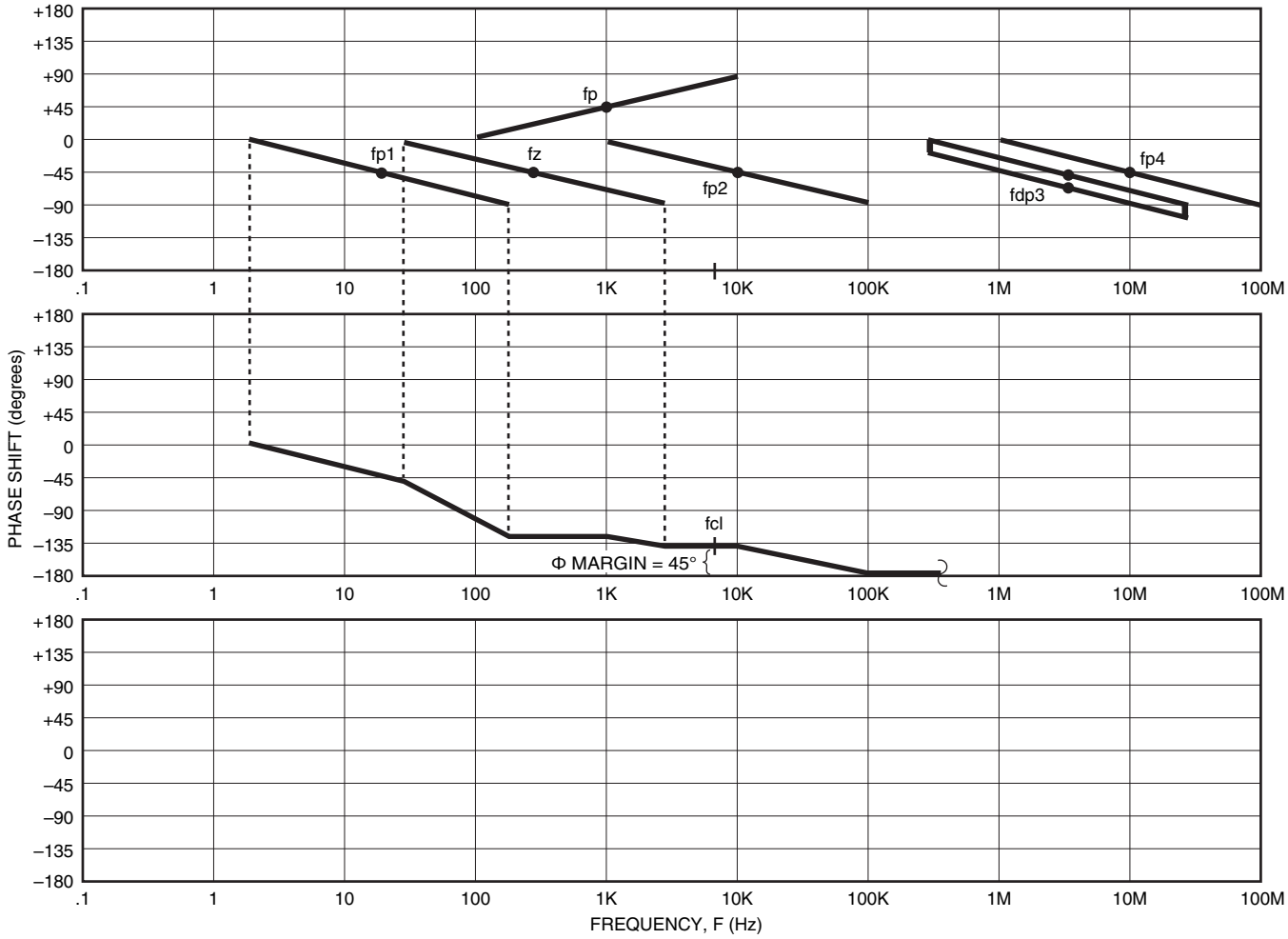


FIGURE 32. NOISE GAIN COMPENSATION OPEN LOOP PHASE PLOT FOR STABILITY

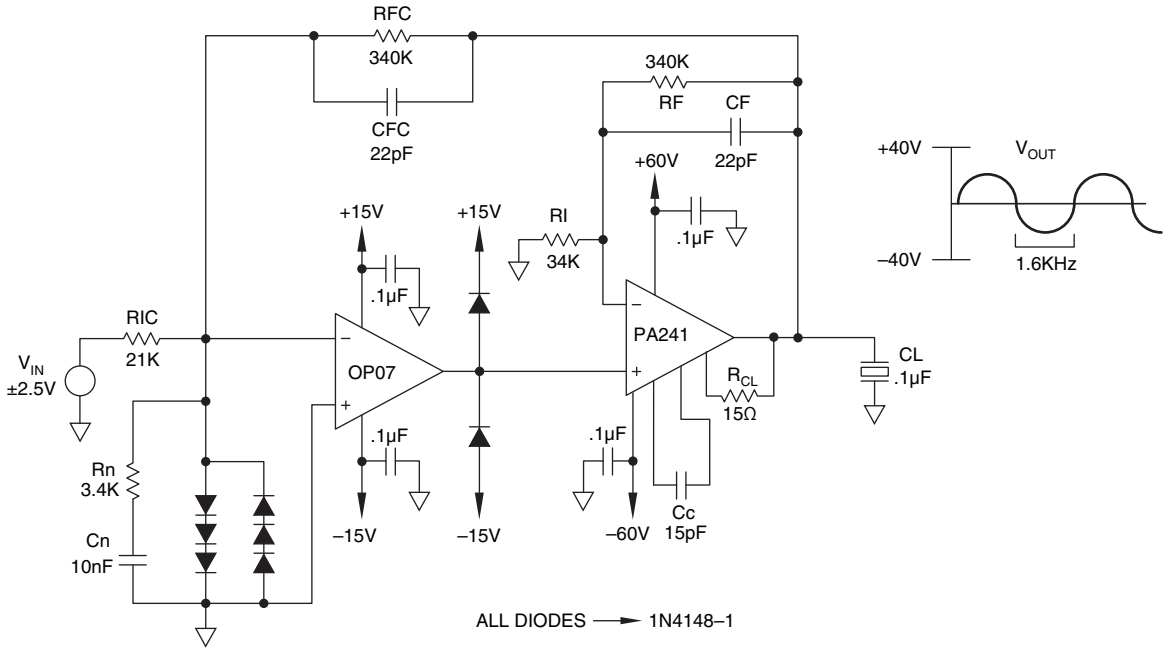


FIGURE 33. PA241 COMPOSITE PIEZO TRANSDUCER DRIVE

The following steps will provide a simple, logical approach to attacking composite amplifier stability problems:

STEP 1: Given specifications:

V_{IN} = ± 2.5 VOLTS
DC ≤ fin ≤ 1.6 KHz
CL = .1µF
V_{OUT} = –/+ 40 VOLTS
± 15 Volts available in system
Input offset voltage ≤ 100µV

STEP 2: From given specifications determine maximum slew rate needed to track highest frequency output.

S.R. [V/µs] = 2(π)f Vopk (1x10–6)
S.R. = 2(π) (1.6K) 40V (1x10–6) = .4V/µs

STEP 3: From calculated slew rate and given CL, determine current needed to drive capacitive load.

I = C dV/dt
I = .1µF (.4V/µs) = 40mA

STEP 4: Select power op amp and host amplifier.
PA240 is the lowest cost power op amp with 40mA of output capability; a slew rate of 20V/us, with Cc=15pF, and Vsat of 12V at 40mA out. PA241 is the same monolithic chip, but in a package with enough pins for programmable current limit. In this application, fault tolerance afforded by having current limit justifies the additional cost of the PA241.

OP07 will provide 75µV of input offset voltage; a slew rate of .17 V/µs; and an output voltage swing of +/-12V from +/-15V supplies. The maximum output voltage swing of the host times the booster gain must meet the desired output voltage swing. Here there is no problem since +/-12V out of OP07 times 11 (booster gain) will yield potential for +/-120V out of the composite amplifier configuration.

The slew rate of the host amplifier times the booster gain should be less than or equal to the booster slew rate. If it is greater than the booster slew rate, the host amplifier can "outrun" the booster during high slew rate demands and consequently the composite amplifier will be running open loop and hence non-linearities and distortion will be uncontrolled.

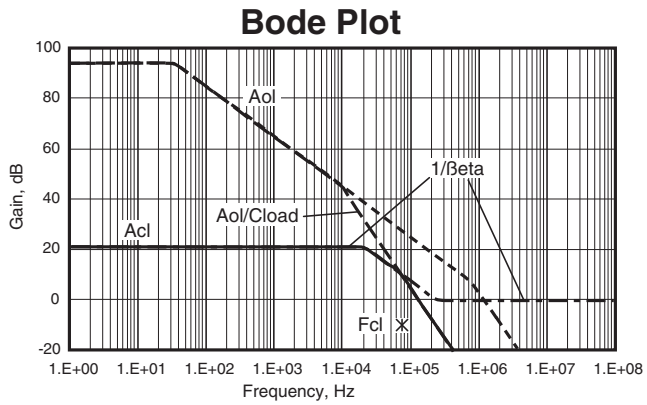
Host S.R. x Booster Gain = .17/µs x 11 = 1.87V/µs
1.87V/µs < 20V/µs (Booster S.R.)

We will run the booster amplifier in a closed loop gain of 11 as shown in Figure 33 to allow more margin to work with when compensating the capacitive load. We know this from experience in designing many power op amp circuits with capacitive loads on the output.

STEP 5: The booster stage of the composite must be stable before we consider the overall composite amplifier. Booster circuit data was entered into the Cload sheet of the Apex Precision Power Power Design spreadsheet. Initial indications were an intersection rate of 40dB per decade and a phase margin of only 19°. Figure 34 shows Power Design has already added the 150Ω amplifier output impedance to the 15Ω current limit resistor and calculated the pole with the capacitive load to be at 9.6KHz. The booster stage was compensated with Cf producing a closed loop pole (a feedback zero) at 21.3KHz. Do not be confused by sub-Hertz or multi-GHz entries in the table; these show up because the spreadsheet avoids division by zero errors by forcing extremely small values for non-existent capacitors. Refer to Figure 35 to see phase contributions of all elements added, closure frequency of 75KHz, closure rate of 20dB per decade, and a phase margin of 52°.

STEP 6: We are now ready to enter the composite circuit data as shown in Figure 36 (next page). Note that the closed loop gain of the booster stage has been added to the Aol of the OP07. Closure rate is 60dB per decade and we have a guaranteed oscillator. An attempt to compensate with just CFC was made, but was not good enough. A better compensation

MODEL	PA241,3-150	Note/PBs	Rn	9999999999	Kohms
Rcl	15	Ohms	Cn	0	nF
Cload	0.1	uF	Cf	22	pF
Rin	34	Kohms	Riso	0	Ohms
Rf	340	Kohms			



Total Rout	165	Ohms
Pole Zout/Cload	9.645744481	KHz
1/Beta (DC)	20.8	dB
Noise Gain	0.0	dB
Pole Noise Gain	0.159154943	KHz
Zero Noise Gain	0.159154938	KHz
Pole Cf/Rf	21.27739784	KHz
Zero Rf/Cf	234.051377	KHz
Zero Riso/Cload	1.59155E+11	KHz

FIGURE 34.

Phase Shift Components

Estimated Closure Frequency =	74.98942	KHz
Suggested maximum bandwidth	11.54782	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	51.78278	Degrees

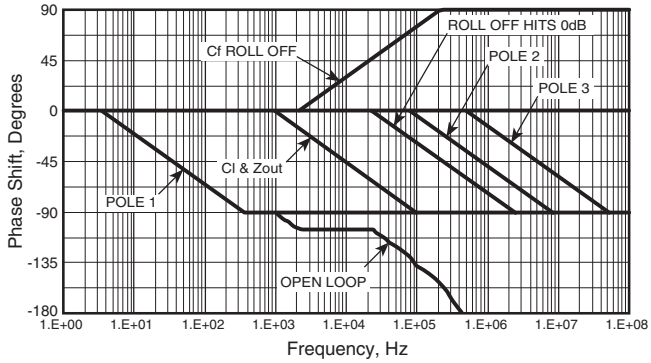


FIGURE 35.

technique will use noise gain to raise the 1/ß curve to 41.4dB and then use CFC to obtain an intersection with the composite Aol of 20dB per decade.

STEP 7: Figure 37 (next page) shows the effect of adding our stabilization components. We have achieved the desired intersection rate of 20dB per decade. Note that the output signal does not rise at 686Hz when the noise gain kicks in, but does begin to roll off at 21.3KHz due to the 22pF roll off capacitor.

Once again our final stability check is completed by the open loop phase plot for the composite amplifier as shown in Figure 38 (next page). The resultant 50 degrees of phase margin guarantees a stable composite amplifier configuration.

P.S.— Refer to Figure 33. The 1N4148-1 diodes on the input of the OP07 provide differential and common mode overvoltage protection from transients through CFC. Piezo elements

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	999999999	Kohms
Rf	340	Kohms	Cn	0	nF
Cf	0	pF	Using Look-Up data		

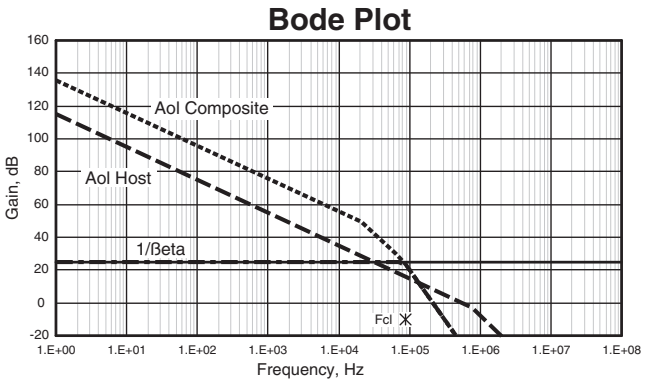
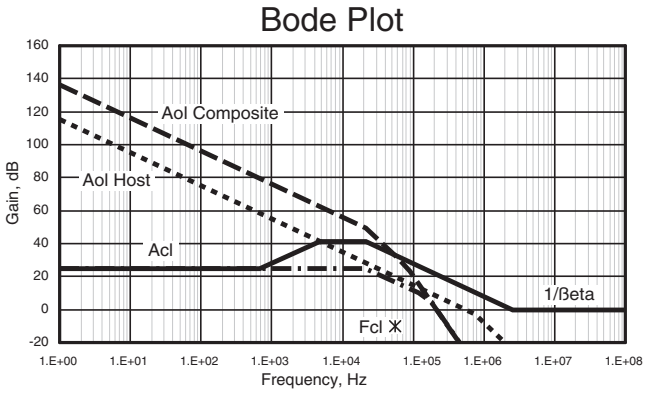


FIGURE 36.

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	3.4	Kohms
Rf	340	Kohms	Cn	10	nF
Cf	22	pF	Using Look-Up data		



1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

FIGURE 37.

being electromechanical devices can generate high voltages if shocked mechanically. Output diodes of the OP07 prevent overvoltage transients that occur through CF and shunted through PA241 internal input protection diodes, from damaging the output of the OP07 connected to +input of PA241.

6.0 REAL WORLD STABILITY TESTS

We have devoted much text to discussing how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power

Estimated Closure Frequency =	56.23413	KHz
Suggested maximum bandwidth	5.623413	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	50.625	Degrees

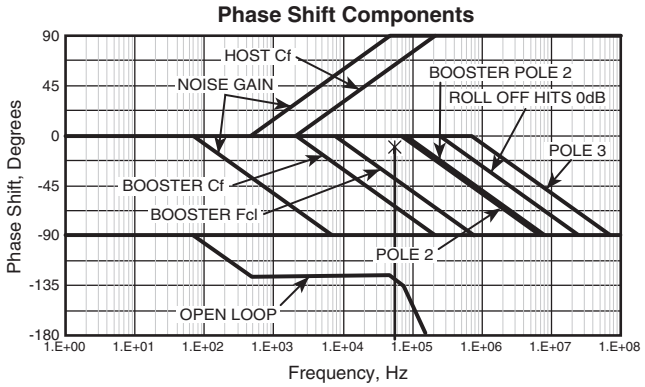
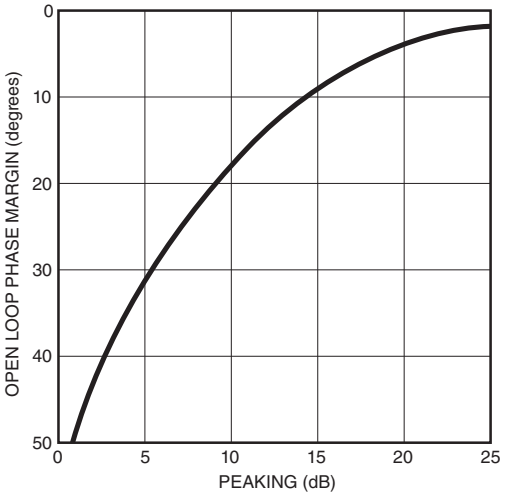


FIGURE 38:

op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

6.1 AVCL PEAKING TEST

Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain. From the closed loop Bode plot, we can measure the peaking in the region of gain roll-off. This will directly correlate to open loop phase margin as shown.



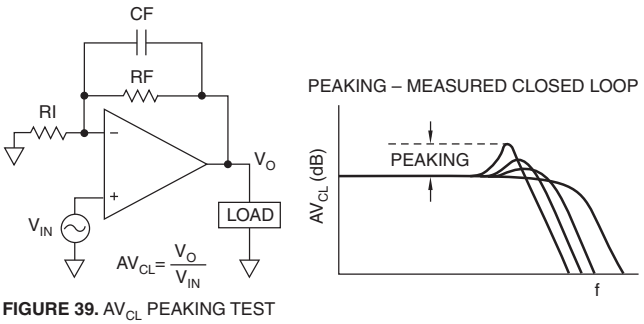


FIGURE 39. AV_{CL} PEAKING TEST

6.2 SQUARE WAVE TEST

Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude

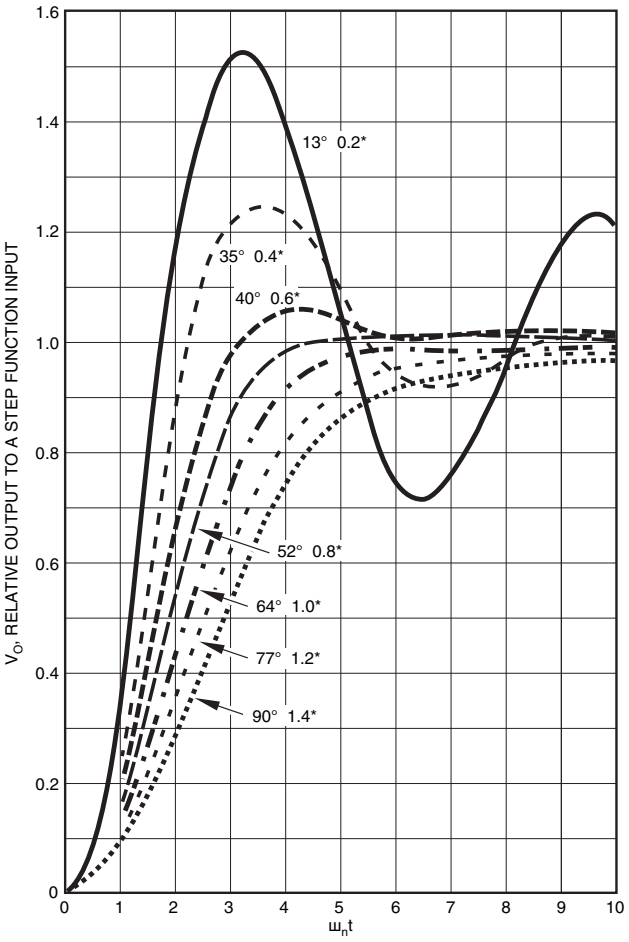


FIGURE 40. SQUARE WAVE TEST

of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

6.3 DYNAMIC STABILITY TEST

An expansion on the Square Wave Test is shown in Figure 41(see second page following this one). The Dynamic Stability Test superimposes a small signal AC square wave on a low frequency, large signal AC sinewave to dynamically test the power op amp circuit under all operating point conditions. The resultant ringing on the square wave can be compared to the graph in Figure 40 for relation to open loop phase margin. Note that R1 // R2 in Figure 41 must be much greater than RIN or the input summing test impedances will affect the compensation of the power op amp circuit under test.

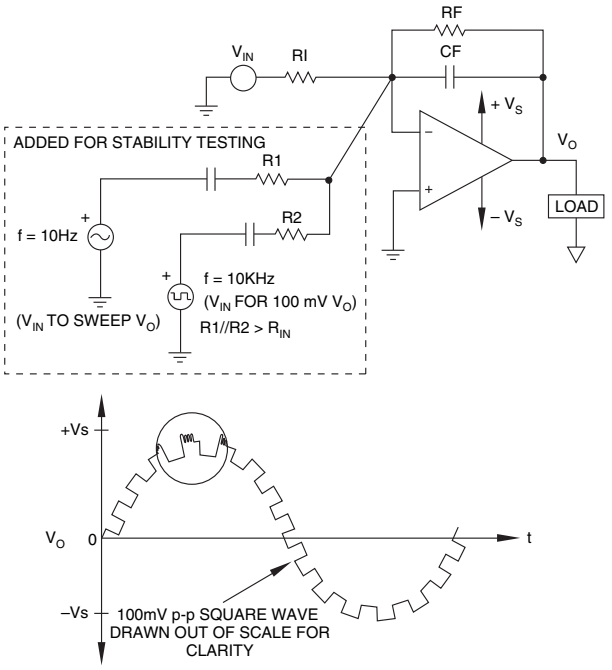


FIGURE 41. DYNAMIC STABILITY TEST

7.0 STABILITY TROUBLESHOOTING GUIDE

Figure 42 (see third page following this one) provides a troubleshooting guide for the most common stability problems. The "Probable Cause/Possible Solution Key" gives insight into the origin of the problem and provides guidance as to the appropriate fix.

8.0 FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply the techniques and ideas in this Application Note under your worst case load conditions and you can conquer your oscillation problems.

If time is short or you can't see the forest from the trees, Apex Precision Power would be happy to provide Technical Support via Design Support Request, (800) 625-4084. More importantly, as we tell all our customers, we would be happy to review your schematic for stability considerations, etc., before you ever build a circuit or even buy a power op amp.

CONDITION AND PROBABLE CAUSE TABLE

Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
$f_{osc} \leq$ UGBW	N	Y	N	C, D
$f_{osc} \leq$ CLBW	Y	Y	Y	K, E, F, J
$f_{osc} \leq$ UGBW	–	–	N	G, A, M, B
$f_{osc} \leq$ CLBW	N	Y	Y	D
$f_{osc} \leq$ UGBW	Y	Y	N*	J, C
$f_{osc} \leq$ CLBW	Y	Y	N	L, C
$f_{osc} >$ UGBW	N	Y	N	B, A
$f_{osc} >$ UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 42A for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 42A) will stop oscillation if Rn << $|X_{CF}|$ at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 2.3.
B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 2.3.
C. Cause: Ground loops.
Solution: Use "Star" grounding. See Figure 9.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use Noise Gain Compensation network. See section 5.2.4.2.
E. Cause: Inductor within the feedback loop (loop gain pole)
Solution: Use alternate feedback path. See section 5.1.
F. Cause: Input capacitance reacting with high RF (noise gain zero).
Solution: Use CF in parallel with RF. (CF =~Cin). Do not use toomuch CF, or you may get problem J.
G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate +RB (the bias current compensation resistor from +IN to ground)
H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output "snubber" network. See Section 2.5.
I. Cause: "Composite PNP" output stage with reactive load.
Solution: Use output "snubber network. See Section 2.5.
J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce CF and/or increase Cc for unity gain stability.
K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use Noise Gain Compensation network. See section 5.2.4.2.
L. Cause: Servo loop stability problem
Solution: Compensate the "front end" or "servo amplifier.
M. Cause: Unwanted signals coupling into op amp through case.
Solution: Ground the case.

FIGURE 42. STABILITY TROUBLESHOOTING GUIDE

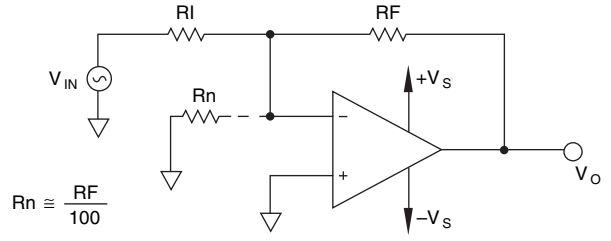


FIGURE 42A. LOOP CHECK CIRCUIT

9.0 REFERENCES

1) Frederiksen, Thomas M. : INTUITIVE IC OP AMPS, R.R. Donnelley & Sons, 1984.
2) Huelsman, Lawrence P. : BASIC CIRCUIT THEORY WITH DIGITAL COMPUTATIONS, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1972.
3) Faulkenberry, Luces M. : AN INTRODUCTION TO OPERATIONAL AMPLIFIERS WITH LINEAR IC APPLICATIONS, John Wiley & Sons, New York, 1982.
4) Dorf, Richard C. : MODERN CONTROL SYSTEMS (Third Edition), Addison-Wesley Publishing Company, Reading, Massachusetts, 1980.

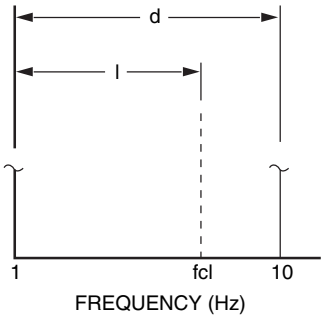
10.0 APPENDIX

This appendix contains some handy tools for plotting magnitude and phase plots for stability analyses. The "Log Scaling Technique" covers an easy way to read exact frequency locations of poles and zeroes from magnitude plots for stability. Included, as well, are blank magnitude and phase plots for copying and using to plot phase and magnitude plots for stability.

One final tip. Once a magnitude plot has been plotted containing the Aol curve and 1/ß, it is easy to translate the poles and zeroes to an open loop phase plot for stability. Simply use a light table (ours is very basic — a piece of plexiglass that fits over a 60W incandescent desk light !) to trace the locations of poles and zeroes. Remember poles and zeroes in the Aol curve are poles and zeroes in the open loop phase check for stability. But poles in the 1/ß plot become zeroes, and zeroes in the 1/ß plot become poles in the open loop phase check for stability.

LOG SCALING TECHNIQUE

When using rate-of-closure graphical techniques it is convenient to measure what frequency fp or fz might be at without detailed calculation. This handy reminder about log scale will give you that power:



$\frac{l}{d}$ = LOG (fcl)

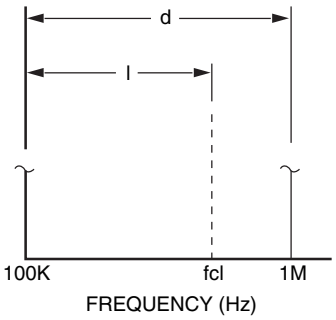
fcl = $LOG^{-1}\left(\frac{l}{d}\right)$

*fcl = $10^{(l/d)}$

fcl = $10^{(1.4"/2")}$ = 5.012Hz

* This can be used between any decade of frequencies by normalization of scale for 1 to 10.

Definition by example is easiest →
What frequency is fcl below?



fcl = $10^{(1.4"/2")}$ = 5.012Hz

fcl = 501.2 KHz

Scale is normalized for 1 to 10 by dividing by 100. Answer to fcl is multiplied by 100 to yield final answer in KHz.

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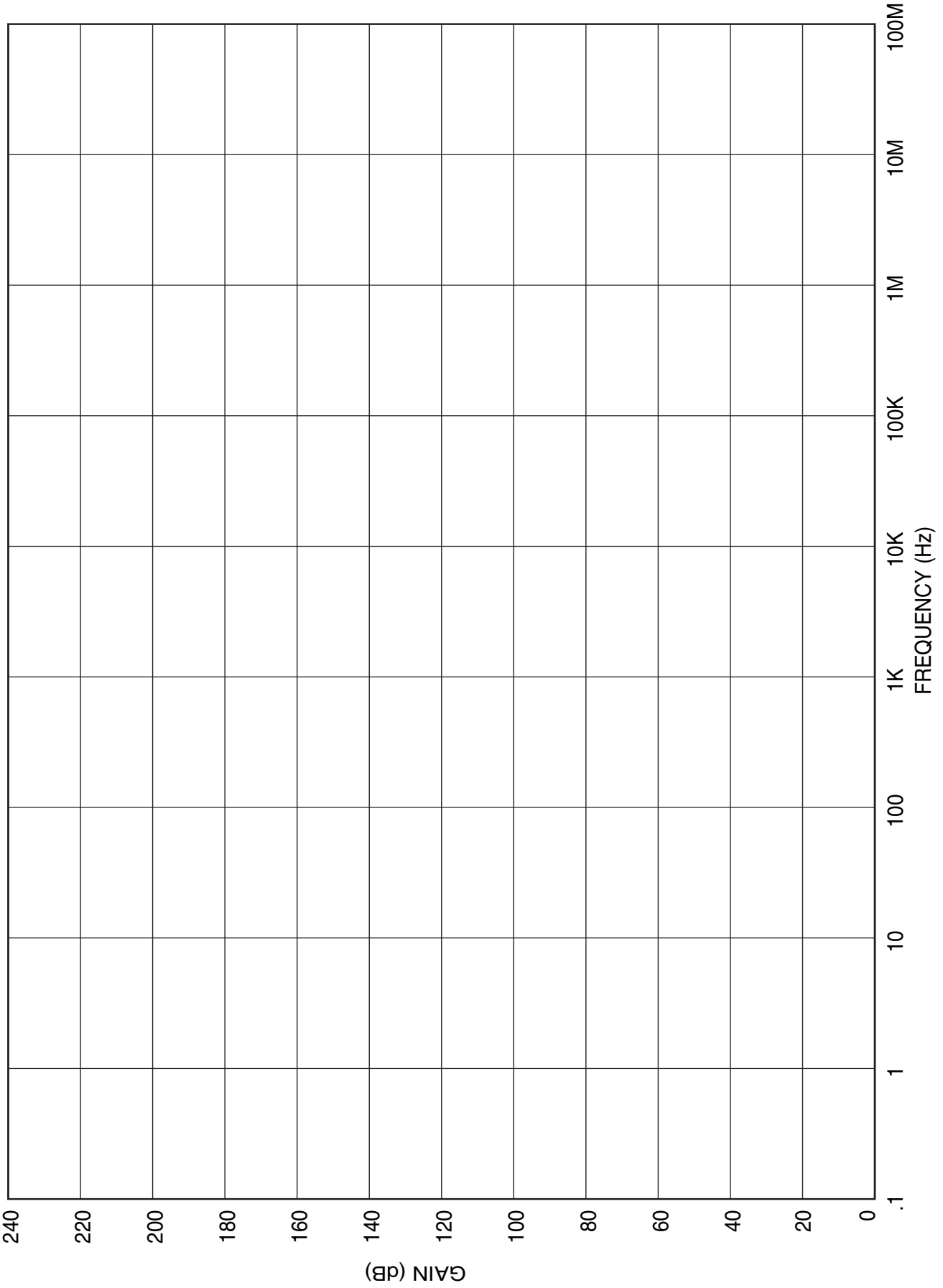
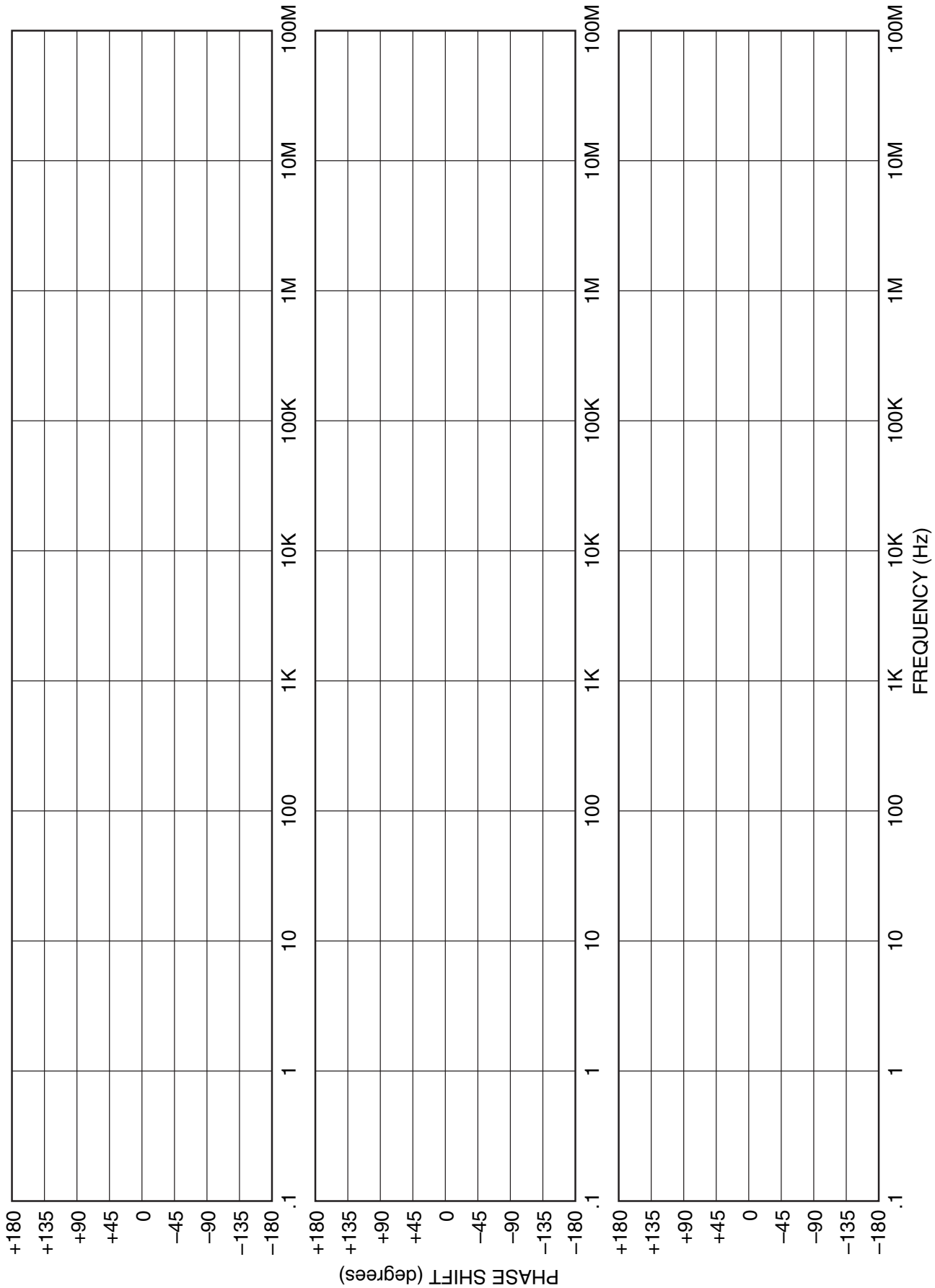
For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com


GAIN (dB)
240
220
200
180
160
140
120
100
80
60
40
20
0
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)


+180
+135
+90
+45
0
–45
–90
–135
–180
.1
1
10
100
1K
10K
100K
1M
10M
100M
PHASE SHIFT (degrees)
FREQUENCY (Hz)

Bridge Mode Operation of Power Operational Amplifiers

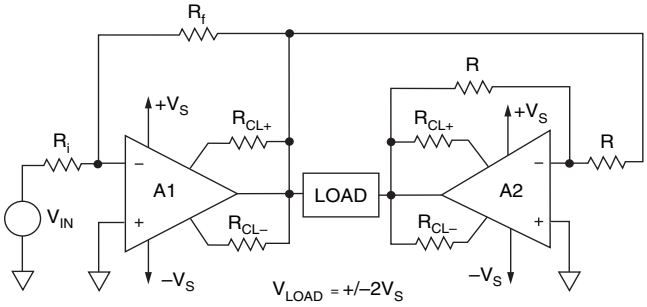
1.0 ADVANTAGES OF THE BRIDGE CONNECTION

The bridge connection of two power op amps provide's output voltage swings twice that of one op amp. And it is the only way to obtain bipolar DC coupled drive in single supply applications. Two possible situations where this is an advantage would be in applications with low supply voltages, or applications that operate amplifiers near their maximum voltage ratings in which a single amplifier could not provide sufficient drive.

There are other incidental advantages of the bridge connection. It effectively doubles the slew rate, and non-linearities become symmetrical reducing second harmonic distortion in comparison to a single amplifier circuit.

2.0 BRIDGE CONCEPTS AND TERMINOLOGY

Figure 1 is a circuit diagram for the most common variation of a bridge connection using power op amps. To clarify the discussion of this circuit, we'll refer to the left hand amplifier A1 as the master amplifier, and A2 as the slave. The master amplifier accepts the input signal and provides the gain necessary to develop full output swing from the input signal. The total gain across the load will be twice the gain of the master amplifier.



• PREVENT SOA VIOLATIONS
SET I_{LIM} (A2) > 1.2 • I_{LIM} (A1)

• BANDWIDTH MISMATCH

FIGURE 1. BRIDGE MODE WITH DUAL SUPPLIES (MASTER/SLAVE)

The master amplifier can be set up in virtually any op amp type circuit: inverting or non-inverting, differential amplifier, or as a current source such as an Improved Howland Current Pump.

Always configure the slave as a unity gain inverting amplifier and drive it from the output of the master. Later discussions in connection with Safe Operating Area (SOA) and protection will show the importance of this point.

3.0 PROTECTION AND SOA

In the following discussions that all general precautions in using power op amps, such as the need for external flyback diodes, transient protection, input protection, etc., must be addressed. These subjects are dealt with in "GENERAL OPERATING CONSIDERATIONS". The following discussion will concern itself only with specific protection issues related to bridge connections.

The concept of driving the slave from the output of the master power op amp is essential for proper protection. The best illustration of the value of that configuration is shown with an example such as Figure 1 where op amps with adjustable external current limiting have been used. With externally settable current limit, set the master to current limit 20% lower than the slave. If the master cannot be reduced, then raise the slave 20% above the master to provide better overall protection than leaving them equal. If a fault occurs in the load such as a short across the load, this will cause the master to current limit and it's output will clip. Since the master is driving the slave, we are effectively clipping the drive to the slave also. Under these conditions the SOA voltage stress will be equally shared between the two amplifiers.

With op amps having fixed internal current limits it is impossible to insure that the master current limits first. This is not a total disaster, it just means that under load fault conditions it cannot be guaranteed that the amplifiers will share the SOA voltage stress, and it must be assumed that one amplifier could bear the entire stress.

Figure 2 is a simplification of output stages to give examples of amplifier stress under a difficult (low resistance such as a stalled DC motor) load condition. The worst case stress must be used where amplifier current limiting cannot be controlled. From this example it can be seen that proper setting of current limiting, when possible, can halve stresses under fault conditions.

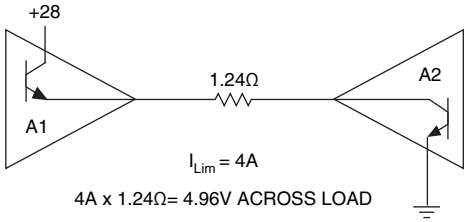


FIGURE 2. EVALUATION AGAINST SOA

Consider each amplifier individually for load analysis, SOA plotting and power dissipation calculations by halving the actual load impedance. Each individual amplifier cannot "see" the amplifier connected to the other end of the load. The other amplifier doubles the voltage, and thus the current, in the load.

4.0 STABILITY

4.1 STABILITY CONSIDERATIONS FOR THE SLAVE

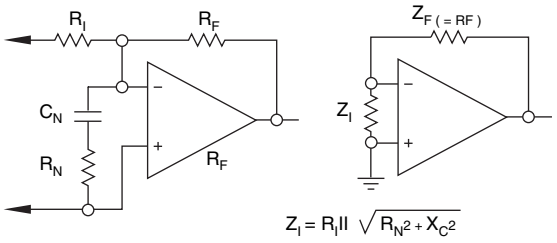
Because the slave amplifier must operate as a unity gain inverter it will be the most critical with regards to stability. Stability enhancement methods invariably involve a tradeoff of frequency response. Fortunately, in the case of the bridge, the master amplifier bandwidth is naturally restricted by operating at higher gains (as well as easing stability considerations for the master). Usually the slave can be compensated such that the resultant circuit will have matching bandwidths on both halves.

Noise gain compensation is the favored method of enhancing stability. Keep in mind that noise gain compensation depends on the non-inverting input being connected to a low impedance (< 0.1Rn). This is not a problem when the non-inverting input can be grounded, as in split supply applications, but it must be considered in single supply applications as the half supply

voltage reference point must be a good AC ground. The simplest way to insure a good AC ground is by good bypassing in the form of a tantalum or electrolytic capacitor in parallel with a ceramic capacitor.

4.2 NOISE GAIN COMPENSATION

As shown in Figure 3, a simple way of visualizing the effect of noise-gain compensation is that it raises the apparent gain that the amplifier "sees" (or in other words, reduces feedback) while not affecting the actual signal gain. Select Rn such that Rn > = 0.1Ri to limit the phase shift added by the noise gain compensation. Note from the graph in Figure 3 that, in the example shown, the noise gain compensation introduces a pole in the feedback path. In this case, at approximately 300 Hz. At 3000 Hz there is a zero in the feedback path. The region between these points should be kept to less than a decade in frequency wide, and a maximum gain difference of 20 dB is implicit in that requirement. In short, noise gain for the slave (which has an uncompensated noise gain of 2, or 6 dB) must be ≤ = 20, or 26 dB.



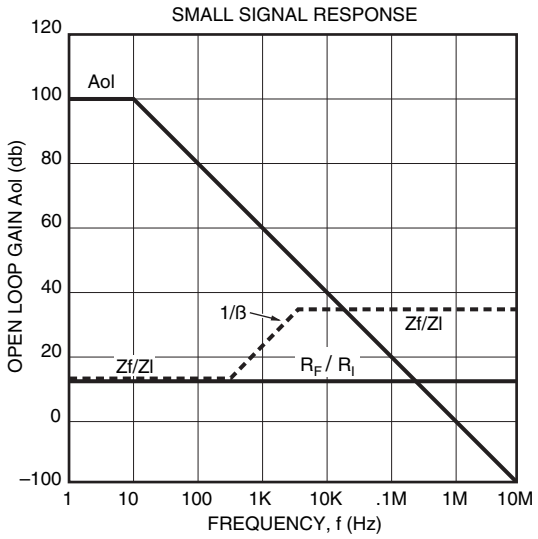


FIGURE 3. NOISE-GAIN COMPENSATION

Another consideration that could be given to the selection of Rn is in regard to frequency response (gain vs. frequency). From Figure 3, the signal gain of a circuit using noise gain compensation rolls off at the point where the noise gain intersects the amplifier Aol. In the case of Figure 3, the normal bandwidth would be about 250 KHz, with compensation about 25 KHz. Without compensation, the slave would have wider bandwidth than the master which is operated at higher gains.

An ideal value for Rn would be one which makes the noise gain of the slave match the signal gain of the master, assuming there is not greater than 20 dB of difference, and the noise gain limit of 26 dB in the slave is not exceeded. In the event the master will also require noise gain compensation for stability, the same principle of matching the noise gain will help to insure matched bandwidths.

The upper corner frequency of the noise gain compensation, or zero, is determined by Cn such that :

$$V_N = \frac{1}{2\pi \bullet F \bullet R_N}$$

where F= desired zero frequency. Cn should be selected so that the zero is lower than one-tenth the frequency where the high frequency noise gain crosses the Aol.

4.3 STABILITY CONSIDERATIONS FOR THE MASTER

In the case of the master, as well as the slave, capacitive loads should also be considered. The only time the master would need noise gain compensation would be for very low gains, capacitive loading, or when using amplifiers with minimal phase margin such as the PA10 and PA12. Methods of analysis for capacitive loads are discussed in detail in "STABILITY FOR POWER OP AMPS", Application Note 19.

Amplifiers with emitter follower or source follower outputs generally do not have problems with inductive loads. However, collector or drain output amplifiers such as the PA19, PA03 and especially the PA02, with it's local feedback loop in the output stage, can oscillate into inductive loads. Monolithic amplifiers with quasi-complementary output stages can also be sensitive to inductive loading. Compensate these amplifiers with a series R-C "snubber" from each amplifier output to ground. For power amplifiers the resistors typically run 1 to 10 ohms and capacitors 0.1 to 1.0 µF.

5.0 SPECIAL CASES OF THE BRIDGE CONNECTION

5.1 CURRENT OUTPUT

The bridge connection can be a useful tool in a current output circuit. The maximum rate-of-change of current in an inductor, as would be used in a deflection application, is a function of available voltage. For that reason the bridge circuit could double the speed of a magnetic deflection application.

In a current source configuration, the slave remains as an inverting voltage amplifier. Only one amplifier needs to be (or should be) a current source. Of the available ways of configuring an op amp for current output, only the Improved Howland Current Pump is practical for a power op amp bridge.

In Figure 4, the master amplifier is configured as the current pump. R8 is the current sensing resistor. The Improved Howland

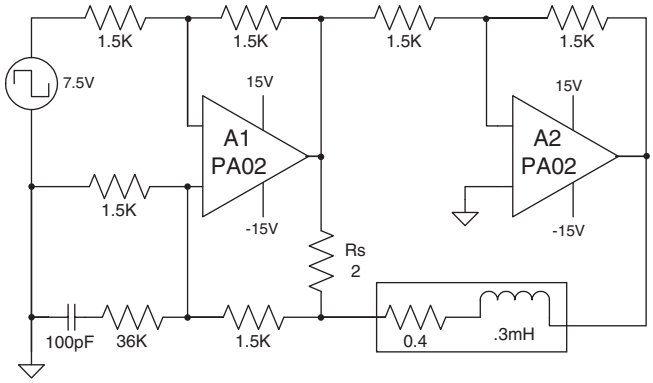


FIGURE 4. ELECTRO-MAGNETIC DEFLECTION (BRIDGE AMPLIFIER)

Current Pump has many special considerations which will not be discussed here, but it will suffice to say that generally the feedback and input resistors should be very closely matched, usually better than 0.1%.

For details on voltage and current waveforms of this circuit, refer to Applications Note 5, Precision Magnetic Deflection.

5.2 UNIPOLAR OUTPUT

A particularly powerful way of applying the bridge is in the unipolar bridge. By unipolar, we mean that the output can only swing from 0 to one polarity. Figure 5 is used to illustrate this technique.

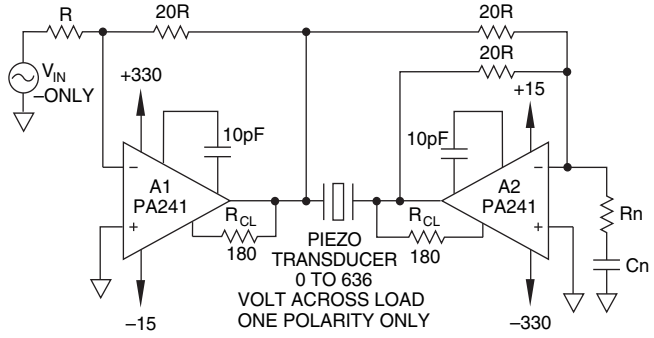


FIGURE 5.

The master is a PA241 operating on supply rails of +330 and -15 volts. The slave is operated at +15 and -330 volts. The lower voltage supplies need only be large enough to respect the linear COMMON MODE voltage range requirements of whatever amplifier is used (14 volts in the case of the PA241).

The circuit is designed to accommodate positive going inputs only. At full output swing the master can reach +318 volts while at the same time the slave is at –318 volts for a total voltage across the load of 636 volts. The full dynamic range with regard to the load is 0 to 636 volts unipolar.

The circuit could also be designed such that it accepts negative going inputs and the output of the master swings negative and the slave positive by reversing the supplies.

5.3 SINGLE SUPPLY APPLICATIONS

In the single supply circuit shown in Figure 6, connect the slave's non-inverting input to a pair of equal value resistors connected between supply and ground. This provides a 1/2 supply center operating point for the entire bridge. This point should be well bypassed.

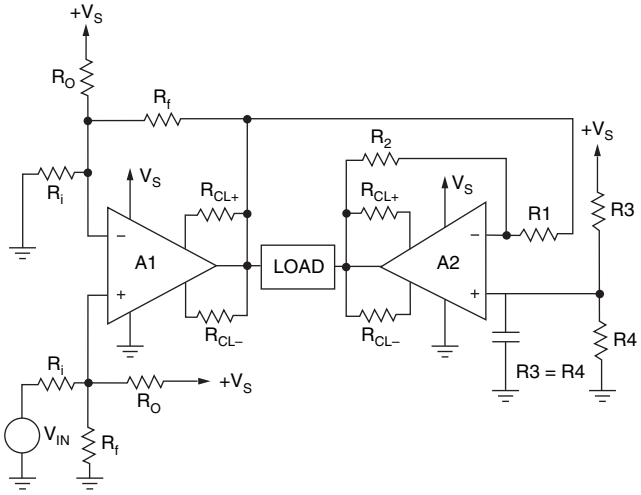


FIGURE 6. BRIDGE MODE WITH SINGLE SUPPLY (OTHER THAN PA21)

The simplest way to understand the configuration for the master is to delete the resistors Ro, upon which the master becomes the standard circuit for a differential amplifier. The two Rf resistors should be reasonably matched to each other, and the two Ri resistors matched to each other. An advantage of this configuration is that the gain is simply the ratio of Rf/Ri.

Now consider the Ro resistors. Their sole purpose is to provide an equal DC bias on each input and to get the quiescent DC level within the amplifiers COMMON MODE voltage range requirements. This is generally anywhere from 5 to 12 volts inside of each supply rail and is given on all amplifier data sheets. For example, using PA05 on a 90 volt supply, the COMMON MODE VOLTAGE RANGE of the PA05 dictates that the inputs must never come closer than within 8 volts of either rail. So the objective is to select Ro, to set the amplifier inputs to at least 8 but not more than 82 volts, and to stay within these limits under normal input swings. As far as exactly what voltage? It could be argued that half supply is the optimum common-mode point assuming this doesn't cause excessive current to flow in the Ri resistors. In higher voltage applications the range of 5 to 15 volts is more practical though. The PA75 is especially easy to use in single supply applications. Since these amplifiers common-mode range includes the negative rail, or ground, their inputs can be driven directly without additional biasing components. The slave must still have it's noninverting input biased at 1/2 supply for proper bridge operation.

5.4 PARALLEL CONNECTION

The bridge circuit can also be combined with the parallel connection of power op amps. Figure 7 shows how substantial audio power outputs can be obtained along with improved reliability since the parallel connection spreads the load among more amplifiers.

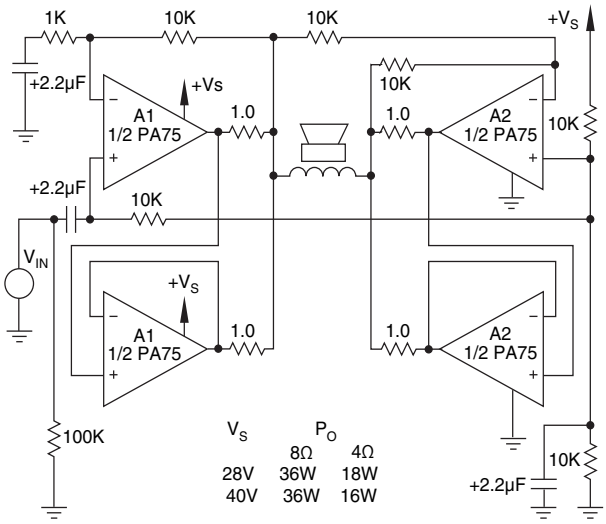


FIGURE 7. SINGLE SUPPLY PARALLEL BRIDGE

Note that in the parallel connection, the pair of paralleled amplifiers are labeled as master and slave also. Because the slave amplifier operates as a unity gain buffer, an amplifier must be selected which has a COMMON MODE voltage range that exceeds its output voltage swing capability. If this cannot

be done, configure the slave as a differential amplifier with 4 equal valued and closely matched resistors.

Stability can also be a problem with the slave in the parallel amplifier. A resistor may have to be inserted in the feedback to allow for the use of noise gain compensation. (Noise gain compensation does absolutely nothing when placed across the inputs of a unity gain buffer with no series resistance in the feedback path)

5.5 BRIDGES USING POWER BOOSTERS

A bridge circuit using the PB50 or PB58 would require a composite amplifier for both master and slave. The composite amplifier is not an optimum configuration to operate at unity gain when stability is considered. Use noise gain compensation to establish an adequately high noise gain at high frequencies. Note that observing the criteria previously discussed regarding noise gain would typically dictate that the noise gain for the slave be ≤ 26 dB (Gain = 20). See Figure 8 for a bridge circuit using power boosters.

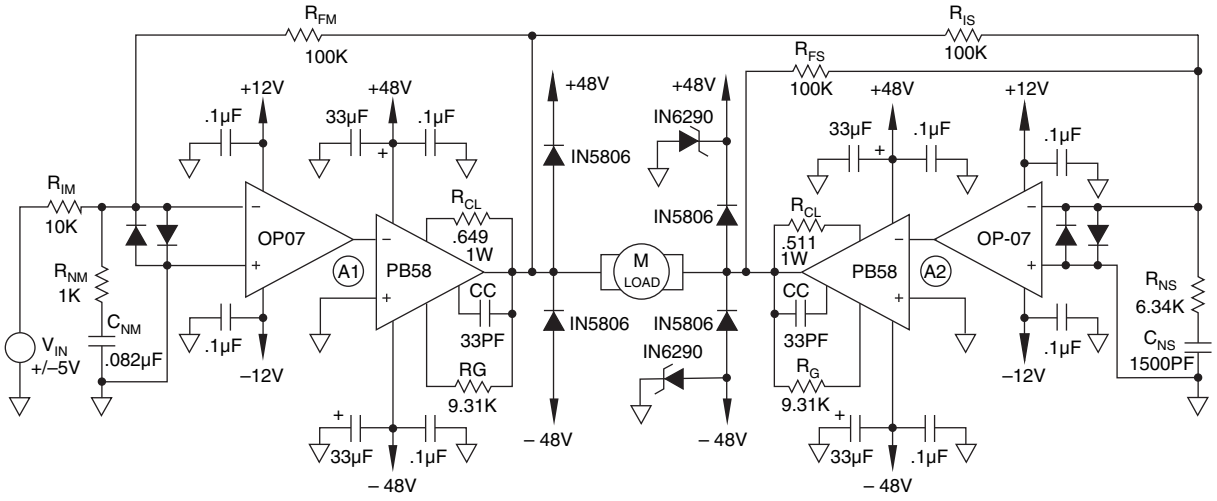


FIGURE 8. PB58A MOTOR DRIVE BRIDGE

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For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Single Supply Operation of Power Operational Amplifiers

1.0 SINGLE SUPPLY OPERATION INTRODUCTION

Single supply operation of power op amps is most often done out of necessity. Examples of such applications are battery powered applications or circuits operating from vehicular power systems.

Single supply operation improves the efficiency of power supply usage. In split supply applications, current is drawn from only one supply at a time, with the opposite supply sitting idle unless bridge circuits are used.

This application note deals exclusively with applications operating off of positive supplies as this occurs 95% of the time. Negative supply principles are identical except for the reversal of polarity.

2.0 RESTRICTIONS OF SINGLE SUPPLY OPERATION

2.1 COMMON-MODE RESTRICTIONS

Keeping op amp inputs biased to within their linear common-mode voltage range is the most important requirement in single supply circuits. The actual value required varies for each amplifier model, and is described in individual model data sheets under SPECIFICATIONS, COMMON MODE VOLTAGE RANGE. DO NOT USE the specification given in the ABSOLUTE MAXIMUM RATINGS block of the data sheet.

2.2 LOAD CONNECTION TO GROUND

There will be several options available for load connection, as shown in Fig. 1. The first option shown in Fig. 1A, is a load connected to ground. Obviously only positive going outputs are possible. Note that when the output voltage the load "sees" is near zero, the amplifier considers its output to be swung to its negative rail.

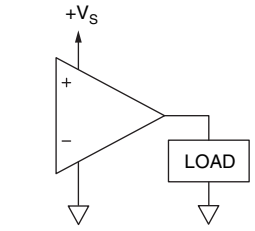
Note also that amplifiers have limits as to how close they can swing to either rail. So the output for the grounded load can never actually go to zero. It has been observed that substantial current is available under these non-zero conditions, and that the amplifier has full source and sink capability. As an example, a PA12 in a single positive supply will swing as low as 2.5 volts on the output. If a load is connected from output to ground, even with the amplifier overdriven in a negative direction, it will supply substantial positive current, on the order of amps, and up to the current limit, into the load.

2.3 BRIDGE LOAD CONNECTION

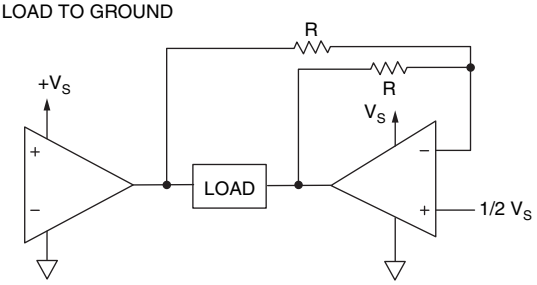
The bridge load connection using two amplifiers, as shown in Fig. 1B, permits bipolar swings across the load. For DC coupled loads this is the only practical way to obtain bipolar swings. Note that the bridge effectively doubles the gain of the circuit.

2.4 LOAD TO HALF SUPPLY

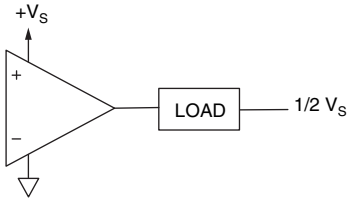
Bipolar drive is possible if the load can be referred to a point at half supply, as in Fig. 1C. This is usually not practical, nor efficient, as the half supply point must have the current capacity to support the load requirements. It might be possible to use a second power op amp as a high current source and sink regulator for this point, but this second op amp would be much more efficiently utilized as the second half of a bridge.



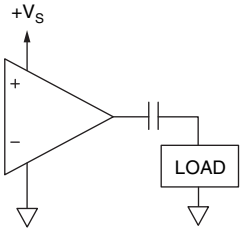
A. LOAD TO GROUND



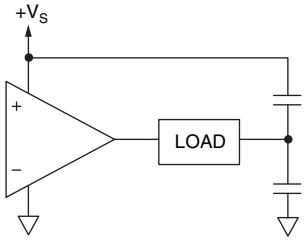
B. BRIDGE



C.1/2 SUPPLY



D. AC COUPLED SINGLE CAP



E. AC COUPLED DUAL CAP

FIGURE 1. LOAD CONNECTION OPTIONS

2.5 CAPACITIVE COUPLED LOAD

In applications such as audio, it is possible and often desirable to AC couple the load with a capacitor. A simple series capacitor allows driving a ground connected load, as in Fig. 1D. An alternative is to connect the ground side of the load to two large electrolytics, as in Fig. 1E. The only possible advantage of Fig. 1E is the possible reduction of turn-on "pop" in circuits where this may be a problem.

3.0 CIRCUIT TOPOLOGIES

3.1 UNSYMMETRICAL SUPPLY

Oddly enough, the first option that should be considered is to not use a single supply. Many applications such as those using high voltage amplifiers require a single large high voltage supply and unipolar output swings. This is to allow incorporation into systems which already have lower bipolar supplies such as ±15 or ±12 volts present. Should this be the case, then use the –15 or –12 volt supply on the negative rail of the op amp (more than a few high voltage applications have large negative supplies along with 12 or 15 volt bipolar supplies).

As shown in Fig. 2, as long as the small supply is large enough to accommodate the common-mode requirements of the amplifier over the range of normal inputs, then no other additional components are required.

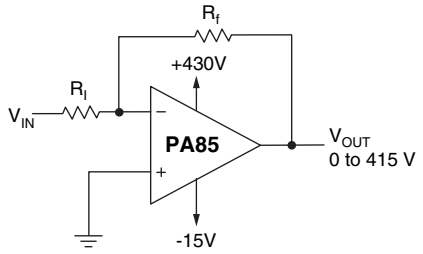
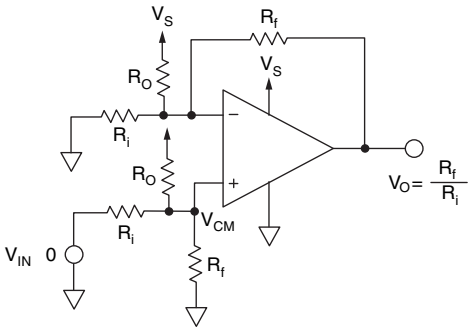


FIGURE 2. UNSYMMETRICAL SUPPLIES

3.2 DIFFERENTIAL CONFIGURATION

The most universally useful single supply circuit is the differential configuration shown in Fig. 3. This topology makes it possible to set the gain simply as the ratio of R_F/R_I where each R_F pair and R_I pair are matched to each other. It is feasible to use the circuit either non-inverting or inverting, but keep in mind that noninverting will accommodate inputs which go positive only with respect to ground, and non-inverting negative only with respect to ground. Also note that the R_O pair must be closely matched to each other.



For $V_{IN} = 0$:

$$V_{CM} = \frac{V_S \ (R_i||R_f)}{R_O + (R_i||R_f)}$$

$$V_{CM\Delta} = \frac{V_{IN} \ (R_O||R_f)}{R_i + (R_O||R_f)}$$

For $V_{IN} > 0$:

$$V_{CM} = V_{CM\ @V_{IN}\ =\ 0} + V_{CM\Delta}$$

FIGURE 3. SINGLE SUPPLY NON-INVERTING CONFIGURATION

The R_O resistors provide the input common-mode biasing to keep the amplifier linear. An advantage of this method is that (assuming adequate resistor matching) the output would be unaffected by variations in power supply voltage. Normally this inherent supply rejection is desirable, but in the case of the bridge amplifier, this could be a problem since the slave of the bridge is referred to a voltage divider operating from supply voltage. That divider is subject to supply fluctuations, and if the master amplifier of the bridge was equally subject to such fluctuations, it would appear as a common-mode signal across the load and be rejected.

R_O needs to be selected to satisfy common mode voltage requirements, and it turns out this encompasses a wide range of acceptable values for any given circuit. The designer is confronted with the question of just exactly what common mode voltage to set the inputs to. It could be set anywhere within the common mode range, but there will be some practical limitations even within that range.

To illustrate, assume the use of a PA85 with +450 volt supplies. R_O can be selected for anything from 12 volts to 438 volts for linear operation. It could be argued that the ideal value is half supply, or 225 volts, but such a selection would require unreasonably large values for R_I to keep currents within reasonable values. A very large R_I would require an even larger R_F, and the net overall impedance would be so high that stray capacitance and amplifier input capacitance would create enormous bandwidth and stability problems. For high voltage applications, minimum values such as 12 to 15 volts of common mode biasing are easier to accommodate.

When selecting R_O, consider it part of a voltage divider where the ground leg of the divider is the parallel resistance of R_F and R_I. Using that assumption, at full negative input voltage swing in conjunction with full theoretical negative output swing of zero, you will be designing to meet common mode requirements. Dynamically, the inputs will only move positive from this point, simplifying worst-case analysis to double checking the most positive excursion. R_O selection can be aided with the following equation:

$$R_O = \frac{(V_S - V_{CM})}{\left(\frac{V_{CM}}{R_I \ || \ R_F}\right)}$$

V_{CM} is the desired common mode voltage. Once a value is settled on for R_O and the common mode bias point, it should be rechecked over the expected range of input signal values to verify common mode restrictions are met dynamically and readjusted if necessary. Also consider that part of the R_O current flows in R_I and through the source driving the input. The source must be able to accommodate this current.

The differential configuration is so useful that in section 7.0, several design examples will be explored. Appendix A outlines a procedure for the design of this circuit.

4.0 EXPANDED TECHNIQUES

4.1 BRIDGE CONNECTION

The bridge connection shown in Fig. 4 (next page) uses the differential configuration for the master, A1 amplifier, and a unity gain inverter for the slave, A2 amplifier. The slave non-inverting input is referred to a point on a divider at half supply voltage. Since this divider is referred to the supply, there will be susceptibility to power supply variation. Note that the zero output point is defined as the point where both amplifier outputs are equal, and this point is set by the non-inverting input of the slave.

The preferred way of improving the bridge circuit tolerance to power supply variations would be to regulate the half supply point. In the event this is not possible or desirable, Fig. 5 (next page) shows a bridge topology that reduces sensitivity to supply variations. The ratio of R2/R1 should be ratio matched to the ratio of R3/R4. Note that gain of A1 will be:

$$A_V = ((Rf/Ri)+1) \bullet (R2/(R2+R1))$$

Or, consider that while R1/R2 attenuate the input signal by half, and the bridge circuit effectively doubles circuit gain with respect to the load, then A_V is equal to the non-inverting gain of A1, or R_F/R_I+1.

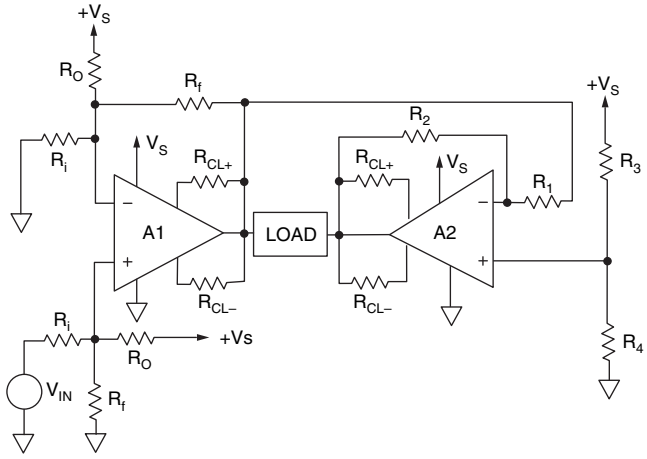


FIGURE 4. BRIDGE MODE WITH SINGLE SUPPLY OTHER THAN PA21

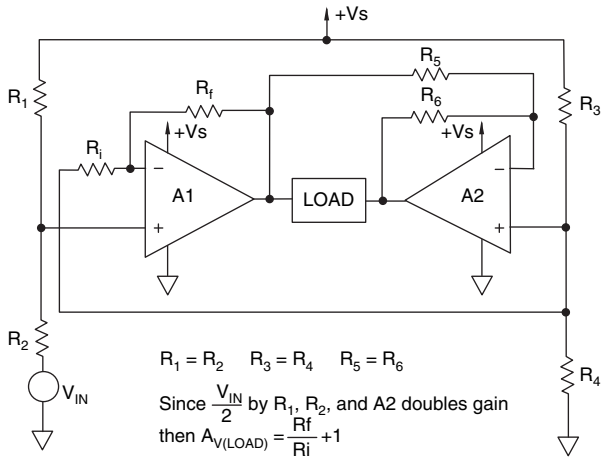


FIGURE 5. MODIFIED SINGLE-SUPPLY BRIDGE FOR IMPROVED SUPPLY REJECTION

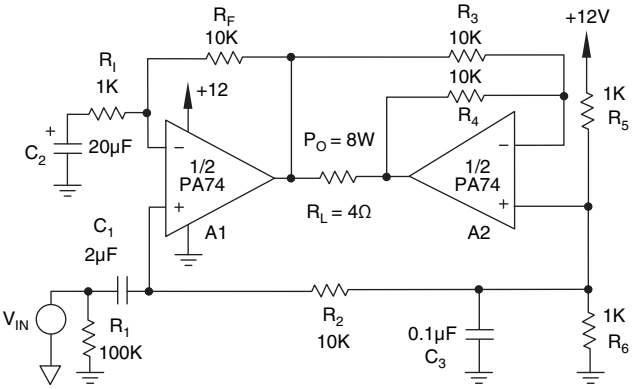


FIGURE 6. AC COUPLED BRIDGE

The AC coupled bridge is a special case of the single supply bridge amplifier circuit, and is especially useful for audio where a stable DC operating point is desirable. Fig. 6 depicts such a circuit. Note that both non-inverting inputs use the half supply point as a bias reference. C1 AC couples the input signal. C2 blocks the DC ground path in the feedback loop insuring a unity gain for A1 at DC.

4.2 CURRENT OUTPUT CONFIGURATION

Any voltage to current configuration is possible in the single supply environment, as long as common mode restrictions are met. The floating load current source will be restricted to unipolar outputs although the output cannot swing to zero current. Of course a bridge topology has many benefits including bipolar output, the ability to deliver zero current, and more voltage available to the load. In magnetic deflection applications, the higher voltages make for faster current transitions.

Since the Improved Howland Current Pump resembles a differential amplifier, it easily lends itself to single supply applications. The only modification will be the addition of the R_O common mode biasing resistors. The Howland is subject to wide dynamic range variations on both input and amplifier output with an infinite number of possibilities when various gains are factored in. Suffice to say the designer must analyze input common mode values at the four extremes of dynamic range:

1. Most positive input, most positive output
2. Most positive input, most negative output
3. Most negative input, most negative output
4. Most negative input, most positive input.

5.0 SPECIAL OP AMP CASES

5.1 PA02 SINGLE SUPPLY BEHAVIOR

A PA02 presents a special problem in single supply application. Like all BiFET input op amps, a negative common mode violation on either or both inputs causes the output to go full positive. Common mode violations are inherent in power up conditions in all op amp circuits since common mode is measured with respect to the supply rail.

In the case of a PA02, when the inputs are closer than 6 volts to either supply rail there is a common mode violation. It is implicit in this requirement that until total rail-to-rail supply voltage has reached at least 12 volts, the amplifier will not be linear. With a PA02 in particular, until the negative supply rail is at least 5 to 6 volts more negative than BOTH inputs, the output will be hard positive. This causes PA02 output to go full positive during power up in single supply applications. When used as an audio amplifier, this results in a loud “pop” from the speaker during power up.

There is no elegant solution to this problem. If the speaker is AC coupled and returned to positive supply rather than ground, this may help some. But most applications have shown the only dependable solution would be a relay that closes the circuit to the speaker once full supply voltage has been reached.

5.2 PA74 SINGLE SUPPLY CONSIDERATIONS

A PA74 is without a doubt the easiest power op amp to use on single supplies since the input common mode range can actually go more negative than the negative rail. Inputs can be applied to a PA74 in single supply applications without the need for additional biasing circuitry. The circuit shown on the front of the PA74 data sheet illustrates just how easy it is to apply for unipolar inputs in a DC motor drive application.

5.3 COMMON MODE BEHAVIOR IN GENERAL

It is helpful if the designer has some idea of which amplifiers are subject to unusual behavior during common mode violations. Like the BiFET PA02 described above, any FET input power op amp can exhibit polarity reversals during common mode violations. The polarity of most FET input stages, such as a PA07, all high voltage op amps, and Burr-Brown's OPA541, are such that a positive common mode violation will cause a reversal of output polarity. This occurs since gate to drain of input FETs becomes forward biased under these conditions and the signal effectively bypasses the FET and its normal inversion.

5.4 AMPLIFIERS WHERE SINGLE SUPPLY OPERATION IS NOT RECOMMENDED

The use of a PA89 in single supply circuits is discouraged. The input common mode voltage range dictates the inputs must always operate at least 50 volts inside of either supply rail, an impractical value to establish bias in the differential configuration. Unsymmetrical supply techniques are more applicable for getting large unipolar swings out of PA89 circuits. In the case of a PA89, the smaller supply needs to be at least 50 volts.

The power boosters PB50 and PB58 also present unique problems. For example, the ground pin of these parts must "see" a clean analog ground with low impedance over a wide bandwidth. This can be difficult to insure in a single supply environment. A PB50 must operate with its ground pin 30 volts more positive than the negative rail, while a PB58 must operate at least 15 volts, and preferably 20 volts more positive than the negative rail. While it is possible to use these parts in a single supply environment, it is far preferable to use them with split or unsymmetrical supplies.

6.0 TURN ON "POPS"

Regardless of amplifier choice, audio applications where the load is AC coupled and connected to ground will always be susceptible to turn on "pops". The two main reasons this occurs are: the amplifier is not linear until supply voltage is high enough; and the amplifier output inherently must go from zero to about half supply.

A bridge configuration will often improve (reduce) the likelihood of pops. Or as mentioned above, a relay which closes the circuit to the load once full supply voltage has been reached can help; although, with an AC coupled grounded load the output capacitor must still be charged.

Controlling power supply rise time to be sufficiently slow can also alleviate this problem. It may require slowing it such that it even takes seconds. Even this technique will add a relay or some type of solid state switch. The easiest way to implement a slow rise supply is with a sufficiently large resistor in series with a filter capacitor.

7.0 DESIGN EXAMPLES

7.1 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input signal range = 0 to 5 volts. Unipolar output, single ended.

A PA12 has been selected for a unipolar voltage output motor drive. Differential configuration is selected, see Fig. 7. (Note that many details will not be discussed here, but are covered in other app notes, such as current limit resistors, flyback diodes, and power supply bypassing.)

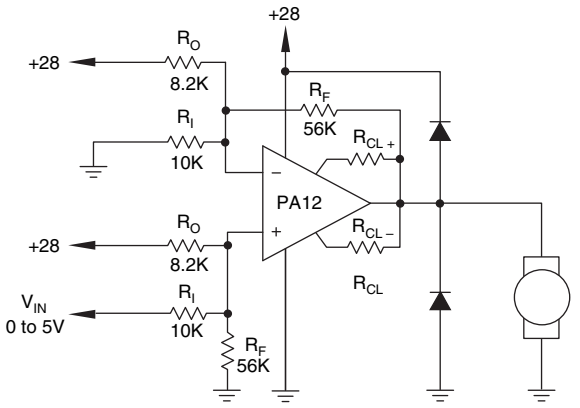


FIGURE 7. UNIPOLAR MOTOR DRIVE EXAMPLE

Select R_F/R_I: This requires arbitrarily fixing one of these resistor values. In general, the best practice is to fix R_I at about 10K ohms, as this is an impedance that most any small signal source will drive with no problem.

dV_{IN} has been established at 5 volts. While it is true that an op amp output cannot actually swing exactly to each rail, the circuit scaling should be selected as if it could; therefore, on a 28 volt supply, dV_{OUT}=28 volts. This results in a value for R_F of 56K ohm.

$$\frac{R_F}{R_I} = \frac{dV_{OUT}}{dV_{IN}}$$

Now R_O must be selected to respect PA12 common mode requirements which dictate that the inputs must be kept 5 volts inside of either supply rail. So the inputs could be set anywhere from 5 to 23 volts. An ideal value would be 14 volts. Let's try an R_O value based on that and see if currents through the input resistors and input terminals remains reasonable. From the equation in 3.2 above, this would result in an R_O value of approximately 8.48K ohms, nearest standard value 8.2K ohms. This would result in 1.65mA flowing to the input terminals and no inordinate power dissipation in any of the input circuit resistors.

Since the process used to select R_O is based on worst case negative voltage input/output relationships, the common mode should be re-checked for full positive inputs and outputs. Assuming +5 volts at the input and a theoretical +28 volts at the amplifier output, the circuit simplifies to R_O and R_F being in parallel to +28 volts and forming a voltage divider with RI as the ground leg. This results in a voltage at the amplifier input of 16.32V, that is within the maximum positive common mode restriction of 23 volts.

7.2 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input voltage -2.5 to +2.5 volts. Voltage in, current output (will require Improved Howland Current Pump). Output range ±2A.

A PA02 is selected for this application along with a bridge circuit. Referring to Fig. 8, the R1, R2 and R4, R3 ratios were selected to provide the required transfer function based on a 0.301 ohm current sense resistor, R_S. Note that over the expected normal range of input signals and output voltages that common mode requirements are met. While true for this application, each one should be checked to verify the voltages are within acceptable limits. Note that even on this circuit that exceeding the ±2.5 volt dynamic range on the inputs will cause common mode violations to occur.

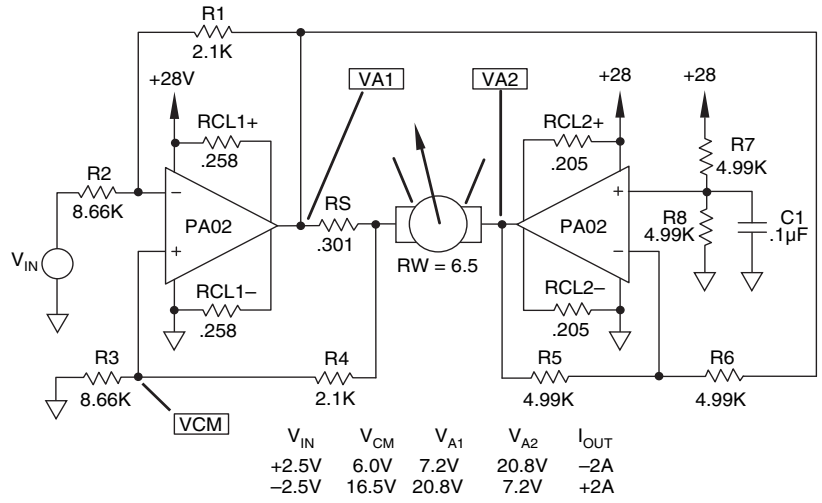


FIGURE 8. LIMITED ANGLE TORQUE CONTROL (SINGLE SUPPLY)

7.3 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. High voltage bridge for piezo drive. Low power consumption.

A PA88 is selected to meet low consumption requirements, the circuit is shown in Fig. 9. R_F and R_I must provide a gain on the master amplifier of 45. In the process of minimizing power consumption and maintaining a reasonable physical size for components, consider there can be as much as 450 volts across R_F. In order to use a half watt resistor, R_F would need to be 510K ohms. For a gain of 45, R_I would then be 11K ohms.

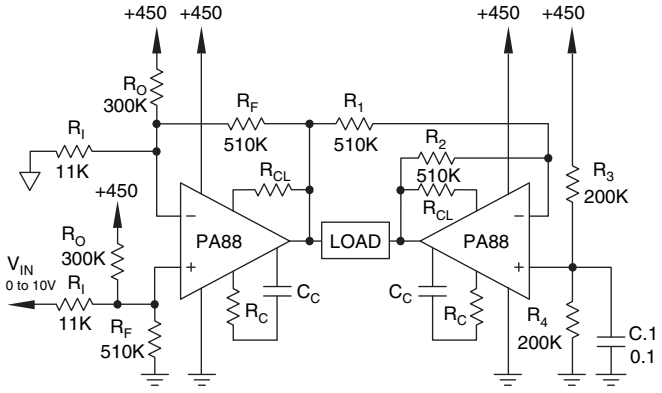


FIGURE 9. PA88 H.V. BRIDGE

In this high voltage application, it is wise to design for the minimum acceptable common mode voltage which is 12 volts for a PA88. 15 volts will be used to provide a little margin. 300K ohms will be required for R_O. 510K ohms will also be required for both gain setting resistors on the slave.

The half supply reference point resistors will each have 225 volts across them. The minimum acceptable value for half watt resistors would be 101K ohms each, but to minimize consumption, 200K ohms each is used. These must be bypassed.

With the large value feedback components around the slave, amplifier problems can result from feedback poles being created by amplifier input capacitance and stray capacitance. This may require a small compensation capacitor from 2 to 20 pF across the feedback resistor.

7.4 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. Wide band high voltage driver. Single ended.

The circuit in Fig. 10 contrasts with the previous example in that it is a wideband circuit and requires the lowest possible impedances at all modes. The standard differential configuration will be used. This is an example where minimum common mode bias will have to be set to avoid excessive current and dissipation problems in resistors.

Gain for this circuit will be 45. In order to use the lowest possible value for R_F to insure good bandwidth, a 5 watt resistor will be used. Assuming worst case voltage stress across R_F to be 450 volts, the lowest permissible standard value is 43K ohms. For a gain of 45 volts, R_I must be (nearest standard value) 910 ohms. Because of such low impedances, a minimum common mode bias (from the PA85 data sheet) of 12 volts must be set.

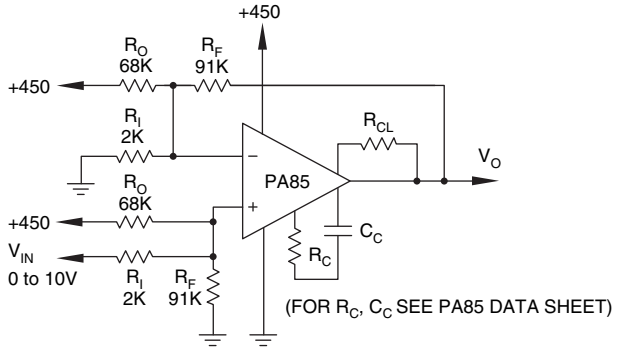


FIGURE 10. PA85 H.V. DRIVE

Solving for R_O, assuming 12 volts of common mode bias, with an input of 0 volts and theoretical 0 volt output, the value is (nearest next lowest standard value) 30K ohms. This resistor will have 438 volts across it and will dissipate 6.4 watts. In addition, 15mA will flow through the input terminal. These values will be difficult, if not impossible, to work with. It may be possible to scale up by a factor of two and have sufficient bandwidth.

Re-calculating using 91K ohms R_F, and 2K ohms R_I, R_O solves to 68K ohms, the nearest standard value. Dissipation in R_O is now 2.8 watts and 6.3mA flows to the input resistor. While these numbers are better, they could still be a problem. Further scaling up of impedances will aggravate bandwidth problems as the effects of parasitic and amplifier input capacitance become significant.

This design example has been shown to be feasible in the design of a single supply circuit. But use of a –15 volt supply for the negative rail will eliminate the impedance constraints and permit the circuit to be designed for maximum possible bandwidth with a conventional circuit.

APPENDIX A: PROCEDURE FOR DESIGN OF DIFFERENTIAL CONFIGURATION

1. Select R_F and Ri:

$$\text{GAIN} = \frac{R_F}{R_I} = \frac{dV_O}{dV_I}$$

In general, R_I should be the resistor value on which all others "pivot." This is because R_I essentially represents the load presented to the input signal. Most small signal op amps work best if R_I is 10K ohms or larger, but many would permit R_I to drop as low as 1K or 2K ohms if necessary.

2. Select R_O:

$$R_O \quad \frac{V_S - V_{CM}}{\left(\frac{V_{CM}}{R_I \,||\, R_F}\right)} \text{ (MIN, from amplifier data sheet)}$$

3. Check dissipation in Ro. If too high, all resistor values need to be re-scaled upward.
4. Re-check V_{CM} at all four possible extremes of both input signal and amplifier output voltage. Although some of these operating conditions may not actually occur, it is wise to have a circuit that has linear common mode bias under all conditions if for no other reason than it is the only hope the op amp has to recover from the following conditions:
   a. Full negative input (usually 0), full negative output (theoretical 0). This condition is accounted for in the equation to select R_O.
   b. Full negative input, full positive output (assume theoretical maximum equal to supply voltage).
   c. Full positive input (don't forget that most small signal op amps could swing beyond their 10 volt linear limit, often up to a full 15 volts), full negative output.
   d. Full positive input, full positive output.

If any of these four conditions do not meet common mode restrictions, adjust R_O accordingly. For instance, if a violation is more negative than minimum allowable common mode bias, reduce R_O (most common likely problem). If the violation is positive, which is unlikely with most realistic bias levels, then R_O should be increased.

5. If being used in a bridge, it is recommended that the slave amplifier noninverting half supply bias point be regulated, either with a zener diode or derived from some regulated voltage.

SOA and Load Lines

1.0 MEANING OF SOA GRAPH

SOA (Safe-Operating-Area) graphs define the acceptable limits of stresses to which power op amps can be subjected. Figure 1 depicts a typical SOA graph.

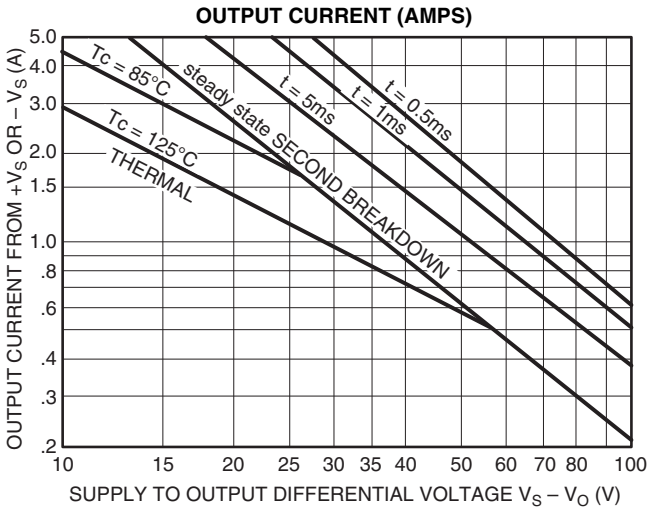


FIGURE 1. TYPICAL SOA PLOT

The voltage value on the right of the graph defines the maximum with no regard to output current or device temperature. Note that this voltage is related to the output voltage but is different; these two voltages are NOT interchangeable. The current value at the top of the graph defines maximum; again, with no regard to temperature or voltage. Inside the graph area will be one or more curves with a slope of -1 (as voltage doubles, current drops to half) labeled with a case temperature. These are constant power lines defined by DC thermal resistance and the rise from case temperature to maximum junction temperature (2.6°C/W and 200°C in this case). Lines with a steeper slope (about -1.5 in this case) are unique to bipolar output transistors. The steady state second breakdown reduces the amplifier's ability to dissipate DC power as voltage becomes more dominant in the power equation. Fortunately, the lines with time labels indicate higher power stress levels are allowed as long as duration of the power stress does not exceed the time label.

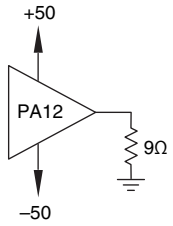
Transient SOA limits shown on data sheets are based on a 10% duty cycle pulse starting with junctions at 25°C. The repetition rate then would logically be defined by the time required for the junction to return to 25°C between pulses. Some amplifiers such as PA85 allow transient currents beyond the maximum continuous current rating. Most often though, the transient ratings are based on power or second breakdown restrictions.

2.0 ANALYTICAL METHODS

2.1 PLOTTING RESISTIVE LOAD LINES

Resistive load lines can be plotted quite easily. Keep in mind that since SOA graphs are log-log graphs, the resistive load line will have a curvature, so several points should be calculated and plotted.

Output voltage and current will always have the same polarity with a resistive load, so calculations can be performed at all times from 0 to 90° of the output cycle. Figure 2 depicts an example of resistive load line. It is interesting to note that this is a safe load which can require a 5 amp peak capability. If the output of the PA12 is unintentionally shorted to ground the voltage stress on the output will be 50 volts, which is not safe at the 5 amp current limit required to drive the load. In applications where the amplifier output would not be subject to abuse these operating conditions are acceptable. Foldback current limiting can be used to improve on the safety of this situation.



V_O	V_S–V_O	I_O
0	50	0
5	45	.556
10	40	1.11
15	35	1.67
20	30	2.22
25	25	2.78
30	20	3.33
35	15	3.89
40	10	4.44
45	5	5.00

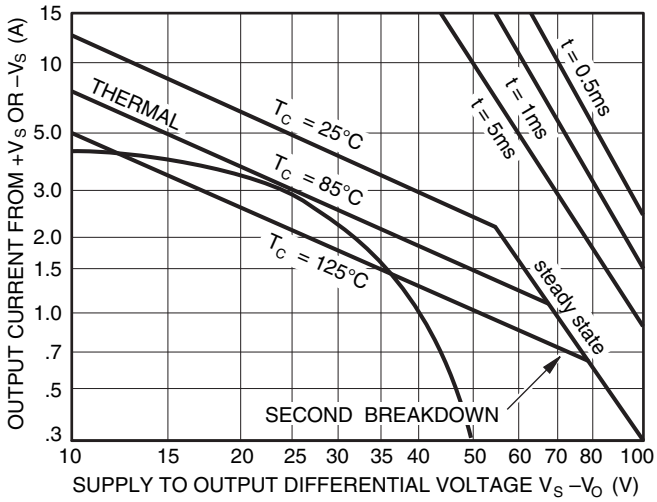


FIGURE 2. PLOTTING RESISTIVE LOAD LINE

2.2 PLOTTING REACTIVE LOAD LINES

Reactive load lines of any phase angle can be plotted with the methods shown here. A completely reactive load line almost looks like an ellipse on the SOA graph since current stresses will occur at two different levels of voltage stress.

The voltage output waveform will define the reference phase angles for all point-by-point stress calculations. The waveform shown in Figure 3 (next page), starts at –90°, since current in capacitive loads will lead in phase. The waveform ends at 270° since that corresponds to the maximum phase lag of the current in an inductive load. All calculations will be within the limits of these angles.

Calculations proceed according to the steps in Figure 4 (next page). Currents will only need to be calculated over 180° since the load line for each half of the amplifier is a mirror image. Capacitive loads will start at –90° and progress through +90°.

Inductive load calculations will start at +90° and progress to +270°. Step 2 in the procedure defines the starting angle for calculations based on the load phase angle. For example, a –45° load would start at –45° and continue to +135°. A 45° load will start at 45° and continue to 225°

VOLTAGE WAVE FORM ESTABLISHES REFERENCE PHASE ANGLE FOR ALL LOAD LINE CALCULATIONS. SHADED AREA REPRESENTS CALCULATION REGIONS

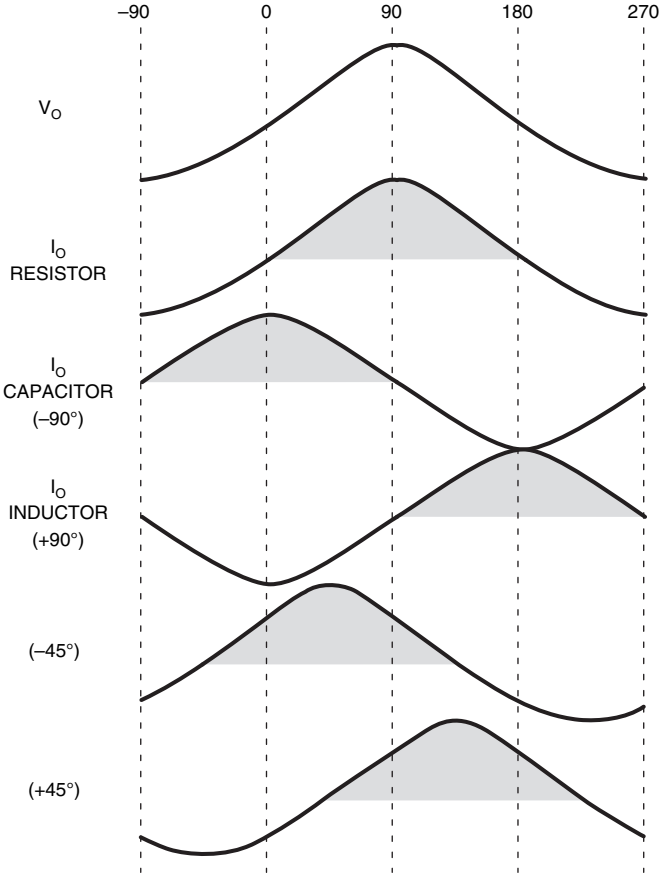


FIGURE 3. TYPICAL WAVEFORMS ASSOCIATED WITH REACTIVE LOAD LINE ANALYSIS

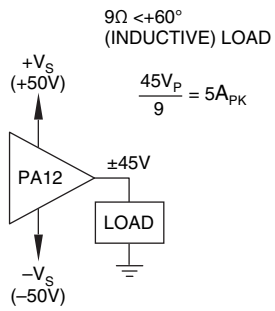
Example of a typical load calculation:

1. KNOWN: Vp , Z_L, Θ_L
2. BEGIN POINT CALCULATIONS WITH Θ_L AT 0° + Θ_L AND PLOT FOR NEXT 180° IN WHATEVER INCREMENTS NEEDED FOR DESIRED ACCURACY (15° OR 30° INCREMENTS RECOMMENDED.)
3. Ipk = $\frac{Vp}{Z_L}$ CALCULATE ONLY ONCE
4. CALCULATE EACH INCREMENT: $I = Ipk (\sin (\Theta_V - \Theta_L))$
5. CALCULATE EACH INCREMENT: $Vd = Vs - Vp (\sin \Theta_V)$

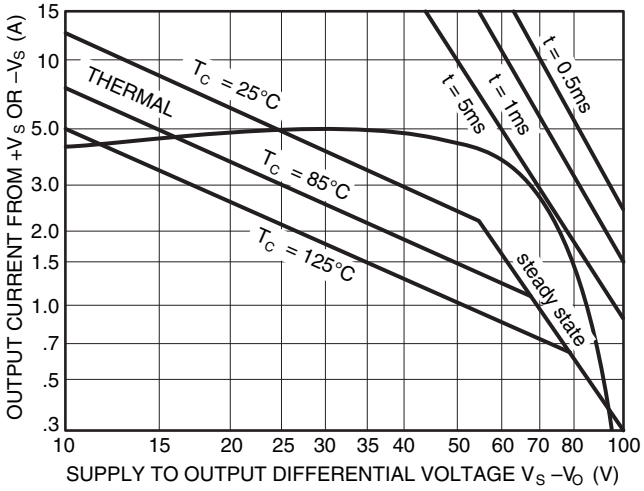
FIGURE 4. REACTIVE LOAD CALCULATIONS

In the resistive load example the load line of a 9 ohm resistive load was plotted and was quite safe. For this example let's use the same impedance but with a 60° phase angle.

Figure 5 shows a PA12 driving an inductive load of 9 ohm at 60°. From step 2 of our procedure we know we begin calculating current at 60° and continue to 60+180 or 240°. For this example we will use 15° increments. Actually, it is only necessary to perform the step-by-step calculations for current up to the point where peak current occurs, in this case 150°. The increments back down to 240° will be a mirror image of what was just calculated. However, don't get this lazy with the voltage calculations we have yet to do.



Θ_V	I	Vd ($V_S - V_O$)
60	0	11
75	1.29	6.53
90	2.5	5
105	3.54	6.53
120	4.33	11
135	4.83	18.2
150	5A	27.5
165	4.83	38.4
180	4.33	50
195	3.54	61.6
210	2.5	72.5
225	1.29	81.8
240	0	89



(NOTE THAT Pd max = $\frac{Vs^2}{2Z_L} \left| \frac{4}{\pi} - \text{Cos } \Theta_L \right| = 107$ w

FIGURE 5. TYPICAL LOAD LINE CALCULATIONS

Even though the point of maximum voltage stress occurring at full negative output swings is not evident in the voltage stress calculations, it is inconsequential since we have established that no current flows through the output device at that time. As long as the amplifier itself is within its voltage ratings, all will be well.

After all points are calculated, they may be plotted on the SOA graph. In this particular case note there are significant excursions beyond the steady state 25°C SOA limit. Is this acceptable? Consider the following factors to help make the decision: 1. The area beyond the continuous SOA is quite sizeable. 2. A calculation of maximum average power dissipation using the formula shown in Fig 5 (refer to General Operating Considerations for background on this calculation) shows the amplifier dissipating 107 watts.

The 107 watt dissipation will certainly cause the amplifier to operate at significantly elevated temperatures, even with a generous heatsink. Realistically the SOA limits are being reduced by the heating. We can even define exactly how badly. Assume a 25°C ambient (that's pretty optimistic). Using an HS05 heatsink rated 0.85°C/watt results in an amplifier case temperature 91°C. It is evident that the PA12 is not well suited

for this application. The alternatives include either paralleling PA12s or upgrading to a PA05.

2.3 SPECIAL CASES OF LOAD LINE PLOTTING AND OTHER GENERALIZATIONS

For parallel connected amplifiers, assume each amplifier drives a load rated at half the current of the total load. In essence, double the load impedance. Do just the opposite for a bridge circuit.

Some simple relationships to keep in mind: for totally reactive loads maximum current occurs at a voltage stress corresponding to Vs and maximum dissipation occurs at a voltage stress of Vs+(0.707Vs), where current is also 0.707*Ipeak. In a resistive load, stresses are much less with maximum current occurring at maximum output voltage swing. This generally corresponds to the maximum swing specification given in every amplifier data sheet.

Also keep in mind that there are many load lines which will fit well within an amplifier SOA and be quite safe to drive. Yet these same loads can demand current capability that requires current limits be set so high the amplifier output will not be able to tolerate inadvertent shorts on its output. This is usually acceptable in applications with committed loads; however, applications where the amplifier output terminals are accessible to poorly defined loads or fault conditions demand fault tolerance on the part of the amplifier. A good example is a set of screw terminals like those found as the output connectors of an audio amplifier.

The methods shown here calculate load lines for reactive loads at only one frequency. For inductive loads worst case stresses will occur at the lowest frequency of interest with the opposite true for capacitive loads.

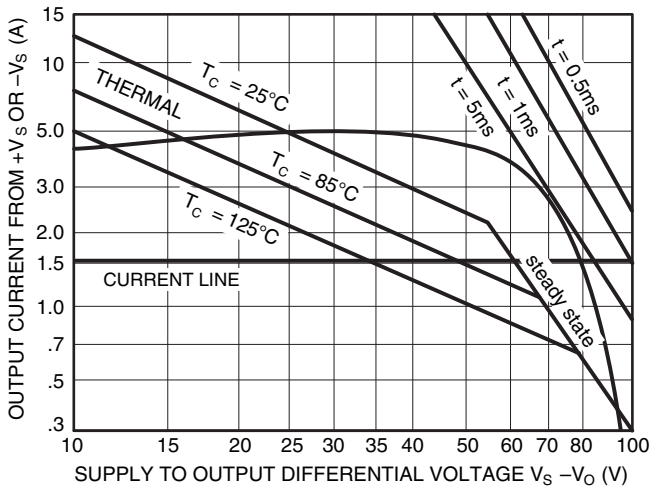
MOSFET amplifiers have an important difference from bipolar amplifiers regarding SOA limits: MOSFETs are only limited by power dissipation, or the product of V*I stress. Bipolar amplifiers are power limited up to certain voltages indicated on the SOA graphs, where second breakdown imposes even lower limits on safe current than power dissipation would allow.

2.4 PLOTTING AMPLIFIER CURRENT LIMITS

Additional information which can be plotted on the SOA graph to help assess amplifier safety is the current limit of the amplifier. Simple fixed current limiting is simply plotted along the current corresponding to that limit. Any load line excursions beyond that level can be disregarded. They are simply not possible.

Figure 6A depicts the SOA graph from Figure 5 with a fixed current limit drawn in. The fixed limit is set to 1.5 amps to provide short circuit safety at up to 85°C case temperature. It is obvious the load line is totally outside this current limit. The maximum available output will be set by the 1.5 amp current limit and impedance of the load. Or in the case of a resistive load, the lowest load impedance is a function of maximum output voltage and current limit.

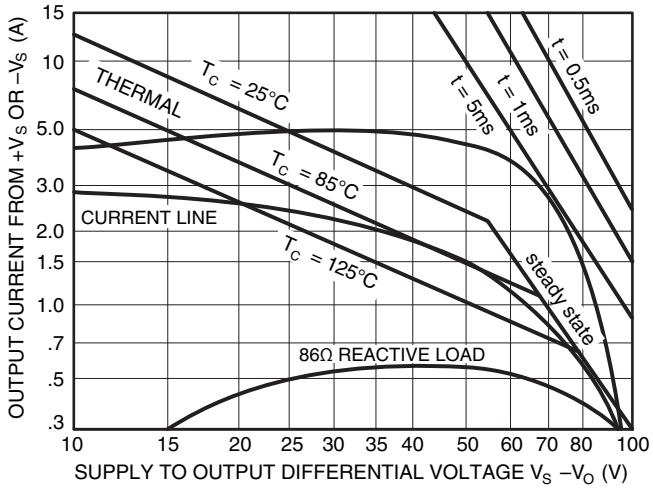
Foldover current limiting can also be plotted on an SOA graph. This is important with inductive loads since foldover limiting in conjunction with inductive loads can cause more problems than it solves unless applied carefully. When foldover current limiting occurs with an inductive load, a violent flyback spike occurs that transitions all the way up to one of the supply rails. External ultra-fast recovery flyback diodes are a must when combining foldover limiting and inductive loads. It is also possible for relaxation oscillation to occur. This can be prevented by insuring that the normal inductive load line is well within



A FIXED 15A CURRENT LIMIT

Max V_O(PEAK) REACTIVE = I_{LIM} x Z_L

$$\text{LOWEST POSSIBLE } R_L = \frac{V_O\,(pK)}{I_{LIM}} = \frac{45}{1.5} = 30\Omega$$



B FOLDOVER CURRENT LIMIT

R_{CL}= 0.433Ω PIN 7 OF PA12 GROUNDED

$$I_O = \frac{.65 + V_O\left(\frac{28}{20}\right)}{R_{CL}}$$

$$\text{LOWEST POSSIBLE } R_L = \frac{45}{2.8} = 16\Omega$$

REACTIVE LOAD

$0.707\ I_{PK}$ @ $V_S + 0.707\ (V_S) = 50 + 35 = 85V$

I_{LIM}@ 85v = 370 mA

$$\frac{0.707\ V_O}{0.37A} = \frac{0.707 \times 45}{0.37} = 86\Omega$$

FIGURE 6. PLOTTING CURRENT LIMITS

all limiting values.

Figure 6B portrays foldover limiting according to formulas contained in Application Note 9 or the PA12 data sheet. The load of Figure 5 obviously cannot be driven. Note that with foldover limiting a peak current of 2.8 amps is available yet short circuit current is limited to 1.5 amps making it possible to safely drive a 16 ohm resistive load. To determine the minimum acceptable value for a reactive load, consider that 70.7% of peak current

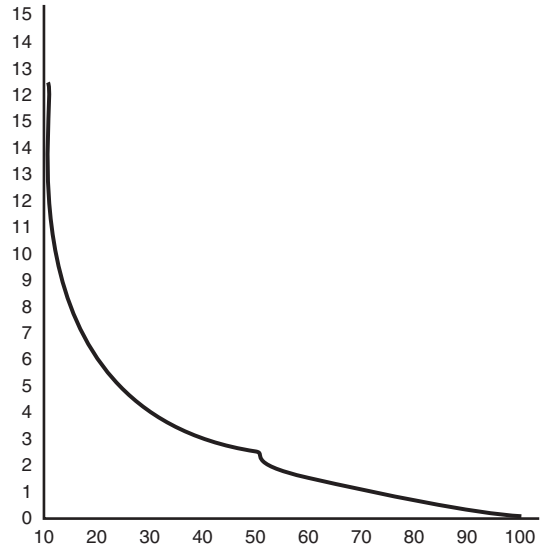
occurs at a voltage stress of Vs+(0.707Vs). A reactive load line within that operating point will likely be within all operating points and representative of minimum acceptable load.

Figure 6B depicts the worst case acceptable reactive load. It really doesn't fill up much of the permissible operating region, but such are the trade-offs involved in driving difficult loads.

3.0 BENCH TESTING SOA

An oscilloscope can be used to do real world plotting of load lines on actual working circuits. The SOA limits can be drawn in on the scope screen if necessary. First, the SOA limits should be redrawn on linear-linear graph paper. This results in an SOA graph as shown in Figure 7A. The graph shown is for a PA12 bipolar amplifier, and second breakdown causes the break in the shape at 55 volts. MOSFET amplifiers will have a continuous curve representative of power dissipation. This can then be transferred to a transparency sized to properly fit on a scope screen.

A



B

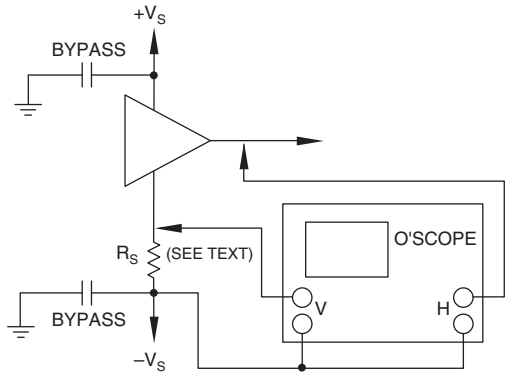


FIGURE 7. OSCILLOSCOPE TESTING OF SOA

The easiest method of connecting a scope to plot actual output device stresses will be to refer the scope ground to the negative supply of the circuit as shown in Figure 7B. This connection results in the proper phases for easy viewing on the oscilloscope. Since the oscilloscope ground is connected to the negative supply line, be certain there is ground isolation either in the amplifier power supply or the oscilloscope is connected to an isolation transformer.

Rs is a current sensing resistor. When possible, use of a 1 ohm resistor provides a direct scale factor on the vertical input of volts = amps. If other values must be used consider scaling accordingly. The current sense resistor must be right at the amplifier power pin. This is one of those rare cases where it is temporarily necessary to violate the rules of proper power supply bypassing. Any capacitance present at the node, where the resistor meets the amplifier will interfere with high frequency measurements. If an oscilloscope current probe is available it is certainly preferable to the current sensing resistor since it provides accuracy and speed without having to disrupt the circuit.

4.0 SOA MEASUREMENT CIRCUITS

Another means of analyzing SOA stresses in operating circuits uses an analog multiplier to calculate real time instantaneous power dissipation. This method is especially applicable where second breakdown is not encountered. For example, working with MOSFET amplifiers under any condition or most bipolar amplifiers at total rail-to-rail supply voltages of less than 30 volts.

The circuit shown in Figure 8 senses output device current and voltage stress as is done with an oscilloscope. Differential amplifiers with wide common-mode ranges are used for sensing these values and levels, translating them to be applied to an analog multiplier. The output of the multiplier will be the product of the voltage and current stress on the output device. The Rs current sense resistor must be in the supply line so current is measured in only the output device corresponding to the voltage stress measurement.

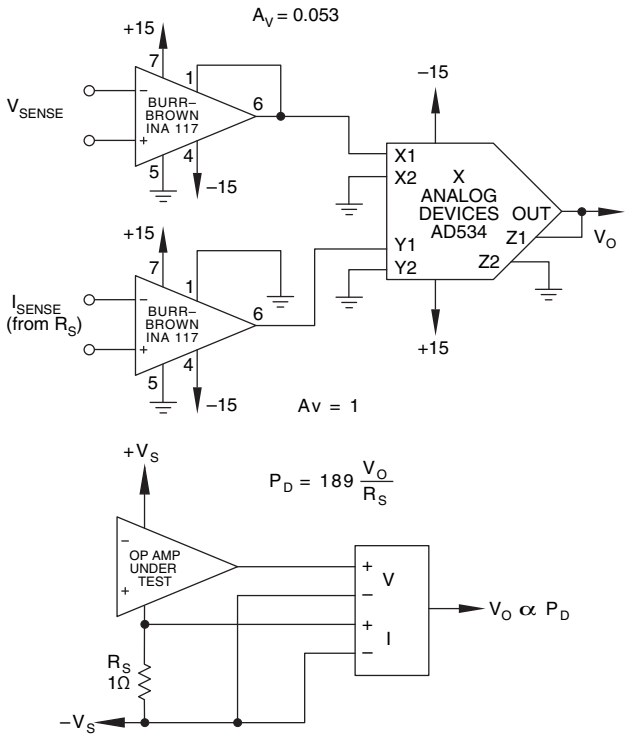


FIGURE 8. INSTANTANEOUS POWER DISSIPATION TESTER

This circuit provides a signal indicating instantaneous power dissipation. When working with a MOSFET amplifier such as the PA04, the designer should be concerned that this output be

$$Z_L = |Z_L|$$

$$P_{D\,(OUT)MAX} = \frac{2Vs^2}{\pi^2 Z_L \cos\Theta}\ ,\ \Theta < 40$$

$$P_{D\,(OUT)MAX} = \frac{Vs^2}{2Z_L}\left[\frac{4}{\pi} - \cos\Theta\right]\ \ \Theta > 40$$

$$P_{TOTAL} = P_{D(OUT)MAX} + P_{D(IQ)}$$

within the 200 watt dissipation of the PA04, or less if elevated temperatures are considered.

5.0 OTHER FACTORS FOR DETERMINING SOA FIT

Since different SOA limits are shown for different temperatures, it is helpful to be able to predict the amplifier temperature. One factor that only the designer can define is ambient temperature. In particular, maximum ambient temperature.

Amplifier power dissipation will also be a factor in determining case temperature. Equations for predicting power dissipation maximums are discussed in the Apex Precision Power Handbook, "General Operating Considerations", section 7.0, and the equations are shown here for convenience:

Once worst case dissipation is known, use the heat sink thermal resistance and ambient temperature to calculate amplifier case temperature since SOA temperature limits are based on case temperature.

Effects of current limiting with reactive loads can also be evaluated when plotting load lines. Current limit lines can be drawn on the SOA representing current limit values. If reactive loads exceed these limits, distortion will occur. Often an inductive load causes what appears at first to be crossover distortion when viewing an amplifier output. In fact, what is actually occurring is that the current peaks when voltage transitions through zero and a light excursion into current limit looks much like crossover distortion.

Foldover current limits can be plotted on SOA graphs point by point as is done with load lines. Again, reactive loads must fit well within current limits. This is especially important when relaxation oscillation can occur if current limits are exceeded. In such cases the foldover effect must be reduced or even eliminated.

6.0 AUTOMATED LOAD LINES

For DC and sine wave outputs, use Power Design[1] to plot a load line. Make sure the load line does not cross the shortest time curve and that excursions beyond any other second breakdown curve do not exceed the time label, and have a duty cycle of no more than 10%.

[1] Note 1. Power Design is a self-extracting Excel spreadsheet available free from www.Cirrus.com.

Brush Type DC Motor Drive with Power Op Amps

1.0 AMPLIFIER SELECTION

One of the most entertaining moments as a power op amp applications engineer is when a customer calls up asking for an op amp to drive a 24V, 2A motor and has already settled on a 5 amp amplifier. It's just not that simple. This current rating could have many meanings, and actually there are two current rating conditions to be considered when designing a reliable application: stall current and reversal current.

Reversing a motor is about the most stressful application to which power op amps are subjected. It's important to establish from the outset if it will be necessary to sustain reversals. Some applications can disregard this; a good example being a simple speed control for a motor always rotating the same direction.

1.1 STALL RESISTANCE

Every motor will be stalled. This is the required state of transition to get a motor rotating. And it is doubtful any mechanical system can be devised which is guaranteed to never jam.

A single operating point for the stalled condition can be plotted. The location of the point is defined by several factors: 1) If the product of current limit and stall resistance is greater than maximum output voltage swing ((Ilim*Rs)>Vomax) the amplifier output will be at maximum swing; or 2) If the product of current limit and stall resistance is less than maximum swing, then the amplifier output voltage will be at the value of Ilim*Rs. To calculate dissipation, subtract this voltage from the supply voltage and multiply by current limit: Pd = (Vs-Vo)*Ilim

Alternatively, stall resistance can be plotted as a load line on the SOA graph. On the SOA graph, current limit should also be plotted. This is useful for conditions where the amplifier output will be attempting to go to some other value than full output voltage under stall conditions. Remember, maximum dissipation occurs at an output voltage one half way between zero and the supply rail.

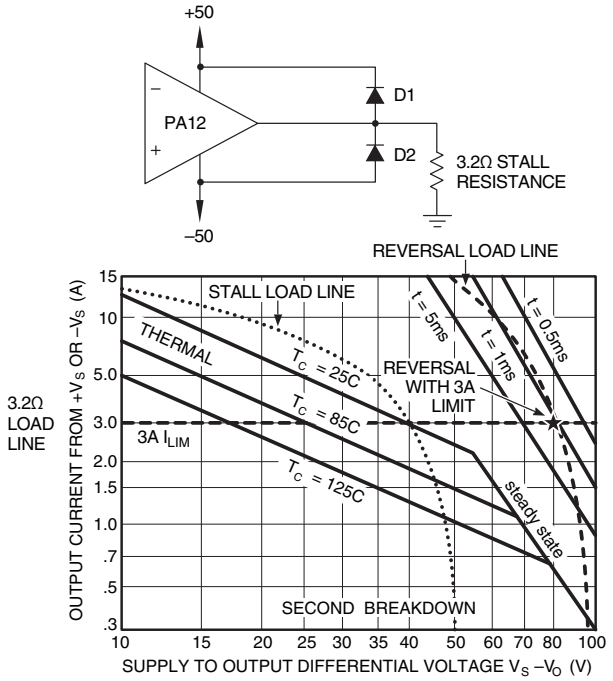


FIGURE 1. EXAMPLE OF MOTOR DRIVE LOAD LINE ANALYSIS

Figure 1 shows just such an example of a calculation. This example uses a PA12A along with a motor which has a 3.2 ohm stall resistance and bipolar ±50V power supplies. If we simply plot the condition where the amplifier is against the rail, we have approximately 44V at the output and 13.8A of current flow. The supply to output differential and current result is a dissipation of 6 * 13.8, or 82.5W, which is within the amplifier SOA. If the amplifier output voltage were commanded to one half supply rail or 25V under a stalled condition, the power dissipation would be 195W, which is beyond the continuous SOA.

This illustrates the value in plotting the stall resistance load line. Both the low output and full output conditions are within the SOA, but intermediate values create excessive dissipation and this is immediately apparent by plotting the load line. The point where the load line exceeds the 25°C continuous SOA is a good value for maximum acceptable current limit.

In summary, design for stalled conditions should at least plot the resistive load line to determine proper setting of current limits. If the load line completely falls within the SOA, then other fault conditions of shorts from output to ground or output to either rail will take precedence in determining current limit values in the event these faults must be accounted for.

1.2 REVERSAL

Reversal brings the back EMF of the motor into the stress equation. The back EMF is equivalent to a new source of voltage with a polarity such that it adds to the supply voltage and increases voltage stress on the output devices. As in the stalled condition, motor resistance also plays a part.

Determining back EMF may seem difficult, but most motor data sheets shed some light on determining its value. Knowing the motor resistance and current draw permits exact calculation of back EMF: it is the applied voltage, less the drop across the motor resistance. Worst case assumption for back EMF should assume it could be equal to applied voltage, and this would be true for any motor drawing negligible current.

The schematic in Figure 2 shows an example of what happens to the circuit in Figure 1 during reversal—assuming the amplifier current limit is set at 3 amps. Motor operating current is a function of load. So for this example, let's assume the motor requires 1A under normal running conditions. Maximum output from the PA12 could be up to 45V. Subtract 3.2V for the drop across the motor resistance for a back EMF of 41.8V. Upon command to reverse the negative half goes into 3A current limit. The resulting voltage drop across the motor resistance subtracts from the back EMF, providing the values shown during the reversal. The dissipation during this event is 246W—clearly outside the PA12 SOA. Motor reversal by nature is a transient condition. If it can be assured the motor can reverse within an amount of time equivalent to transient stress limits on the SOA graph, then the application could be safe.

1.2.1 PLOTTING REVERSAL LOAD LINE

Just as stall load lines can be plotted, so can reversal load lines. The process of plotting a worst-case reversal load line starts with the assumption that back EMF is equal to maximum amplifier output voltage. An even worse assumption is that it is equal to the supply voltage of one of the rails.

Plot the load line by:

1. Calculate the drop across the motor resistance at various currents within the SOA.

2. Subtract that voltage from the back EMF to result in the amplifier output voltage.
3. Take the resulting difference between supply rail and output as the stress point.

Figure 1 also shows its reversal load line. This load line indicates that it is not within the continuous SOA unless current is limited to approximately less than 400mA. If this application were required to tolerate reversal, an amplifier with better SOA should probably be used.

Load lines that exceed the continuous SOA, but are within transient SOA, may be safe if the time conditions are met with certainty. This is difficult to assess, and usually requires a judgement call when any signal other than pulse is present. In general, as in any case, life is simpler and more reliable if we at least make the effort to keep within continuous SOA limits.

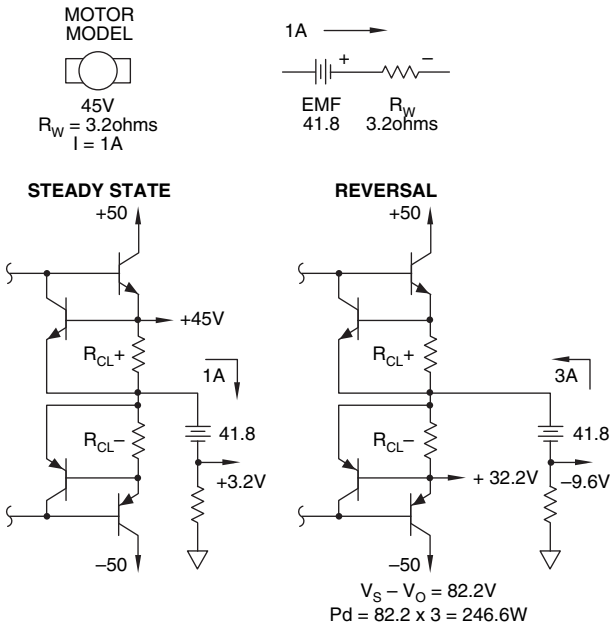


FIGURE 2. MOTOR REVERSAL

1.3 NOMINAL OPERATING CONDITIONS

Nominal operating conditions can only be determined on a by application basis. All motor data sheets shows torque and RPM constants allowing the engineer to determine required voltage and current once the load is known. The worst case normal operating point will be when the amplifier output is halfway between zero and the supply rail.

2.0 AMPLIFIER PROTECTION AND HEATSINKING

As has already been shown, the load lines must be within the amplifiers capabilities or current limit must be configured to restrict operation to within the SOA. However, the SOA shrinks with increasing temperature. Therefore, either adequate (read: generous) heatsinking must be provided for, or SOA analysis should consider limits of higher case temperature curves. Using standard heatsink formulae the exact amplifier case temperature can be determined under any operating condition (as well as junction temperature).

2.1 FOLDBACK CURRENT LIMITING

Current limit, as demonstrated, is truly a good thing and necessary. But designers must not be lured into the attraction of using foldback current limiting as available on PA10, PA12 and can be used on PA04, PA05. Reason being that foldover current limiting causes more problems than it solves when used with nonlinear loads. For instance, with inductive loads (and motors are very inductive), the amplifier can go into relaxation oscillation. And with an inductive load, when the amplifier goes into current limit, it generates a violent pulse all the way up to the supply rail (limited only by flyback diodes, without which it would go beyond the rail).

If a designer insists on experimenting with foldover current limiting, then it would be wise to plot the current limit line on the SOA along with the expected load lines. If the load lines are within the current limit boundaries, then you're OK. Keep in mind that foldover current limiting slope can be varied and sometimes a gentle foldover characteristic can provide adequate protection.

2.2 FLYBACK DIODES

Brush type DC motors generate a continuous pulse train of inductive kick-back due to brush commutation. This inductive kickback must be clamped within the limits set by the power supply rails by flyback diodes as shown in Fig. 1.

Many amplifier schematics show these diodes internally, but this does not mean they can be depended upon in motor drive applications. In most bipolar, darlington, emitter-follower output stages, these diodes are the substrate diodes of the darlington output transistors. This causes the diodes to exhibit slow recovery, which will in turn overheat under the stress of a continuous pulse train of inductive kickback.

Amplifiers with no diodes, or slow recovery diodes, internally must have external fast or ultra-fast recovery diodes added. If these are not available, then standard recovery is better than nothing. The diodes must be rated for voltage well in excess of the total rail-to-rail voltage. Current requirements are not demanding. One amp types will suffice.

All Apex Precision Power amplifiers require external flyback diodes except the MOSFET output amplifiers PA04, PA05, PA09, PA19; and the PA02 and PA03 which are bipolar amplifiers with built-in high speed flyback diodes. In general, on any Apex Precision Power data sheet schematic or in the Apex Precision Power data book, if the flyback diodes have a different part numeral than the output transistor, then they are separate fast recovery diodes. Diodes with the same part number as the output transistor are slow recovery diodes and external additions will be needed. For example in the PA12, the upper output transistor is Q2A and Q2B and the flyback diode is D2. If you're not sure, there is no harm in adding them even if they are not needed.

3.0 AMPLIFIER PERFORMANCE

3.1 VOLTAGE VS CURRENT OUTPUT BEHAVIOR

Voltage output configurations are generally used for speed control. Although a voltage output configuration can be incorporated within a larger current control loop. The importance of voltage output in the amplifier itself relates to output impedance, which will be very low. As such, the output voltage as seen on a scope will generally be quiet and steady under steady state conditions.

Current output can be implemented as mentioned above with a larger current sense loop that incorporates a voltage output power amp. Alternatively, current output circuits can be implemented within the feedback loop around the op amp alone. When this is done, the amplifier apparently exhibits a very high output impedance. A current source should do this by definition. This is mentioned because if the output of such a circuit is scoped, the flyback pulses will be exaggerated by this high impedance — a perfectly normal behavior for current output.

There is no performance advantage in selecting voltage or current output, at least not due to power op amp circuit choice alone. Many other factors will play a part in which choice provides the best performance. In general, without using larger control loops, the voltage output configuration is preferred for speed control, and the current output for torque control.

Driving Capacitive Loads

1.0 INTRODUCTION

High voltage power op amps are often selected to drive capacitive loads, such as **PIEZOTRANSDUCERS, CAPACITORS, ELECTRO-LUMINESCENT DISPLAYS, ELECTROFLUORESCENT LIGHTING, ELECTROSTATIC DEFLECTION,** etc. There are some special considerations when designing circuits to meet your high voltage needs.

We will look in detail at the selection of the power op amp, stability considerations, power dissipation in the op amp and heatsink selection, support components for the circuit, and power supplies and their effect on circuit performance. When we complete these areas of investigation we will look at some alternative power op amp circuits for attaining high voltage control across capacitive loads.

The format of our information will be "definition by example" along with generic formulae for your specific design.

2.0 EXAMPLE DESIGN FOR DRIVING A CAPACITIVE LOAD

GIVEN: +/-Vs= +/-200Vdc
frequency = DC to 10KHz (sinewave)
V_{IN} = +/-10V
piezo load with CL = 10.6nF
V_{OUT} = 360Vpp
Tambient = 25°C, free air convection cooling only
Inverting gain okay

FIND: Power op amp, heatsink and recommended schematic for piezo drive.

SOLUTION: Sections 2.1 thru 2.6 will provide a detailed, logical approach to designing a solution for this capacitive load drive problem.

2.1 POWER OP AMP SELECTION

STEP 1: Define capacitive load. Here we are given CL = 10.6nF

STEP 2: Calculate large signal response (slew rate) using highest frequency and largest voltage swing. The required slew rate to track a sinewave at a given frequency for a given output amplitude is as follows:

S.R. = 2 π f Vop (1 X 10^{-6})
Slew Rate [V/µs] = 2 X π X frequency X V_{OUT} peak X (1 X 10^{-6})
S.R. = 2 π10KHz 180 (1 X 10^{-6}) = 11.3V/µs

STEP 3: Calculate maximum current requirements. This will occur at highest frequency with capacitive loads.

METHOD 1: Calculate Xc @ highest frequency.
METHOD 2: Use highest slew rate and largest voltage swin

$$Xc = \frac{1}{2\,\pi\,f\,CL}$$

$$Xc = \frac{1}{2\,\pi\,10\ KHz\ 10.6nF} = 1.5K\Omega$$

$$Iop = \frac{Vop}{Xc} = \frac{180V}{1.5K\Omega} = 120mAp$$

STEP 4: Do a first pass worst case power dissipation calculation. For details on derivation of this formula see "General Operating Considerations."

$$Iop = CL\,\frac{dV}{dt}$$

$$Iop = 10.6nF\,\frac{11.3V}{\mu s} = 120mAp$$

For capacitive load applications this formula reduces to:

$$P_{DOUT}\ max = \frac{Vs^2}{2\ ZL}\left[\frac{4}{\pi} - \cos\Theta\right]$$

STEP 5: Summarize what we know and pick power op amp.

$$P_{DOUT}\ max = \frac{4\ Vs^2}{2\ \pi\ Xc} = \frac{4\ (200)^2}{2\ \pi\ 1.5K\Omega} = 17W$$

+/-Vs = +/-200Vdc
S.R. = 11.3V/µs
Iop = 120mAp
Vop = 180Vp
$P_{DOUT\ MAX}$ = 17W
In viewing the Apex Precision Power High Voltage Selector Guide there is only one likely candidate for this design—PA85.

STEP 6: Review the chosen amplifier's data sheets for details.
Figure 1: Contains relevant excerpts from the PA85 data sheet.
Figure 1A: From the output specifications, a worst case saturation voltage of 10V at 200mA is identified. Therefore we can meet 180Vp out at 120mAp without a problem.
Figure 1B: From the power response curve we see 360Vpp at 10KHz is within the power response curve for any value of Cc (PA85 compensation capacitor).
Figure 1C: Since we want 180Vp out for 10Vp in we will be operating at a gain of 18. This is close enough to 20 to choose Cc = 10pF and Rc = 330Ω. This will maximize small signal bandwidth as well as slew rate should a last minute decision require more performance out of the design.
Figure 1D: At Cc =10pF the slew rate is about 400V/µs, so there is no question about meeting the requirement for an 11.3V/µs slew rate.
Figure 1E: At a closed loop gain of 18, (25 dB), it can be determined that for Cc =10pF the closed loop bandwidth of this circuit (fcl) is about 2MHz. This first check says not only can a 10KHz sinewave be tracked in the large signal domain, but the PA85 will also have enough bandwidth to have a flat response at 10KHz in the small signal domain.
Figure 1F: From our previous calculation $P_{DOUT\ MAX}$ = 17W. An Applications Engineer's rule of thumb for power derating curves works as follows:

For a 25°C ambient temperature you can find a heatsink that will allow you to keep the case temperature at 85°C using free air convection cooling.

Therefore, 17W output power dissipation almost intersects with the Tc = 85°C line on the power derating curve. This means our first look says we should be able to heatsink the PA85 for this design.

Now it would seem the work is done and you can proceed to build a breadboard or commit to printed circuit board layout. But first you must proceed to look at other key issues for driving capacitive loads with power op amps such as stability.

2.2 SMALL SIGNAL STABILITY

Figure 2 is a complete schematic of our PA85 drive circuit. The gain of -18 will give us 360Vpp out for 20Vpp in. We will now look at the details for selecting stability components Rn, Cn, and CF.

Figure 3 illustrates how the amplifier's Aol curve gets modified by Ro, the amplifier's unloaded output impedance, and CL, the capacitive load. Output impedance, Ro, of the amplifier, is flat within the bandwidth of the amplifier and predominantly resistive. Refer to Apex Precision Power Application Note 19 for a detailed discussion of this issue.

2.2.1 MODIFIED AOL FOR CAPACITIVE LOADS

FIGURE 1A

OUTPUT		MIN	TYP	MAX	UNITS
VOLTAGE SWING	I_O = ±200mA	±Vs – 10	±Vs – 6.5		V
VOLTAGE SWING	I_O = ±75mA	±Vs – 8.5	±Vs – 6.0		V
VOLTAGE SWING	I_O= ±20mA	±Vs – 7.5	±Vs – 5.5		V
CURRENT, continuous	T_C= 85°C	±200			mA
SLEW RATE, A_V = 20	C_C= 10pf		400		V/µs
SLEW RATE, A_V = 100	C_C= OPEN		1000		V/µs
CAPACITIVE LOAD, A_V = +1	Full Temperature Range	470			pf
SETTLING TIME to .1%	C_C= 10pf, 2V step		1		µs
RESISTANCE, no load	R_{CL}= 0		50		Ω

FIGURE 1B

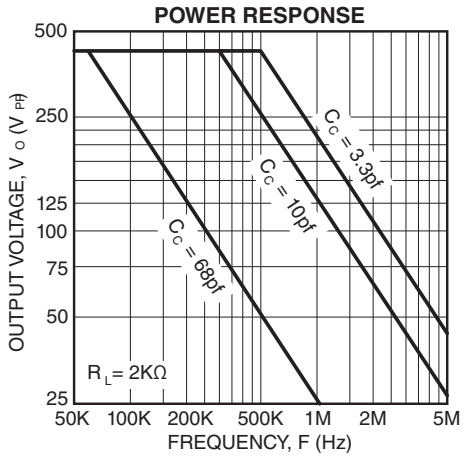


FIGURE 1E

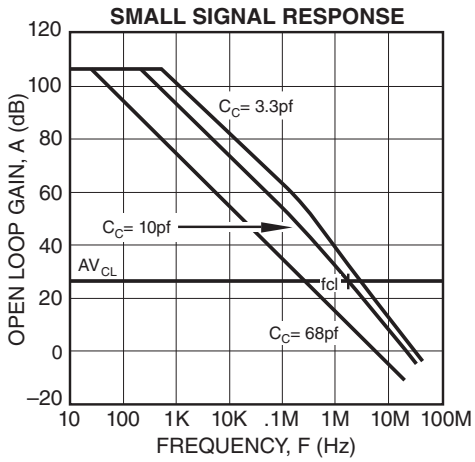
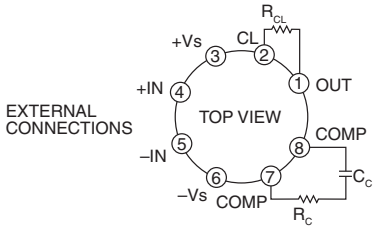


FIGURE 1C



PHASE COMPENSATION

Gain	C_C	R_C
1	68pf	100Ω
20	10pf	330Ω
100	3.3pf	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

FIGURE 1D

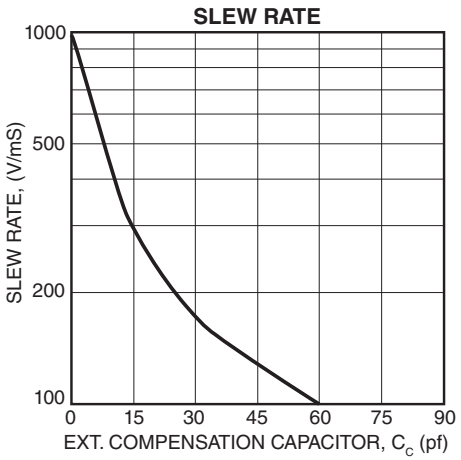


FIGURE 1F

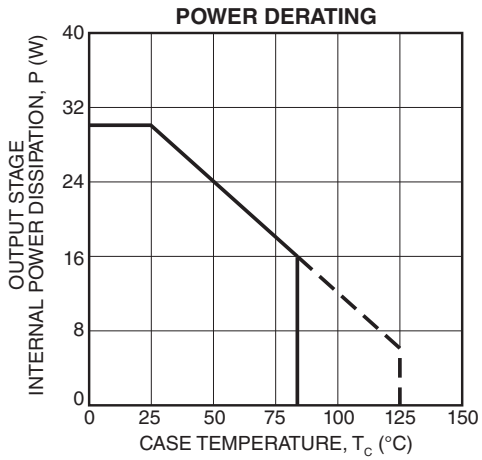


FIGURE 1. PA85 DATA SHEET EXCERPTS

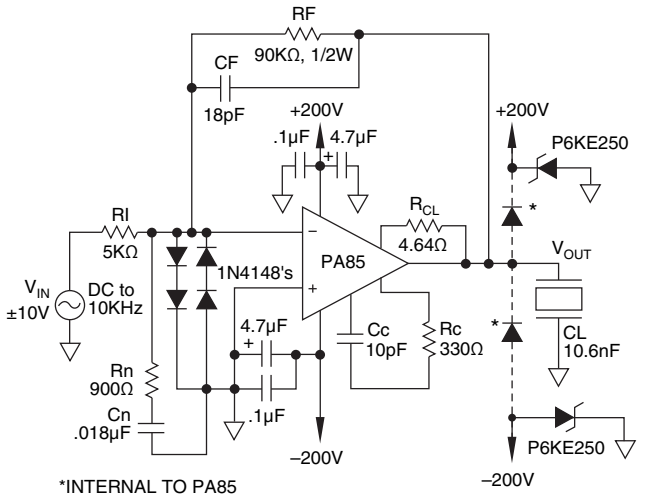


FIGURE 2. PA85 PIEZO TRANSDUCER DRIVE

Figure 4 lists high voltage Apex Precision Power amplifiers and boosters most commonly used to drive capacitive loads and their corresponding output impedance.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA41	150 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8Kohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

FIGURE 4. OUTPUT IMPEDANCE HIGH VOLTAGE OP AMPS AND BOOSTERS

2.2.2 STABILITY PLOTS

Figure 5 illustrates the magnitude plot for stability needed to analyze and check for good stability on our PA85 drive circuit. The low frequency pole for the Aol curve can be determined from the "Small Signal Response" curve, and the high frequency pole can be extrapolated from the "Phase Response" curve in the Apex Precision Power data sheet for the PA85.

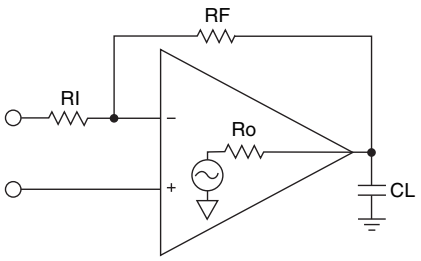
STEP 1: Modify Aol due to capacitive load and amplifier's output impedance:

STEP 2: Check 1/ß for resistive feedback alone:

$$fp2 = \frac{1}{2\pi (Ro + R_{CL})\, CL} = \frac{1}{2\pi (50\Omega + 4.64\Omega)\, 10.6nF} = 275\ KHz$$

fp4 = 10MHz pole from amplifier's original Aol plot (fp3)

1/ß [1/(beta)] is the small signal AC gain at which the op amp runs. Refer to Apex Precision Power Application Note 19 for details. First order stability criteria for magnitude plots states that the Rate-of-Closure (difference between the slopes of Modified Aol and the 1/ß plot) be 20dB per decade at fcl. Refer to Apex Precision Power Application Note 19 for details on Rate-of-Closure. With AC small signal gain set only by RF and RI the 1/ß plot will be a flat line at 25.6dB. At the intersection of modified Aol and 25.6dB the Rate-of-Closure will be 40 dB per decade indicating marginal stability and potentially destructive oscillations.



UNITY GAIN STABLE AMPLIFIER
UNSTABLE 40 dB/DECADE WITH CL

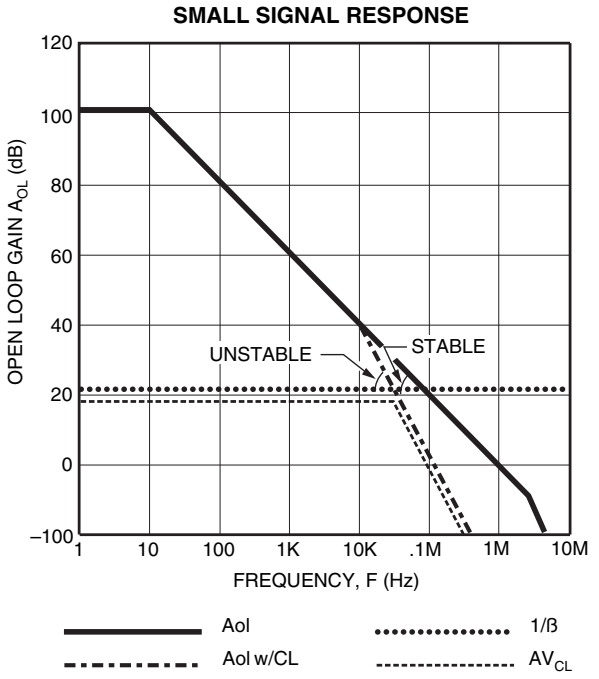


FIGURE 3. CAPACITIVE LOADING

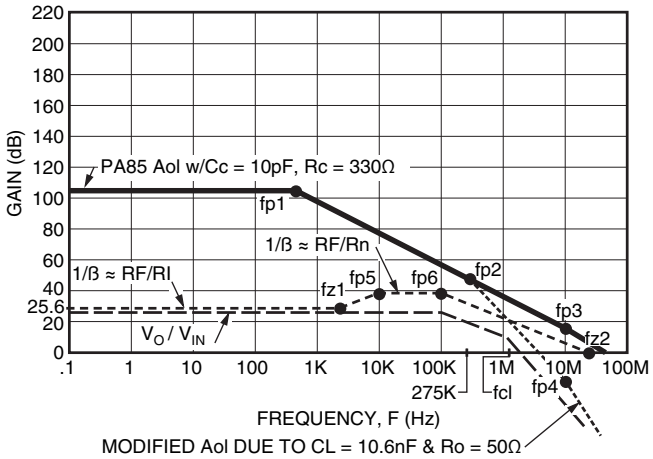


FIGURE 5. MAGNITUDE PLOT FOR STABILITY (PA85 PIEZO TRANSDUCER DRIVE)

STEP 3: Add Noise Gain Compensation as a first step towards good stability:

Rn and Cn will form a noise gain compensation network which will raise the gain of the 1/ß plot without directly affecting the V_{OUT}/V_{IN} relationship. Refer to Apex Preci-

sion Power Application Note 19 for details.
Noise Gain equations:
High frequency gain = RF/Rn = 90KΩ/900Ω = 100 ==> 40dB

$$fp5 = \frac{1}{2\,\pi\,Rn\,Cn} = \frac{1}{2\,\pi\,900\Omega\,.018\mu F} = 9.8\ KHz$$

fz1 ==> Can be obtained graphically using +20dB per decade slope starting at the intersection of fp5 and the high frequency gain of the noise gain compensation and proceeding towards the DC gain.

Even though we have raised the higher frequency portion of the 1/ß curve to 40dB, it will still intersect the modified Aol at 40dB per decade Rate-of-Closure.

STEP 4: Add feedback zero (1/ß pole) to 1/ß plot to gain best AC small signal stability (Refer to Apex Precision Power Application Note 19 for details):

$$fp6 = \frac{1}{2\pi\,RF\,CF} = \frac{1}{2\pi\,90k\,18pF} = 98\ KHz$$

Now at fcl, you have the desired 20dB per decade Rate-of-Closure and good stability according to our first order criteria for magnitude plots. You will now need to plot the open loop phase plot for a complete stability check.

STEP 5: Review of rules for open loop phase plots:

1) Poles in the 1/ß plot become zeros in the open loop stability check.
2) Zeros in the 1/ß plot become poles in the open loop stability check.
3) Poles and zeros in the Aol curve or modified Aol curve of the op amp remain respectively poles and zeros in the open loop stability check since the op amp Aol curve is an open loop curve already.
4) Phase for zeros is represented by a +45 degree phase shift at the frequency of the zero with +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.
5) Phase for poles is represented by a –45 degree phase shift at the frequency of the pole with a –45 degree per decade slope, extending this line with 0 degree and –90 degree horizontal lines. Refer to Apex Precision Power Application Note 19 for further details.

STEP 6: Plot open loop phase using information from magnitude plot: Figure 6 is the open loop phase plot for our PA85 drive circuit.

Notice in Figure 5 that the 1/ß plot continues beyond fcl all the way until it intersects at 0dB forming fz2 in the 1/ß plot. An amplifier will not run in an AC small signal gain of less than 0dB. You must account for an additional high frequency pole in the open loop phase check. This pole is easily read

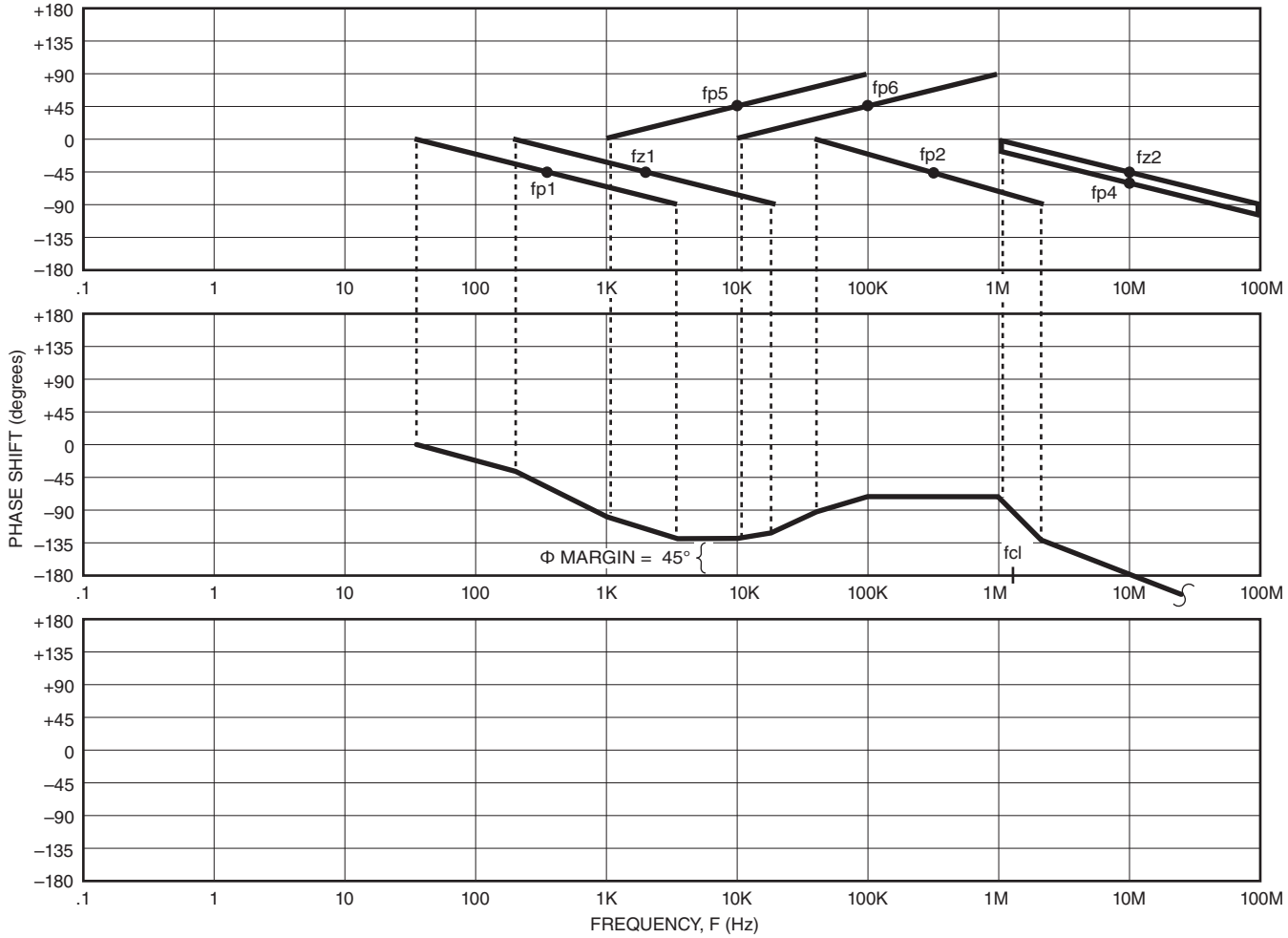


FIGURE 6. OPEN LOOP PHASE CHECK FOR STABILITY (PA85 PIEZO TRANSDUCER DRIVE)

graphically from Figure 5 rather than calculating it from lengthy derivations.

A review of Figure 6 shows graphical addition of the contributions from all poles and zeros to yield a net open loop phase plot. The phase margin from DC to fcl is never less than 45 degrees which implies good stability for this circuit.

2.2.2.1 RULES OF THUMB FOR STABILITY PLOTS

Now that we know we have good stability, let's return to the magnitude plot in Figure 5 for a few handy rules of thumb:

1) Think of open loop phase when you play with the 1/ß plot: Notice that fp1 (pole in open loop) is spaced about a decade away from fz1 (pole in open loop). If you don't add fp5 (zero in open loop) within a decade of fz1, (pole in open loop) the open loop phase margin will dip to less than 45 degrees.
2) As you run out of loop gain (difference between Aol curve and 1/ß plot), keep poles and zeros one-half to one decade away from zero loop gain. Notice that fp6 is about one-half decade away from the modified Aol curve near fp2. This allows "Real World" Aol curves and component tolerances to stack against you without creating stability nightmares.
3) Always design your circuits, using these stability techniques, for 45 degrees of phase margin in the open loop phase check for stability. This is because the first order linear approximations for phase have a six degree error. As well, there is no guarantee you will consistently receive op amps with the typical Aol graph.

In a typical design procedure, you will plot magnitude plots for stability first, do an open loop phase plot, and then return to calculate final component values to create the desired magnitude plot that yields 45 degrees open loop phase margin for stability.

Refer to Apex Precision Power Application Note 19 for handy tips and short cuts for plotting magnitude and phase plots.

2.2.3 "REAL WORLD" STABILITY TEST

Once a circuit is built, there is a relatively easy test you can run to verify if the predicted open loop phase margin made it from design to the "real world".

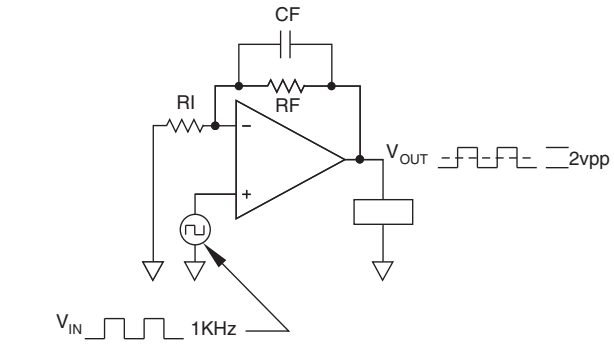
Figure 7 details the Square Wave Test for measuring open loop phase margin by closed loop testing. The output amplitude of the square wave is adjusted to be 2Vpp at a frequency of 1 KHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can then be compared to the graph in Figure 7 to yield a reading for open loop phase margin.

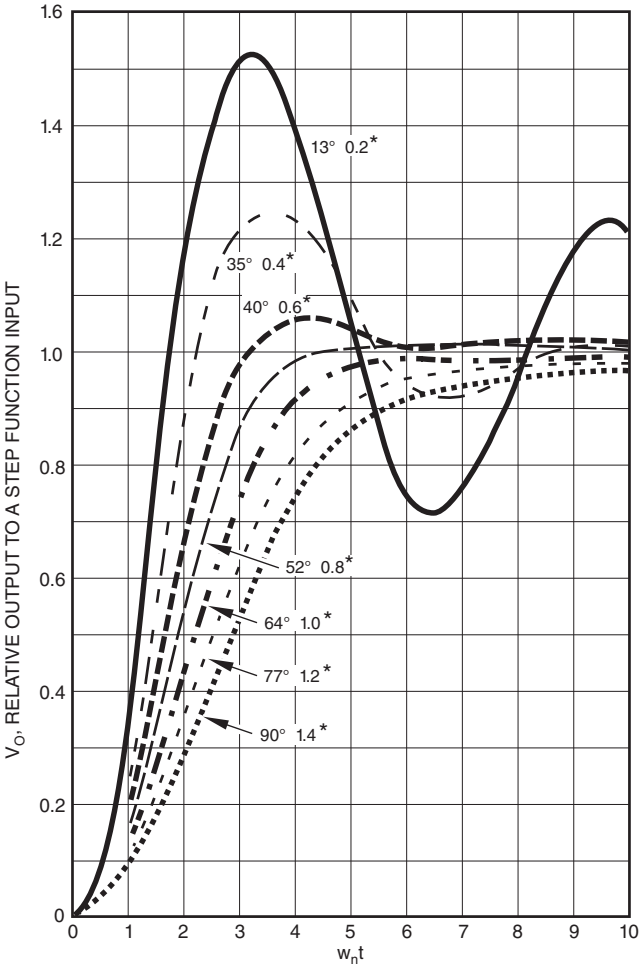
A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

Refer to Apex Precision Power Application Note 19 for more involved closed loop tests for measuring open loop phase margin and checking "real world" stability.

2.3 CLOSED LOOP RESPONSE

From Figure 5 the V_{OUT}/V_{IN} relationship for our PA85 circuit is seen as flat from DC to 100 KHz, where it begins to roll at





* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 7. SQUARE WAVE TEST

20dB per decade. It continues until we reach 1.33 MHz where it rolls off at 40dB per decade until reaching 10MHz, where our slope changes to 60dB per decade.

The V_{OUT}/V_{IN} phase shift for any given frequency is given by the following:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{f}{fp6} \quad -\text{Tan}^{-1}\frac{f}{fcl} \quad -\text{Tan}^{-1}\frac{f}{fp4}$$

where f = frequency of interest for phase shift

For our upper frequency of interest of 10 KHz let's see what the V_{OUT}/V_{IN} phase shift is:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{10\text{ KHz}}{100\text{ KHz}} - \text{Tan}^{-1}\frac{10\text{ KHz}}{1.33\text{MHz}}$$

$$-\text{Tan}^{-1}\frac{10\text{ KHz}}{10\text{MHz}} = -6.2\text{ degrees}$$

The formula above can be expanded to include any number of poles. If the V_{OUT}/V_{IN} relationship has zeros simply add the following for each zero:

$$+\text{Tan}^{-1}\frac{f}{fz}\text{ ; where fz is the frequency of the zero}$$

2.4 POWER DISSIPATION AND HEATSINKING

Power dissipation inside the amplifier consists of two components, P_{DQ}, quiescent power dissipation, and P_{DOUT}, output stage power dissipation. Simply compute $P_{DQ} = Iq[+Vs - (-Vs)]$ and add the worst case power dissipation for the output stage to this to form P_{DINT}, total internal power dissipation. Figure 8 shows the Thermo-Electric Model that is applicable for this situation.

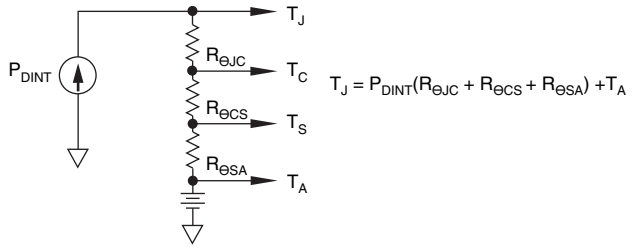


FIGURE 8. THERMO–ELECTRIC MODEL

In our PA85 design case we have AC power dissipation in the output stage. From Section 2.1, Step 4, that power dissipation is:

$$P_{DOUT}\text{ max} = \frac{4\text{ Vs}^2}{2\,\pi\,\text{Xc}} = \frac{4\,(200)^2}{2\,\pi\,1.5\text{K}\Omega} = 17\text{W}$$

Quiescent power is:

$$P_{DQ} = I_Q\,[+V_S - (-V_S)] = 25\text{mA}\,[+200 - (-200)] = 10\text{W}$$

There are two thermal requirements we must meet in this application. First, the case temperature must be kept below 85°C. Second, the junction temperature must be kept below 150°C. We know the application is dissipating a total of 27W, but the data sheet contains three different thermal resistance ratings which vary substantially. The first is an AC rating where the two output transistors share the heat load at a frequency of 60Hz or greater. When the power is dissipated in mainly one output transistor, use the DC thermal resistance. The last rating is applied only if no heatsink is used.

This is a rare practice with power op amps. Let us briefly pursue the possibility we might be able to not heatsink the amplifier in this application. Figure 9 models this case. TO-3 packages

FIGURE 9. THERMO–ELECTRIC MODEL (NO HEATSINK)

are rated at 30°C/W. When the case of the amplifier must be kept below 85°C, this imposes a maximum power dissipation of 2W even with an ideal ambient temperature of 25°C. At 27W our PA85 would burn up very quickly without a heatsink.

The PA85 data sheet tells us the AC thermal resistance is 2.5°C/W. We will allow 0.2°C/W for $R_{ΘCS}$ and use the following to determine a maximum heatsink rating.

$$R_{ΘSA}\ \frac{T_J - T_A}{PD_{INT}(\text{max})} - R_{ΘJC} - R_{ΘCS}$$

$$\frac{(150 - 25)°\text{C}}{27\text{W}} - 2.5°\text{C/W} - 0.2°\text{C/W}$$

$$R_{ΘSA}\quad 1.9°\text{C/W}$$

Select Apex Precision Power HS03; $R_{ΘSA}$ = 1.7°C/W with forced air flow at 100 ft/min.

As a last check, multiply the total power times the sum of the thermal resistance of the heatsink and the mounting interface and add to ambient temperature to verify the case temperature does not exceed 85°C.

$$27\text{W} \bullet (1.7°\text{C/W} + 0.2°\text{C/W}) + 25°\text{C} = 76.3°\text{C}$$

Refer to **"Package and Accessories Information"** section of Apex Precision Power Amplifier Handbook. See Apex Precision Power catalog "GENERAL OPERATING CONSIDERATIONS" for details on heatsinking and mounting the amplifier.

2.5 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

High voltage op amps require some special considerations when selecting support components for completion of your circuit design. The following list covers these critical areas of concern:

1) ESD Handling Precautions:

All Apex Precision Power high voltage amplifiers are rated Class 1 for ESD sensitivity, as defined in MIL-H-38534. This requires that proper ESD handling precautions be observed from receiving through manufacturing until the device is installed in a properly designed circuit. Areas which will require strict ESD control include, but are not limited to, personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2) Input Protection (Refer to Figure 10):

Most high voltage amplifiers have a differential input voltage rating of +/-25V. It is easier on high voltage amplifiers to cause differential input overvoltages than on lower voltage op amps. These overvoltages on the input can occur during power cycling or can be transients fed back through CF from the output to the input.

The input diodes, Dp, clamp the maximum input differential voltage to +/-1.4V while allowing sufficient differential voltage for overdrive when demanding maximum slew rate from the amplifier. The diodes shown are low capacitance fast signal diodes. If lower leakage and lower capacitance diodes are desired, J-FETs may be connected as diodes as shown.

3) Output Diodes (Refer to Figure 10):

MOSFET high voltage amplifiers have internal, intrinsic diodes that are connected from the output to each supply rail. High voltage Bipolar amplifiers do not have these diodes and must be added externally as shown. The MOSFET amplifiers' internal diodes are sufficient for an occasional transient that may be created in a piezo drive situation where the piezo element is stressed mechanically, thereby creating an electrical voltage. For applications where there is poten-

tial for sustained high energy flyback, in ATE applications, where everything that is not supposed to happen usually can and does, or in applications where Kilovolt flashovers can occur and be inmpressed onto the amplifier's output, it is recommended to use fast (500nS or less depending upon the anticipated flyback energy frequency) reverse recovery diodes, DFB, external to the amplifier. Remember to size the diodes for a Peak Reverse Voltage rating of at least the rail to rail supplies the amplifier is operating at (for Vs=+/–200V ==> 400V Peak Reverse Voltage rated diode).

4) Transient Voltage Suppressors (See Figure 10):

Transient Voltage Suppressors, V_{TR}, can be added to the supply lines to provide protection from undesired transients on the power supply line. The first is power supply overvoltage on power cycling. Secondly, when energy is dumped into the supplies from DFB, if the power supply terminals at the amplifier do not look like a low impedance for the frequency of that energy, the amplifier could become overvoltaged. Transient suppressors, such as TRANSZORBS, manufactured by General Semiconductor Industries, Inc, will provide a low impedance path for this energy. If you use unipolar transient suppressors, they will prevent polarity reversal across the amplifier since they will become a forward biased diode if supplies are reversed.

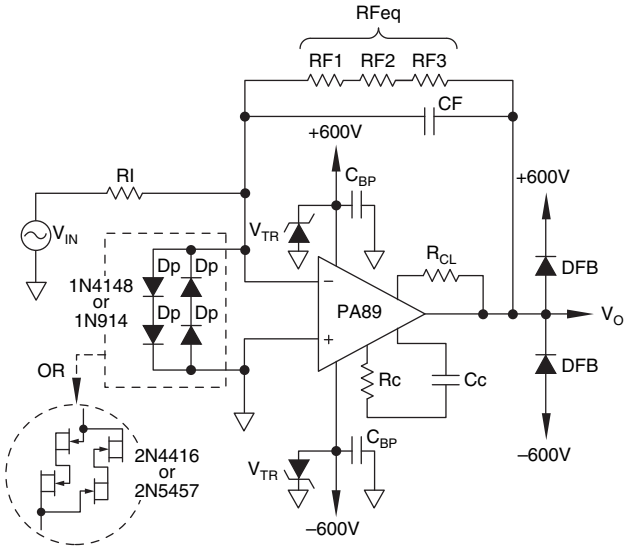


FIGURE 10. HIGH VOLTAGE SUPPORT COMPONENTS

Selection of the transient suppressors may require a series string of devices to reach the desired reverse stand-off voltage rating for higher voltage op amps. Choose the transient suppressor for a reverse stand-off voltage slightly greater than the maximum DC or continuous peak operating voltage level. This selected device will then have an actual breakdown voltage that is typically 1.1 to 1.36 times higher. For example, a P6KE250 has a reverse stand-off voltage of 202V with a breakdown voltage of 225V to 275V. Herein lies the trade-offs of transient suppressors. They are excellent devices with a sharp breakdown curve and can dissipate large amounts of power for short periods of time. The problem is the exact breakdown voltage is not a tightly controlled parameter for any given model.

A typical design dilemma is the case where an engineer desires to use a part at its full power supply rating and still provide transient voltage protection on the supply lines. Now you ask, how high is Apex Precision Power's Absolute Maximum Rating for Supply Voltage, REALLY? Well, the guaranteed Absolute Maximum Rating for Supply Voltage is exactly what our vendors guarantee to us. Lawyers aside, it is known in the electronics industry that a 400V transistor may actually breakdown at 500V from a given lot. In a nutshell, you are in no-man's land above the Absolute Maximum Rating; however, it is much better to limit the transient voltages to as low as possible than to not limit at all!

5) Power Supply Bypassing (See Figure 10):

The rule of thumb is .1µF ceramics directly at the op amp with 10µF/Ampere of peak output current in parallel within 2 inches or so of each amplifier. Many of the high voltage amplifiers are less than 200mA and the .1µF ceramic is all that will be needed. In cases of PA89, +/600V supplies, .01µF seems to be more readily available and this is adequate for high frequency bypassing on the power supply line. Watch the voltage ratings for these capacitors!

6) Compensation Capacitor and Resistor (See Figure 10):

Cc must be rated for the rail-to-rail supply voltage at which the amplifier is operating. In this case a 1200V rating. It is recommended that the compensation capacitor be a temperature stable capacitor for reliable performance over temperature. Mepco / Centralab, Inc, series D and S type capacitors are available in 50Vdc through 6KVdc ratings in various temperature characteristics.

Rc will normally see little or no voltage since most of the voltage stresses will be across Cc. Rc then can be a standard 1/8W metal film resistor.

7) Feedback and Input Components (See Figure 10):

RI will generally have little voltage stress or power dissipation since most input signals are less than 10 volts peak. Standard metal film resistors will work fine.

CF can have up to one supply impressed across it. In this case it would need to be a 600Vdc minimum rated capacitor.

RF1, RF2, and RF3 will need some special considerations. Power dissipation will become of prime importance since up to one of the supply rails can be impressed across these resistors at a given time. This could yield power dissipations of: $P_D = Vs^2 / RFeq$. The second consideration is voltage coefficient of resistance. This is a parameter that defines how a resistor changes its resistance with applied voltage. At low voltages this characteristic is not a dominant factor. At higher voltages it can become a more significant factor causing reductions in gain for a given resistor ratio or increased distortion. Dale RNX, ROX, FHV, MVW, and HVX series resistors are well characterized for high voltage use. The power dissipation factors and voltage coefficient of resistance may require several resistors to be used in series in the feedback path of the op amp.

8) Current Limit Resistor (See Figure 10):

Remember that all the load current flows through the current limit resistor, R_{CL}, and therefore size it according to the value of current limit, Ilim, by $P_D = (Ilim^2)(R_{CL})$. Maximum voltage stress across R_{CL} will be about +/-.7V for most amplifiers. Check the "Current Limit" section of the applicable data sheet for exceptions to this.

9) PWB Layout:

Higher voltages will require wider spacings between traces on a printed circuit board layout as well as spacings between ground planes and other conductive layers. Mil-Std-275 provides some guidelines in these areas.

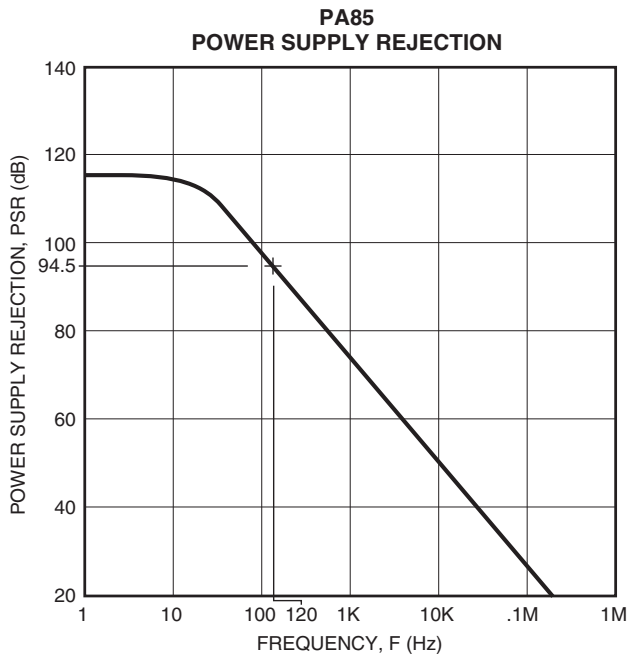


FIGURE 11. PA85 PSR

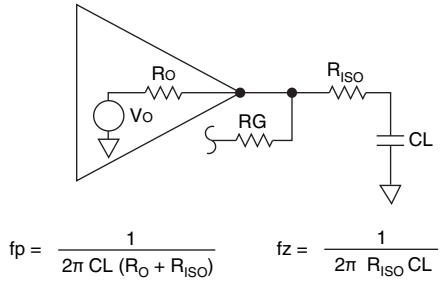


FIGURE 12A: R_{ISO} & CL

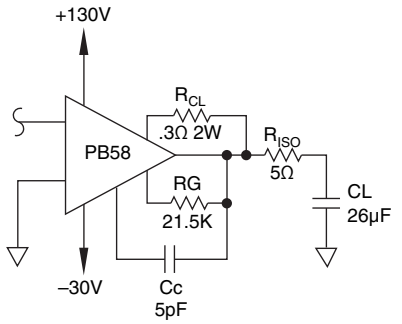


FIGURE 12B: PB58 w/ R_{ISO} & CL

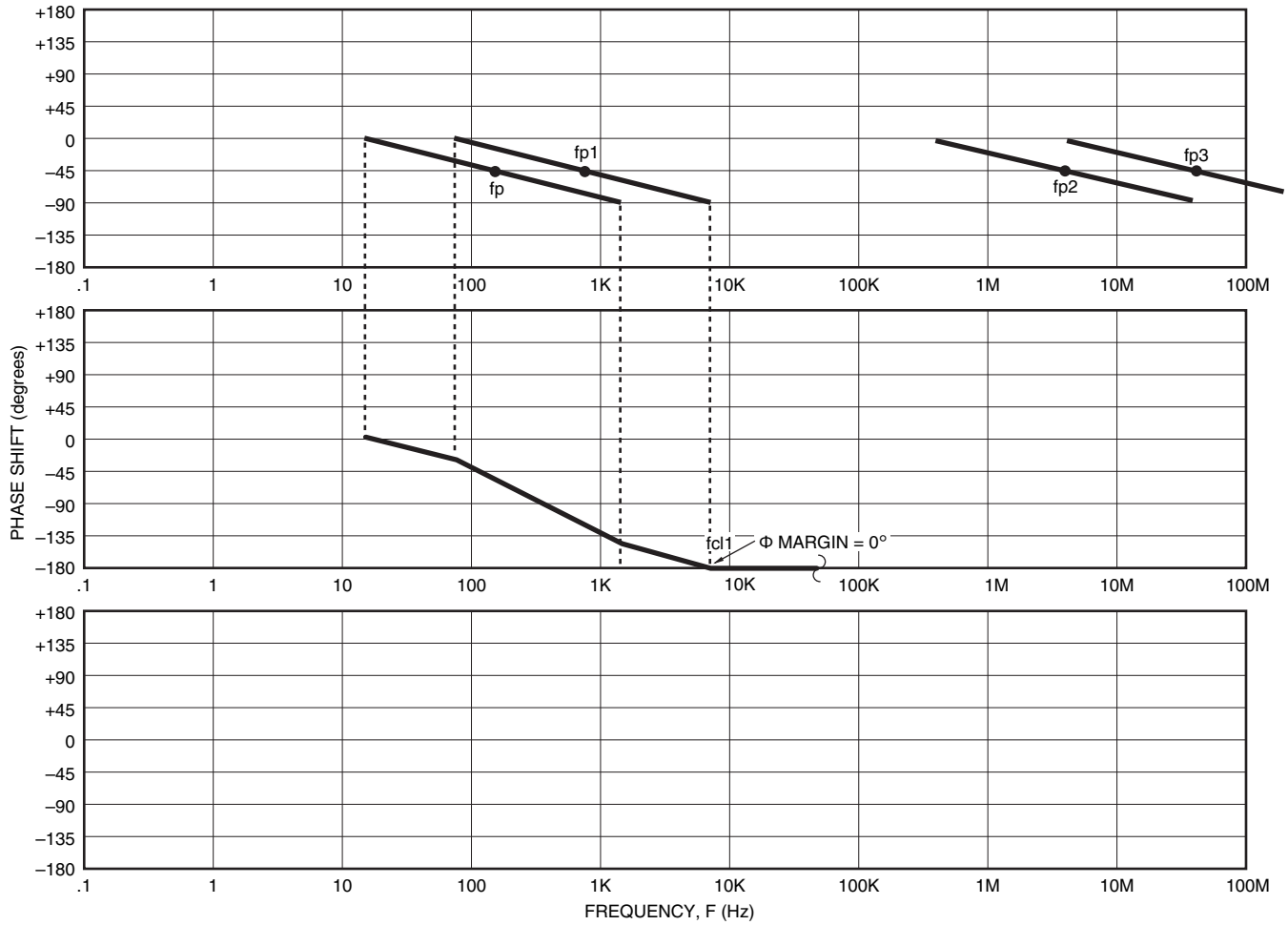


FIGURE 14. OPEN LOOP PHASE PLOT FOR STABILITY CURVE ① (w/o R_{ISO})

10) Probing, Plugging and Powering:

Be extremely careful when probing a high voltage amplifier with the power on. An inadvertent slip of a probe can destroy a high voltage amplifier. There are often compensation pins adjacent to power supply pins. Those compensation pins are often connected to the gates of MOSFETs which do not take kindly to the full power supply being impressed upon them.

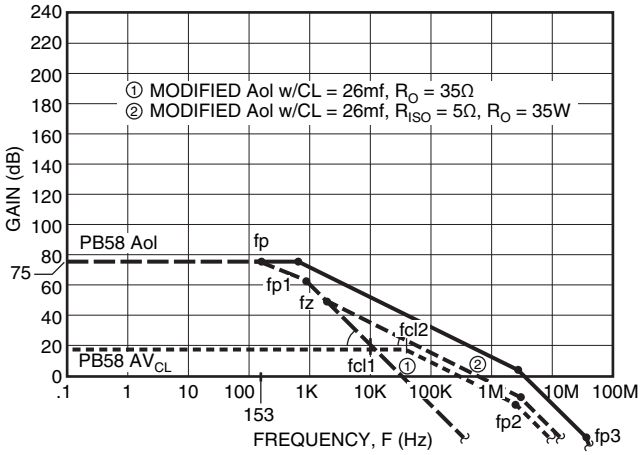


FIGURE 13. R_{ISO} & CAPACITIVE LOAD EFFECTS

Do not plug or unplug an amplifier into a live, powered socket. The transients generated can destroy the high voltage amplifier.

Do not use fuses in the power supply lines of high voltage amplifiers or ever power them with one supply disconnected and no path to ground for that disconnected power supply. This can lead to a sneak path for permanent destruction on several of the high voltage amplifiers.

2.6 POWER SUPPLIES

2.6.1 POWER SUPPLY REJECTION

Often times high voltage amplifiers require the use of either a switching power supply or a simple AC full-wave bridge rectified supply (make real sure you use transient suppressors if you use this type of supply). The question then is asked what will be the effect on the output of the amplifier due to the ripple of the power supply?

Figure 11 (previous page) is the Power Supply Rejection curve for the PA85. We will use this and our familiar circuit of Figure 2 to understand power supply ripple effect on amplifier output. Figure 11 is a referred-to-input specification. Let's assume there is a 1Vpp, 120Hz ripple on the power supply line. From Figure 11 this implies PSR of 94.5dB. Since this is a rejection curve, the gain is actually -94.5dB which is a gain of .000018836. This gain times 1Vpp on the power supply line means you will see .018836mVpp appear as an input offset

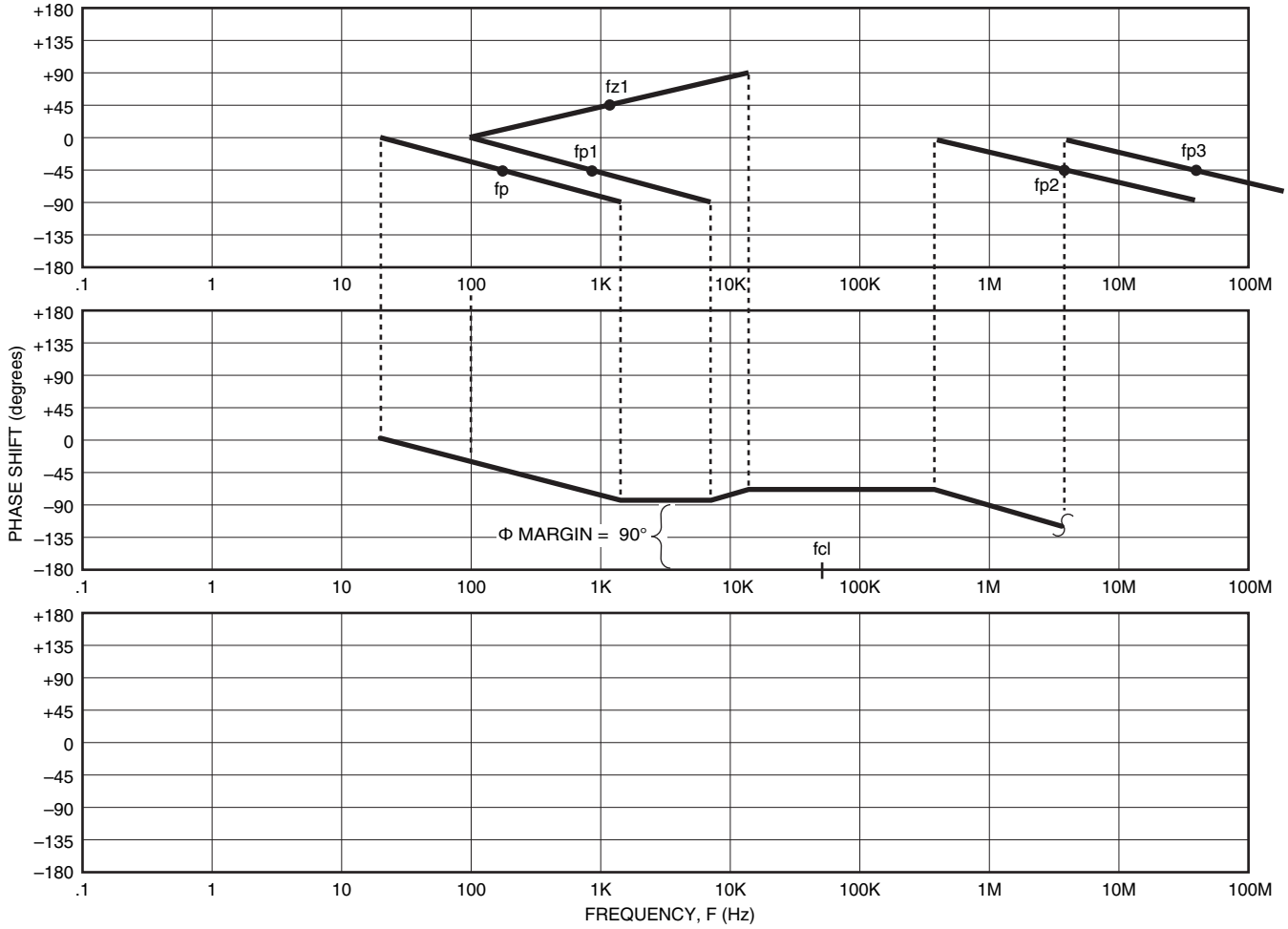


FIGURE 15. OPEN LOOP PHASE PLOT FOR STABILITY CURVE ② (w/R_{ISO})

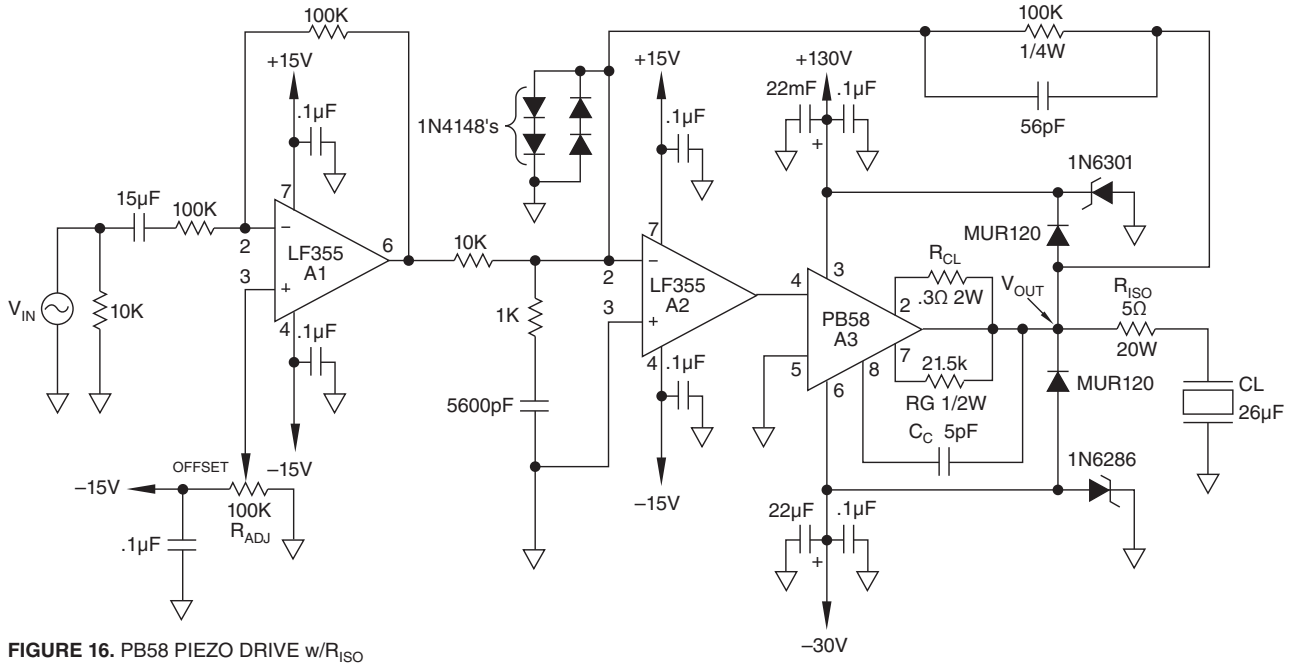


FIGURE 16. PB58 PIEZO DRIVE w/R_{ISO}

voltage in the circuit. At a gain of 19 this means our output will see .358mVpp ripple at 120Hz due to power supply fluctuations.

2.6.2 HIGH VOLTAGE POWER SUPPLIES

See the last few pages of the ACCESSORIES INFORMATION data sheet for a list of manufacturers of high voltage supplies. As a group, these vendors offer AC and DC inputs, standard and custom units in linear and switching topologies. No matter what supply you use, check it for possible overshoot at power up, power down and even power cycling. Beware that many high voltage supplies feature foldback or foldover current limiting. In these circuits, current limit is reduced at low voltages compared to full output voltage. Current sources in Apex Precision Power high voltage amplifiers draw their rated quiescent current at somewhere around half their minimum supply voltage rating. For example, the PA85 is likely to draw over 20mA as soon as the supplies reach +/-7 to 10V. If a foldback feature does not allow this operating point, the system will latch up.

3.0 HIGH VOLTAGE AMPLIFIER VARIATIONS

3.1 RESISTOR ISOLATION FOR CAPACITIVE LOADS

In Section 2.2.2 one method for stabilizing capacitive loads was discussed. There is another common way to isolate capacitive loads and thereby acquire good stability.

Figure 12A (back 2 pages) illustrates a technique for isolating the capacitive load through the use of R_{ISO}. This isolates the point of feedback, where RG is connected, from the capacitive load. The addition of R_{ISO} adds a zero in the modified Aol plot to counteract the pole formed by Ro and CL. Figure 12A also contains the equations for the modified Aol curve defining fp and fz.

Figure 12B (back 2 pages) will be part of a real world design for a PIEZO DRIVE CIRCUIT. Here a PB58 will be required to drive a 26µF capacitive load. Figure 13 (previous page) illustrates the modified Aol curve with and without the use of Riso. From Figure 14 (back 2 pages) we see –28 degrees of phase margin without R_{ISO}. However, in Figure 15 (previous page) we have 90 degrees of phase margin through the use of R_{ISO}.

STEPS FOR CALCULATING R_{ISO}: (See Figure 13, previous page)

STEP 1: Calculate initial fp: Use Ro and CL which are given by virtue of the load for the application and the choice of power op amp. Plot location of fp.

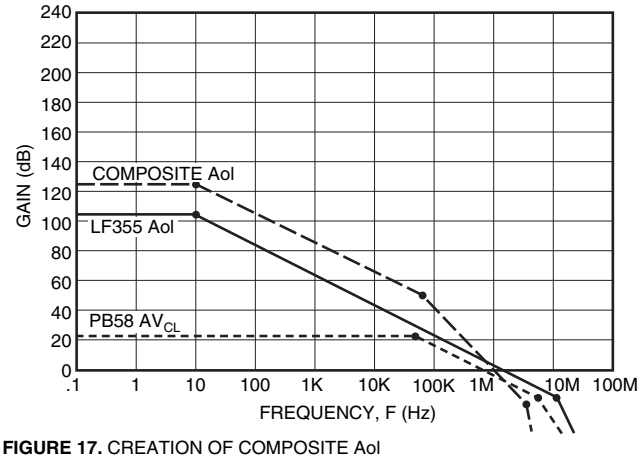


FIGURE 17. CREATION OF COMPOSITE Aol

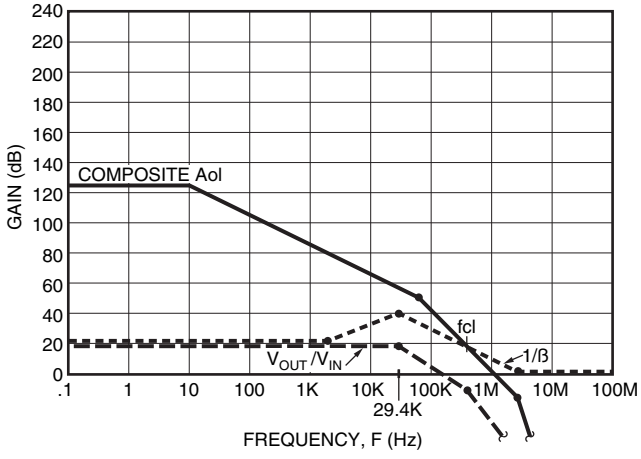


FIGURE 18. COMPOSITE MAGNITUDE PLOT FOR STABILITY

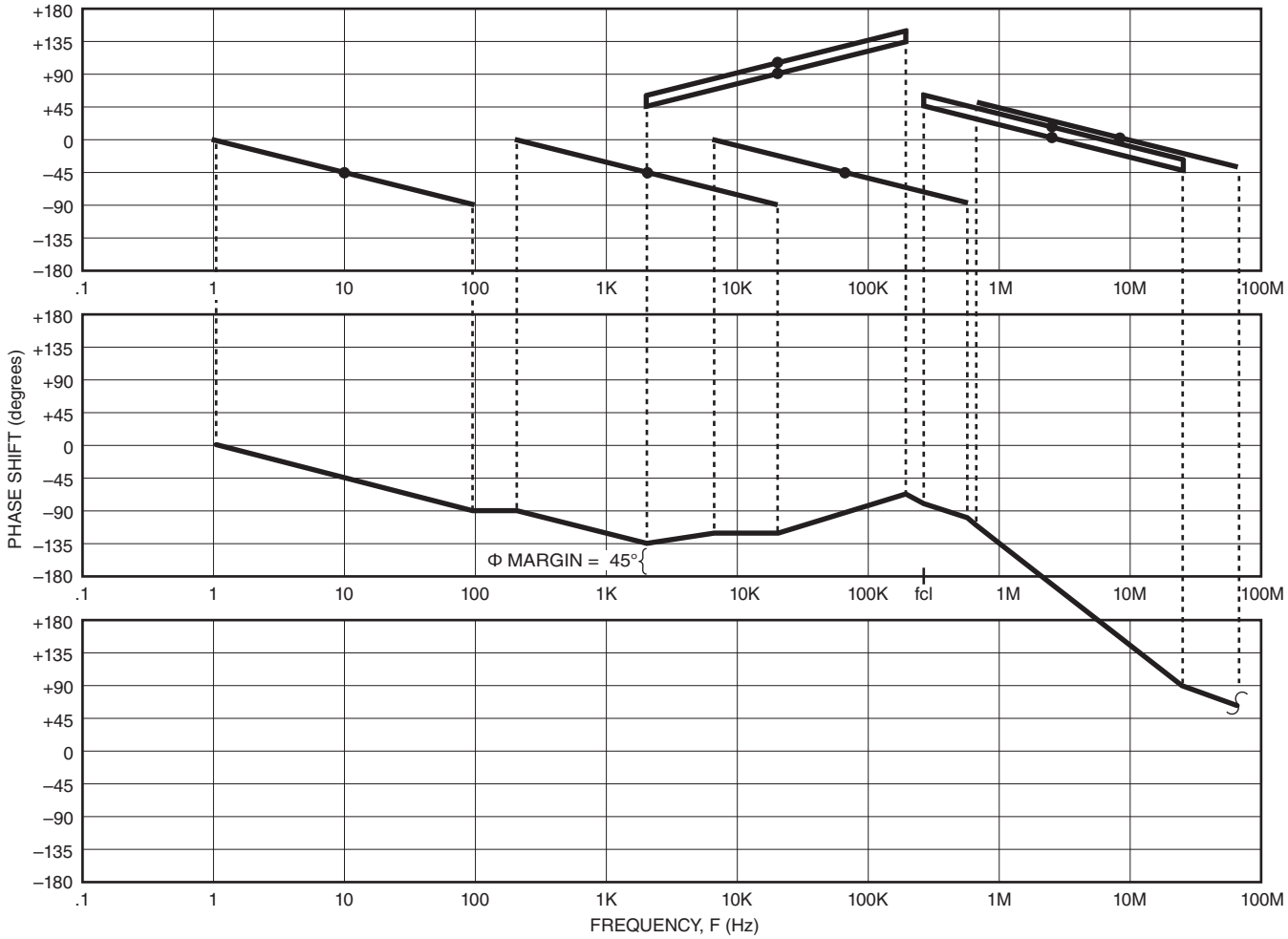


FIGURE 19. COMPOSITE OPEN LOOP PHASE PLOT FOR STABILITY

STEP 2: Graphically choose fz: From plot of fp and fp1 you can see a 40 dB/decade slope heading towards 0 dB gain. Choose fz at a location such that it will change slope of modified Aol from 40 dB/decade to 20 dB/decade for at least a decade above AV_{CL} and within a decade of fp1.

STEP 3: Calculate final value for R_{ISO}: Calculate from formula for fz in Figure 12A the value for R_{ISO} from fz location in Figure 13. Recalculate final value for fp and plot final modified Aol ensuring final location of fz meets criteria in STEP 2.

One disadvantage with the use of R_{ISO} is that the point of feedback is not directly at the capacitive load. This means that accurate control of the voltage at CL is not obtained. This is usually not a problem since most piezo drives are used inside of an outer control loop such as position feedback

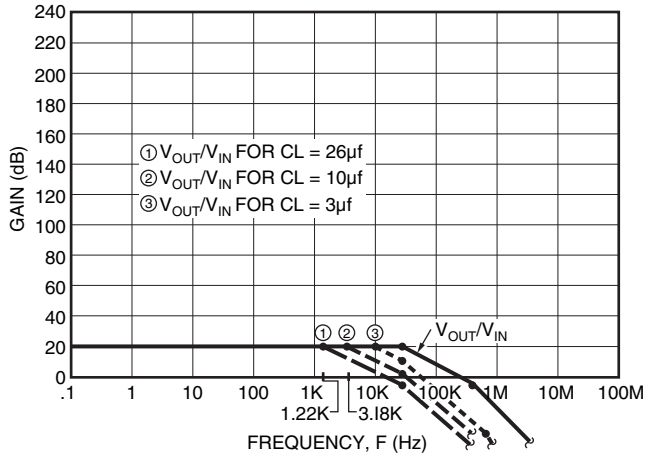


FIGURE 20. V_{OUT}/V_{IN} FOR VARIOUS CL

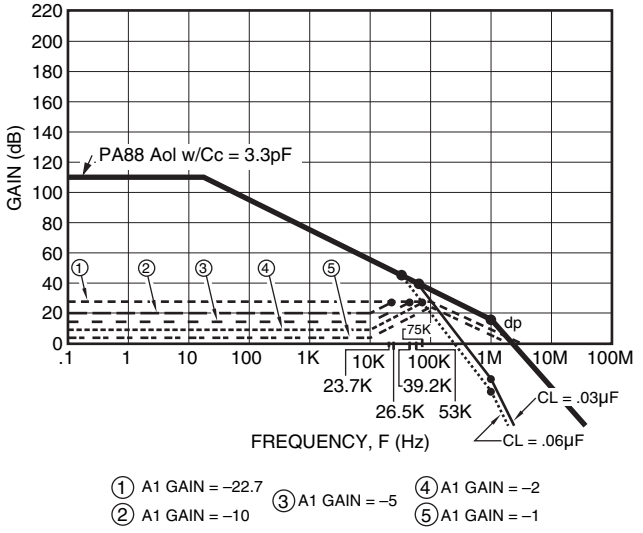
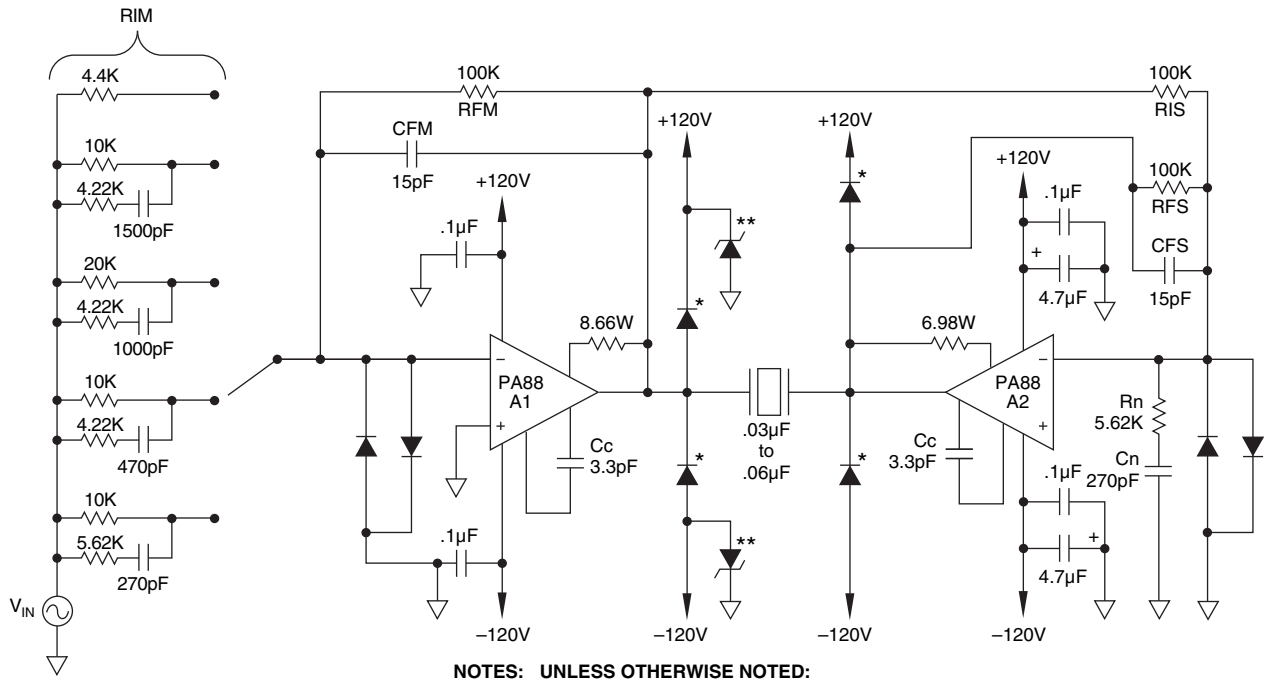


FIGURE 22. A1: MASTER AMPLIFIER MAGNITUDE PLOT FOR STABILITY

One disadvantage with the use of R_{ISO} is that the point of feedback is not directly at the capacitive load. This means that accurate control of the voltage at CL is not obtained. This is usually not a problem since most piezo drives are used inside of an outer control loop such as position feedback



NOTES: UNLESS OTHERWISE NOTED:
1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBS = 1N6300 or 1.5KE160
2) USE HS02 HEATSINK @ 25°C AMBIENT

FIGURE 21. PA88 BRIDGE PZT DRIVE WITH SELECTABLE GAIN

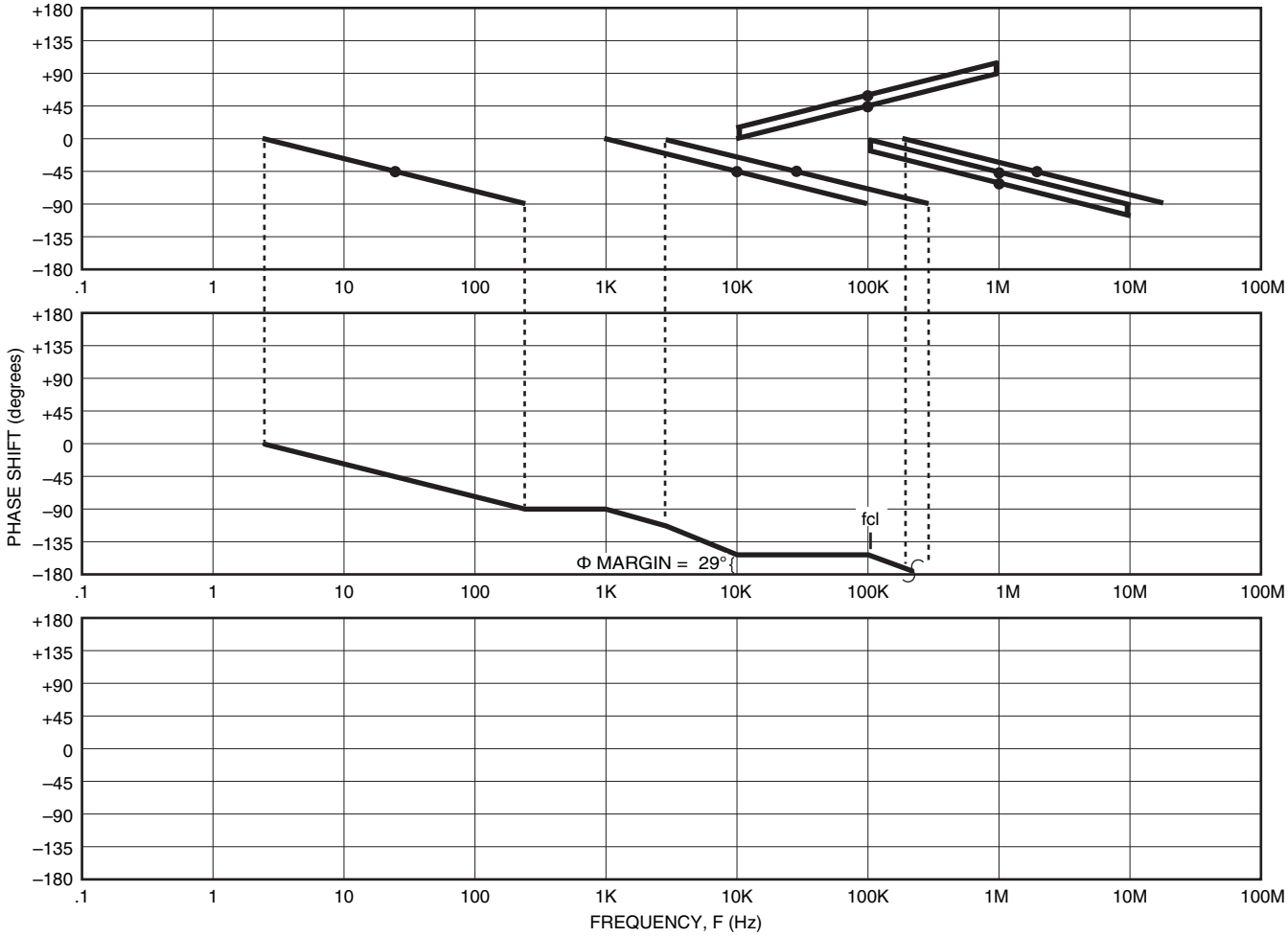


FIGURE 23. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT CL = .06mf GAIN = 6dB

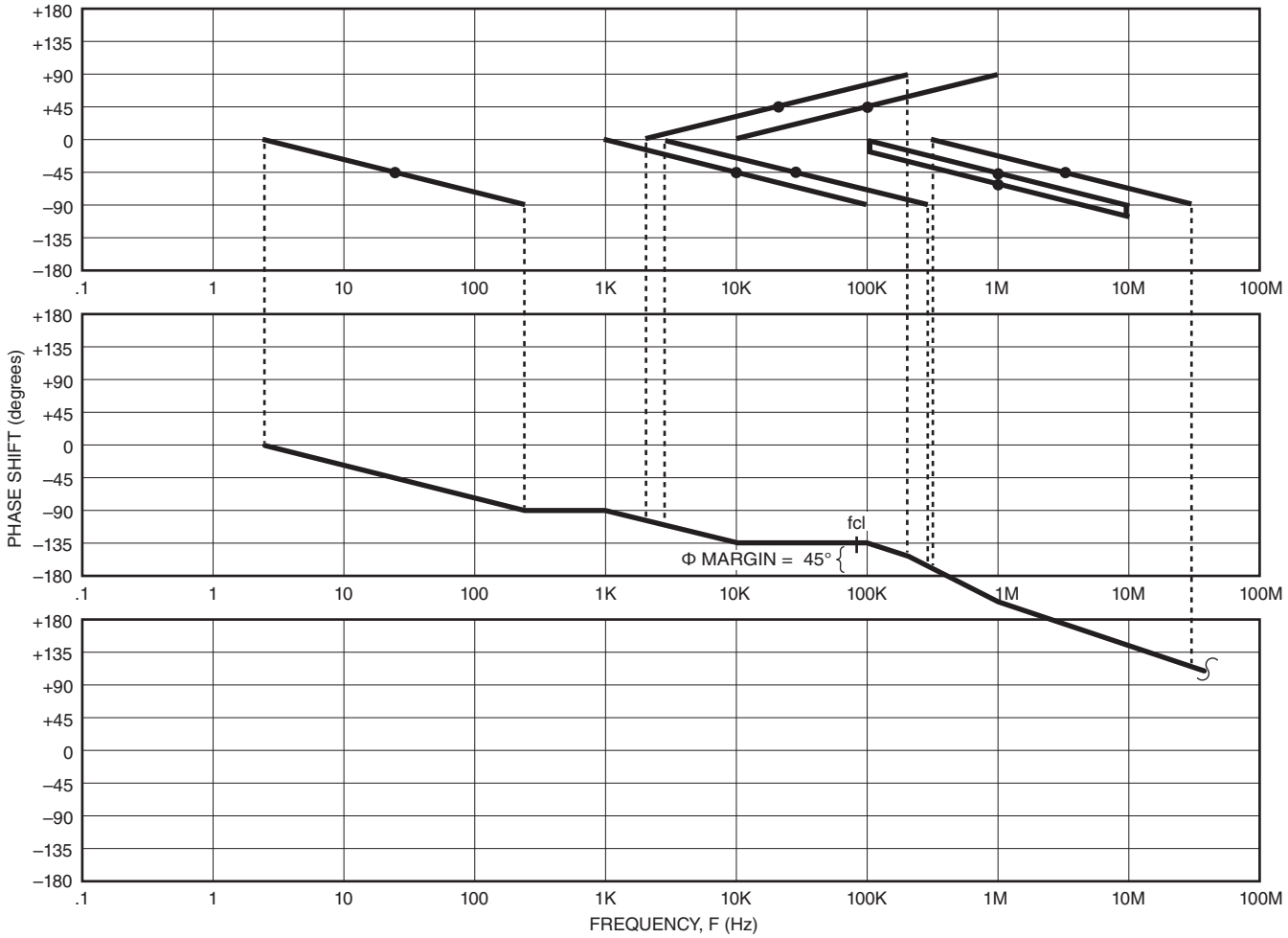


FIGURE 24. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT CL = .06µf GAIN = 20dB

into a microprocessor which will then generate an error command to the input of the PB58 piezo drive circuit. The major advantage of R_{ISO} is that a wide range of capacitive loads can now be driven with good stability.

3.1.1 PB58 PIEZO DRIVE WITH R_{ISO}

Figure 16 (previous page) is a piezo drive amplifier using the PB58 and our R_{ISO} technique for capacitive load stability.

The design goal for this amplifier was to have an adjustable DC offset and still allow an AC input signal to swing about the DC offset. Amplifier A1 AC couples V_{IN} and offsets it around the selected DC offset set by R_{ADJ}.

The stability of the PB58 composite amplifier begins with first ensuring the PB58 itself is stable. This is accomplished with the use of R_{ISO} in Section 3.1 and Figure 13. Figure 17 (previous page) creates the composite Aol by adding the closed loop voltage gain of the PB58 to the open loop gain of the LF355 front end amplifier. For details on stabilizing composite amplifiers, refer to Apex Precision Power Application Note 19. Figure 18 (back 3 pages) illustrates the 1ß plot selected for good stability. Note the V_{OUT}/V_{IN} relationship which will be discussed later. Figure 19 (back 2 pages) verifies good stability through the open loop phase plot.

Since output voltage across CL is not controlled directly, it is of interest to see how the V_{OUT}/V_{IN} relationship changes with capacitive loads. Figure 20 (back 2 pages) shows the V_{OUT}/V_{IN} which is at the output of the amplifier. Curves 1 thru 3 show the effect of the additional V_{OUT}/V_{IN} pole formed by R_{ISO} and CL. As the capacitive load is decreased it's possible to gain a wider bandwidth since the additional pole due to R_{ISO} and CL is moving out higher in frequency.

So far the small signal response for this amplifier has been examined. The large signal response has two limitations. The first is slew rate. The slew rate for the composite is limited to slew rate of the front end times the booster gain. In this case S.R. = 5V/µS X 10 = 50V/µS. The upper frequency of a sinewave we can track is a 120Vpp sinewave of 133KHz from S.R.=2 π f V_{OP}. This is not a limiting factor for this circuit since the small signal bandwidth begins to roll off at 28.4 KHz for V_{OUT}/V_{IN} (refer to Figure 20). The second large signal limitation is current drive capability. As the capacitive load is increased, the impedance is lowered as the frequency increases. This translates to higher currents.

The following is lab data taken on the circuit of Figure 16 for power response:

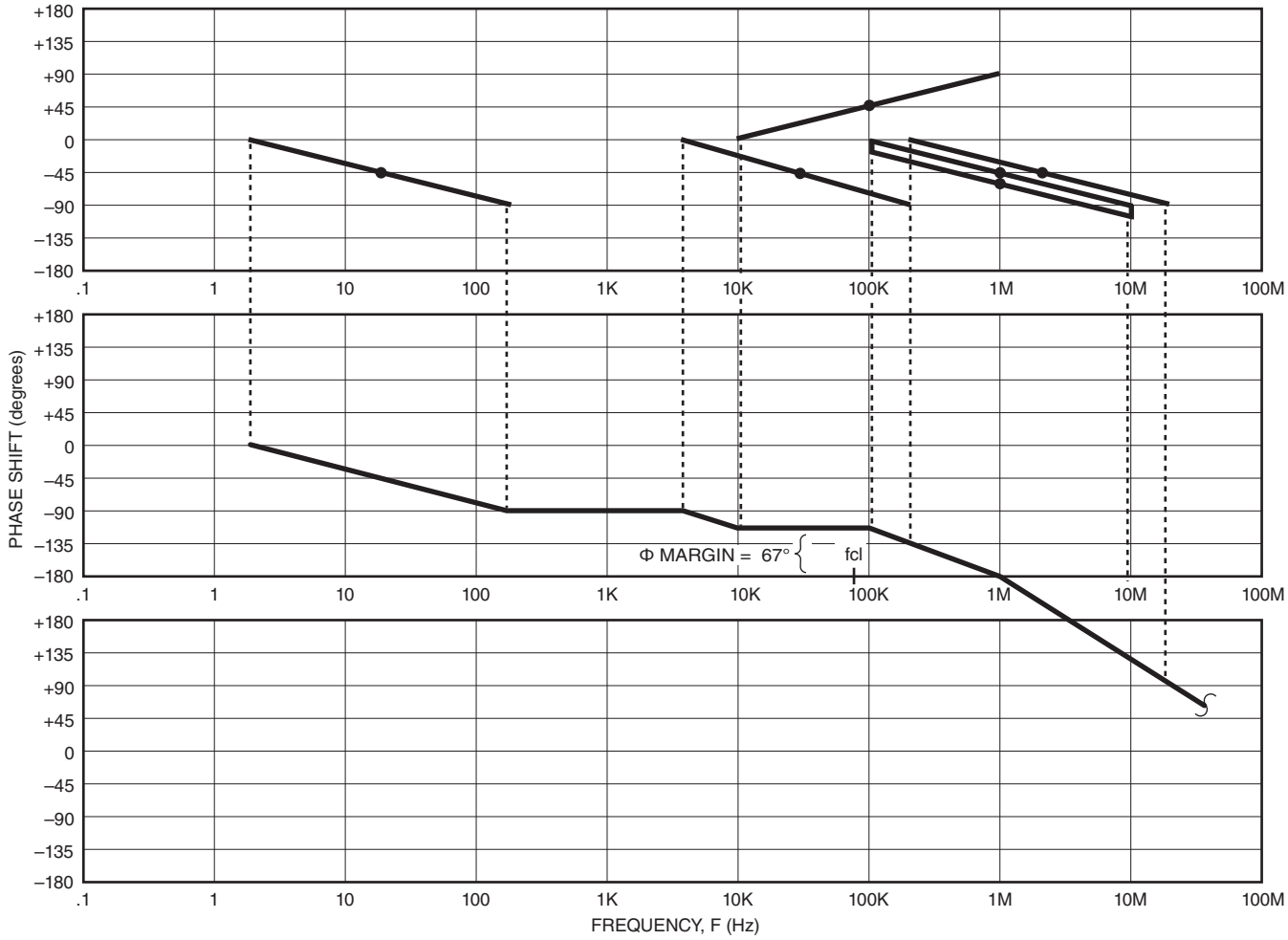


FIGURE 25. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT CL = .06µf GAIN = 27.5 dB

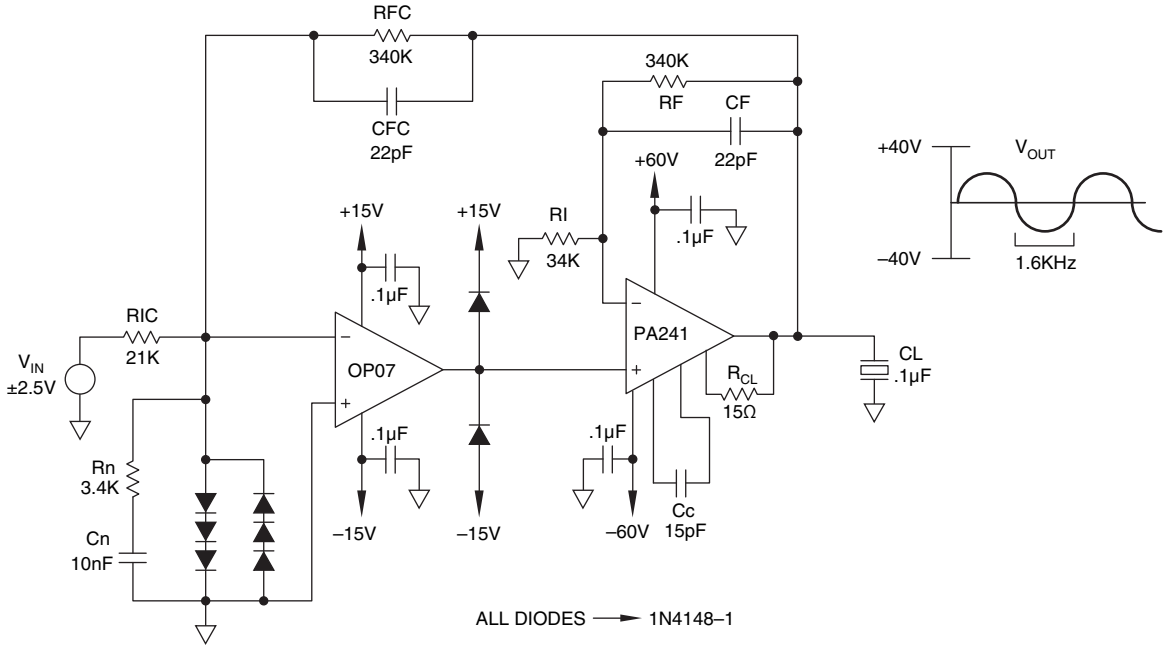


FIGURE 26. PA241 COMPOSITE PIEZO TRANSDUCER DRIVE

POWER RESPONSE (Ilim = 1.3A)

CL = 10µF	f	V_{OUT}
	400Hz	100Vpp
	700Hz	50Vpp
	4KHz	10Vpp
CL = 22µF	f	V_{OUT}
	200Hz	100Vpp
	400Hz	50Vpp
	2KHz	10Vpp

Of equal interest is the power supply rejection for this composite since the choice of front end amplifier will change this number to some degree. The following lab data for the circuit of Figure 16 illustrates the PSR for the positive supply.

POSITIVE POWER SUPPLY REJECTION

(DC set for +Vs = +110V, AC set for 2Vpp Ripple)

f	V_{OUT} Ripple	Attenuation	Referred to input	PSR
1KHz	30mVpp	.015	.0015	-56.5db
10KHz	290mVpp	.145	.0145	-36.8db
100KHz	420mVpp	.210	.0210	-33.6db

3.2 CAPACITIVE LOADS AND GAIN SWITCHING

Often times in an end product or test system a customer desires control over the gain setting for the amplifier. With any load this raises some important questions. Capacitive loads only complicate matters somewhat.

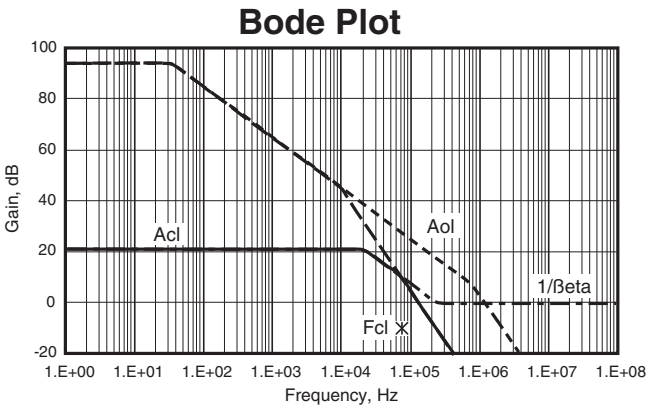
Figure 21 (back 3 pages) shows a bridge circuit for driving piezo transducers. The bridge circuit allows up to twice the peak voltage across the load than driving the load ground referenced. This is because as A1 goes towards +120V, A2 drives towards -120V yielding up to twice the peak voltage across the load. Correspondingly, the bridge circuit also doubles the voltage slew rate across the load for the same reason. Forcing the master amplifier, A1, to current limit first, equally distributes SOA stresses between A1 and A2 in case of a shorted load.

A range of loads was defined for this amplifier as shown in Figure 21 (back 3 pages) . The key to successfully changing the gains in this circuit is to change the noise gain compensation components as the input resistor is changed to select the desired gain setting. It is HIGHLY RECOMMENDED NOT to switch in different values of Cc around the PA88 amplifier A1 as gains are changed. There are MOSFET gates that are connected to the compensation pins that could be destroyed with compensation capacitor switching. It is also critical for stability that Cc be located directly at the amplifier which does not yield itself easily to switching. Figure 22 (back 2 pages) illustrates the 1/ß plots for stability for all selectable gain settings. Notice that the stability technique applied here uses both noise gain compensation on the input along with the feedback zero to maximize phase margin for stability. The modified Aol curves are shown for CL =.06µF and CL =.03µF. Output impedance for the PA88 of 100 ohms was used. Figures 23, (back 3 pages) 24, (back 2 pages) and 25 (previous page) prove through open loop phase plots that good stability is guaranteed. Open loop phase plot for A2 will be the same as Figure 23.

3.3 HIGH ACCURACY, HIGH VOLTAGE, LOW COST PZT DRIVE

Figure 26 (previous page) is an example of a high accuracy (input offset = 60µV), low drift high voltage amplifier. Though only used here at +/-60V, the PA241 can be used up to +/-175V supplies. The PA241 is a low cost monolithic ASIC designed for high voltage. The limitations of the high voltage ASIC technology do not allow for optimization of input characteristics, thus

MODEL	PA241,3-150	Note/PBs	Rn	9999999999	Kohms
Rcl	15	Ohms	Cn	0	nF
Cload	0.1	uF	Cf	22	pF
Rin	34	Kohms	Riso	0	Ohms
Rf	340	Kohms			



Total Rout	165	Ohms
Pole Zout/Cload	9.645744481	KHz
1/Beta (DC)	20.8	dB
Noise Gain	0.0	dB
Pole Noise Gain	0.159154943	KHz
Zero Noise Gain	0.159154938	KHz
Pole Cf/Rf	21.27739784	KHz
Zero Rf/Cf	234.051377	KHz
Zero Riso/Cload	1.59155E+11	KHz

FIGURE 27.

Phase Shift Components

Estimated Closure Frequency =	74.98942	KHz
Suggested maximum bandwidth	11.54782	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	51.78278	Degrees

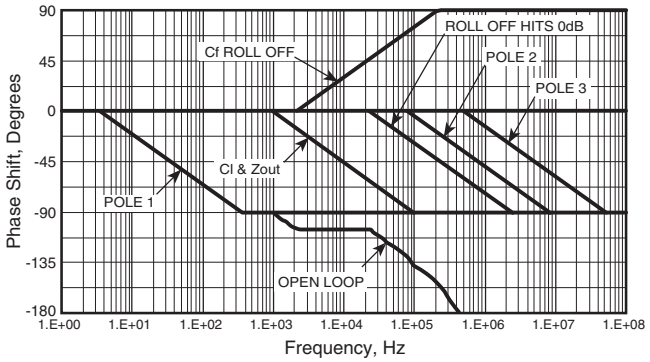


FIGURE 28.

the PA241 has a 40mV input offset voltage. In high voltage applications where low drift or high accuracy are desired this can be accomplished through the use of a composite amplifier which uses a low cost monolithic front end amplifier to control accuracy and drift. The PA241 now acts as a voltage and current booster.

There are three simple steps to stabilize a composite with a capacitive load:

STEP 1: Compensate PA241 for stability first: Refer to Figure 27 which shows how capacitive load modifies Aol. Figure 28 confirms that the selected 1/ß plot will guarantee stability for the PA241.

STEP 2: Create composite Aol: Refer to Figure 29 (see next Page) which shows addition of closed loop gain of PA241 to OP07 Aol on dB plot to yield net Composite Aol.

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	999999999	Kohms
Rf	340	Kohms	Cn	0	nF
Cf	0	pF	Using Look-Up data		

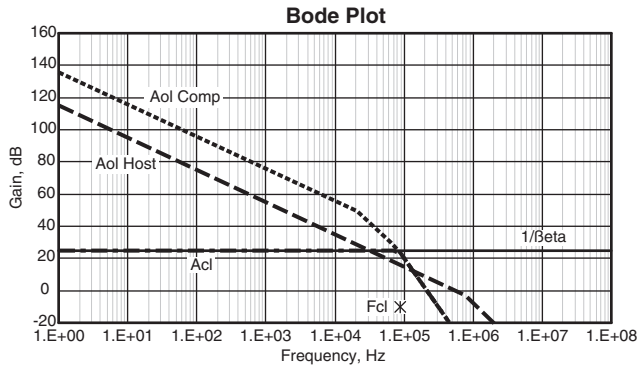
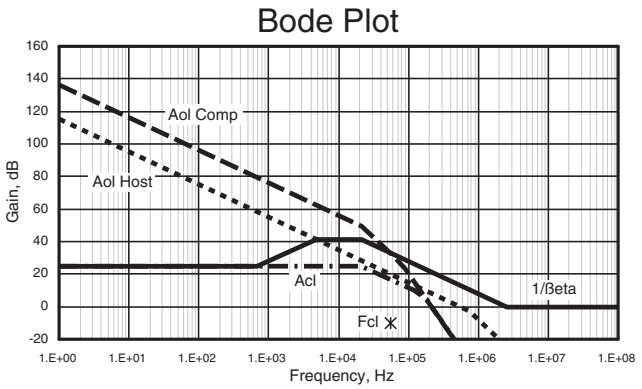


FIGURE 29.

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	3.4	Kohms
Rf	340	Kohms	Cn	10	nF
Cf	22	pF	Using Look-Up data		



1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

FIGURE 30.

STEP 3: Compensate composite op amp: Figure 30 (see next page) shows the selected 1/ß plot to stabilize composite amplifier. Both noise gain compensation and feedback zero compensation are used to maximize stability. Figure 31 (see next page) plots the open loop phase for the composite amplifier yielding 50 degrees phase margin and good stability.

3.4 HIGH HIGH VOLTAGE AMPLIFIER CIRCUIT

Figure 32 (see next page) illustrates the current state of the industry with regards to highest voltage available using op amps. This bridge circuit will give us up to +/-1160V across the load.

Remember when using the PA89 to pay particular attention to input protection, heatsinking (low quiescent current times high voltage ==> power dissipation!), components (power dissipation and voltage coefficient of resistance), and compensation capacitor (1200V rating necessary).

Estimated Closure Frequency =	56.23413	KHz
Suggested maximum bandwidth	5.623413	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	50.625	Degrees

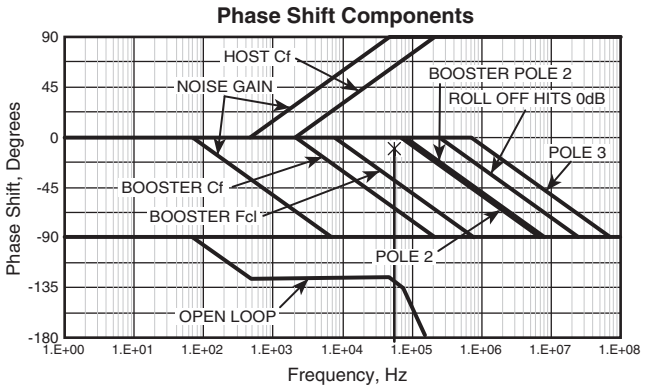


FIGURE 31.

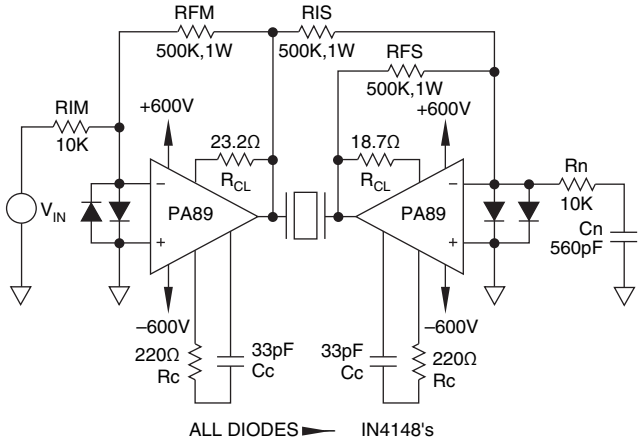


FIGURE 32. ±1160V PIEZO DRIVE BRIDGE

3.5 860VPP SINGLE SUPPLY PIEZO DRIVE

Occasionally it is desired to provide a bipolar drive to a capacitive load using only a single supply. This will reduce area and cost by only requiring one power supply. It will however require the use of a bridge circuit with two high voltage amplifiers.

Figure 33 (next page) is an implementation of an 860Vpp piezo drive. There are four simple steps to setting up the single supply scaling:

STEP 1: Define maximum V_{OP}:

MAX V_{OP} = +Vs - VsatA - VsatB

MAX V_{OP} = +450 - 10V -10V = 430Vp

STEP 2: Calculate gain:

Gain = V_{OPP} / V_{INPP} = (VA - VB)pp / V_{INPP}

Gain = 860Vpp / 12Vpp = 71.67

Gain = 2 RF/RI with the bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the midpoint power supply reference of +225V. Therefore: RF/RI = 71.67/2 = 35.833

STEP 3: Calculate offset:

$$VA - VB = +Vs(2\ (1+ RF/RI)\left(\frac{RB}{RA + RB}\right) - 1) - 2(RF/RI)V_{IN}$$

But when V_{IN} = 0 then VA-VB =+430V

Using RF/RI = 35.833 and solving above equation yields

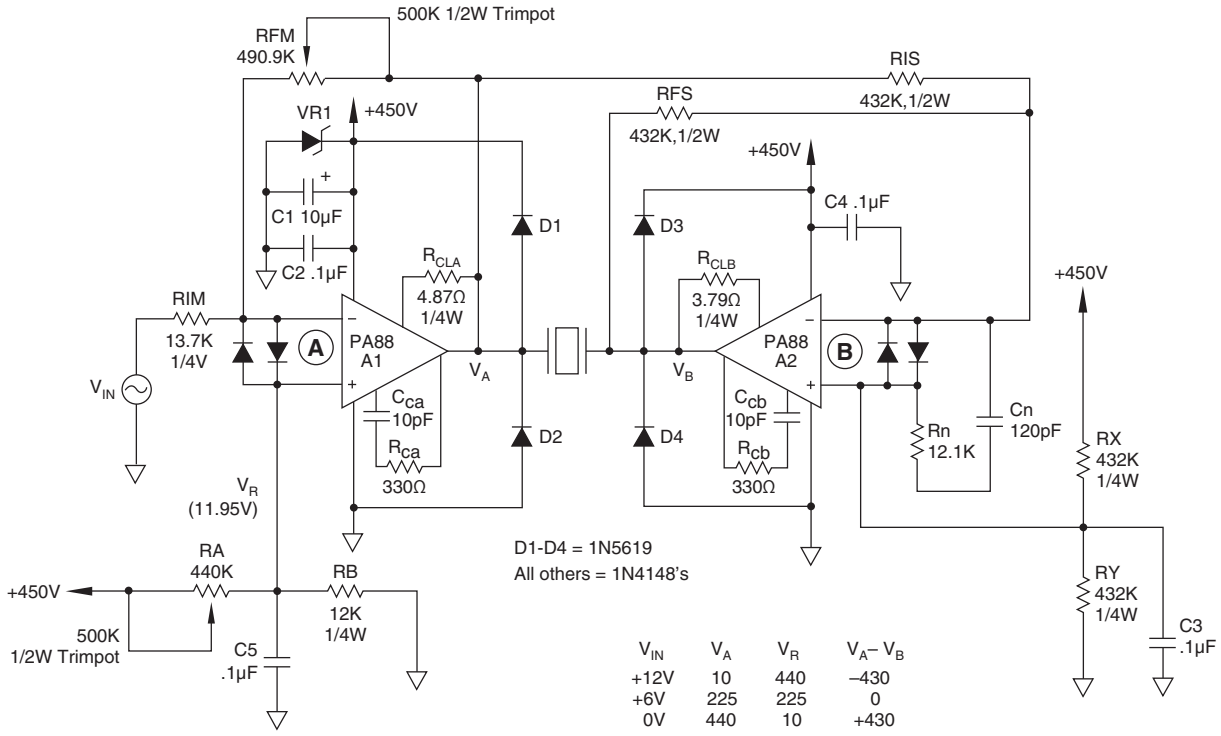


FIGURE 33. 860Vpp PIEZO DRIVE (SINGLE SUPPLY BRIDGE)

RA = 36.669RB

Choosing RB = 12K implies RA = 440K

STEP 4: Check for common mode voltage compliance:

The resistor divider of RA and RB was set to yield the desired offset. These values yield V_R = 11.95V which is greater than the minimum common mode voltage specification of 10V for the PA85.

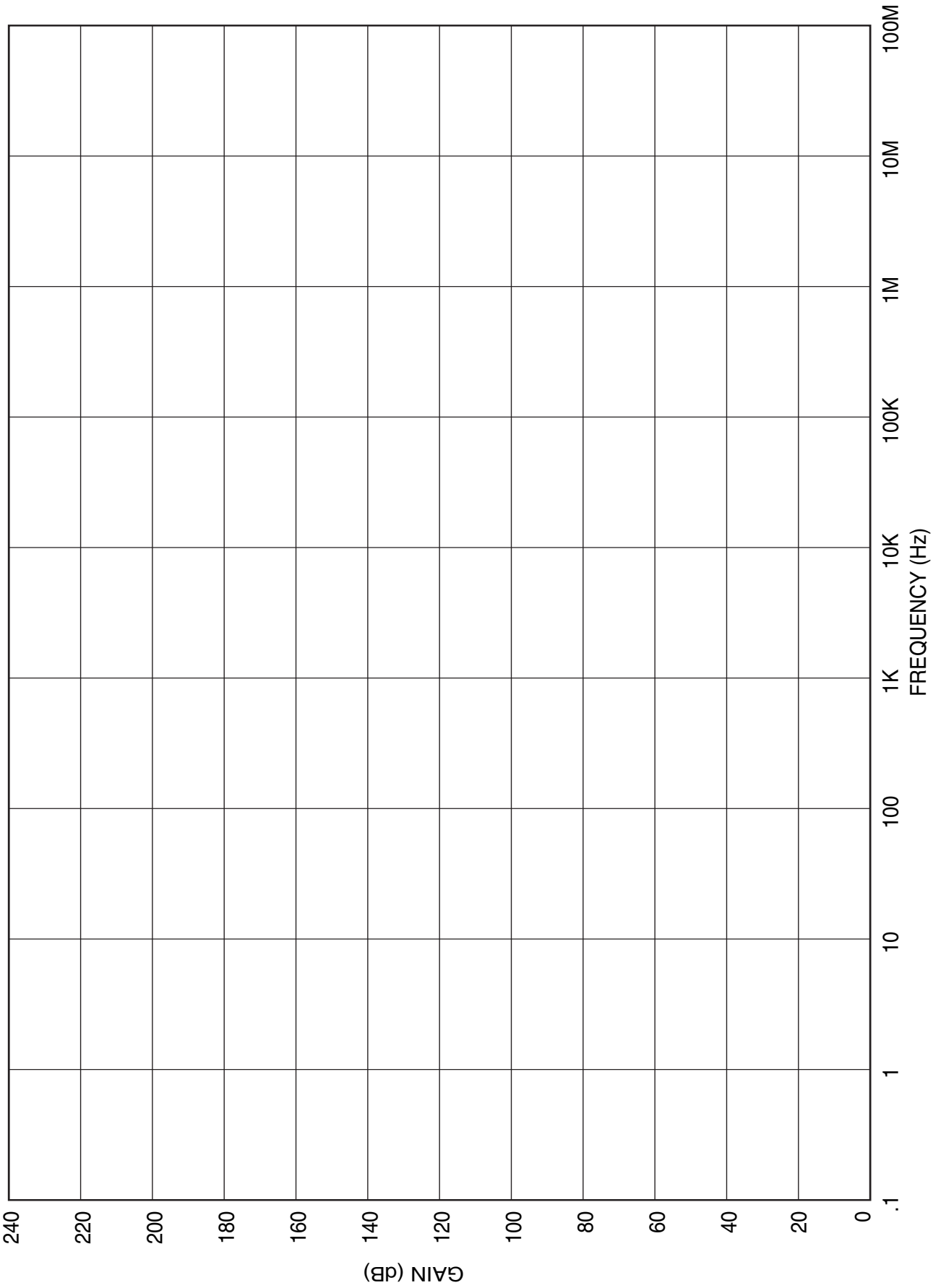
4.0 FINAL NOTE

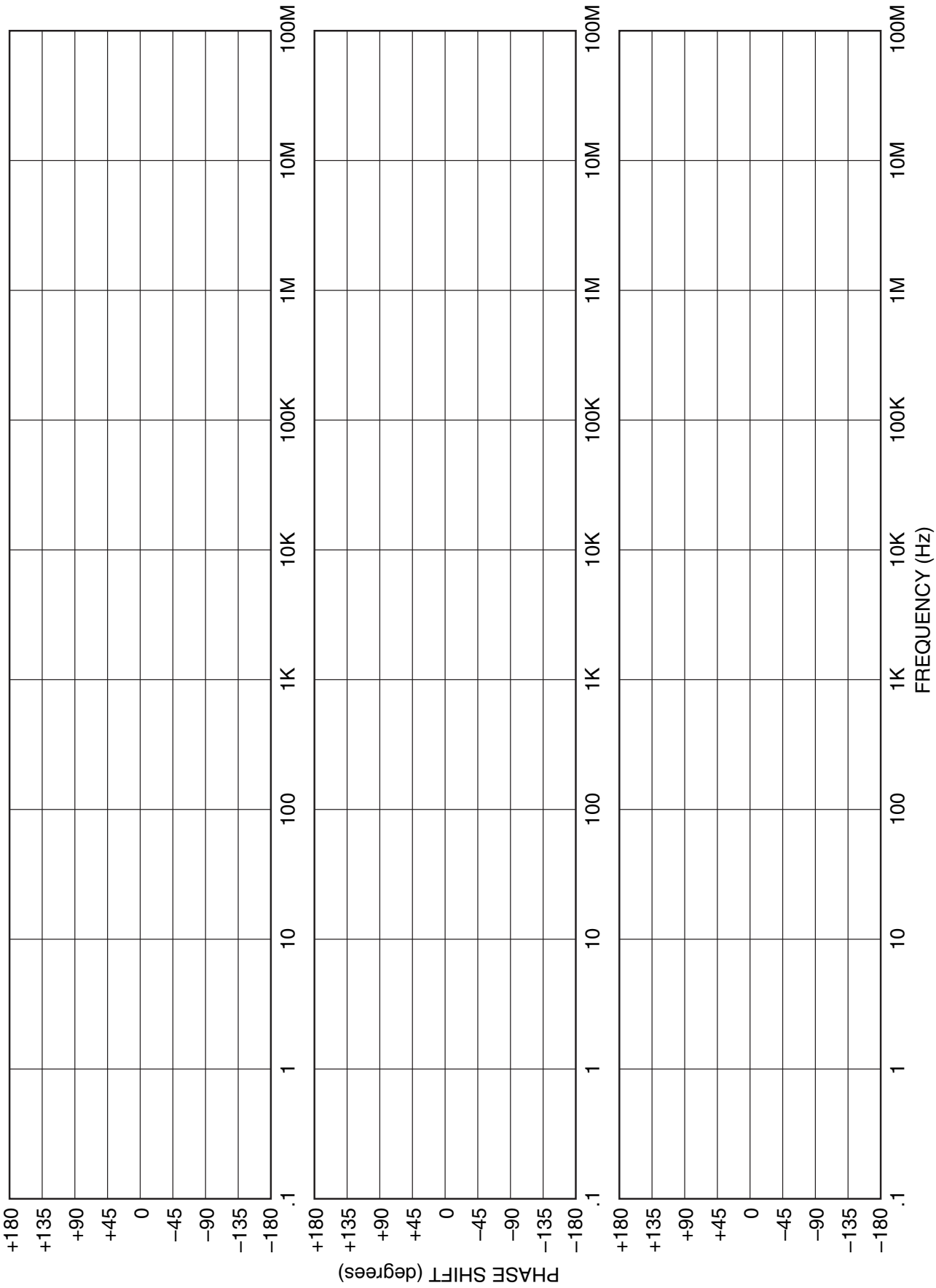
You have now looked at several ways to drive capacitive loads using high voltage amplifiers. The techniques presented here are intended to enable you to complete your circuit designs in a short time.

If there are additional questions or concerns not covered in this application note, please feel free to contact Cirrus APPLICATIONS ENGINEERING through our TOLL FREE Design Support Request, (800) 625-4084.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com


GAIN (dB)
240
220
200
180
160
140
120
100
80
60
40
20
0
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)


PHASE SHIFT (degrees)
+180
+135
+90
+45
0
–45
–90
–135
–180
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)

Parallel Connection

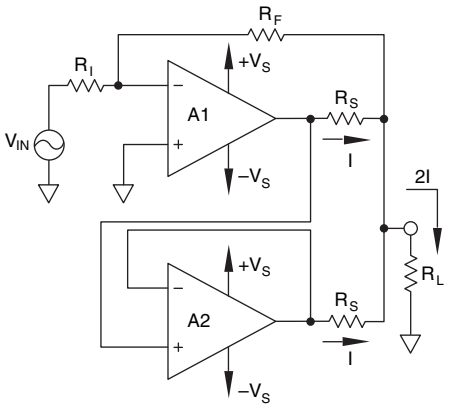
PARALLEL CONNECTION OF POWER OP AMPS

Power op amps can be paralleled to increase current, improve SOA (Safe-Operating-Area), or double thermal capability. While the basic topology seems simple, there are design details which require careful attention such as common-mode range considerations, stability, slew rate, and losses which can reduce efficiency and increase power dissipation.

1.0 BASIC PARALLEL TOPOLOGY

A1 in Figure 1 referred to as the master amplifier, can be configured in any form desired, inverting or non-inverting, and any gain desired. Feedback for A1, and only A1, will come from the overall output of the parallel connection. The output of each amplifier will have in series equal small-value resistors to improve current sharing characteristics. The slave amplifiers, A2 and up to An, are configured as unity gain non-inverting buffers driven from the output terminal of the master amplifier A1. Each slave's individual feedback is taken directly at its output terminal.

The idea of this connection is since each slave is a unity gain buffer, the slave outputs will match as closely as possible the output of the master. Yet with the master feedback being wrapped around the entire circuit, overall accuracy is maintained.



CONSIDERATIONS

- $I_{LOSS} = V_{OS}/2R_S$
- $V_{LOSS} = I_{OUT}R_S$
- SLEW RATE MISMATCH WILL GIVE LARGE I_{CIRC}

FIGURE 1. BASIC CONNECTION.

2.0 LOSSES

The output of the slaves in this configuration will not exactly match the master. Since the slaves operate at unity gain, the difference will be equal to the worst case offset of a single amplifier for two amplifiers in parallel since only the offset of the slave causes this mismatch. With more than one slave, each slave could have worst case offset in opposite directions, and in the worst case, the mismatch is twice the input offset voltage.

These offset voltages produce a drop across the current sharing resistors and a corresponding current flow. This is current that is "lost", never appearing in the load and increasing amplifier dissipation.

Even a unity gain buffer (the slave amplifier) has phase shift making it's instantaneous output voltage different from the master amplifier, and again producing a voltage drop across the sharing resistors. If the desired signal frequency is grater than half the power bandwidth of the amplifier, the parallel connection will likely not be practical. To check a specific application, Use Power Design to find closed loop phase shift, multiply the sine of that angle times the peak output voltage to find the peak difference voltage across the sharing resistors. This current is again "lost", never appears in the load and increases amplifier heating.

2.1 CURRENT SHARING RESISTOR CHOICE

Increasing values of current sharing resistors will reduce the circulating current loss. But this improvement must be weighed against direct losses through the current sharing resistors when delivering current to the load. The challenge to the designer is to find the happy medium for Rs values. As a general rule, power amplifiers will be used with Rs values of from 0.1 ohm to 1.0 ohm.

3.0 CURRENT LIMITING

Current limit of the master should be set 20% lower than the slaves if possible, and the ultimate current limit of the overall circuit will be that limit multiplied by the total number of amplifiers. The idea here is the master current limits first, and since it provides the drive for all other amplifiers, that drive is also clipped. This insures equal sharing of all stresses during current limit.

4.0 SLEW RATE CONSIDERATIONS

Assume an initial condition where the output of the circuit in Figure 1 is resting close to the negative rail. Then apply a step function to the input of the master amplifier to drive the output positive. The output will slew as fast as the amplifier's slew rate to the positive rail. With the slave being driven from the master, the slave doesn't get its input transition until the master slews, and then the slave requires additional time to slew positive.

In the interval where the master has reached positive output and the slave is trying to catch up, there is a large difference in the output voltage of the two amplifiers developing current through the two current sharing resistors. This can be a large current equivalent to the current limit of the amplifier. That's the bad news. The good news is that it is a transient current and as such may be within transient SOA limits. But this can be difficult to prove for certain.

When in doubt, the best rule of thumb is to not use the parallel connection at greater than half the rated slew rate of the amplifiers.

5.0 STABILITY CONSIDERATIONS

For detailed information on stability, refer to Application Note 19, "Stability For Power Operational Amplifiers". All discussion here is based on the stability theory contained in Application Note 19.

5.1 SLAVE STABILITY

The most obvious problem from a stability standpoint is the unity gain buffer connection of the slaves. This configuration has the least ability to tolerate poor phase margin. Poor phase margin usually occurs as a result of excessive capacitive loading. But in the case of the PA12, the unity gain buffer connection should not be used without additional compensation. Externally compensated amplifiers should normally be compensated for unity gain and may still require additional compensation. Alternatively, they may be decompensated to improve slew rate and use noise gain compensation to insure stability.

The most common way we recommend to compensate the slave is with a noise gain compensation network across the inputs to the amplifier. However, for noise gain compensation to work, there must be impedance in the feedback path. Figure 2 shows the modifications necessary to incorporate noise gain compensation.

The R_{FS} value of Figure 2 is somewhat arbitrary, but its choice will dictate the final values of Rn and Cn. As is the general case in any op amp circuit, excessive impedance for RFs is something to be avoided. A realistic range of values for RFs is from 1 KΩ to 1 MΩ with a good starting point being 10 KΩ.

Once the value of R_{FS} is pegged, noise gain compensation should usually be set to give a noise gain of 10. This corresponds to Rn being one-tenth Rf. Cn must be found analytically according to procedures outlined in Application Note 19 after considering the effects of amplifier bode plot and additional poles resulting from capacitive loading. In many cases, selecting Cn for a corner frequency of 10KHz based on the value of Rn (Xcn = Rn@10KHz) will result in a stable circuit; although, analytical methods will maximize bandwidth in comparison to this method.

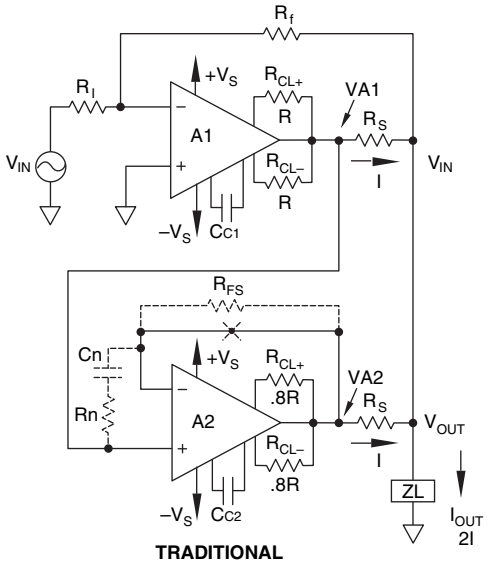


FIGURE 2. SLAVE STABILITY.

5.2 MASTER STABILITY

A1 is subject to all normal considerations for stability. If A1 is a gain of 10 or greater, its stability will be equal to that of the slave with noise gain compensation described above. At gains below 10, the optimum noise gain will be a gain of 10 to match the slaves.

6.0 COMMON MODE CONSIDERATIONS

The unity gain buffer configuration must be able to accept inputs equal to the maximum output swing of the master. This will be a problem with MOST amplifiers. Light loads make the situation worse. Both the output voltage swing and the common mode voltage range specifications are given as volts from the supply rail. Read the output voltage swing from the typical graph at the lowest possible current the amplifier will be required to drive when the input signal calls for saturation. Read the common mode voltage specification from the specification table in the MIN column. For the parallel configuration to work without special circuitry, the output voltage swing must be at least as large as the common mode voltage specification.

The PA02 does not lend itself to parallel connection. Negative inputs which get closer than 6 volts of the negative supply rail can cause output polarity reversals which can be catastrophic in the parallel connection.

6.1 OVERCOMING COMMON MODE RESTRICTIONS

A method most useful with high voltage amplifiers where currents are low, is to simply use zener diodes in series with the supply line to the master amplifier as shown in Figure 3A. These drop the master supply low enough to restrict its output swing to be within the common-mode range of the slaves. Determine wattage ratings based on expected load + quiescent current flow.

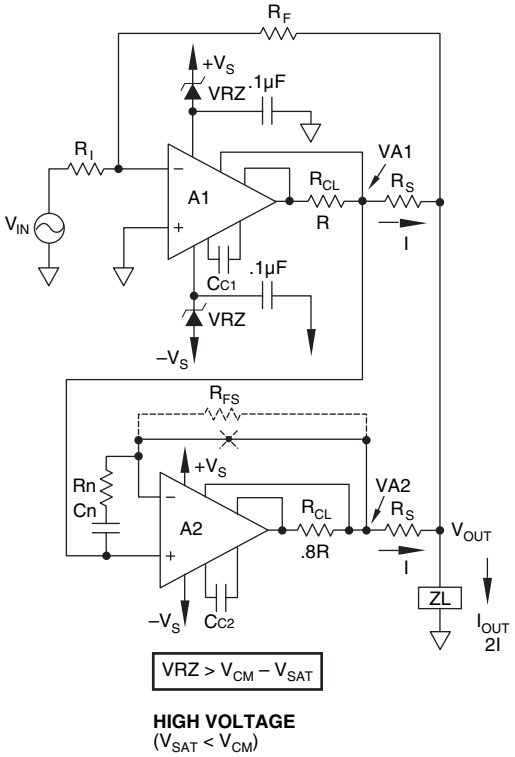


FIGURE 3A. OVERCOMING COMMON MODE RESTRICTIONS.

The PA04 and PA05 present another opportunity to overcome common-mode limitations by taking advantage of their boost pins. Originally incorporated to improve output voltage swing, we effectively increase common-mode range by increasing front-end supply voltages. A boost of at least 5 volts will be adequate to overcome this limitation. Figure 3B elaborates on this connection.

Other methods include operating slaves on slightly higher voltages than the master. This is what is accomplished with the zeners described previously, but is not easily applied to high current power amplifiers unless they have boost voltage provisions. In such cases the zeners can be included in series with the Vboost pins of the master amplifier.

It may seem possible to attenuate the output of the master and set the slaves up with corresponding gain, but it will be found that unless very strict matching requirements of the associated resistors are met, extremely large circulating currents will flow.

7.0 BRIDGE CIRCUITS

The master-slave combination once realized and taken as a whole, comprises one effective op amp. Treated this way, incorporation into a bridge circuit is simply a matter of using an inverting unity gain configuration on the slave side of the bridge (note that the slave of the parallel combination and the slave side of a bridge are two different things). Bridge techniques are discussed in detail in Application Note 20, “Bridge Operation.”

8.0 SINGLE SUPPLY

There are no unique considerations concerning single supply except those described in Application Note 21, “Single Supply Operation.” Again, as in the bridge, treat the parallel combination as a single op amp.

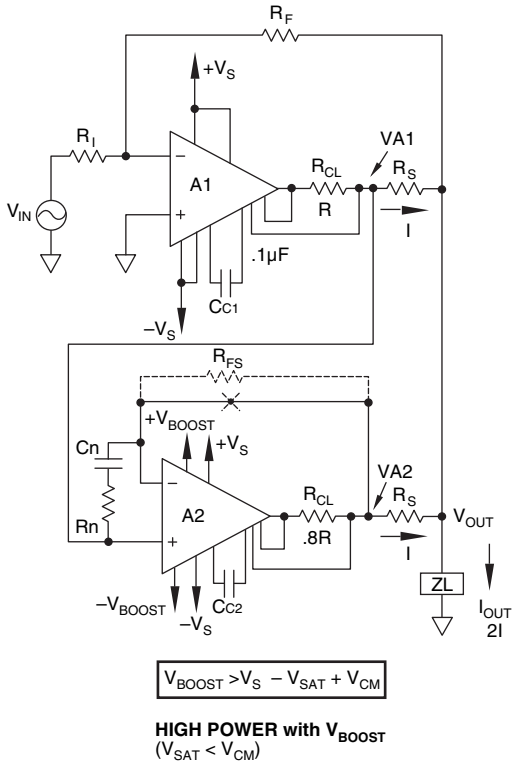


FIGURE 3B. OVERCOMING COMMON MODE RESTRICTIONS.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Proper Analog Wiring for Power Operational Amplifiers

1.0 AVOID PREDICTABLE FAILURES

This brief application note is intended to guide you through successful prototyping and final construction of power op amp circuits by using proper component location and interconnection techniques.

Proper analog construction of power op amps is just as critical as choosing the proper power op amp, heatsink, or schematic design. For reliable success, you should treat all power op amps as high frequency devices. Even though you may have designed a circuit to operate at 400Hz, the amplifier will, in general, have a bandwidth capability out to 4MHz or so and will be happy to oscillate at that frequency if not constructed properly.

In addition to this application note, be sure to read "General Operating Considerations" in the Apex Precision Power handbook for details on stability, supplies, heatsinking, mounting, current limit, SOA, and specifications interpretation.

2.0 PROPER MECHANICAL MOUNTING

Refer to Figure 1. This side view of the amplifier mounted to a heatsink shows optimum mounting to allow for wiring ease of the peripheral components associated with the power op amp. Notice the necessity of teflon sleeving to insulate the amplifier leads from the heatsink; the use of a mating socket for ease of solderable component connections; and the use of an Apex Precision Power thermal washer (or thermal grease) as the only approved interface between the amplifier and the heatsink.

You also want to be sure the recommended mounting torque of 4-7in-lbs (.45-.79 N-m) for the 8-pin TO-3 package and 8-10in-lbs (.90-1.13 N-m) for the Power Dip, JEDEC MO-127, package is used. This torque needs to be applied in small increments alternating between the two mounting bolts, similar to tightening the lug nuts on a car tire.

2.1 8-PIN TO-3 MOUNTING

Since the 8-pin TO-3 package is more sensitive to improper mounting torque, here is a rule of thumb for those who do not have ready access to a torque screwdriver:

i) After an Apex Precision Power thermal washer or grease is applied and the teflon sleeving installed on the leads, assemble the power op amp onto the heatsink and press it firmly into the mating socket until it is firmly seated and there is no gap in the assembly.

ii) Insert the two mounting bolts through the mounting holes in the flange of the amplifier and tighten them "finger-nail" tight. Literally use your fingernail as a screwdriver. This ensures no overtorque and gives a starting point so that the nut fits snugly against the mating socket.

iii) After using "finger-nail" tightening, one complete revolution on the head of each mounting bolt is 4-7in-lbs. Apply this torque one quarter of a turn at a time, alternating between the two mounting bolts, until one complete revolution is reached.

3.0 PROPER ANALOG CONSTRUCTION

Figure 2 illustrates a typical inverting power op amp circuit which will be used to discuss proper component locations and wiring. Other power op amp circuits will use similar techniques.

Refer to Figure 3. This Figure shows the proper routing of connections and component locations for the circuit of Figure 2.

The mating socket will be facing towards you to allow for "unlimited" height so a "circuit ball" or "bird's nest" of components can be soldered directly to the mating socket. This will result in an analog construction equivalent to a properly designed printed circuit board.

Note the location of all components associated with the power op amp circuit shown in Figure 2 are directly at the power op amp's mating socket. A single point ground is illustrated by physical connection of the power supply ground, input signal ground, and output load ground.

For the single point ground wire running from the power supply to the power op amp, strip back the wire's insulation about 2 or 3 inches and tin it with solder. This wire can then be bent or "bussed" wherever it needs to go to pick up all ground points for the power op amp and its associated components.

Stand components on end, "cordwood style", or leave them hanging in mid-air, using the leads of the components themselves as interconnection wires.

DO NOT RUN WIRES FROM EACH PIN OF THE POWER OP AMP OVER TO A PIECE OF VECTOR BOARD, PERF BOARD, OR PRINTED CIRCUIT BOARD WHERE THE POWER OP AMP'S ASSOCIATED COMPONENTS ARE LOCATED—THIS WILL BECOME AN OSCILLATORY, ANALOG DISASTER!

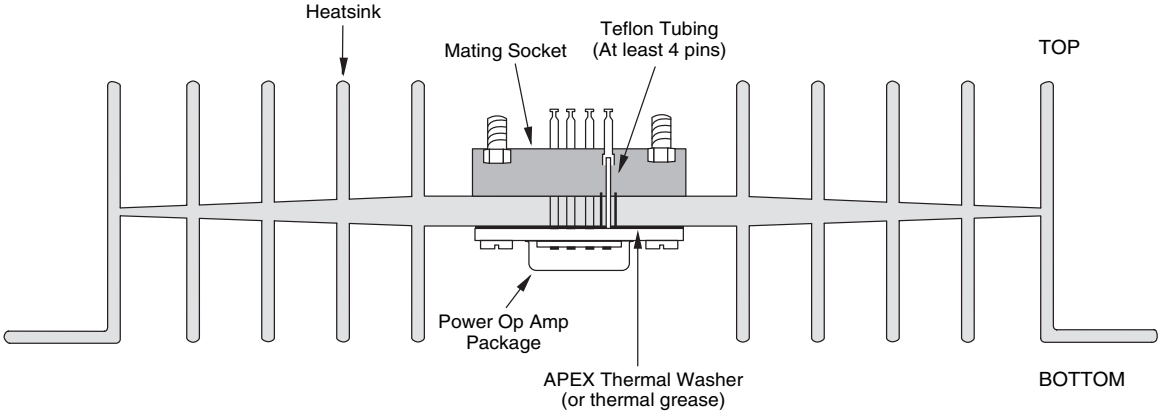


FIGURE 1. SIDE VIEW.

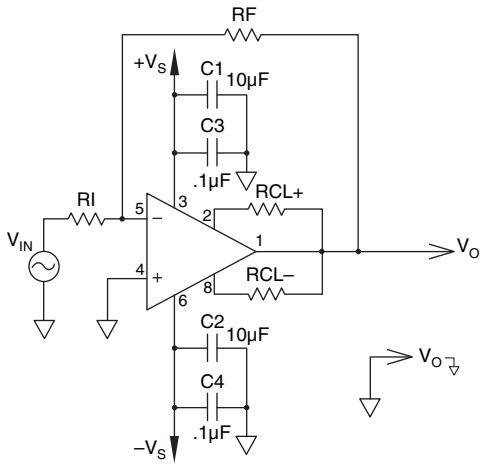


FIGURE 2. SCHEMATIC.

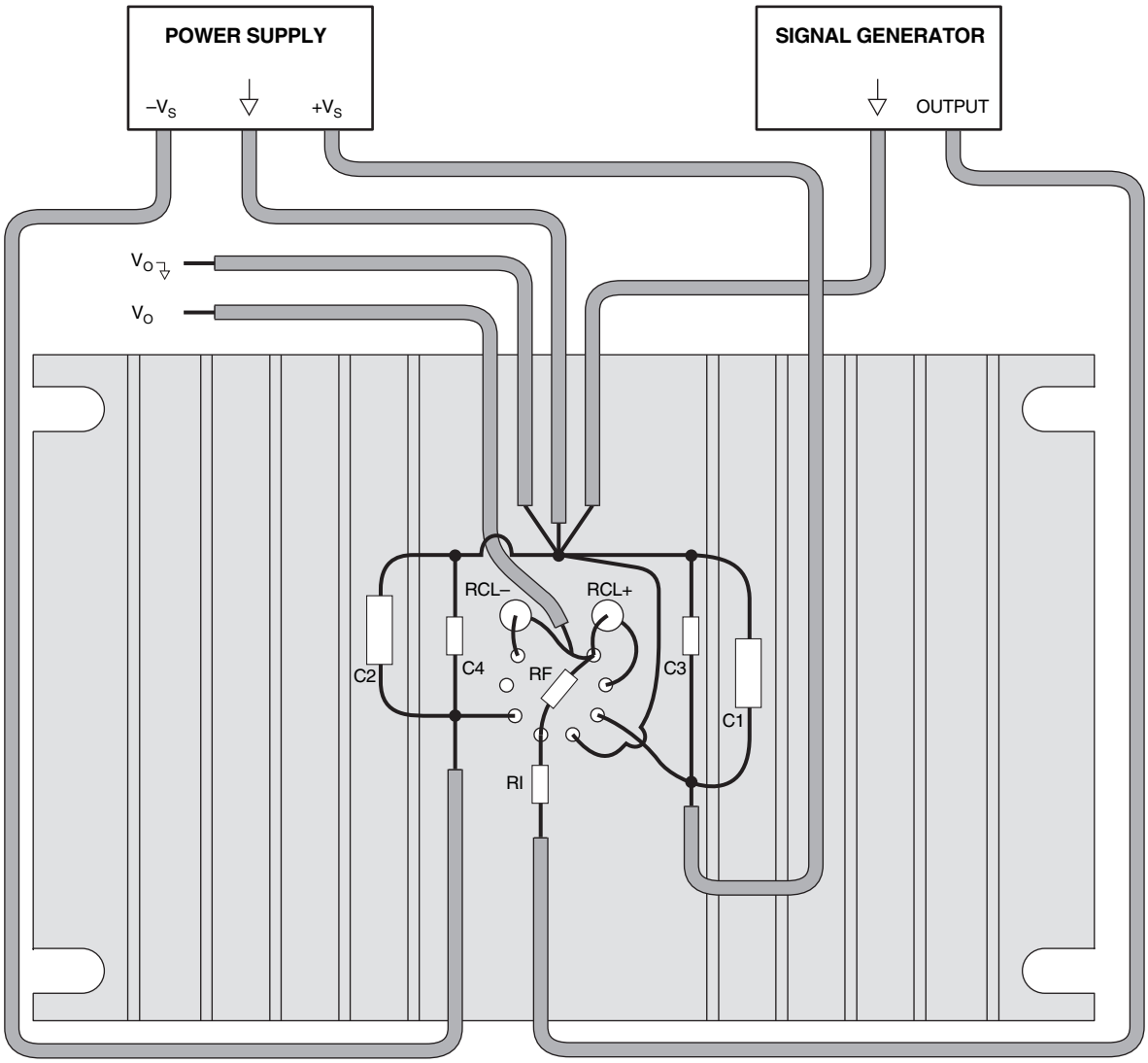


FIGURE 3. TOP VIEW. BOTTOM VIEW OF AMPLIFIER.

PWM Basics

1.0 INTRODUCTION

This note is divided into three sections. The first section provides general information on Pulse Width Modulation amplifiers and examines a typical block diagram. The second section on designing with PWM amplifiers is NOT intended for optional reading. The family of PWM amplifiers are not equal in protection features and some of the design errors that would cause a linear amplifier to oscillate will destroy some of the less protected PWM amplifiers. The final section examines some ways to use PWM amplifiers.

PWM circuits are taking the same general course of development traveled by op amps and many other electronic functions. Concepts were brought to life using discrete components and were followed by modules, hybrids and then monolithics. Since the introduction of the first hybrid PWM amplifiers from Apex Precision Power, the product family has broadened to include a wide range of power levels and package types. The family includes models with up to three levels of internal protection circuitry and low cost models that feature no frills PWM power. With digital or analog input capability on most amplifiers, the Apex Precision Power PWM family can fit the requirements of many applications.

2.0 WHY PWM

As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. A 20A output stage often requires multiple 20A semiconductors mounted on massive heatsinks and usually employs noisy fans or liquid cooling in some cases.

Figure 1 illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level losses in the linear circuit are relatively low. When zero output is commanded the pass element resistance approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to midrange power levels. When loads appear reactive this efficiency drops even further.

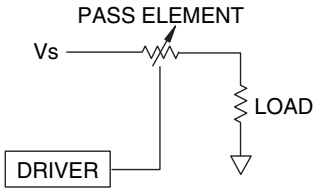


FIGURE 1. LINEAR POWER DELIVERY

Figure 2 illustrates the most basic PWM operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. As higher outputs are commanded, the switch is held ON longer portions of the period. Normally, the switch is ON and OFF once during each cycle of the switching frequency, but there are many designs capable of holding a 100% ON duty cycle. In this case, losses are simply a factor of the ON resistance of the switch plus the inductor resistance. As less output is commanded the duty cycle or percent of ON time is reduced. Losses include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a very small portion of the time and this voltage drop is a small fraction of the supply voltage.

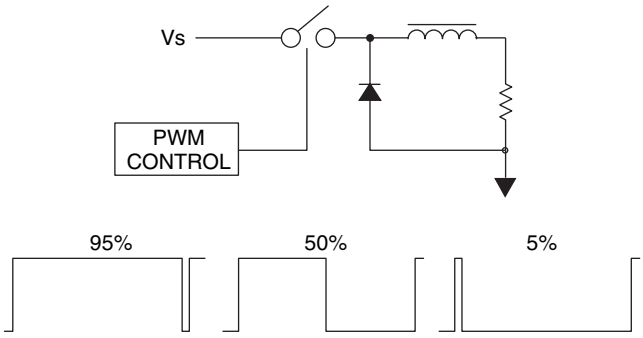


FIGURE 2. PWM POWER DELIVERY

The job of the inductor is storing energy during the ON portion of the cycle for filtering. In this manner the load sees very little of the switching frequency but responds to frequencies significantly below the switching frequency. A rule of thumb is to expect a usable bandwidth to be one decade below the switching frequency. Inductive loads often provide adequate filtering without dedicated filters.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Note that efficiency claims on the hybrid PWM amplifier data sheet do not include filter losses. Typical efficiency of filtered PWM circuits range from 80 to 95%.

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature, and lowest efficiency output level. In the case of reactive loads, maximum voltage-to-current phase angle (lowest power factor) must also be addressed.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of waste heat when running full output and around 50W delivering half power. The theoretically perfect linear circuit will generate 500W of waste heat while delivering 500W. Table 1 shows three possible ap-

	Discrete Linear	Hybrid Linear	Hybrid PWM
Waste heat	500W	500W	100W
Pkg count	16 x TO-3	2 x PA03	1 x SA01
Heat sink	0.11°C/W	0.11°C/W	0.55°C/W

TABLE 1. CONTRASTING DISCRETE LINEAR, HYBRID LINEAR AND HYBRID PWM 1kW DESIGNS

proaches to this type design. In all three cases it is assumed ambient temperature is 30°C and maximum case temperature is 85°C. It is also assumed power ratings of the TO-3 devices is 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections. The linear approaches require five times the heatsink rating of the PWM approach. The bad news with the hybrid linear design is that the heat is concentrated in such a small area that this design is right on the edge of requiring liquid cooling. With its high package count the discrete linear approach will likely have more than five times the heatsink size and weight of the PWM.

3.0 HOW IT WORKS

The simple form of PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Carrying this one step further we get the PWM circuit employing four switches configured as an H-bridge providing bipolar load current from a single supply. This does mandate that both load terminals are driven and zero drive results from 50% of supply voltage on both load terminals. See Figures 3 and 4 for the basic bridge operation and typical waveforms.

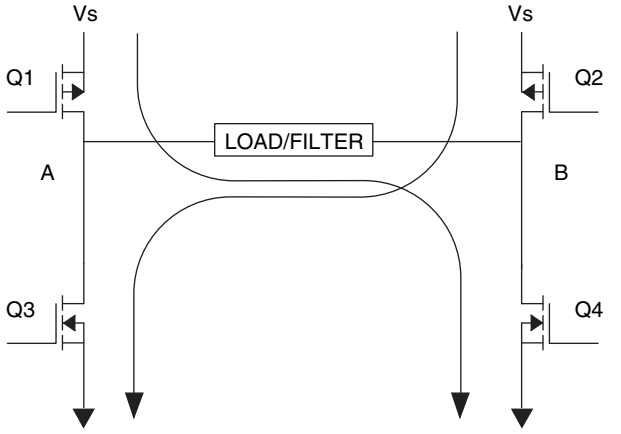


FIGURE 3. BIPOLAR OUTPUT OF THE BRIDGE

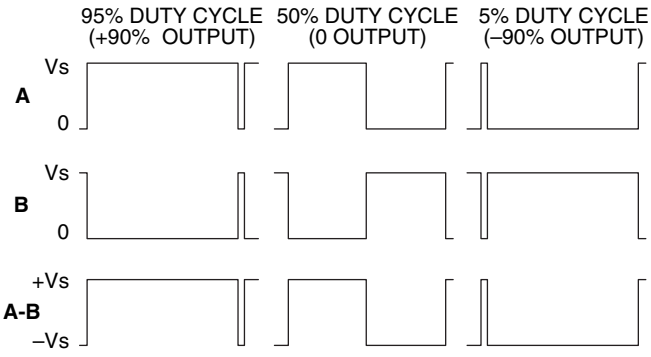


FIGURE 4. H-BRIDGE WAVEFORMS

3.1 HYBRID H-BRIDGE BASICS

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Notice how the levels of the A-B waveform are different even though shape is identical to the A waveform. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle.

Figure 5 shows a block diagram typical of Apex Precision Power PWM amplifiers. The hybrid construction of these amplifiers can allow monitoring of temperature directly on the surface of each power die rather than case or heatsink temperature monitoring - the best that a discrete design could implement. Direct die temperature measurement eliminates thermal resistance variables and reduces response time by orders of magnitude. The thermal limit is set at approximately 165°C. Activation of the thermal shutdown circuit will latch all of the H-bridge switches off. Toggle the shutdown pin or cycle the power to reset the amplifier and resume normal operation.

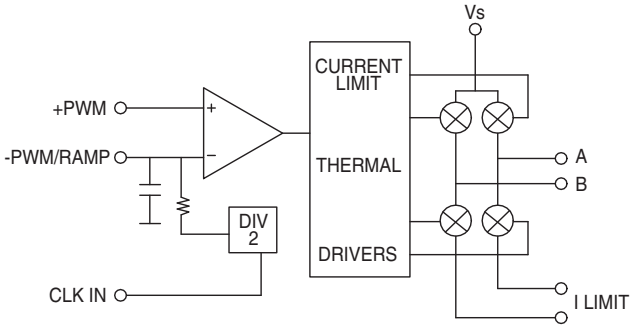


FIGURE 5. BLOCK DIAGRAM

3.2 CURRENT SENSE, CURRENT LIMIT AND CURRENT SHUTDOWN

The first of two current limits in the PWM block is the high side current limit that activates only upon output shorts to ground (assuming the programmable current has been properly configured.) This circuit has a variable response time based on the current magnitude in $+V_S$ line. With a fault current of about 1.5 times the rated output current it will require several cycles of the switching frequency to activate the circuit. As higher currents are sensed the response time decreases. Once a fault has been sensed the amplifier will remain latched off until power is cycled or the shutdown pin is toggled.

The second current limit circuit in the block diagram is programmable and activates upon a load fault or a short to the power supply. An external resistor senses current flowing between ground and the low side of the H-bridge. The sensed voltage is fed to the current limit pin. When this voltage exceeds the threshold (see individual datasheets for this value), all switches in the H-bridge are shut off for the remainder of the switching cycle. Because the sense voltage will have considerable spike content, the hybrid includes an internal filter stage. A second external stage of R-C filtering allows larger peak currents for any given value of current sense resistor. In some models, the current limit function can be used to shut the amplifier down on command of a logic level input voltage.

In most circumstances (half bridges are a common exception) all of the load current finds its way through a sense resistor to ground. This implies that the choice of resistor should be capable of handling the maximum load current defined by the current limit resistor value.

NOTE: Some amplifiers, such as the SA60 and others, do not have the current limit feature, but do allow the use of current sensing resistors for use in a current feedback loop. Because these amplifiers are unprotected, it can be tempting to use large resistance values for R_{SENSE} to limit the current ($I_{MAX} = V_{SUPPLY} \bullet R_{SENSE}$). However tempted you may be, DO NOT attempt to use high value resistors for R_{SENSE}. When you do this, there is significant voltage developed across R_{SENSE} - between the source of the lower output FET and ground. This can allow the gate driver circuit to drive the gate of the FETs below the source enough to blow them.

3.3 ACCURACY - CLOSED LOOP

In closed loop applications (the only kind that have any accuracy), an integrating error amplifier is used to eliminate the difference between command signals and feedback signals. Its output voltage will go to the exact voltage required by the PWM block to generate the proper duty cycle corresponding to the desired output. The first job of the error amplifier is responding to input signal changes, but it also compensates other variables inside the feedback loop. Variations in supply voltage will require an adjustment of the input to maintain a output stability. On resistance of the H-bridge, resistance of the filter inductor and sometimes load resistance temperature variations are compensated. Systems such as speed controls may place mechanical factors such as conveyer belt load weight inside the loop where the error amplifier compensates the variations. Closing a voltage or current loop around PWM amplifier is non-trivial. Application Note 41 discusses closed loop PWM in great detail and is recommended reading for designers looking for precision control from their PWM circuit.

The PWM circuit converts the error amplifier output into a variable duty cycle drive signal that includes 0% and 100%. A dead time (all 4 of the H-bridge switches turned OFF) is inserted between each change of polarity at the output. This prevents “shoot through” current spikes caused by both H-bridge switches in the same leg of the H conducting at the same time. If these spikes were allowed to exist they would cause high stress and possibly destruction of both amplifier and power supply components.

3.4 DUTY CYCLE

There are many methods for converting an analog input into a PWM output. Of the methods used in Apex Precision Power products, the following is most common and provides a good foundation for understanding any of the various techniques used by Apex Precision Power and others. Accurate analog PWM generation is founded on a triangular reference signal (sometimes simply called RAMP). To provide a good reference, the ramp must have a linear rise and fall. The most economical method for generating this ramp signal is to start with a moderately stable square wave oscillator and use a divide by two circuit to ensure that the duty cycle is exactly 50%. An R-C network can convert this square wave into a reasonably linear triangle wave that is really exponential rise and fall. With carefully chosen peak voltages, the error caused by a non-linear triangle reference can be kept around 1% in an open loop system because most of the error on the rise is compensated on the fall. With a closed loop, the affect of this non-linearity is virtually unnoticeable.

To generate a PWM signal, the analog input voltage is compared to the triangle ramp reference. When the input signal is greater than the ramp voltage the A side of the H-bridge

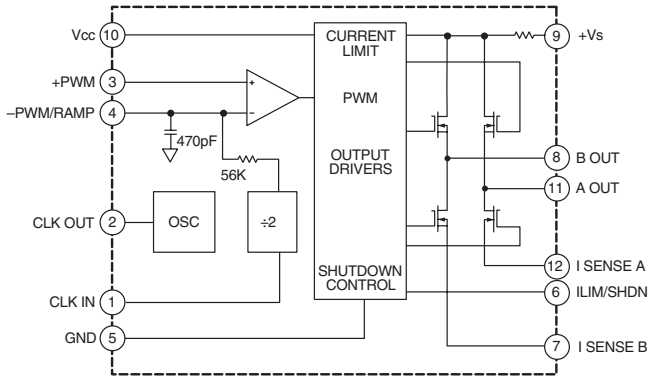


FIGURE 6. PWM CONTROL BLOCK

switches to V_S and the B side to GND. Similarly, when the input signal is less than the ramp, the B side switches to V_S. Figure 7 illustrates this principle. If the input is always within the peak to peak ramp voltage then an infinitely variable duty cycle can be achieved. If the input signal is outside the peak to peak ramp voltage there is no switching - the A side or the B side is V_S (0% or 100% duty cycle)

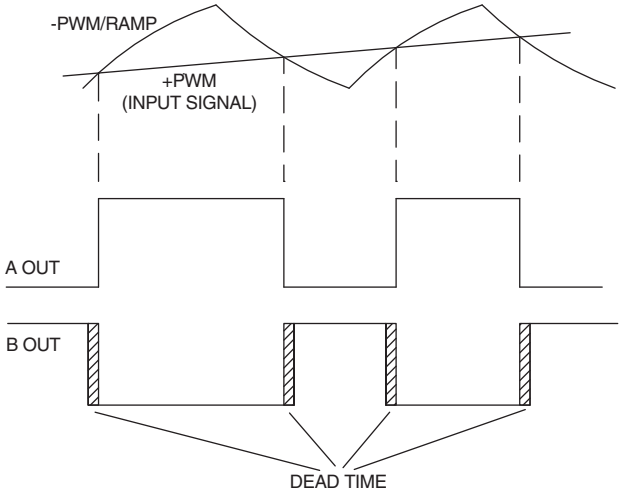


FIGURE 7. PWM WAVEFORMS

For the safety of the amplifier, the load, and bystanders in the general vicinity, it is important that the two switches on the same side of the H-bridge are never on at the same time. This would essentially create a short from V_S to GND and it would not be pretty. Dead time is the solution to this potential problem. During the transition from the A side to the B side of the H-bridge, there is a period of time in which neither side is high - this is the dead time. Each amplifier has a fixed dead time based on the properties of the switches used inside. Dead time causes a small non-linear region in the variable duty cycle near 0% and 100%. Notice in each product datasheet that the output duty cycle will jump from approximately 97% to 100% (or 3% to 0%). Dead time also contributes a very small amount of inefficiency to the system. It is important to note that some models have variable switching frequencies. Since the dead time is not variable, efficiencies will drop as switching frequency increases - the dead time accounts for a larger percentage of the switching cycle.

In figure 7, note that the input voltage depicted is a straight line. The input voltage will obviously vary, but keep in mind that the useful bandwidth of the PWM amplifier is significantly

less than the switching frequency. If the slew rate of the input voltage were allowed to approach that of the triangle wave, dead time circuitry could be ineffective at preventing shoot through.

The output waveform during dead time is primarily a function of load impedance. Current flow is interrupted by the dead time and the load or filter inductance will discharge its flyback energy at this time. While generally not shown in the block diagrams, each power switch has a diode to conduct the flyback current.

The outputs of this block labeled A OUT and B OUT do not directly represent high and low states of the two amplifier output pins. When the A Drive line is high it turns on the switch between the A output and the power supply and also the switch between the B output and ground. When the A Drive is low, both these switches are off. B Drive controls the other two switches in the bridge.

4.0 FREQUENCY, FREQUENCY, FREQUENCY

In designing with and using PWM technology, the switching frequency is one of the critical system parameters. Note however, that most Apex Precision Power PWM datasheets specify a clock frequency. Circuitry in the amplifier divides this clock frequency by two to provide the basis for the triangle or ramp signal. For example, the SA08 has an internal clock frequency of 45kHz and therefore has a switching frequency of 22.5kHz. The switching frequency is the basis for any filter design that might be required.

Some PWM amplifier models include CLK OUT and CLK IN pins. Generally these pins are simply connected together so the amplifier generates its own clock source. You can, however, use the CLK IN pin to synchronize the clock frequencies of multiple amplifiers in a system or to some other external source. In some cases this can be helpful for managing EMI. However, the divide-by-two function does not guarantee that the ramp signals of multiple devices are in phase, so simply sharing the same clock source does not allow multiple amplifiers to be used in parallel. A parallel PWM design is not trivial and is far beyond the scope of this text.

The third frequency important to consider in any PWM system is the signal frequency. As mentioned previously, the PWM signal must be averaged over time to achieve an analog type of output. The precision and cleanliness of the signal depends on how many output pulses are used to achieve the signal level. As a rule of thumb, the analog signal frequency should be at most 10% of the switching frequency. This relationship of signal and switching frequency is analogous to analog to digital conversion and the necessity to have many digital samples to accurately represent the changes in the analog signal.

4.1 CHANGING THE CLOCK FREQUENCY

At times it may be useful to reduce the switching frequency of an Apex Precision Power PWM amplifier. In some amplifiers, this is possible with the addition of an external capacitor and a clock signal of the desired frequency. The Operating Considerations discussion in the datasheet will indicate if this is possible. The clock signal should be connected to the CLK IN input pin and should swing from GND to V_{CC}. The properly sized external capacitor connected between the -PWM/RAMP pin and ground will return the peak to peak ramp voltage to the datasheet specifications.

The exponential charge and discharge of the capacitor in the R-C network determine the clock frequency. However, only a simple ratio is required to calculate the size of the external capacitor for the new switching frequency. Note that the tolerance of the natural switching frequency is ±2%.

$F_{SW(natural)} \bullet C_{(internal)} = F_{SW(desired)} \bullet C_{(total)}$

So,

$C_{(external)} = ((F_{SW(natural)} \bullet C_{(internal)}) / F_{SW(desired)}) - C_{(internal)}$

SA14 Example:

Desired switching frequency = 10kHz

Natural switching frequency = 22.5kHz

Internal Capacitor = 470pF

Solving for C:

Total C = 1058pF

588pF required externally.

560pF is the closest standard value and corresponds to a switching frequency of 10.27kHz. If you insert a 10kHz clock signal, the peak to peak ramp voltage will vary slightly from the datasheet, but the center voltage will not change. Non-linearity will result if the ramp voltages are extended far beyond the datasheet specifications.

5.0 DESIGNING WITH PWMS

PWM amplifiers are high power switching devices whose voltage and current slew rates often surpass those found in either digital or analog circuits. Even though signal bandwidth may not top 1KHz, adopting the viewpoint of an RF designer can be very wise. Here are a few useful things to keep in mind:

** Wire inductance @ 20nH per inch

** Inductor voltage = dI/dt • L

** Capacitor current = dV/dt • C

** A good square wave = very large harmonic content

5.1 POWER SUPPLY BYPASS

It is difficult to over emphasize this aspect of the PWM design. Most of us are familiar with the good design practice of including a supply bypass capacitor at every IC in a low level logic design. If this is not done, the high switching rates cause problems on the power bus. As the most common fault in switching circuit design, inadequate bypass causes ripple and spikes on the supply line which make circuits inoperative and can even destroy components. Careful attention to location, size, ESR and ripple current capacity can result in a good design.

Power supply bypassing is a wideband job requiring at least two components for satisfactory operation of the amplifier. Use at least 10µF per ampere of load current to bypass the lower frequencies. Some applications appear to require many times this amount of capacitance. Capacitors with lower ESR ratings may ease the burden of finding space for such large devices. Locate this capacitor within a few inches of the amplifier. The high frequency bypass is absolutely critical! Think of frequencies in the 1 to 10Mhz range. Remember that many capacitors appear inductive in this range. Use ceramic capacitor(s) totaling 1µF to 10µF. Type X7R is recommended to ensure low ESR and ESL. Connect these capacitors directly between the supply and ground pins of the amplifier minimizing trace length, i.e. trace inductance. To illustrate the importance of this, consider a design having 3" between the supply pin and the ground point that terminates the capacitor: At 20nH per inch of parasitic trace inductance, the supply pin can have spikes equal to the supply voltage! When this happens, signal integrity is in question and peak voltages applied to components may be twice expected values. Connect the capacitor right at the amplifier pin.

The function of bypass capacitors is to satisfy AC current demands of the amplifier, which is isolated from the power

supply by the inductance of the very same line that connects them. The degree of isolation increases with current magnitude, frequency and distance. When this isolation prevents current flow to the power supply, it must come from the bypass capacitors. Attempting to calculate capacitor currents is a questionable investment but ignoring them is no solution. Keep the requirement in mind when selecting components and follow up with temperature measurements on the prototype. Run the system at maximum frequency and power until temperatures stabilize. During this process, keep in mind that under-rated capacitors can explode.

5.2 HOW MUCH INDUCTANCE?

PWM amplifiers driving resistive loads with no filtering are unable to modulate the output voltage, they can only switch polarity. Loads with small amounts of inductance may over heat with high ripple current even with a 50% duty cycle (zero output) drive. Other types of loads may suffer performance degradation if ripple currents exceed 1% or even 0.1% of the full-scale current. Once a design limit on peak-to-peak ripple current has been set, calculate minimum total inductance. It is proportional to supply voltage and inversely proportional to I_{P-P} and switching frequency:

$$L = V_S/(2 \bullet F \bullet I)$$

where V_S is the supply voltage and F is the switching frequency. As an example, this means the SA01 (switching at 42Khz) on 100V needs 300mH to keep ripple current down to $4A_{P-P}$.

5.3 GROUND CONCERNS AND LAYOUT CONSIDERATIONS

The circuit layout allows little room for compromise because the PWM amplifier combines both high-speed switching of large current and small-signal analog levels in one circuit. Though challenging, successful PBC layouts are not unreachable with some effort and care. However, some ordinary layout techniques and practices (including those used by auto-routing software) often cause major problems in switching applications, so be sure not to violate the following rules.

1) Power supply bypass. Connect all capacitors directly to the power-supply pins keeping trace/lead length as short as possible. Use ceramic capacitors for the high frequency content. Review the previous bypass discussion for more details.
2) Star ground. Make all ground connections in a star pattern with the ground pin of the amplifier at the center of the star. The dI/dt produced by switching circuits can produce substantial voltages over even short conductors that may interfere with low-level analog signals.
3) Separate small signal and power grounds. Connect your small signal ground the power ground star at only one point - the center of the star. If your circuit uses low level logic as well as small signal analog and high current PWM devices, keep these three grounds separate, connecting only at the center of the star.
   Improper grounding can allow switching noise to enter the small signal analog channels disrupting the control of the signal. Using the star ground technique will ensure that high currents in one ground path do not induce voltages at other ground points. This is the only way to guarantee that the ground reference is clean and stable at all important points.
4) Avoid capacitively coupled feedback. Parasitic capacitance between traces or layers can couple unintended feedback from the output to the input section of the amplifier. With PWM outputs switching hundreds of volts in a few nanoseconds, it is not difficult to calculate what a few pF of parasitic coupling might do in the circuit.
5) Keep small signal traces away from outputs. High current outputs can magnetically couple to the small signal sections of your circuit. Never, ever, consider running small signal traces between the output pins.
6) Keep ground plane current to a minimum. If you are convinced that you must have a ground plane, do not under any circumstances connect high current return lines to it.
7) Keep traces to and from current limit resistors as short as possible. The current limit threshold voltage on most Apex Precision Power PWM amplifiers is 100mV. Fast rise times in the current limit resistors and parasitic inductance can cause false current limiting or confuse the control logic in the device. This particular bit of the layout can cause high levels of hair loss if the proper attention is not given.

5.4 IS THE SCOPE TELLING THE TRUTH?

Could be, but touching the probe tip to the ground clip may reveal otherwise. If the scope shows a waveform with this "grounded" input, or all high impedance nodes appear to have spikes that they should not, there are at least three possible sources of error. The amplifier local ground may be quite different from the local ground seen by the scope's input amplifiers and their common mode rejection is less than perfect. First, disconnect all other signal cables from the scope to remove interaction with any other local grounds. If a battery-operated scope is available give it a try. If not, install a ground breaker on the scope power cord.

Use only shielded probes, and do not use any extenders, grabbers, or clips which do not have nearly complete shielding. Capacitive coupling into high impedance nodes works best when voltage slew rate is high and these switching amplifiers have plenty to get in trouble.

That 3" to 6" ground lead may have to go. It is forming an inductive pickup loop and the PWM is moving lots of high frequency current. If luck holds, the scope accessory kit will yield an RF adapter capable of providing a ground lead less than 1/4" long. If not, consider buying one or making your own from a length of spring wire.

5.5 INTERNAL POWER DISSIPATION

PWM amplifiers share the following thermal principles with their linear counterparts.

- Quiescent current and supply voltage determines standby power.
- Driving the load generates additional heat.
- The heatsink must dissipate both the above.
- The case temperature range must not be exceeded.
- Load related power elevates power transistor junctions above case temperature.
- Maximum junction temperatures must be observed.
- Lower temperatures (case and junction) increase reliability.

There are two major differences in the thermal aspects of linear power amplifiers and PWM amplifiers. First, power in the PWM amplifier due to loading can be calculated without knowing the output voltage or the supply voltage. The second difference is subtle but affects the very reason a PWM amplifier is used: Efficiency drops rapidly as junction temperature increases. This means heatsinking the PWM is more than a reliability issue. Thermal design of the PWM amplifier has a first order affect on circuit performance.

First order calculation of power due to loading involves the output current and the total ON resistance of the amplifier. The high-speed waveforms present at the output pins do indicate second order calculations could be made but this document will concentrate only on the basic elements of power dissipation.

Total On resistance includes impedance of the H-bridge power switches (most often FETs) plus resistance of the metal interconnects. Consult the amplifier data sheet to find the contribution of each element. If interconnect resistance is not specified, consider it to be insignificant. Consider interconnect resistance to be constant over temperature. Because FET ON resistance is a function of temperature, choose a maximum junction temperature consistent with your design standards (not to exceed the data sheet absolute maximum). Find FET ON resistance(s) at your maximum junction temperature. $I^2 \bullet R$ now yields power due to loading. This is a single calculation on lower current amplifiers using all N-channel FETs, but requires another calculation if P-channel FETs are used and a third if interconnect resistance is broken out separately. Sum the above calculations with standby power to obtain total heat loading on the heatsink. If the amplifier has a separate low voltage supply pin, don't forget to include it in the total power calculation.

With total internal power dissipation now known, it is time to determine the heatsink requirement. Again, consistent with your design standards, choose a maximum case temperature. Do not exceed the product operating temperature range listed on the last line of the specifications table. $R_{\Theta CS}$ is the thermal resistance of the package to heatsink interface.

$$R_{\Theta SA} \leq \frac{T_C \text{ max} - T_A \text{ max}}{\text{Total Power}} - R_{\Theta CS}$$

The last item to check is the junction temperature. Multiply power in a single FET by the thermal resistance of the amplifier and add to the maximum case temperature. In models that have higher P-channel on resistance use the P-channel power level and realize the N-channel devices will run cooler. An alternative to finding the specific junction temperature is to find the appropriate fraction of total power and then use the power derating graph to make sure junctions do not exceed 150°C.

As an example consider an SA01 delivering up to 10A from a supply of 70V in a maximum ambient of 35°C. Design rules allow case and junction temperatures up to data sheet maximums.

- Standby power = 70V • 90mA = 6.3W
- N-channel power = $10A^2 \bullet .145\Omega$ = 14.5W
- P-channel power = $10A^2 \bullet .26\Omega$ = 26W
- Interconnect power = $10A^2 \bullet .05\Omega$ = 5W
- Total power = 51.8W
- Maximum case rise = 85°C - 35°C = 50°C
- Allow .02°C/W for case to heatsink thermal resistance
- Heatsink maximum rating = 50°C/51.8W - .02°C/W = .95°C/W
- Junction temperature = 85°C + 26W • 1°C/W = 111°C

This example would actually run cooler than the above calculations would seem to indicate because junction temperatures are lower than the assumed starting point and FET ON resistance is lower. An iteration of the above based on an assumed maximum junction of 110°C would yield a heatsink rating of 1.1°C/W and result in maximum junction temperatures of 106°C. This will still have a small safety margin because the N-channel junctions run cooler than the P-channel junctions.

It is interesting to note that heatsinking will not only protect the amplifier from thermal problems, but it will also increase the efficiency of the amplifier by maintaining low on resistance. At lower temperatures, the FET ON resistance is lower and there is less dissipation. Essentially, using a larger heatsink will increase efficiency as well as protect the devices.

6.0 PWM TRANSFER FUNCTION

The transfer function of an op amp circuit is simple: $V_{OUT} = V_{IN} \bullet$ gain. With the high PSRR of most op amps, supply voltage variations are largely ignored. Thermal effects are mostly second order, and changes in the load have little affect on the output voltage. Of course, op amps are almost always run closed loop.

PWMs can offer similar performance in a closed loop system. How to close the loop is a topic for another discussion, but it is important to understand how a PWM system behaves open loop. PWM amplifiers are affected by a variety of influences that rarely come into the picture in a linear design, or they are present in a much more subtle way than with PWMs. Hopefully, this discussion impresses the importance of closing the loop in most PWM systems.

The transfer function of a PWM amplifier is stated as follows:

$$V_O=(((V_{MID}-V_{IN})/V_{PK})\bullet V_S)-(I_{OUT}\bullet R_{ON})$$

Where:
V_O = output voltage (averaged over time, i.e., filtered)
V_{MID} = midpoint of the ramp signal
V_{PK} = + of the ramp p-p voltage
V_{IN} = input voltage
V_S = supply voltage
I_O = output current
R_{ON} = total on resistance (1 switch if 1/2 bridge, 2 switches if full bridge)

The equation above relates the output voltage (averaged over time) to the input voltage, the ramp signal, and the losses of the switches. There are several things to notice from the equation above.

** There is no supply line regulation. As the power supply varies, so does the output voltage.
** There is poor load regulation. As the load changes, so will the output current, and the output voltage will vary by $I_O \bullet R_{ON}$
** The PWM amplifier is temperature sensitive. As discussed in the previous section, the ON resistance changes with temperature. Since R_{ON} is a factor in the output voltage, this must be dealt with.

So, it is easy to see that open loop operation of a PWM amplifier is far from a precise endeavor. Closing the loop locally around the PWM amplifier or using system feedback to close the whole system are equally valid. It is sometimes easier, but far from trivial to close the loop locally around the PWM amplifier. This can eliminate all of the effects of the sources mentioned above - and others that have not been mentioned. Application note 41 discusses several methods for analog closed loop solutions and how to use the PowerDesign spreadsheet to aid in the design process.

7.0 DIGITAL INTERFACE TECHNIQUES

Apex Precision Power PWM Amplifiers are analog products by design. Most of the previous discussion has assumed that

the input signal is analog and a comparison is made to a triangle ramp reference to generate the PWM signal. But, with a few exceptions, Apex Precision Power PWM amplifiers can also be driven with digital input signals. The following discussion explains how to interface an Apex Precision Power PWM amplifier with a digital signal from a DSP or microcontroller.

Most Apex Precision Power PWM amplifiers have 2 inputs, PWM+ and PWM-/RAMP. To control the amplifier digitally, apply the logic signal to PWM+. For the input signal to be processed properly the PWM-/RAMP pin must be biased to 1/2 of the logic level. For example, for 5V logic signal, bias PWM-/RAMP to 2.5V. The exact voltage of the bias is not critical as the two inputs go directly into a comparator, however it is very important to use a low impedance reference. The PWM-/RAMP pin has an internally generated triangle ramp signal that must be overcome sufficiently that the comparator can operate properly.

There may be a temptation to disable the internally generated clock signal when using digital control. After all, if the DSP or microcontroller is generating the PWM frequency, there is no obvious reason for the internal clock. There is however, a not-so-obvious reason to keep the CLK IN pin connected. For amplifiers with current limit circuitry, a low-side current limit activation is reset once every clock cycle. If there is no signal at CLK IN then any signal on the current limit pin that activates the low-side current limit will shut down the amplifier outputs until power is cycled.

7.1 SPEED KILLS

In most cases, the natural internal clock frequency of an Apex Precision Power PWM is balanced to provide reasonable efficiency while maintaining reasonable bandwidth. There are cases that require more bandwidth than the natural internal clock frequency will allow. By driving the PWM digitally, you can extend the usable bandwidth. If digital control is approached without caution, however, the consequences can range from undesirable to devastating.

Really fast switching speeds can be dangerous. As input cycle time approaches the rise time of the output drive signal there is a real potential for destruction of the amplifier as well as surrounding components and the load. The controlling circuit inside the amplifier simply becomes overwhelmed and confused when the input changes more quickly than the output can follow.

Always observe the following rules when selecting a PWM frequency:

1) Never increase the switching frequency more than twice the internal PWM frequency of the amplifier given in the datasheet.
2) Never apply any pulse shorter than 3% of the natural PWM period of the amplifier.

8.0 TYPICAL APPLICATIONS

The following are a few example design discussions. In most cases, the actual amplifier model is not important and almost any model could be used in the same circuit topology. However, there may be design considerations mentioned that are specific to a supply voltage issue or PWM frequency issue.

8.1 MOTOR SPEED CONTROL

The design steps of the PWM speed control employing a tachometer feedback shown in Figure 8 are as follows: The 7.5V reference output is used to bias the non-inverting input of the error amplifier to the middle of its 2V to 8V common

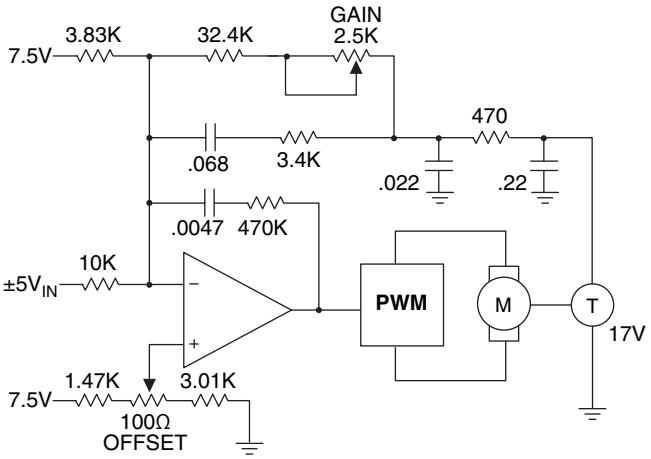


FIGURE 8. PWM SPEED CONTROL

mode voltage range. The gain adjust potentiometer corrects initial inaccuracies stemming from error amplifier voltage offset, tolerance of the 3.83KΩ bias resistor in the inverting input and possibly even for offsets in the input signal. The 470Ω resistor and the two associated capacitors form a low pass filter to attenuate components of the switching frequency which may be coupled to the tachometer through the motor. The gain adjust potentiometer compensates tachometer variables of accuracy and internal resistance plus tolerances of other resistors in the feed back path. The 10KΩ input resistor sets overall gain to 3.4. The 3.83KΩ resistor was selected to pull the inverting input of the error amplifier up to 5V when both the input voltage and tachometer output voltage are zero. The two R-C networks were selected to provide circuit stability while maximizing system response time. Specific values will depend on both motor parameters and mechanical load characteristics.

8.1 MOTOR POSITION CONTROL

While one of the simplest forms of position sensing is shown in Figure 9, options such as optical encoders, LVDT sensors and variable capacitance transducers are also viable. Again, error amplifier inputs are biased to 5V. While 20KΩ input and feedback resistors would have set proper gain and biasing for the inverting input, they would have allowed common mode violations at the error amplifier. This could happen if the system was at one position extreme while a very quick command came in to travel to the opposite extreme. The three 30KΩ resistors

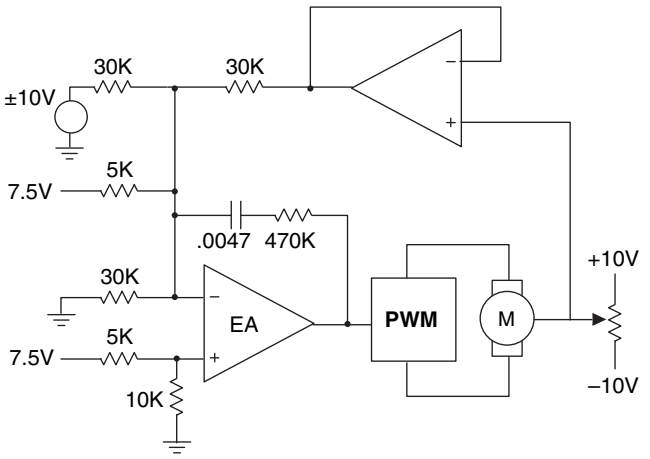


FIGURE 9. PWM POSITION CONTROL

prevent common mode problems by increasing impedance from summing junction to the two 10V signal levels at the output and at the input while adding an impedance to ground.

8.2 COMMON VOLTAGE FEEDBACK CIRCUIT

Figure 10 shows a differential input, voltage controlled output circuit resembling the familiar differential op amp configuration. The SA01 includes the error amplifier within the package so the circuit can really be quite minimal. Signal gain is 2•RF/RI. Again, two pull-up resistors are used to bias error amplifier inputs within the common mode range. Select this value to get 5V bias when both inputs are zero and both outputs are 1/2 the supply voltage (50/50 duty cycle.) At zero drive to the load, this differential stage is rejecting 1/2 the supply voltage present on both outputs. This means resistor ratio matching becomes critical. It should also be noted that even though the signal gain is 20, the gain of offset errors is 50 because the effective input resistance is the parallel combination of the signal input resistor and the pull-up resistor.

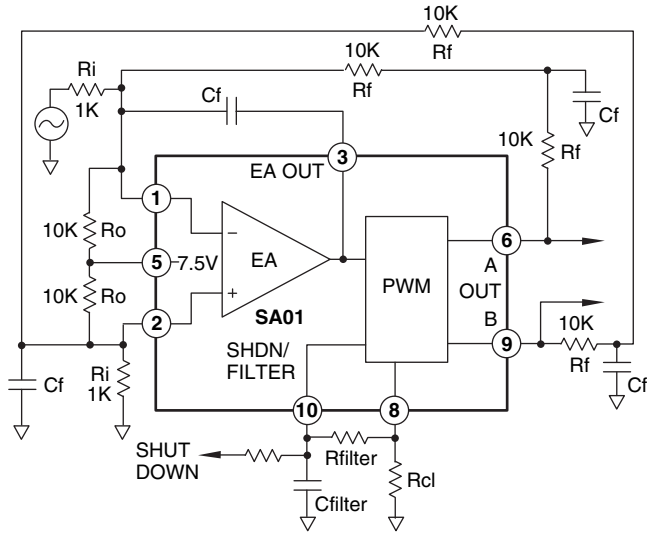


FIGURE 10. VOLTAGE FEEDBACK - SA01

8.3 PROGRAMMABLE CURRENT SOURCE - DIGITAL

Figure 11 shows a digital implementation of a programmable current source. Only a half bridge is required for this single sided current source. In a half bridge, the current sense resistor (R_{SENSE}) must be in series with the load to sense source and sink currents. An instrumentation amplifier with a high common-mode voltage range senses the voltage across the sense resistor and feeds the information back to the controller.

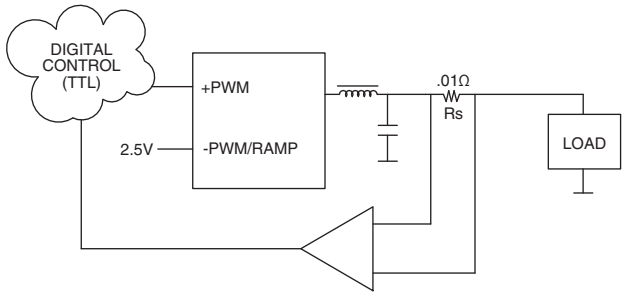


FIGURE 11. DIGITALLY CONTROLLED PROGRAMMABLE CURRENT SOURCE

9.0 CONCLUSION

The switching amplifier provides a solution to high power drives that could otherwise require an inordinate amount of heat sinking hardware. The arrival of the hybrid PWM speeds the design process and in many cases greatly enhances fault tolerance by offering protection circuits simply not possible in a discrete implementation.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Operational Amplifier Basics

HISTORY

The performance and shape of operational amplifiers has changed considerably since the vacuum tube units were produced by George Philbrick, and others, over three decades ago. Discrete transistor-circuit op amps were the main catalog item for companies like Burr-Brown Research Corp. and Analog Devices. The monolithic age of high-production-volume op amps began with the uA709 from Fairchild. Modern op amps have taken on many signal processing challenges. The Apex Precision Power family has been specialized for high power and high voltage. Whatever the specialty or construction technique, the underlying theory remains the same.

IDEAL MODEL

An ideal operational amplifier (modeled in Figure 1) is a voltage controlled voltage source. The input sense pins have infinite impedance to ground and to each other. The output source has a zero output impedance and the transfer constant (Open-loop Gain, A_{ol}) approaches infinity. This unit, simply placed in a system, would be of little use in a linear mode without the benefits of closed loop control in the form of negative feedback.

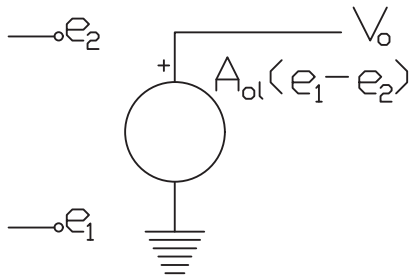


FIGURE 1. ELEMENTARY MODEL OF AN OPERATIONAL AMPLIFIER.

FEEDBACK CONTROL

Consider the circuit in Figure 2. For this first example, the op amp is placed in an inverting configuration with input resistor R_i and feedback resistor R_f. Since the op amp input impedance is infinite, all current flowing through R_i must flow through R_f.

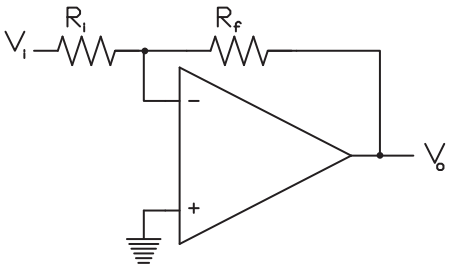


FIGURE 2. BASIC INVERTING CONFIGURATION.

If one writes the equations for current flow from V_i to V_o and solves for the V_i to V_o ratio the result is:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

Where: A_{ol} approaches infinity.

The operational amplifier has now been converted into a linear circuit element with significant possible extensions.

It is important to notice that the inverting input of the op amp (junction of R_i and R_f) is maintained very near to the potential of the non-inverting input. This point is a "summing junction" and is called a virtual ground. The op amp output is adjusting to maintain this relationship. This fact gives rise to two significant extensions. The input impedance is constant at the value of R_i and it is possible to have multiple inputs which are summed at the output. Each input may have a different gain associated with it as shown in Figure 3.

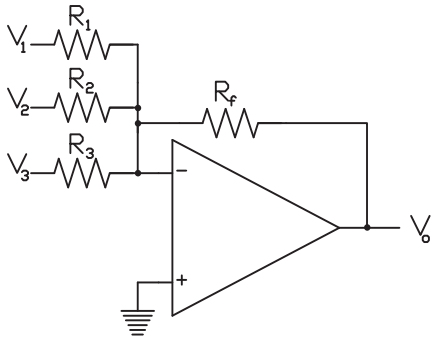


FIGURE 3. SUMMING AMPLIFIER CONNECTION.

The output of this configuration is given by the expression:

$$V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

Our discussion up to here has ignored the non-inverting input. Write the current summation equations for the circuit in Figure 4 and solve for V_o in terms of V_i as above. With A_{ol} approaching infinity, the following relationship results.

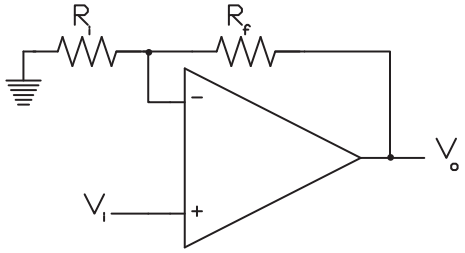


FIGURE 4. NON-INVERTING CONFIGURATION.

This circuit has the features that the output signal is not inverted as it is amplified, the input impedance approaches infinity, and the gain can not be less than unity.

$$V_o = V_i\left(1 + \frac{R_f}{R_i}\right)$$

By combining the inverting and non-inverting circuits it is possible to make a full, weighted sum and difference system element as shown in Figure 5.

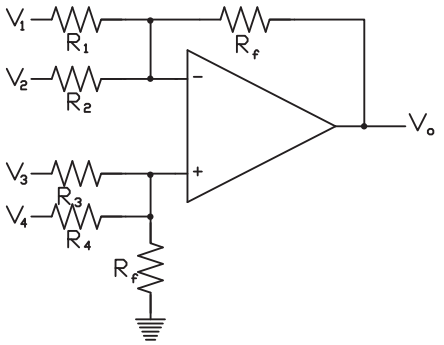


FIGURE 5. SUM AND DIFFERENCE AMPLIFIER.

Through the use of super-position the sum and difference amplifier can be analyzed. The accuracy of this relationship depends on the matching accuracy of the two resistors labeled R_f. The complete transfer function is given by:

$$V_o = R_f\left(-\frac{V_1}{R_1}-\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_4}{R_4}\right)$$

NON-IDEAL OP AMPS

All of the discussion to this point has assumed an ideal device. With real world op amps there are deviations from the ideal, or errors. The magnitude of some of the possible errors for an op amp are listed in the specification sheet for that device. A description of the circuits used to measure these parameters can be found in the section titled "Parameter Definitions & Test Methods".

When the magnitude of the error, as seen at the output, is a direct function of the closed loop gain that error magnitude is specified referred to the input (RTI). The maximum error to be expected at the output is the error value times the non-inverting gain of the amplifier. The most common of these errors is initial voltage offset.

Recall that the op amp works because the negative feedback brings the inverting input to equal the non-inverting input. When connected as a non-inverting amplifier both inputs will be at a potential equal to the input signal. Since this input is common to both inputs it is called the "Common Mode Voltage". In an ideal amplifier the common mode signal would be subtracted out and not appear at the output. Due to limitations imposed by the real world circuits there is an error signal at the output which is a function of the common mode voltage. A limit exists on the range of the common mode voltage that the op amp can withstand.

POWER SUPPLY SYMMETRY

To this point we have not considered the power supply configuration. When op amps are furnished symmetric power supplies common mode voltage limits are easy to meet. It is generally possible to operate from a single supply if the common mode voltage limits are honored. For further extensions on single supply operation Application Note 21 should be studied.

AC CONSIDERATIONS

All of the relationships discussed above can be extended to the AC domain by replacing resistance with impedance and allowing for the finite frequency response of the op amp. If a plot is made of open loop gain vs frequency it would look similar to Figure 6. This graphic display is used to describe the op amp's open loop performance as a function of frequency and to predict stability.

The two change of slope points in the response curve are caused by the existence of poles in the transfer function of the op amp. Most op amps have Bode plots very similar to that shown in Figure 6. The slope of the trace between 10 Hz and 1 MHz is -20 dB per frequency decade. Extensive discussions of stability are presented in Application Note 19 and others. In the opening discussion we assumed the op amp gain to approach infinity. The difference between the open loop gain of the op amp and the closed loop gain, set by the feed-back network, is referred to as excess loop gain. As the excess loop gain decreases the op amp circuit deviates more from the ideal. Consider the op amp of Figure 6 if it were used in a closed loop gain configuration of 20 dB (X10) as shown by the dashed line. At low frequencies the excess loop gain is 80 dB. As the frequency is increased the excess loop gain decreases until it reaches zero dB at 100 KHz. The performance of the circuit would be very near ideal at low frequencies and deviate more from ideal as the frequency approached 100 KHz. If the closed loop gain was increased to 40dB(X100). The non-ideal response would become apparent one frequency decade earlier.

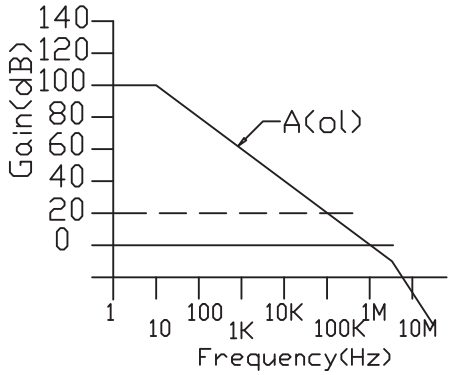


FIGURE 6. TYPICAL BODE PLOT.

CONCLUSION

Some of the basic features of operational amplifier circuits have been discussed here. The concept of negative feedback and the graphical representation of the Bode plot are the most common tools used in op amp circuit design. The application notes that follow present techniques for solving many of the problems which arise in the use of op amps.

PWM Low Pass Filtering

1.0 INTRODUCTION

Pulse width modulation (PWM) amplifiers require low pass filtering of the output to demodulate the PWM carrier. Some applications also utilize the filter as a way to achieve an impedance transformation which draws less power supply current than is delivered to the load. These filters can be as simple as a single inductor, to multiple LC nodes depending on the application. In some applications the load will have enough inductance to act as its own filter. Deciding on the type and size of a filter can be time consuming since the calculations can be tedious and often give component values that are not easily obtainable. This application note is an effort to reduce filter calculation time. Using the Apex Precision Power Power Design tool, available at www.Cirrus.com. will further reduce time. Power Design.exe is a self-extracting Excel97 spreadsheet and will be used extensively in this application note.

2.0 FILTER TYPES

PWM filters are normally a low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 Hertz to the frequency of cutoff (F_C). This low attenuation region is called the pass band. Beyond the F_C, attenuation increases at a rate determined by the filter type and the number of poles (order). Figure 1 indicates the general response of the low pass filter.

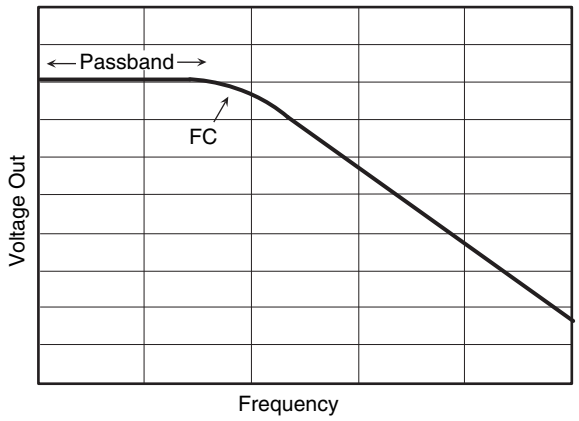


FIGURE 1. LOW PASS FILTER RESPONSE

Many different types of low pass filters exist. Each has favorable and unfavorable traits and the selection usually is a compromise of performance in one area to achieve desired performance in another area. Some characterizations are: pass band flatness, rate of attenuation, and phase shift versus frequency. Common filters include Butterworth, Chebyshev, and Bessel.

The Butterworth filter has a flat response in the pass band and good roll off beyond the cutoff frequency. Component variations do not greatly affect the performance. It is considered a good general filter that is often used and therefore will only be considered here.

3.0 INITIAL CONSIDERATIONS

If you are unfamiliar with Apex Precision Power PWM amplifiers or with locked anti-phase modulation, please refer to Application Note 30. This should convince you that using unfiltered PWM outputs is useless for some loads (applies only full supply voltage) and can often be destructive to the load or the amplifier. Filter design requires trading off many variables. Here are some things to consider:

1. This filter design technique assumes amplifier output impedance is low compared to the load impedance and that the combined impedance of the load plus matching network is constant over frequency. The demand for circuit efficiency will insure the impedance relationship requirement is met. Beware that changing load element values, without corresponding matching network value changes, will alter the filter response curve. With some loads, such as solenoids or valves that tend to change inductance with position, the textbook response curve is nearly impossible to achieve. In these cases, try designing for the highest impedance, and then check performance driving the lower impedance.
2. As shown in Figure 2, a full bridge PWM amplifier driving a first order (single pole) filter with F_C set at 1/10, the switching frequency will be required to deliver approximately 15% of the peak output current as peak ripple current. The ripple is at the switching frequency; measured when the modulation level is 50%; and assumes peak output current equals Vs/R_L. Figure 2 also indicates that changing to a second or higher order filter will drop this to almost 10%. A second and even more effective way to reduce this ripple current is to widen the ratio between signal and switching frequencies. As switching frequencies of Apex Precision Power PWM amplifiers range from 22.5KHz to 500KHz, this technique has obvious limits

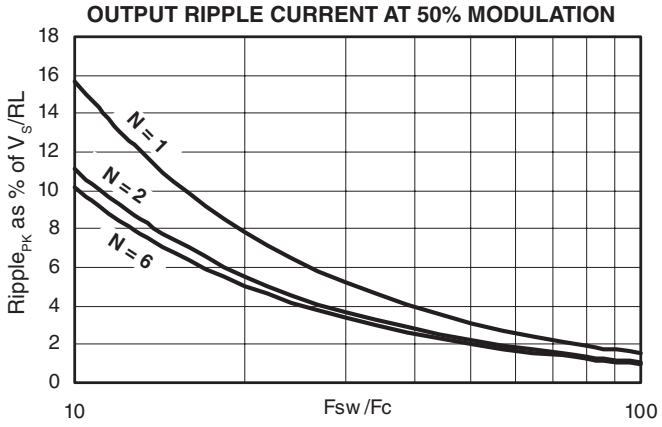


FIGURE 2. OUTPUT RIPPLE CURRENT VARIES WITH ORDER AND RATIO OF SWITCHING TO SIGNAL FREQUENCY

2.1 This ripple current flows through the first inductor of the filter, meaning high frequency core loss is of concern. With first order filters driving resistive loads, it also flows through the load. With higher order filters, most of the ripple current flows in the first filter capacitor, affecting the ripple capacity rating of these components.

2.2 In applications where full modulation is expected (output current is expected to approach V_S/R_L), the workload imposed on the amplifier by delivering the ripple current is of minor concern. While 15% (or less as shown in Figure 2) of maxi-

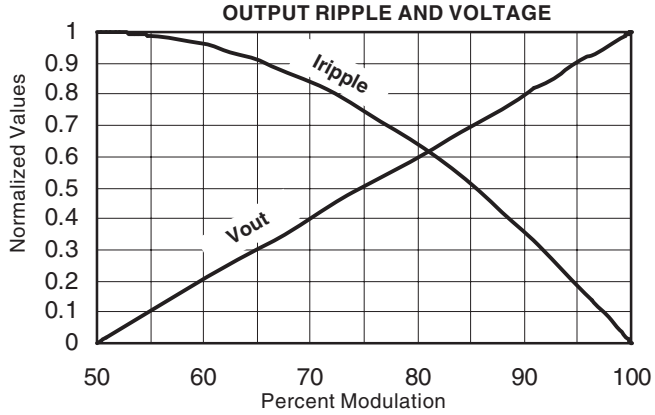


FIGURE 3. RIPPLE CURRENT AND OUTPUT VOLTAGE IN THE FULL BRIDGE

mum output may seem more than minor, Figure 3 shows this ripple current decreases as modulation percentage moves away from 50% (a graph of zero to 50% would produce a mirror image curve) In other words, heatsink size is not increased 15% because maximum DC output and maximum ripple output never occur at the same time. The heatsink will be sized to handle the much larger output current. The ripple current curve of Figure 3 is also valid for half bridge circuits, but the Vout curve would need to be re-scaled from 0.5 at 50% modulation to 1 at 100%.

2.3 For applications spending a major portion of the time near the 50% modulation level, the ripple current will be quite noticeable in terms of lowered efficiency (power supply loading and heatsink temperature). These circuits include full bridges spending most of their time delivering small signals compared to peak output capability; full bridges whose peak output voltage is considerably less than supply voltage; and half bridges spending most of their time delivering half the supply voltage.

3. Filter attenuation at 100% of cutoff frequency is 3db, that is, a factor of 0.707 for voltage output (and consequentially, current) and 0.5 for power output. Refer to Figures 4 and 5 for more data on attenuation as signal frequency approaches cutoff frequency. Designing the cutoff frequency at least twice the actual maximum signal frequency is a very common technique to obtain a flatter response in the portion of the pass band actually used.

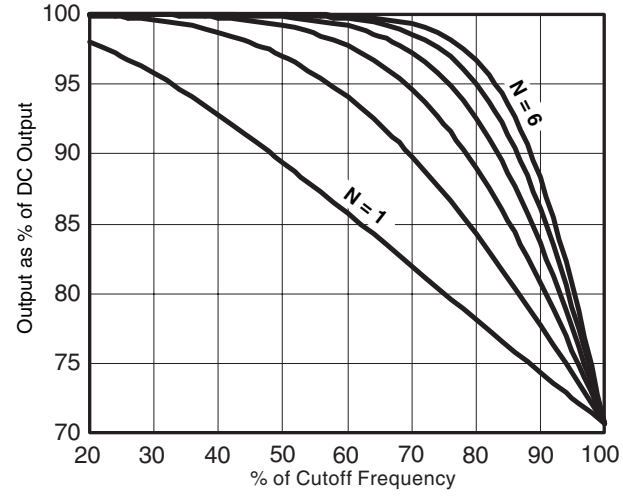


FIGURE 4. REDUCED V & I AS FSIGNAL APPROACHES Fc

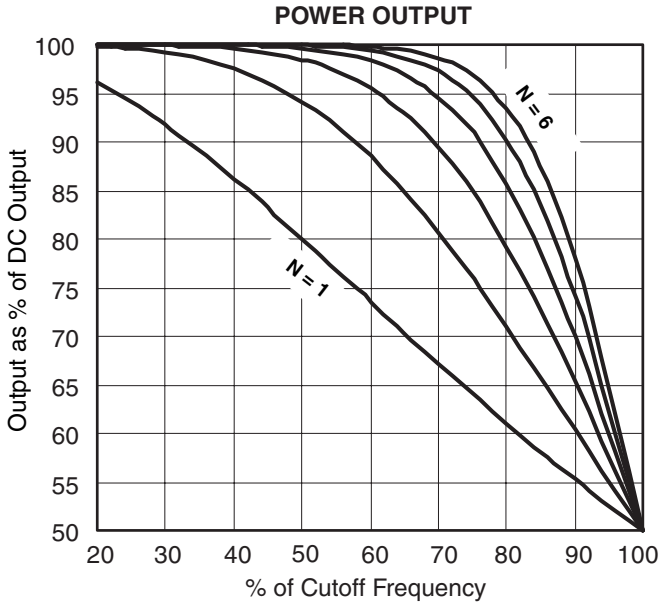


FIGURE 5. REDUCED POWER AS FSIGNAL APPROACHES FC

4. With supply voltage and desired maximum ripple voltage at the load held constant, a larger ratio between signal frequency and switching frequency will lower the number of filter poles required. This will lower cost, weight and size. For example, starting with a 10:1 ratio requiring a 4 pole filter; changing to 21.4:1 brings N down to 3; and changing to 100:1 yields N=2.

5. In the design of servo loops or any other application where feedback is taken at the filter output or beyond, phase shift of the filter is critical to stability of the overall loop. With properly terminated filters, phase shift at the cutoff frequency will be 45° per pole and the shift will decrease in a linear fashion at lower frequencies. Power Design will calculate voltage and current phase shift at the load for all cases, but first and second order filters are likely to be the maximum acceptable. In fact, many designs use no dedicated filter components, but instead rely on load inductance and resistance to form a first order filter. The important point to check is how this inductance reacts to square waves of the switching frequency.

6. When using second and higher order filters, impedance

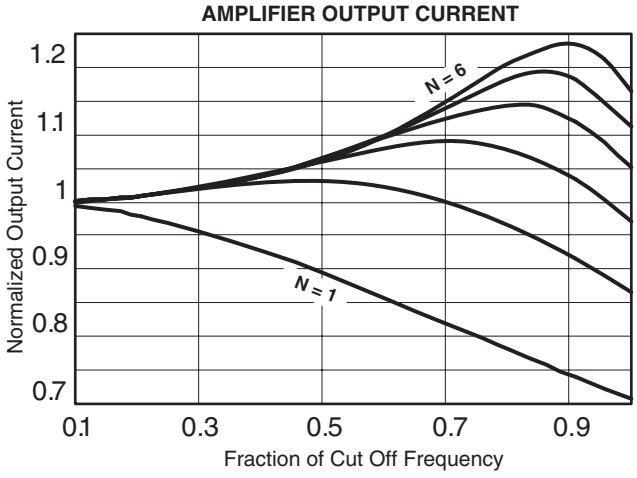


FIGURE 6. AMPLIFIER OUTPUT CURRENT CAN BE MORE THAN EXPECTED

presented to the PWM amplifier will dip below the load impedance as signal frequency approaches F_C. Figure 6 shows this in reciprocal form. Putting some numbers to go with the worst point: N=6, F_C=1KHz, F_{SIGNAL}=900Hz, I_{LOAD}=10A, amplifier output=12.3A. This "extra" current flows in the output devices of the PWM amplifier increasing internal power, increasing ON resistance, increasing junction temperatures and reducing efficiency. This effect should be considered also with regard to amplifier and power supply current ratings and design of current limit circuits. We will see what looks almost like a duplicate of this graph when discussing filter component stress levels.

Figure 7 shows efficiency data for a perfect component filter (no parasitics) designed for an SA03 running maximum output voltage into a 10Ω load while mounted on a 0.1°C/W heatsink. At 10% of F_C, about 3.3% is lost in the amplifier and the filter is having very little affect on efficiency. As signal frequency increases, three effects combine to bring high frequency efficiency down further. First, quiescent power remains constant even though the output signal is rolled off. Secondly, the peaking output current demanded by second and higher order filters increases internal PWM losses. The last item is the positive non-linear temperature coefficient of the ON resistance of the PWM, which increased about 1% in this example. The point here is that filter choices can double efficiency loss even before allowing for filter component loss. Importance of this data varies with the spectral content of the signal being amplified. Consider an audio application versus a fixed 400Hz inverter application.

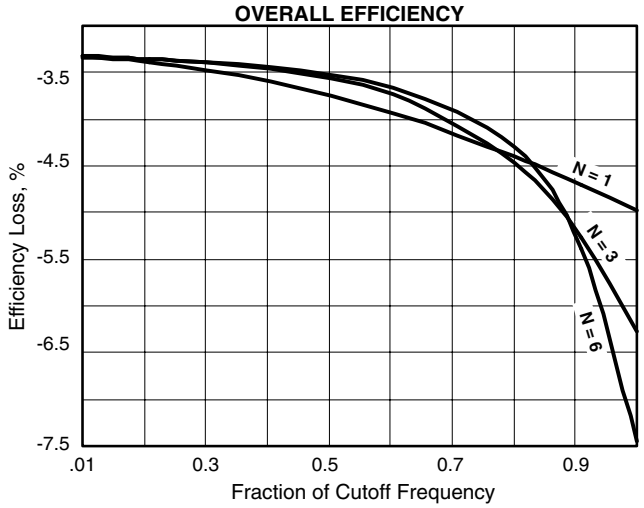


FIGURE 7. EVEN A THEORETICAL FILTER CAUSES REAL POWER LOSS

Desired attenuation of the PWM square wave output must be known to establish the order of the filter. While standard filter equations assume sine wave inputs, the PWM applies square waves at the switching frequency. Artificially increasing the bridge supply voltage by 25% approximates a correction factor for this. A non-integer value of this requirement is given in the following equation:

$$N \frac{\frac{A}{10}}{2 \bullet \mathrm{LOG}\left[\frac{F_X}{F_C}\right]}$$

Where:

A (in db) = 20 log (bridge supply voltage * 1.25/load peak ripple voltage)

F_X = frequency of the desired attenuation (usually the switching frequency)

F_C = filter cutoff frequency

N is rounded up to the next integer

Note that ripple voltage on the load is a differential specification. With a full bridge circuit, it is not the voltage seen at either load terminal with respect to ground.

4.0 FILTER TABLES

Filter analysis begins by developing general mathematical equations to describe the filters. Each filter equation can be reduced to a set of coefficients.

Filter coefficient tables are usually in a normalized form. Normalized coefficients are calculated at a frequency of 1 radian per second and an impedance of 1 ohm. This is done for convenience so the designer does not have to calculate coefficients for every case. The normalized coefficients require the designer only to scale the frequencies and impedances to fit the particular requirement.

The filters most designers are familiar with are the symmetrical load type. These assume equal terminations on both ends of the filter. These configurations will generally not work here because the output impedance of the amplifier bridge is usually low and the actual load usually will be much higher. Apex Precision Power PWM amplifiers have room temperature output impedances from less than 0.1 ohm to about 1 ohm and are mostly resistive. The filter tables here assume a very low source impedance and a higher impedance load.

The coefficient table also assumes zero loss components; therefore, real components will compromise results.

Filter orders up to 6 are given which is more than what is usually needed. Beyond order 5 or 6, the point of diminishing returns begins as losses in the filter components, parasitics of the physical layout, and undesired coupling eat up all the theoretical advantages of additional poles.

The single-ended filter configuration is shown in Figure 8. A first order filter would use only L1, a second order adds C1, a third order adds L2, and so on. The coefficients of Table 1 are used directly to find values for these filters. This configuration must be used with half bridge circuits and can be used with full bridge circuits by substituting the second PWM output for all the ground connections. This substitution is very rarely done because it places the high speed square waves of the PWM output on both load terminals and all the cabling between the amplifier and load. With rise and fall times usually in the tens of nanoseconds, and amplitude nearly equal to supply voltage, this is an extreme RFI problem

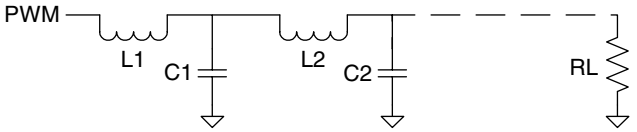


FIGURE 8. FOURTH ORDER, SINGLE-ENDED FILTER CONFIGURATION

5.0 FULL BRIDGE FILTER TOPOLOGIES

With full bridge circuits, an additional filter requirement is introduced in that common mode voltage applied to both load terminals usually needs to be minimized. The technique to achieve low common mode voltage is to simply split the inductor values in half, applying half to each PWM output as shown in Figure 9.

If one could acquire a perfect PWM amplifier (equal rise and

ORDER	L1	C1	L2	C2	L3	C3
1	1					
2	1.4142	.7071				
3	1.5	1.3333	.5			
4	1.5307	1.5772	1.0824	.3827		
5	1.5451	1.6944	1.382	.8944	.309	
6	1.5529	1.7593	1.5529	1.2016	.7579	.2588

$$L = \frac{COEF * R_L}{2 * \pi * F} \qquad C = \frac{COEF}{2 * \pi * F * R_L}$$

L in Henries
C in Farads
R_L in Ohms

TABLE 1. FILTER COEFFICIENTS

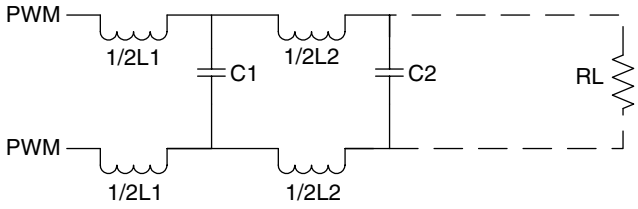


FIGURE 9. BASIC SPLIT INDUCTOR TOPOLOGY FOR THE FULL BRIDGE

fall times, no dead time plus an exact out of phase condition), this filter would output common mode voltage proportional to inductor mismatch only. With real PWM amplifiers, the output will contain large amounts of high frequency harmonics. Each application is different, but peak-to-peak noise amplitude may approach the supply voltage. The spectral content of this noise extends well above the switching frequency. A pair of small capacitors added from the output side of each half of L1 to ground, as shown in Figure 10, will remedy this problem. It is not necessary (and sometimes it is counterproductive) to use more than this one pair of leg capacitors. Placing these small capacitors on the load side of L2 or L3 is not as effective as the placement shown.

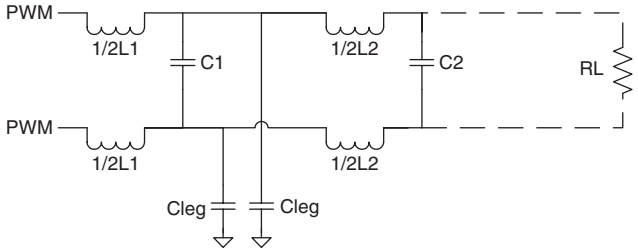


FIGURE 10. GROUND LEG CAPACITORS FILTER HIGH FREQUENCY COMMON MODE NOISE

Value selection for these ground leg capacitors is less critical than for the main filter capacitors. It has been determined empirically that setting the impedance value of these capacitors at the cutoff frequency, to between 10 to 30 times the value of the load resistance will provide reasonable common mode filtering. The addition of these capacitors will typically produce no more than 0.05db peaking, nor more than 0.2db change at the cutoff frequency in any order filter. From the technical point of view, the two Clegs are in series, and this is in parallel with C1. This means that on all but first order filters, C1 could be reduced by half the value of Cleg to eliminate even these small errors. Figure 11 shows the results of the following equation where the impedance ratio was set to 23:1:

$$C = \frac{1}{145 \bullet FC \bullet RL}$$

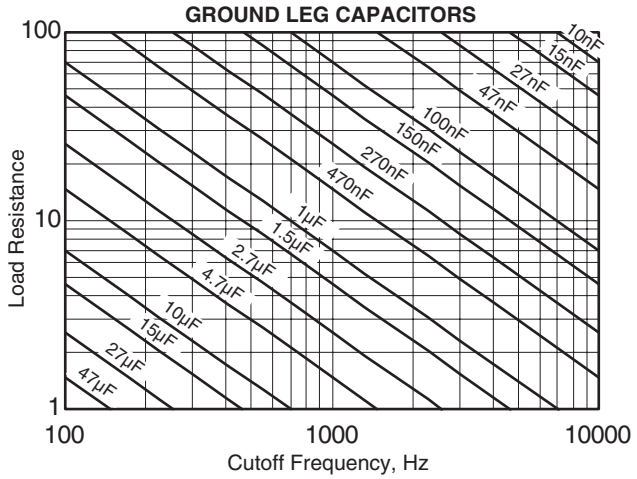


FIGURE 11. GROUND LEG CAPACITORS FOR COMMON MODE FILTERING

From a practical point of view, the lower left quadrant of this graph is textbook material only when using second and higher order filters. C1, C2, and C3 must be capable of bipolar operation and will be an order of magnitude or more larger than the leg capacitors. While the bipolar capacitors exhibit very low ESL and ESR to provide good roll off in the high frequency spectrum, this leads to very large and expensive banks of capacitors.

We previously noted that the two ground leg capacitors form an equivalent capacitor one half the value of the two individual devices. Carrying this thought a little further, we arrive at the common topology shown in Figure 12 where only unipolar capacitors are used, and where very good common mode filtering is inherent.

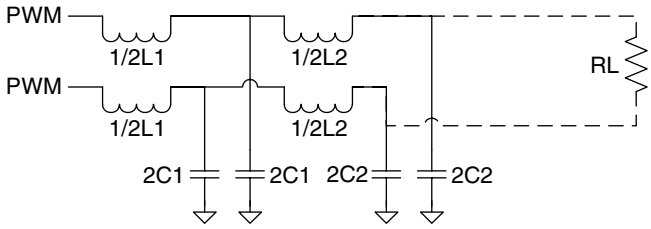


FIGURE 12. DUAL CAPACITOR TOPOLOGY MAY ALLOW UNIPOLAR CAPACITORS

Do not assume this dual capacitor topology is a panacea for all high current, low frequency filters. The total amount of capacitance increases fourfold over the single capacitor topology. Additionally, the high frequency performance of these large unipolar capacitors tends to fall off more rapidly than bipolar varieties (ESL and ESR rise faster). As the two capacitors are in series, the equivalent ESL and ESR are TWICE the individual values rather than half. If maximum high frequency attenuation is required, large high quality bipolar capacitors are a must.

The dual capacitor topology using unipolar capacitors always works with second order filters and may work with higher order filters. Be sure to read section 6.0 FILTER COMPONENTS, where we will find it is very common for higher order filters to apply negative voltage to these capacitors.

6.0 REACTIVE LOADS

One more time: to achieve these filter responses a constant and purely resistive load termination is required. If a reactive load can be modeled as resistance in series with either capacitance

or inductance, a simple conjugate match network can be used as shown in Figure 13. The resistor in the network will equal the resistor of the load model. As the network is in parallel with the load, all signals in the pass band will be applied to the network and power dissipation must be checked. Realize that combined impedance of the network plus load is constant and that changing frequency shifts the power between the network and the load. This means a 100W capacitive load drive will require a 100W matching network if DC signals are allowed.

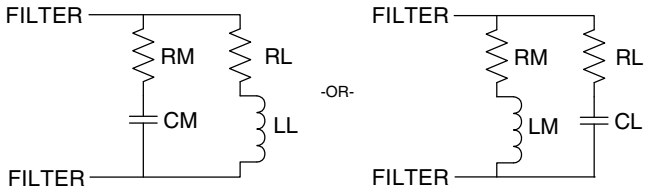


FIGURE 13. CONJUGATE MATCHING NETWORKS

The Power Design frequency sweep capability will prove quite useful in determining power dissipation and in possibly choosing a non-perfect network trading off lower power dissipation for some distortion of the ideal filter response curve.

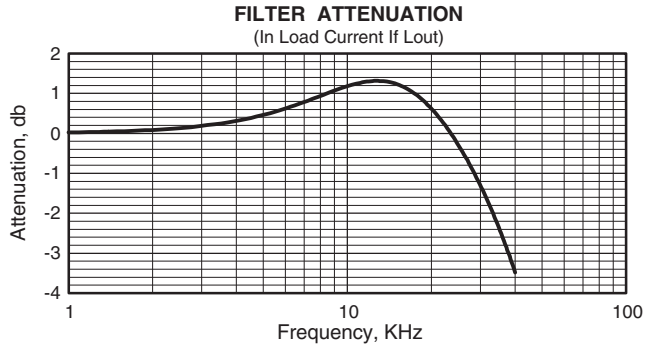


FIGURE 14. TRADING MATCH NETWORK POWER FOR SOME PEAKING OF THE FILTER

Figure 14 illustrates one response example where the ideal match network resistor was doubled to reduce power dissipation. It is perfectly acceptable to omit the network as long as the resulting attenuation curve is also acceptable.

7.0 FILTER COMPONENTS

Filters used in high power switching circuits often are the largest physical part of the circuit. Expect the filter to occupy more space than the rest of the circuitry. Expect currents and voltages to be greater than the output signal.

Filter components should be low loss, high current, high frequency devices. Check current ratings carefully as different manufacturers can use different rating methods. Make sure the inductors chosen have the required inductance at the maximum rated current and at the square wave switching frequency (many inductors are rated only with sine waves applied). We have seen laminated steel core inductors destroy circuits even when cutoff frequency was only 100 Hz! Successful applications usually implement powdered iron, ferrite, or air cores.

Polyester, polycarbonate, polypropylene, and chip ceramic capacitors are often used in the best PWM filters. Tantalum (preferred if voltages and temperatures allow) or electrolytic capacitors may be required in low frequency filters. The capacitors should have low loss at the switching frequency and well beyond (to at least the tenth harmonic).

While there is absolutely no substitute for finding real parasitic values for filter components, Power Design provides a default parasitic calculator for first pass design efforts, as shown in Figure 15. Parasitics vary WILDLY form part to part. The default calculator is ONLY intended to get somewhere in the pall park. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse.

Consult manufacture's data sheets or measure the parts to get accurate data.

Components loaded into this sheet by the PWM Filters sheet are for single-ended filters (to minimize spreadsheet size and sweep execution time). Use buttons 85-87 to put physical component values here for the type of filter you intend to build. Values to design single-ended filters will not be changed. For split-inductor designs, L will be divided by 2. For dual-capacitor designs, L will be divided by 2, plus C will be doubled.

Enter actual parasitics or calculate default values with button 91.

Use buttons 88-90 to re-load into the filter/load area and run the sweep. Values for Single-ended designs are not changed. For split-inductor designs, L and the parasitic R will be doubled plus parasitic C will be divided by 2. For dual-capacitor designs, inductors will be treated the same as for split-inductor designs

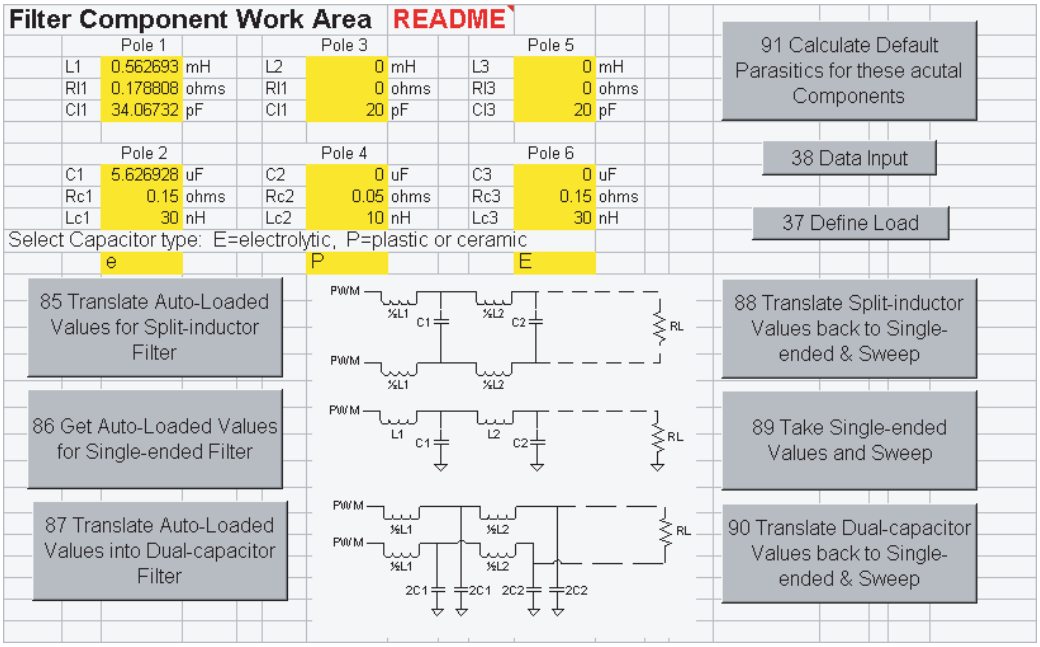


FIGURE 15. TRANSLATING VALUES FOR THE THREE TOPOLOGIES AND DEFAULT PARASITIC CALCULATION

and C will divided by 2, plus parasitic R & L will be doubled. Please note that even when using similar quality capacitors, the Q of a dual capacitor equivalent of a single capacitor is likely to be four times lower.

The folly of ignoring parasitics is illustrated by the data in Table 2. A second order filter was designed to provide 100.9db

TOPOLOGY	ELECTROLYTIC	PLASTIC
Split-inductor	68.1db	81.8db
Single-ended	68.6db	82.4db
Dual-capacitor	62.4db	75.3db

TABLE 2. COMPARING FILTER TOPOLOGY AND CAPACITOR TYPES

attenuation at the switching frequency. Using default parasitics, attenuation is listed for the three filter topologies using electrolytic and plastic capacitors.

There are two conclusions to draw from this data: first, plastic capacitors have a definite advantage over electrolytic types. Secondly, the dual-capacitor topology is inferior to the other two. In a related issue, do not fall into the trap of thinking that adding a small high frequency capacitor in parallel with a much larger one having poor ESR and ESL will regain the ideal attenuation. Adding a plastic or ceramic capacitor equal to 1/10 the value of the large electrolytic brings attenuation up to only 81.1db for the split-inductor topology, still almost 20db short of ideal.

7.1 FILTER COMPONENT STRESS LEVELS

Multi-pole filters are a combination of one or more series resonant circuits and they do develop currents and voltages above the input and output levels as the signal frequency approaches the cutoff frequency. The highest stress levels will be born by L1 and C1. Higher order filters produce higher amplification levels. The last two components of the filter do not see stress levels above the signal level. Figure 16 illustrates these stress levels for L1, L2, C1, and C2 for all filter orders up to 6. Voltages and currents are normalized to the DC or very low frequency output signal amplitude and are based on ideal components.

Data on current can be used directly for any filter topology for both inductors and capacitors. If a split inductor topology is used, the inductor voltage data must be divided by two. Voltage data can be used directly for capacitors not connected to ground. Ground terminated capacitors have a DC bias equal to 1/2 the supply voltage which must be added to half the peak voltage calculated from the graphs. To find peak capacitor voltages the equation is:

$V_{PEAK} = Vs/2 + Vout_{PEAK}/2$ * graph reading

Do this calculation for BOTH the positive and negative peak output voltages. Note that if output voltage is nearly equal to supply voltage, and the filter order is three or more, the most

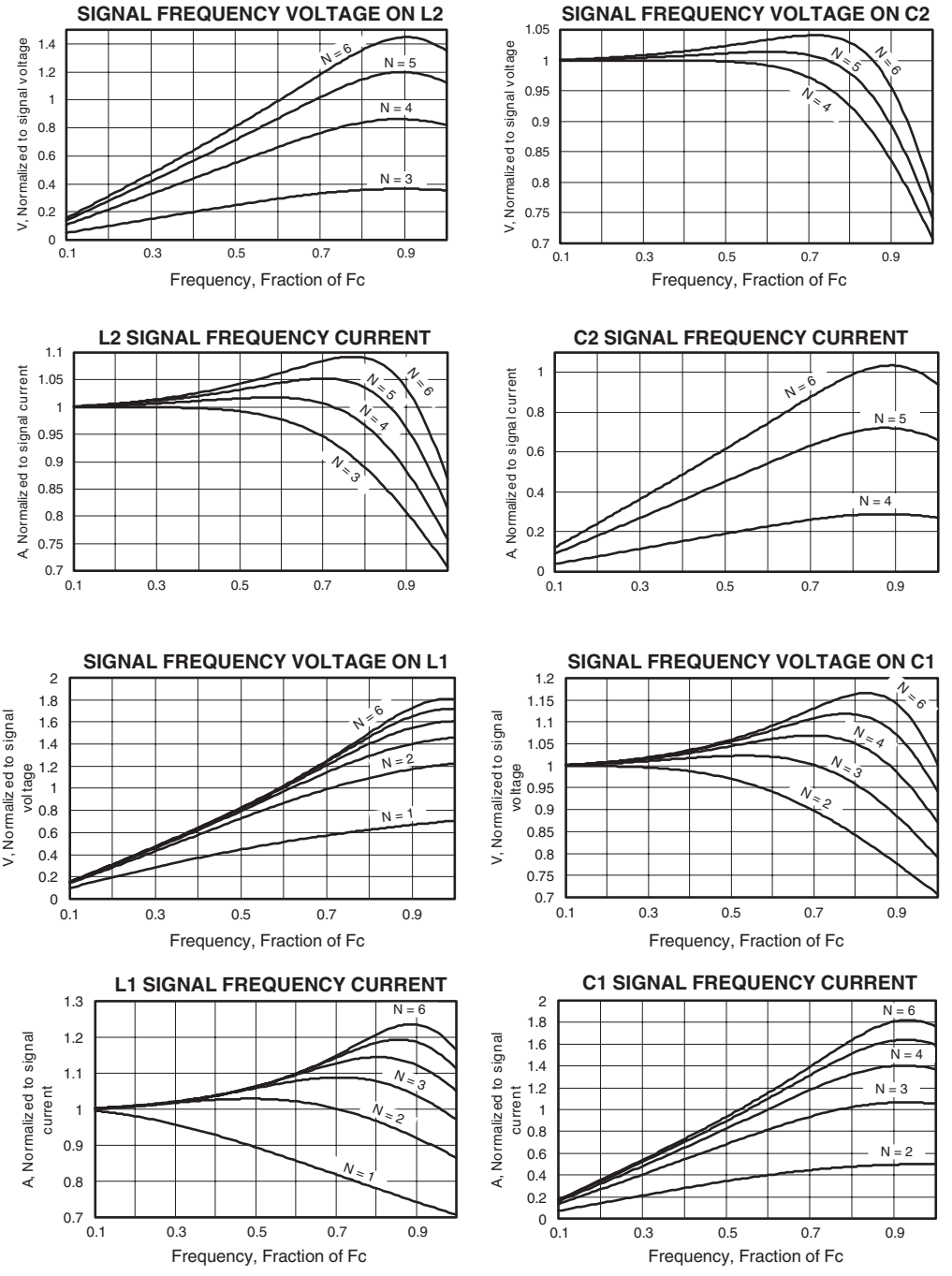


FIGURE 16. FILTER COMPONENT STRESS LEVELS

negative going peak for C1 will be negative with respect to ground. The same is true for C2 with fifth and sixth order filters. This means even a ground-terminated capacitor can have BIPOLAR voltages applied. From a practical point of view, this situation implies the use of unipolar capacitors limits filter order to two.

As an example, consider filter options for an SA06, which is to deliver ±470V to a 332Ω resistive load at 1KHz. Current will be 1.414A peak or 1A RMS. Power will be 665W peak or 332Wrms. A supply of 480V will provide plenty of headroom for internal losses and maximum linear duty cycle limitations. The worst case for voltage and current extremes will be a sixth order filter.

L1 peak current = 1.414A * ~1.23 = 1.75A
L1 peak voltage = 470V * ~1.82 = 850V
C1 RMS ripple current = 1A * ~1.82 = 1.82A
C1 peak voltage (differential) = 470V * ~1.17 = 548V
C1 + peak voltage (grounded) = 240V + 274V = 514V
C1- peak voltage (grounded) = 240V - 274V = -34V Must be bipolar

The same math with graph values from the other four graphs will yield stress levels for L2 and C2.

We can now make some general statements about filter design. Higher order filters can increase component ratings by as much as 82%. The two most costly increases are first, the ripple current on C1 and then the voltage rating of L1. While lowering filter order helps this situation, an even better way to minimize component requirements is to design the cutoff frequency as a multiple of the maximum input signal frequency. Turning this around, limiting input signal to one half or less of the cutoff frequency, limits these stress level increases to about 6% for sixth order filters and even less for more moderate (and practical) orders. Figures 17 and 18 show the Power Design answers for L1 and C1 stress levels of this example modified for a cutoff frequency of 2KHz rather than 1KHz. An additional benefit of this change is a 2:1 reduction in the values of filter components. The performance cost of this change at the switching frequency is a reduction of attenuation equal to 6db for each order (@ N=4, -108db drops to -84db).

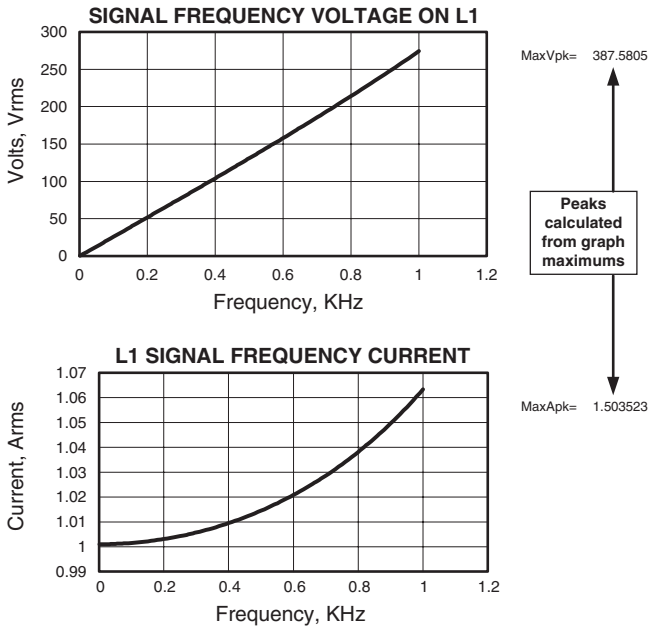


FIGURE 17. DOUBLING Fc LOWERS L1 STRESS LEVELS

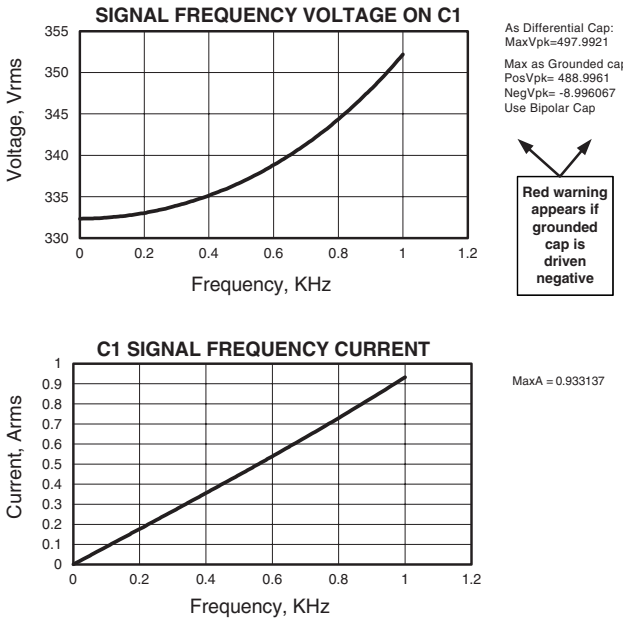


FIGURE 18. DOUBLING Fc LOWERS C1 STRESS LEVELS

8.0 SAFETY CONCERNS

A word of CAUTION. These graphs were generated with perfect components giving the best possible circuit Q, compared to real components having losses and therefore generating lower peaks. On the opposite side, these graphs reflect perfectly terminated filters; and normal component tolerances destroy this perfection. Do NOT power up filters unless your are sure they are properly terminated. Use Power Design to **CHECK COMPONENT TOLERANCES.**

These graphs also assume sine wave inputs (the only waveform Power Design deals with). Figure 19 is a Spice simulation of this original example showing L1 and C1 stresses when the input signal is a 900Hz, 470V square wave. L1 voltage = ±582V and is for 1/2 the total inductance. L1 current peaks at ±2.14A. C1 current peaks at ±3.18A. C1 is grounded and has voltage peaks of 587V and -107V. The output is a very good looking sine wave instead of a square, and peak amplitudes have risen from 470V to 527V, from 1.414A to 1.59A and from 665W to 838W.

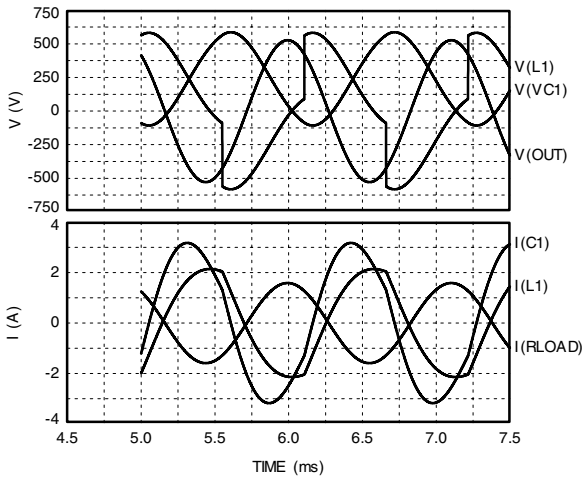


FIGURE 19. SQUARE WAVES THROUGH A 6 POLE FILTER COME OUT AS LARGER SINE WAVES

9.0 EXAMPLES

Example 1. The voice coil of a shaker table has 7Ω resistance and 100uH inductance. The desired drive level is 50V peak from 10Hz to 2KHz. Starting with the Power Design, Part Selection sheet, SA60, PA93, PA04, and SA01 are the first choices in order of cost. SA60 was rejected because it has no current limit. In the Power sheet, it takes only about a minute to find that the PA93 cannot handle the internal power dissipation (about 140W). Switching to PA04 reveals the circuit is possible, but would require a 0.2°C/W heatsink to keep junction temperatures to 150°C and has efficiency in the 50% area. This temperature may not be acceptable from a reliability point of view and leaves poor choices for the heatsink. Choice one is the Apex Precision Power HS11 with liquid cooling; read this as costing nearly as much as the amplifier before calling a plumber. Choice two involves a custom heatsink.

The SA01 PWM amplifier is the most cost effective choice and will run much cooler. With PWM amplifiers, a power supply voltage substantially higher than peak output voltage is not a killer in terms of internal power dissipation. This allows an 80V unregulated supply, saving a lot in terms of efficiency, cost and design time over a regulated supply required by a linear solution. The SA01 circuit will follow the voltage control example given in Application Note 30 PWM BASICS. It was determined that 150mV peak ripple at the 42KHz switching frequency would be acceptable. In order to maximize pass band flatness and avoid the numerous pitfalls of driving signals right up to the cutoff frequency, Fc will be designed for 4KHz. Figure 20 shows this data loaded into the PWM Filters sheet of Power Design.

Filter Design for PWM Amplifiers READ ME — Using the Complex Load:

CAUTION! Refer to Applications Note 32

Input Data

Model	SA01			**Order Calculation**		
Vs	80	Volts		Atten. @ Fsw	56.478	db
Fsw	42	KHz	42	N(exact)	2.7653	
Fmin	0.01	KHz				
Fmax	2	KHz		N(recommended)	3	
Fcutoff	4	KHz				
Rload	7	Ohms		**Matching network**		
Cload	0	uF		Cm =	2.0408	uF
Lload	0.1	mH		Lm =	0	mH
Vripple	0.15	Vpk		Rm =	7	Ohms
Signal	50	Units				
Sig as ?	V peak	Note/W				

60 Load All Data For N=1
61 Load All Data For N=2
62 Load All Data For N=3
63 Load All Data For N=4
64 Load All Data For N=5
83 Load All Data For N=6
Read Me
No — Auto Sweep on Load?

Notes: SA01 Shaker Table Example

46 Print Filter
55 Show Attenuation in db & %
56 Show Attenuation Graph
66 Show Filter Components

FIGURE 20. SETTING UP THE PWM DESIGN FOR ANALYSIS

Figure 21 gives all the component choices for the third order filter. If a single ended filter was desired, components under that heading would be used. If a dual capacitor topology is desired, use components from the dual cap column. To form the most common topology, the split inductor, this example will use inductors from the differential column and capacitors from the single-ended column. Leg capacitors will be 0.27uF per Figure 11. The 2.28Ap-p ripple will be the maximum ripple in L1 at the switching frequency. The 0.57A is used to calculate power loss in the amplifier.

Shading indicates values for Split Inductor topology

		Dual Cap Filter		Single-ended Filter	
N = 3	L1 =	0.2089	mH	0.4178	mH
	C =	15.157	uF	7.5786	uF
	L2 =	0.0696	mH	0.1393	mH

P-P Iripple = 2.2796 Amps out of the amplifier

Avg. Iout for thermal calculations = 0.5699

FIGURE 21. THIRD ORDER DATA ONLY FROM THE COMPONENTS SCREEN

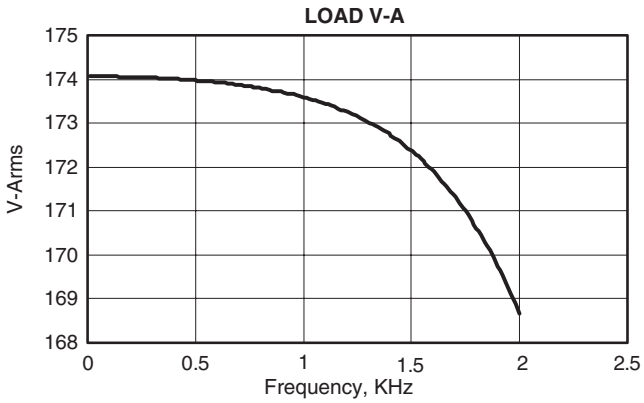


FIGURE 22. POWER DELIVERY TO THE SHAKER TABLE

The inductors will be custom wound. L1s are 47 turns of #12 on a Micrometals T184-18 torriodal core. L2s are 39 turns of #12 on a T130-18 core. The single ended capacitor is metallized polypropylene and the leg capacitors are X7R ceramic. The matching network capacitor is a pair of 1uF, X7R ceramics in parallel. Figure 22 shows the delivered power to be about 2% low at the lowest frequencies. This is primarily from copper loss in the inductors and suggests a simple gain adjustment be included in the circuit. At first glance the power roll-off at 2KHz looks a bit large. However a linear sweep analysis of a perfect drive to the voice coil reveals the coil inductance itself is responsible for over half this droop.

With your own copy of Power Design, you will use the PWM Power sheet to find the SA01 delivers full power while averaging an internal loss of under 15W. When mounted on the Apex Precision Power HS16 without a fan, the SA01 will have a case temperature rise of only 19°C and junctions only 3°warmer. Adding in filter loss (including the matching network) as shown in Figure 23, still yields efficiency better than 92% over most of the frequency band.

Example 2. This example illustrates the transformer-like action of a PWM system. The requirement is to drive a 2Ω thermo-electric cooler at ±10V, using an existing single 48V supply. Any linear solution will draw 5A or 240W from the supply and will need to dissipate 190W. SA60 is the least expensive PWM amplifier having analog input capability. A 10Hz bandwidth will be plenty and ripple voltage should be kept below 100mV across the cooler. It is also desirable to keep the common mode ripple as low as possible, so a dual capacitor filter will be considered. A first pass with the PWM Filter sheet loaded with switching frequency=45KHz and cutoff frequency=100Hz, called for inductors of 2.25mH and capacitors of 1125uF. The large capacitance values suggest electrolytic types which generally offer lower performance in

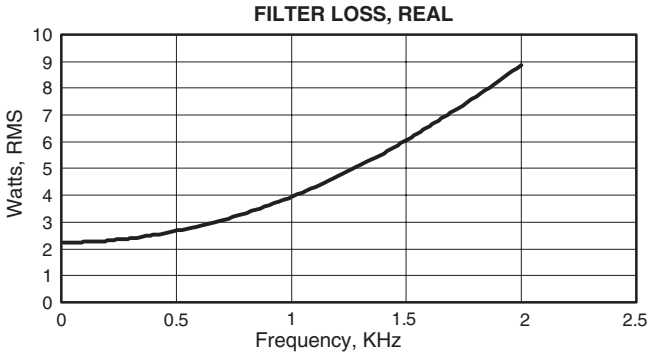


FIGURE 23. POWER LOSS IN THE FILTER AND MATCHING NETWORK

Shading indicates values for Split Inductor topology

		Dual Cap Filter			Single-ended Filter	
N = 2	L =	0.2251	mH		0.4502	mH
	C =	112.54	uF		56.269	uF
	P-P Iripple =	1.1848	Amps out of the amplifier			
	Avg. Iout for thermal calculations =	0.2962				

FIGURE 24. CHANGING Fc TO 1KHz YIELDS MORE REASONABLE COMPONENT VALUES

the high frequency spectrum. A second pass at the design set cutoff frequency at 1KHz, yielding the data in Figure 24.

In checking available metallized polypropylene capacitors, it was discovered that a single-ended capacitor would cost less than a third that of the pair of dual value capacitors. The final filter shown in Figure 25 is a hybrid where the table for leg capacitors is ignored and the three capacitors form the equivalent of a 55uF single capacitor and provide excellent common mode attenuation.

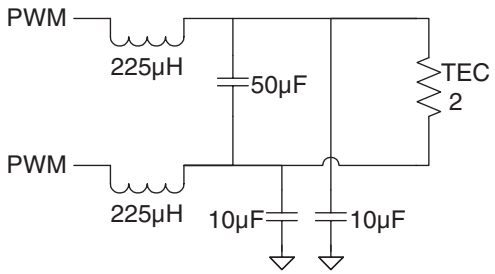


FIGURE 25. A CROSS BETWEEN SPLIT INDUCTOR AND DUAL CAPACITOR TOPOLOGIES

Figure 26 illustrates finding default parasitics and loading equivalent components to run the frequency sweep on. In the Filter Component Work Area, enter values by hand and then use button 91 to calculate the parasitics. Note the 0.1Ω and

Filter Component Work Area			README							
		Pole 1			Pole 3			Pole 5		
	L1	0.225	mH	L2	0	mH	L3	0	mH	
	Rl1	0.0775	ohms	Rl1	0	ohms	Rl3	0	ohms	
	Cl1	25.625	pF	Cl1	20	pF	Cl3	20	pF	
		Pole 2			Pole 4			Pole 6		
	C1	50	uF	C2	10	uF	C3	0	uF	
	Rc1	0.134949	ohms	Rc2	0.1	ohms	Rc3	0.15	ohms	
	Lc1	32.08661	nH	Lc2	23	nH	Lc3	30	nH	
Select Capacitor type: E=electrolytic, P=plastic or ceramic										
		p			P			E		

FIGURE 26. FINDING DEFAULT PARASITICS FOR A HYBRID FILTER TOPOLOGY

23nH values calculated for the 10µF capacitors. The equivalent single-ended capacitor has half the capacitance and twice the resistance and twice the inductance. Translate back to single-ended with button 88 and return to the Define Load area when the sweep is complete. Now enter the equivalent values for the pair of 10µF capacitors as shown in Figure 27, and run the sweep.

Pole 1				Pole 3		
L1	0.45	mH		L2	0	mH
Rl1	0.155	ohms		Rl1	0	ohms
Cl1	12.8125	pF		Cl1	5	pF
Pole 2				Pole 4		
C1	50	uF		C2	5	uF
Rc1	0.134949	ohms		Rc2	0.1	ohms
Lc1	32.08661	nH		Lc2	23	nH

FIGURE 27. MANUAL ENTRY OF COMPONENT EQUIVALENTS FOR A HYBRID FILTER TOPOLOGY

Now for the real beauty of this circuit: when delivering the full 5A (50W), the SA60 mounted on an Apex Precision Power HS03 1.7°C/W heatsink (needs a mounting hole drilled), has an internal dissipation of only about 15W! Throwing in filter loss also, the supply is working to the tune of only about 70W, or about 1.5A.

Example 3. This circuit drives a magnetic bearing requiring up to 12A DC plus up to 3A peak AC up to 300Hz. Bearing coil inductance is 5mH and resistance is 2Ω. Using the Power sheet reveals the AC drive will require 29Vpk, which brings total peak voltage up to 54V. As the PWM circuit will be inside a larger loop based on a position sensor, low phase shift is much more important than amplitude accuracy. The SA03 will handle this job using a current output circuit based on its data sheet typical application. Maximum 22.5KHz ripple voltage at the bearing is 1V peak. Knowing that filters shift phase the least amount in the lowest portion of the bandpass, it was decided to set the cutoff frequency to 3KHz. A split inductor topology will be used with N=3. This data was loaded into Power Design yielding 80uH for the L1s, 35uF for the capacitor, 27uH for the L2s, and 1250uF for the capacitor in the matching network. Leg capacitors will be 1uF. Figure 28 shows the initial current control results.

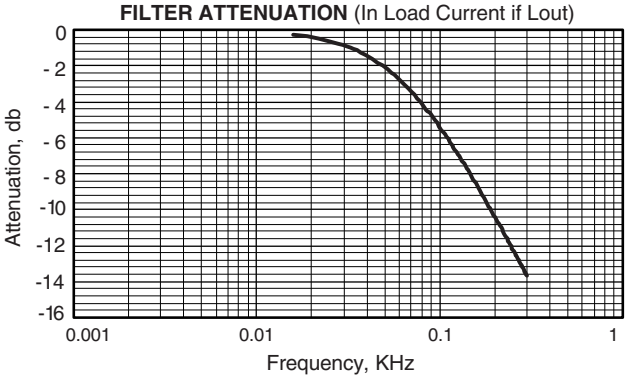


FIGURE 28. THIS IS IDEAL RESPONSE?

In checking the graph on load current, it agrees by saying current at 300Hz is down to about 20% of DC levels. The ideal filter keeps output voltage constant in the pass band. In this case the large inductance of the load called for an R-C matching network, which draws most of the current at 300Hz.

We found earlier that removing a matching network causes voltage peaking at the filter output; this is exactly what we need to keep current constant due to the bearing inductance. Total removal causes about an 8db peaking (a gain of about 2.5), but a few iterations later, 470uF and 13Ω was found to produce the results shown in Figures 29-34.

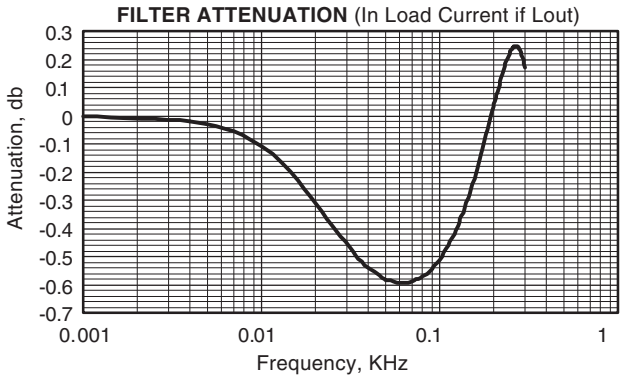


FIGURE 29. DB RESPONSE OF THE MODIFIED MATCHING NETWORK

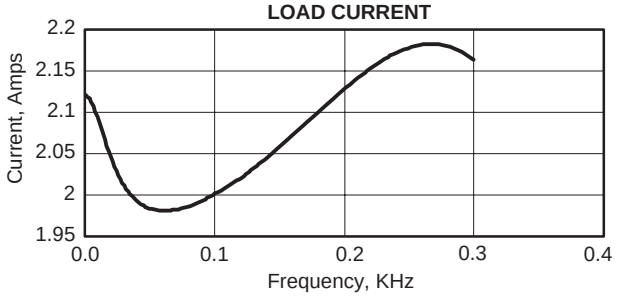


FIGURE 30. CURRENT OUTPUT WITH THE MODIFIED MATCHING NETWORK

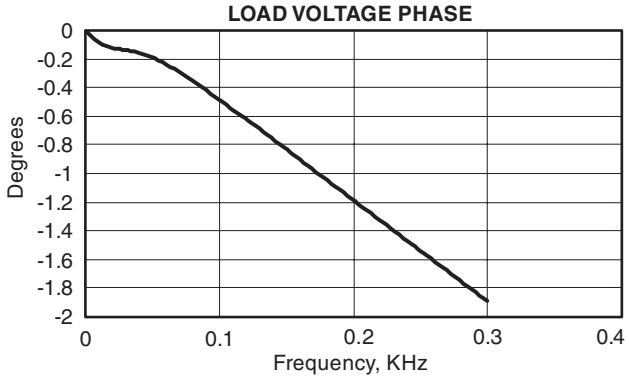


FIGURE 31. OUTPUT VOLTAGE PHASE WITH THE MODIFIED MATCHING NETWORK

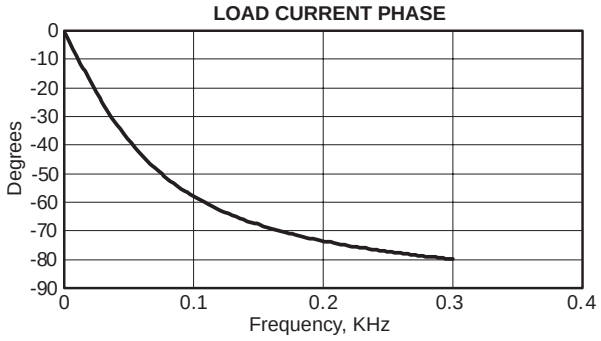


FIGURE 32. CURRENT OUTPUT PHASE WITH THE MODIFIED MATCHING NETWORK

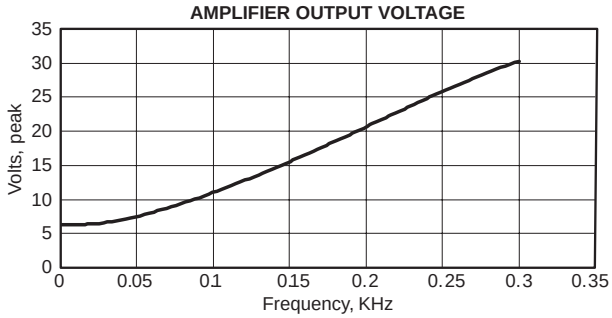


FIGURE 33. AMPLIFIER OUTPUT VOLTAGE WITH THE MODIFIED MATCHING NETWORK

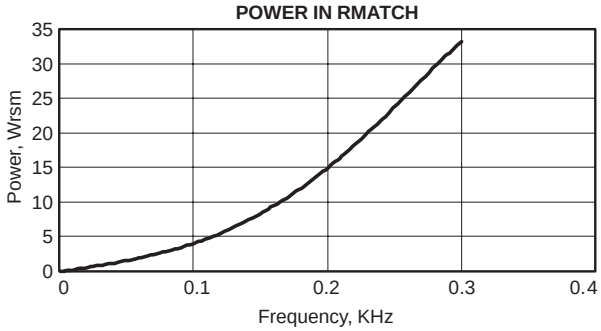


FIGURE 34. POWER DISSIPATION IN THE MODIFIED MATCHING NETWORK

To estimate internal power dissipation for the SA03, a new sweep was run with amplitude set to the RMS sum of 12A DC and 3Apk AC (~12.2Apk). Putting the 1.48°C/W minimum rating from this sweep into the Heatsinks sheet brings up the HS06 rated at .96°C/W. This will result in a case temperature a little over 60° and junctions a little over 70° at maximum drive.

10.0 FINAL CONSIDERATIONS

DO NOT DRIVE THESE FILTERS WITHOUT PROPER LOADING.

If you were taught to never have a load on a power circuit the first time you turn it on, be aware that the resonant circuits of these filters can generate voltages many times larger than the input voltage.

Poor circuit layout cannot be remedied by good filtering. PWM circuits, by their nature, have high frequency, and high power transients, that are difficult to eliminate from the desired output signal. Use ground planes and shielding as much as possible, but do not use these as a high current path. Use wide traces on circuit boards for power supply and output signals and heavy gauge wire for interconnects. Use star grounding techniques with the PWM amplifier ground pin as the center. A very small amount of inductance can cause large transients where high currents switch quickly. A rule of thumb is to expect 20nH per inch of conductor. Assume all output current changes its path through the PWM output switches each cycle of the switching frequency in 20 to 50ns. Space circuit board traces and wiring away from sensitive circuits to avoid extraneous noise pickup. Use bypass capacitors liberally.

The response curves for prefect components imply that the attenuation increases continuously with increasing frequency. With real components and real interconnects this is simply not the case. If you have a design claiming 150db attenuation, check it again.

Spice Model and PWM Amplifier Applications

PWM AMPLIFIER INTRODUCTION

The recent availability of high-voltage and high-current PWM amplifiers in hybrid packages has attracted the interest of many designers who traditionally use linear amplifiers. The advantage of PWM amplifiers is obvious: efficiency of 70 to 97%. High efficiency translates to lower internal power loss, smaller heat sinks, and reduced overall physical size.

To make it easier to design with these amplifiers, a simple and versatile generic PWM Spice model lets you check out PWM waveforms without the fear of blowing up the amplifiers or getting shocked by high voltages. The methodology behind generating such a model applies not only to hybrid PWM amplifiers, but also to monolithic and discrete PWM amplifiers. The inputs to the model come from the PWM amplifier's data sheet, and you can run the model on any commercial Spice program.

Even though a PWM amplifier offers analog signals in and analog signals out, its circuit functionality is entirely different from a linear amplifier's. A PWM amplifier modulates a pulse train in the time domain and uses LC filtering to extract the analog-signal output. You can use PWM amplifiers to emulate linear constant- voltage amplifiers or linear constant-current amplifiers, both at much higher levels of efficiency.

If you're unfamiliar with how a PWM amplifier works, you're not alone. Just like op amps, PWM amplifiers come in many sizes and flavors, some with fancy bells and whistles. Fortunately, the amplifiers all operate under the same principle.

A PWM amplifier converts an analog signal into a pulse train of variable duty cycle. The analog input controls the duty cycle of the output pulse train, which switches on and off once during each cycle. When a high output is necessary, the pulse train switches on most of the time and vice versa.

Figure 1a shows a basic PWM amplifier. Vin is the analog input of 1 to 8V dc. AOUT is a pulse train, and BOUT is its inverse. The PWM oscillator determines the frequency of the pulse train, and some PWM amplifiers allow you to put in your own PWM oscillator. As Vin changes from its minimum to its maximum value, the duty cycle of AOUT changes from 0 to 100%, and the duty cycle of BOUT changes from 100 to 0%. The difference voltage of AOUT–BOUT has the same pulse train as AOUT but with double the amplitude of 2xVs p-p (Figure 1b).

If you connect a dc brush-type motor across AOUT and BOUT, you can control the motor speed with Vin. When you set Vin in the middle of its range, for 50% duty cycle at AOUT and BOUT, the motor stands still. With Vin at its maximum, the motor turns at maximum rpm; with Vin at its minimum, the motor reverses direction of rotation and turns at maximum rpm again. You can directly connect AOUT and BOUT to a motor because the winding inductance of the motor turns the pulsed voltage into a rippled dc current whose magnitude controls the motor speed and whose polarity controls the clockwise or counterclockwise direction of the motor. As Figure 1a indicates, most other applications need LC filters to filter out the PWM pulse train to ensure that an analog signal appears at the load.

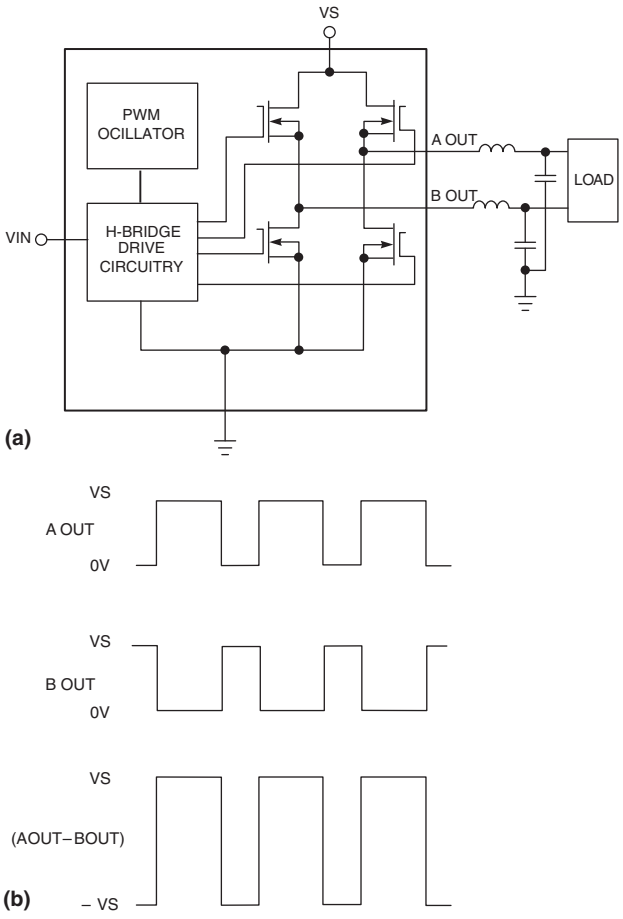


FIGURE 1. A PWM amplifier (a) converts an analog signal into a pulse train of variable duty cycle (b). AOUT and BOUT can directly drive a dc motor, but most other loads require additional LC filtering.

USE A GENERIC SPICE MODEL

Figure 2 shows the generic Spice subcircuit model of a PWM amplifier. V1 is a ramp of fixed frequency. E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable-dutycycle pulse train (Figure 3). S5, V5, S6, and V6 limit the amplitude of the pulse train to ±5V. S1/R1, S2/R2, S3/R3, and S4/R4 represent the four MOSFET drivers for which

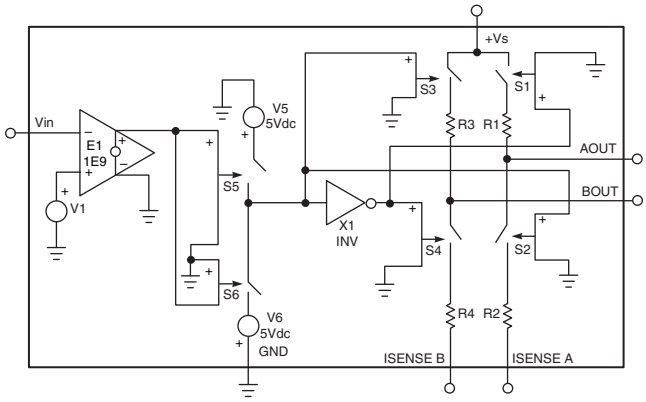


FIGURE 2. A generic Spice model of a PWM amplifier includes a fixed-frequency ramp (V1), a comparator (E1), an inverter (X1), and MOSFET drivers (S1 to S4) and their respective on-resistances(R1 to R4).

R1, R2, R3, and R4 are the respective on-resistances. The four MOSFETs always turn on and off in diagonal sets, that is, when S1 and S4 are on, S2 and S3 are off and vice versa. The inverter X1 provides the diagonal switching control. ISENSE A and ISENSE B are current-sensing terminals, usually available at two output pins for current-feedback control circuitry. For open-loop operation or for voltage-feedback control, just connect ISENSE A and ISENSE B to ground.

When an external load connects between AOUT and BOUT, current flows from Vs to ground through one of two routes: Vs to S1/R1, to an externally connected load between

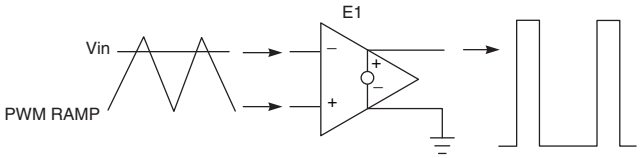


FIGURE 3. In the PWM amplifier model, E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable duty cycle pulse train.

AOUT and BOUT, to S4/R4, and then to ground or Vs to S3/R3, to the external load, to S2/R2, and finally to ground. The voltage across the load actually doubles the Vs voltage. For example, when Vs=100V, the voltage across the load is 200V pp. This voltage-doubling feature is another advantage PWM amplifiers offer for high-voltage applications. To double voltage using linear amplifiers you must use two linear amplifiers in a bridge-mode configuration.

DESIGN EXAMPLE: CONSTANT–CURRENT AMPLIFIER

You commonly use constant-current amplifiers for applications

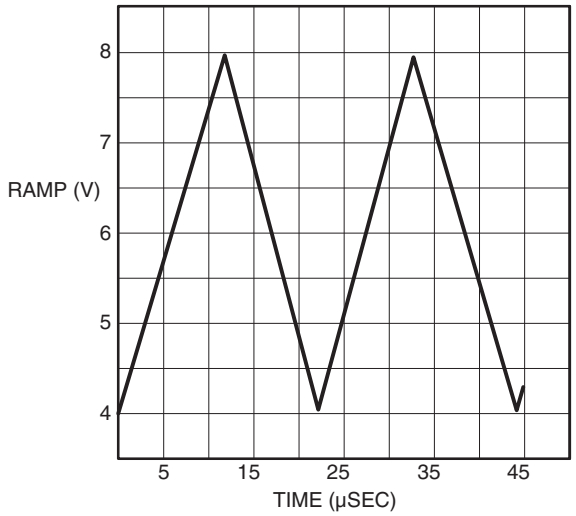


FIGURE 4. The analog input-voltage range and the switching frequency (in this case, 4 to 8V and 45kHz, respectively) determine the wave form of the PWM ramp.

such as motor-torque control and battery chargers. You can use the model and the specifications of a commercial PWM amplifier—in this case, the Apex Precision Power SA50—to design a constant-current amplifier (also called a voltage-to-current converter). You start out with the following specifications from the SA50 data sheet:

Analog input voltage/output duty cycles:
Vin=4V; AOUT=0% and BOUT=100%
Vin=6V; AOUT=50% and BOUT=50%

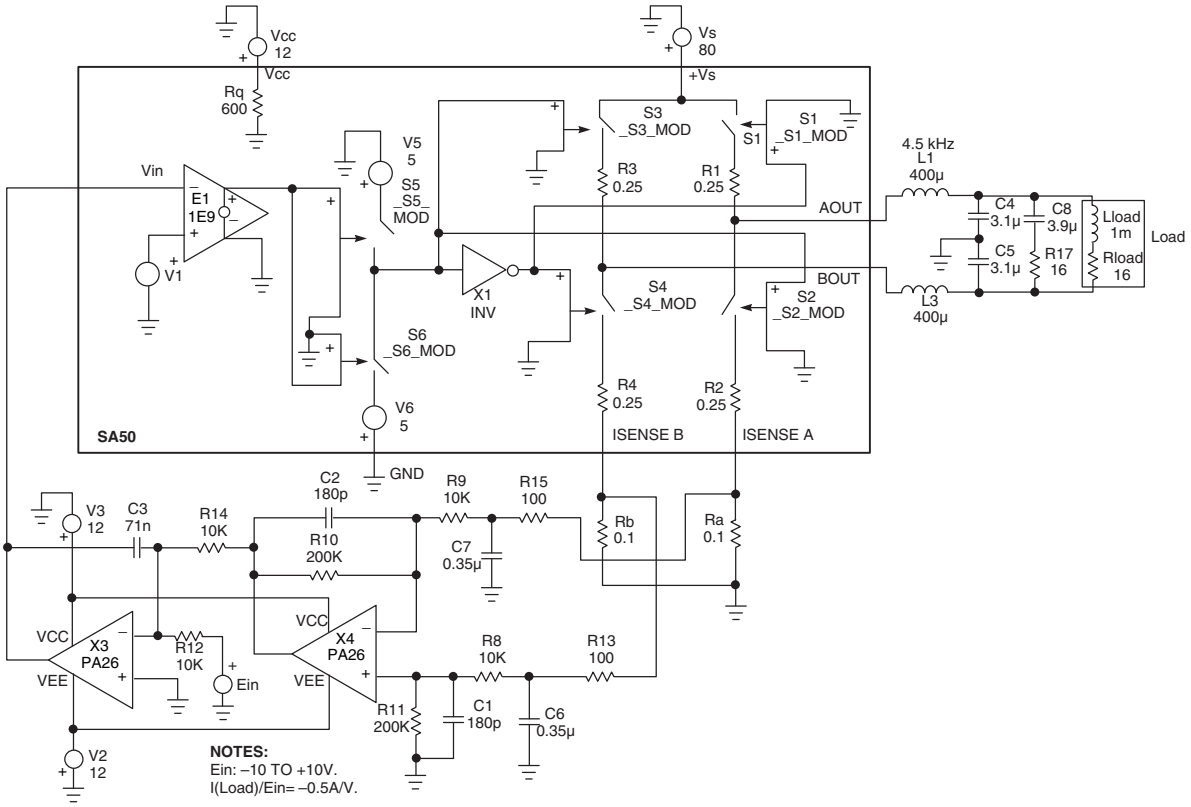


FIGURE 5. Combining the generic Spice model with the specifications for the SA50 PWM amplifier, you can use the model to simulate a voltage-controlled, constant-current amplifier.

Vin=8V; AOUT=100% and BOUT=0%
switching frequency: 45 kHz.
MOSFET on-resistance: 0.5Ω total or 0.25Ω each

The analog input voltage range of 4 to 8V dc and the switching frequency of 45 kHz determine the waveform of the PWM ramp (Figure 4), which V1 in Figure 2 produces. You can describe this waveform as a constant-voltage source in any commercial Spice program, such as Intusoft's Model ICAP/4Rx V8.8.1. You enter V1's parameters as manual-driven inputs, and this Spice program automatically generates the following statement for V1: V1 12 0 PULSE 4 8 0 11.1E-6 11.1E- 6 1E-12 22.2E-6, where "12 0" designates the two nodes for V1.

The MOSFET on-resistance of 0.25V determines the values of R1, R2, R3, and R4. The addition of Rq=600Ω and Vcc=12V model the SA50 amplifier's quiescent current and the low-voltage power supply necessary to power the H-bridge drive circuitry.

Figure 5 shows the complete Spice subcircuit for the SA50. This basic SA50 can drive a bidirectional motor for which Vin controls the motor speed and direction of rotation. You can add LC filters that let you drive other loads. Even when driving a motor, LC filters next to the amplifier module are useful for EMI and EMC purposes. Without filters, the long cables to the motor carry high-voltage switching pulses and act as antennas. Because the waveform across AOUT and BOUT is a pulse train of variable duty cycle and because Vin, the analog input signal, controls the pulse train's duty cycle or pulse width, you must first filter the PWM pulse train to extract the analog output signal.

In Figure 5, the load comprises Rload and Lload. L1, C4, L3, and C5 form a low pass filter with a cut off frequency (Fc) of 4.5 kHz to filter out the SA50 amplifier's 45-kHz PWM pulse train. A rule of thumb is to set the LC filter's corner frequency one decade below the PWM frequency. Of course, you can push the corner frequency higher by using multiple-pole LC filters. The equations to calculate filter LC values are as follows:

Because of the filter's differential configuration, these equations include a x0.5 factor for L1 and L3 and a x2 factor for C4 and C5. In this example, Rload=16Ω, and Fc=4.5 kHz, so L1=L3=400 µH, and C4=C5=3.1 µF. Because the load for this

$$L1 = L3 = \frac{1.4142 \bullet Rload}{2\pi \bullet Fc} \bullet 0.5, \qquad (1)$$

and

$$C4 = C5 = \frac{0.7071}{2\pi \bullet Fc \bullet Rload} \bullet 2. \qquad (2)$$

example is inductive, adding the matching network of R17 and C8 creates a combined load of 16Ω. The equations for R17 and C8 are as follows:

In this example, Lload=1 mH, and Rload=16Ω, so C8=3.9 µF, and R17=16Ω. Similarly , if you have a capacitive load, you can use a LR matching network to make the combined load resistive, for which

$$R17 = Rload, \qquad (3)$$

$$C8 = \frac{Lload}{Rload^2} \qquad (4)$$

Figure 6 shows the frequency response of the filter with and without the matching network. Ignoring the feedback circuitry of X3 and X4, a 1kHz 3.5V p-p sine wave with 6Vdc offset at Vin produces a 120V pp sine wave across the load (Figure 7).

$$L = Cload \cdot Rload^2 \qquad (5)$$

To complete the design of a constant-current amplifier , you must have some means of sensing the load current and provide feedback control in case of a load change. Ra and Rb are the two current-sensing resistors. Op amp X4 and its associated

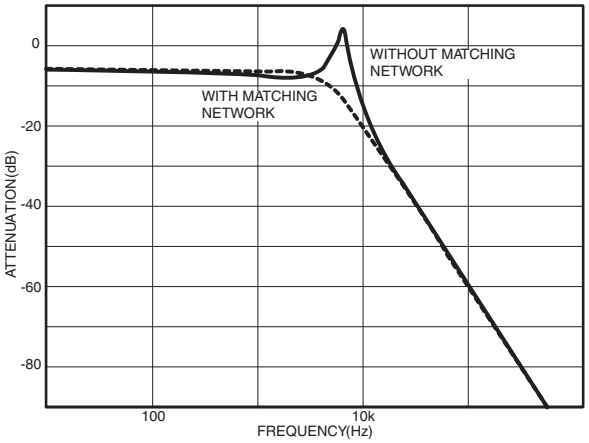


FIGURE 6. The LC filter's frequency response differs with and without the matching network.

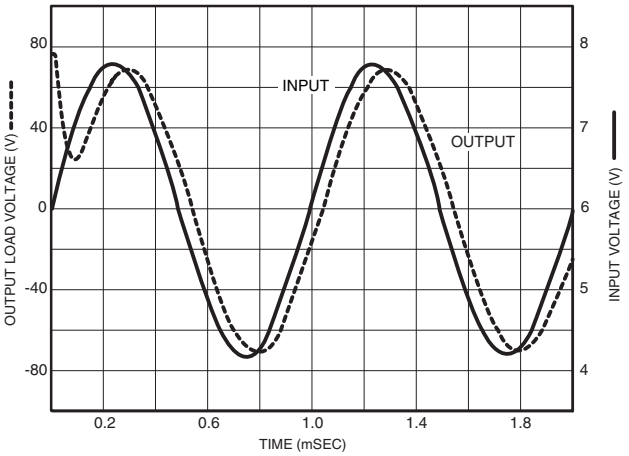


FIGURE 7. Ignoring the feedback circuitry of X3 and X4, a 1-kHz, 3.5V p-p sine wave with offset at Vin produces a 120V p-p sine wave across the load.

components serve two purposes: first, as a difference amplifier with a gain of 20 that converts the current difference between Ra and Rb into a voltage output of – 0.5A/V and, second, as a lowpass filter comprising C1, C2, C6, and C7 that filters the ripple currents in Ra and Rb with a corner frequency of 4.5 kHz. The design equations are as follows:

To minimize power losses, you should choose Ra and Rb values of 0.01 to 0.1Ω. In this example, Fc=4.5 kHz, R8=R9=10 kΩ. To minimize loading effects, these resistors must be much greater than R13=R15=100Ω. Substituting these values into

$$GAIN = -\frac{R9}{R10 \bullet Ra}\ A/V, \qquad (6)$$

$$C6 = C7 = \frac{1}{2\pi \bullet R13 \bullet Fc}, \qquad (7)$$

$$C1 = C2 = \frac{1}{2\pi \bullet R10 \bullet Fc}, \qquad (8)$$

Equation 7 and Equation 8, C6=C7=0.35 µF, and C1=C2=180 pF. Choosing R10=200 kΩ, Equation 6 yields a gain of –0.5 A/V.

X3 is an integrator that compares the error voltage from X4 with the input voltage Ein and provides the correct input voltage for the SA50 amplifier to close the feedback loop. The design equations for the integrator are as follows:

You can complete the design by choosing R12=R14=10 kΩ and C3=71 nF (Figure 6).

You can now run the Spice program. The load current waveforms (Figure 8) are as expected. Note that there is a small error between the Spice output and the expected value.

$$R12 = R14, \qquad (9)$$

$$C3 = \frac{1}{2\pi \bullet (0.05Fc) \bullet R12}, \qquad (10)$$

For example, with Ein=10V, the expected output current should be –5A, but Figure 8 shows –4.8A. This difference is because of the loss resulting from the 0.25Ω MOSFET's on-resistance. If you set the on-resistance to zero, you get exactly

LISTING 1–SA50 CONSTANT-CURRENT-AMPLIFIER SPICE CIRCUIT

```
*#save V(1) V(25) @R4[i] @R4[p] V(3) @R1[i] @R1[p] V(5)
*#save V(29) @R3[i] @R3[p] V(7) V(19) @R2[i] @R2[p] V(9)
*#save @Vs[i] @Vs[p] V(10) @S4[i] @S4[p] V(11) @S2[i] @S2[p]
*#save @S3[i] @S3[p] @S1[i] @S1[p] V(12) @V1[i] @V1[p] V(13)
*#save V(18) @E1[i] @E1[p] @V5[i] @V5[p] V(8) @S6[i] @S6[p]
*#save @V6[i] @V6[p] V(17) @Rload[i] @Rload[p] @Lload[i] @Rb[i] @Rb[p]
*#save @Ra[i] @Ra[p] V(16) V(14) V(20) V(21) @R8[i] @R8[p]
*#save @R9[i] @R9[p] @R10[i] @R10[p] @R11[i] @R11[p] @V3[i] @V3[p]
*#save @C1[i] @C2[i] V(24) V(18) V(26) @R12[i] @R12[p] @VEin[i]
*#save @VEin[p] @C3[i] @R14[i] @R14[p] @S5[i] @S5[p] V(15) V(30)
*#save V(2) @L1[i] @L3[i] @C4[i] @C5[i] @R13[i] @R13[p] @C6[i]
*#save @R15[i] @R15[p] @C7[i] V(23) V(29) V(6) V(4) V(21)
*#save V(22) @V2[i] @V2[p] V(27) @Vcc[i] @Vcc[p] @Rq[i] @Rq[p]
*#save V(28) @R17[i] @R17[p] @C8[i] @Rload[i]
*#VIEW TRAN Y1
*#alias Y1 @Rload[i]
.TRAN 22.2E-9 4000E-6 0 22.2E-8 UIC
.PRINT TRAN Y1
R4 1 25 0.25
R1 3 23 0.25
R3 5 29 0.25
R2 7 19 0.25
Vs 9 0 DC=80
S4 29 1 10 0 _S4_mod
.MODEL _S4_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S2 23 7 11 0 _S2_mod
.MODEL _S2_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S3 9 5 11 0 _S3_mod
.MODEL _S3_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S1 3 9 10 0 _S1_mod
.MODEL _S1_mod SW VT=2.5 RON=1E-9 ROFF=1E9
X1 11 10 INV { }
.SUBCKT INV 1 2
* in out
B1 3 0 V= ~V(1)
RD 3 2 1
CD 2 0 .87NF
.ENDS
V1 12 0 PULSE 4 8 0 11.1E-6 11.1E-6 1E-12 22.2E-6
E1 13 0 12 18 1E9
*#save @E1[i] @E1[p]
L1 23 4 400u
V5 15 0 DC=5
S6 11 8 0 13 _S6_mod
.MODEL _S6_mod SW VT=2.5 RON=1E-9 ROFF=1E9
V6 0 8 DC=5
Rload 17 6 16
V2 0 22 DC=12
Lload 4 17 1m
Rb 25 0 0.1
Ra 19 0 0.1
X4 16 14 20 21 22 PA21 { }
.SUBCKT PA21 1 2 3 4 5
* PINOUT ORDER +IN -IN OUT +V -V
Q1 10 1 8 QI1
Q2 11 2 9 QI2
R3 12 8 7.39E+03
R4 12 9 7.39E+03
I2 12 5 3.61E-05
C1 12 5 2.73E-12
R5 12 5 1.11E+06
R1 4 10 8.85E+03
R2 4 11 8.85E+03
C2 10 11 9.00E-12
I1 4 5 3.70E-02
G1 6 15 11 10 1.13E-04
G2 6 15 12 15 6.36E-09
R6 6 15 1.00E+05
D1 6 15 DD
D2 15 6 DD
C3 6 7 3.00E-11
G3 15 7 15 6 8.85E+00
R7 7 15 1E3
D3 7 16 DD
V1 18 16 1.60E+00
D4 17 7 DD
V2 17 19 1.60E+00
RE1 15 0 0.001
E2 18 0 4 0 1
E3 19 0 5 0 1
R8 7 20 50
C4 20 15 3.08E-09
Q3 19 20 21 QOP
Q4 18 20 22 QON
Q5 4 23 29 QON
Q6 5 24 30 QOP
Q7 25 27 31 QLN
Q8 26 28 31 QLP
R11 21 23 1.70E-01
RCLP 29 31 1.70E-01
RCLN 30 31 1.70E-01
R13 22 24 1.70E-01
D5 23 25 DL
D6 26 24 DL
R9 27 29 1E3
R10 28 30 1E3
I3 18 23 7.92E-03
I4 24 19 7.92E-03
R15 31 3 5.42E-01
RSN 3 34 1
CSN 34 5 0.1E-6
.MODEL DD D(CJO=0.1PF IS=1E-17)
.MODEL DL D(CJO=3PF IS=1E-13)
.MODEL QI1 NPN (BF=6.55E+02 IS=8E-16)
.MODEL QI2 NPN (BF=4.24E+02 IS=8.46E-16)
.MODEL QOP PNP (BF=4.64E+02 IS=1E-14)
.MODEL QON NPN (BF=4.64E+02 IS=1E-14)
.MODEL QLN NPN (BF=100 IS=1E-14)
.MODEL QLP PNP (BF=100 IS=1E-14)
.ENDS
R8 16 30 10K
R9 14 2 10K
R10 14 20 200K
R11 16 0 200K
Vcc 27 0 DC=12
V3 21 0 DC=12
C1 16 0 180p
C2 14 20 180p
Rq 27 0 600
X3 0 24 18 21 22 PA21 { }
R12 24 26 10K
VEin 26 0 DC=10
C3 18 24 71n
S5 15 11 13 0 _S5_mod
.MODEL _S5_mod SW VT=2.5 RON=1E-9 ROFF=1E9
L3 29 6 400u
R14 24 20 10K
C4 4 0 3.1u
C5 0 6 3.1u
R17 28 6 16
R13 30 25 100
C6 30 0 0.35u
C8 4 28 3.9u
R15 2 19 100
C7 2 0 0.35u
.END
```

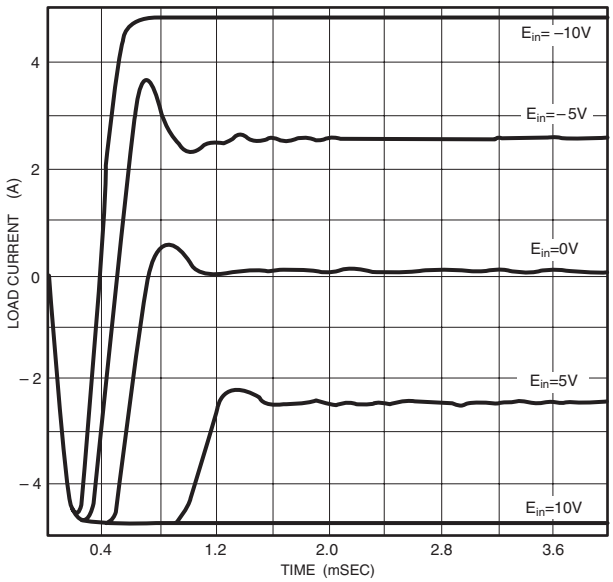


FIGURE 8. Spice-simulation runs indicate the load-current waveforms of the constant-current amplifier for various values of Ein.

–5A. Listing 1 is the complete Spice circuit description for the constant-current amplifier.

CONSTANT–VOLTAGE AMPLIFIER

In applications such as audio-speaker drivers, motor-speed control, and power inverters, you need a constant voltage amplifier. You can use the Apex Precision Power SA02 to design a high efficiency, high-power PWM audio-speaker driver. The SA02 data sheet lists the following specifications:

Analog input voltage/output duty cycles:
Vin=1.25V; AOUT=0%, BOUT=100%
Vin=2.50V; AOUT=50%, BOUT=50%
Vin=3.75V; AOUT=100%, BOUT=0%
switching frequency: 250-kHz
MOSFET on-resistance: 0.42Ω total or 0.21Ω each.

The LC filter design is similar to that of the constant-current amplifier except the LC filter requires no matching network because of the 8Ω resistive load (Figure 9a). The SA02 amplifier's PWM frequency is 250 kHz, so the design sets the LC filter's corner frequency to 25 kHz. The design of the difference amplifier (X4) is somewhat different, however. This constant-voltage amplifier configuration senses the output voltage, not the output current. The voltage at AOUT and BOUT is much higher than the voltage across the current-sensing resistors in the previous example. Instead of boosting the gain, resistor dividers lower the sense voltage to levels that a small signal amplifier can handle. The integrator's (X3) time constant is faster to provide the frequency response necessary for audio applications. The SA02 audio-speaker driver has a –10V/V voltage gain and a 10-kHz power bandwidth. Figure 9b shows the circuit's input and output waveforms. Note that it takes about 50 µsec for the output's sine wave to stabilize.

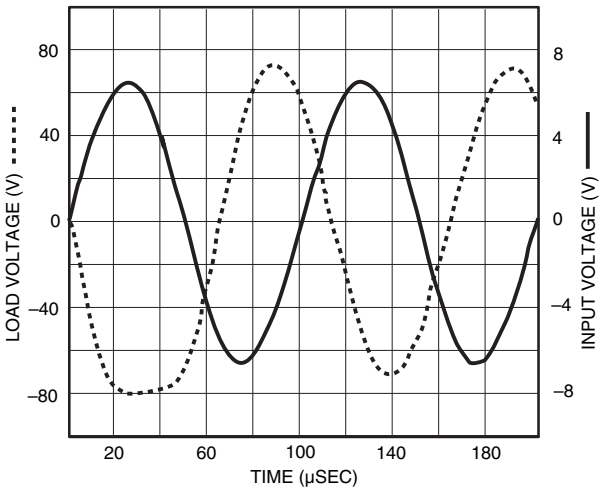


FIGURE 9 (B).

The SA02 has many bells and whistles, such as thermal sensing and external-logic shutdown, that the generic model does not implement. A design engineer can easily analyze these independent features with a paper and pencil. However, this simple yet versatile model makes it easy to model the main PWM function when manual analysis of this feed-back-control circuit becomes unmanageable.

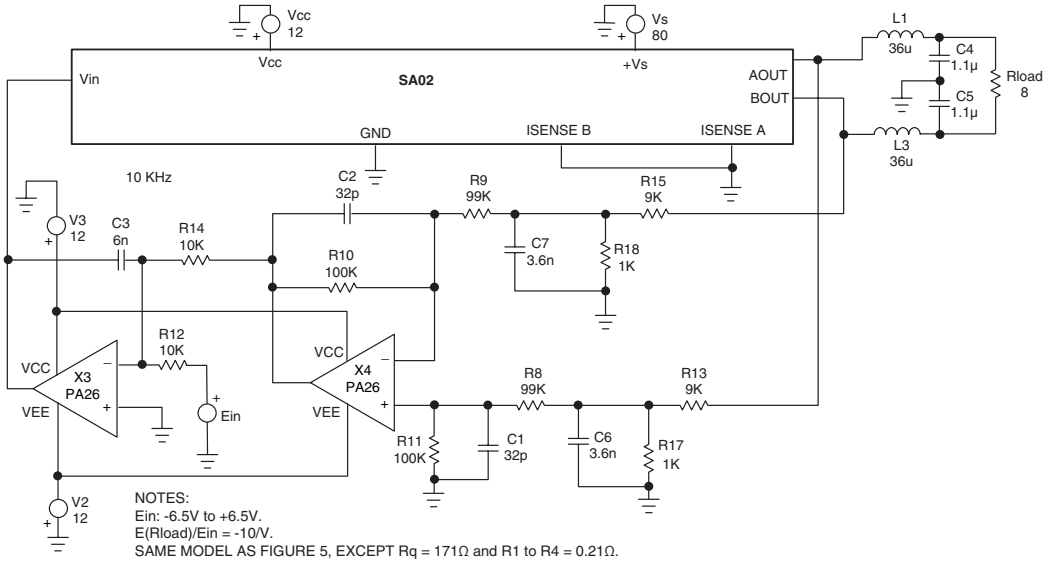


FIGURE 9 (A). A similar model using specifications from the SA02 amplifier is part of a constant-voltage feedback amplifier (a). The output sine wave takes about 50 µsec to stabilize (b).

Power Dissipation the Easy Way

1.0 INTRODUCTION

With the massive amounts of literature on the subject of power dissipation, one may question why any more time should be devoted to such a basic subject. Assume for a moment you have your favorite text book(s) in front of you. Your mission is to look up formulas to find heat both in the load and the driving amplifier. The chances are high that you will find yourself in several chapters before you find Ohm's Law (OK, forget that one), impedance, phase shift and power factor for reactive load elements and finally power dissipation in the amplifier. By now you probably have 10 to 20 formulas with at least three devoted to the amplifier.

Of the three amplifier related equations (typically DC, current-to-voltage phase angles less than 40°, and phase angles greater than 40°), only one may be required. Even the power amplifier data sheet is likely to present two separate thermal ratings for below or above 60Hz. With the proper equations selected and worked out in the right order, you have a wattage rating to apply to the next group of equations needed to select a heatsink. The sad part is that hours have passed.

By the way, did your research turn up a procedure for plotting load lines? This is especially important for bipolar transistor output amplifiers having second breakdown limitations which can be destructive even though a properly selected heatsink keeps the amplifier cool. On top of all this, text covering amplifier power dissipation presents classic circuits where one amplifier using dual symmetric supplies drives a load with respect to ground. This still leaves you on your own when it comes to bridge circuits, single supplies, highly reactive loads at very low frequencies or parallel amplifiers. Calculating power dissipation is anything but a basic subject.

If intuition or experience tells you it would be a major benefit to have one piece of software that remembers all the equations, can select the right ones and can apply them in the right order, then Apex Precision Power's Power Design is a tool you need. It is a Spice alternative dedicated to the analysis of power dissipation and local loop stability of the most common power amplifier circuits. While written with hybrid power operational amplifiers in mind, it can be used with just about any power amplifier from multiple KW discrete monsters down to the monolithic world.

2.0 FASTER WAY TO MORE ACCURATE ANSWERS

The traditional power dissipation equations for amplifiers do not appear in any cell of Power Design. Calculations start by finding peak and RMS values of current, voltage and power (both apparent and true) in the load. For frequencies less than 60Hz, stress levels are picked off the load line plot. This procedure catches some stress levels that can slip by the traditional equations. The DC equation yields peak power levels, but assumes zero current-to-voltage phase shift. Both AC equations account for increased heating in the amplifier due to the phase shift, but yield only RMS power levels. Consider a 5Hz, 60° load where the frequency is too low to use RMS power, but the peak power is substantially more than identical currents and voltages in a purely resistive application.

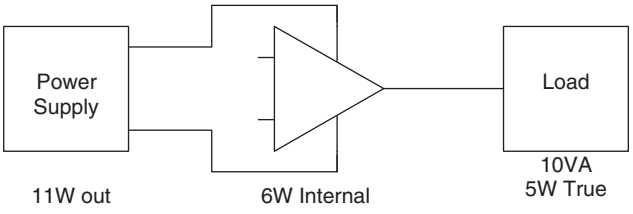


FIGURE 1. A SIMPLE VIEW OF WORK AND HEAT

Power Design next calculates power delivered to the amplifier from the power supplies. For frequencies at or above 60Hz, true power in the load is subtracted from delivered power to yield internal power dissipation. The key element here is knowing what signal amplitude corresponds to worst case power dissipation. A polynomial approximating worst case signal amplitude is used to eliminate the step function found when switching between the pair of traditional equations at the 40° mark.

3.0 THE CLASSIC AMPLIFIER

Figure 2 illustrates the most common power amplifier configuration and the one that relates directly to the traditional power dissipation equations. It is also the starting point for Power Design which will compute power levels for DC and sine wave signals.

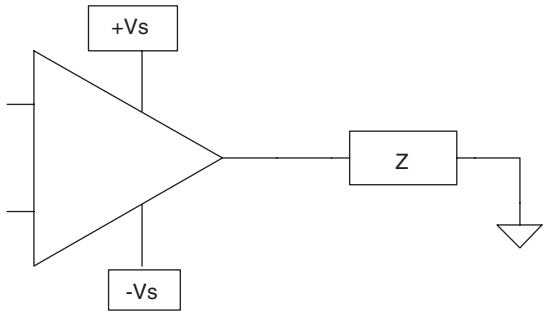


FIGURE 2. THE CLASSIC DUAL SYMMETRIC SUPPLY OP AMP DRIVING A GROUNDED LOAD

All data entry cells in Power Design are yellow on the monitor (shaded in black and white as in Figure 3 shown on next page). The data shown here will be used in the following example. In the top left, a pull-down entry of amplifier model reads an internal database containing enough specifications to flag operation outside the amplifier's capability and to calculate a heatsink rating. The data base contains all amplifiers manufactured by Apex Precision Power and comments in the cells with red triangles tell users how to enter other data. This feature makes Power Design valuable to a very wide spectrum of engineers designing one ton rack mount systems down to monolithic users. Model data has no effect on calculation of load parameters. Going down, enter the supply voltage that will be assumed to be the magnitude of both positive and negative supplies. The next two cells specify minimum and maximum frequencies for the output signal. .001KHz will work fine for most DC applications. Next is magnitude of the output signal followed by a pull down entry labeled "Sig as ?". This is where those magnitude units are defined as volts, amps or watts with choices of peak, peak-to-peak or RMS. Yes, it's that easy to find what is needed to drive a 3.2 ohm speaker to 150W!

If your load can be modeled by one of the four simple dia-

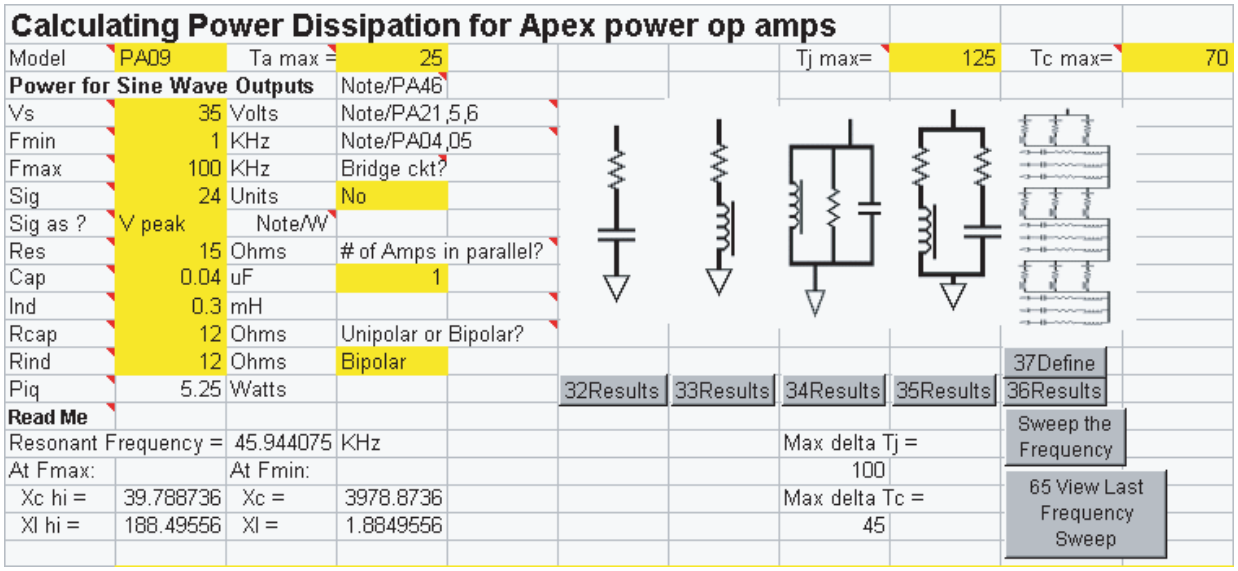


FIGURE 3. POWER DESIGN DATA INPUT SCREEN

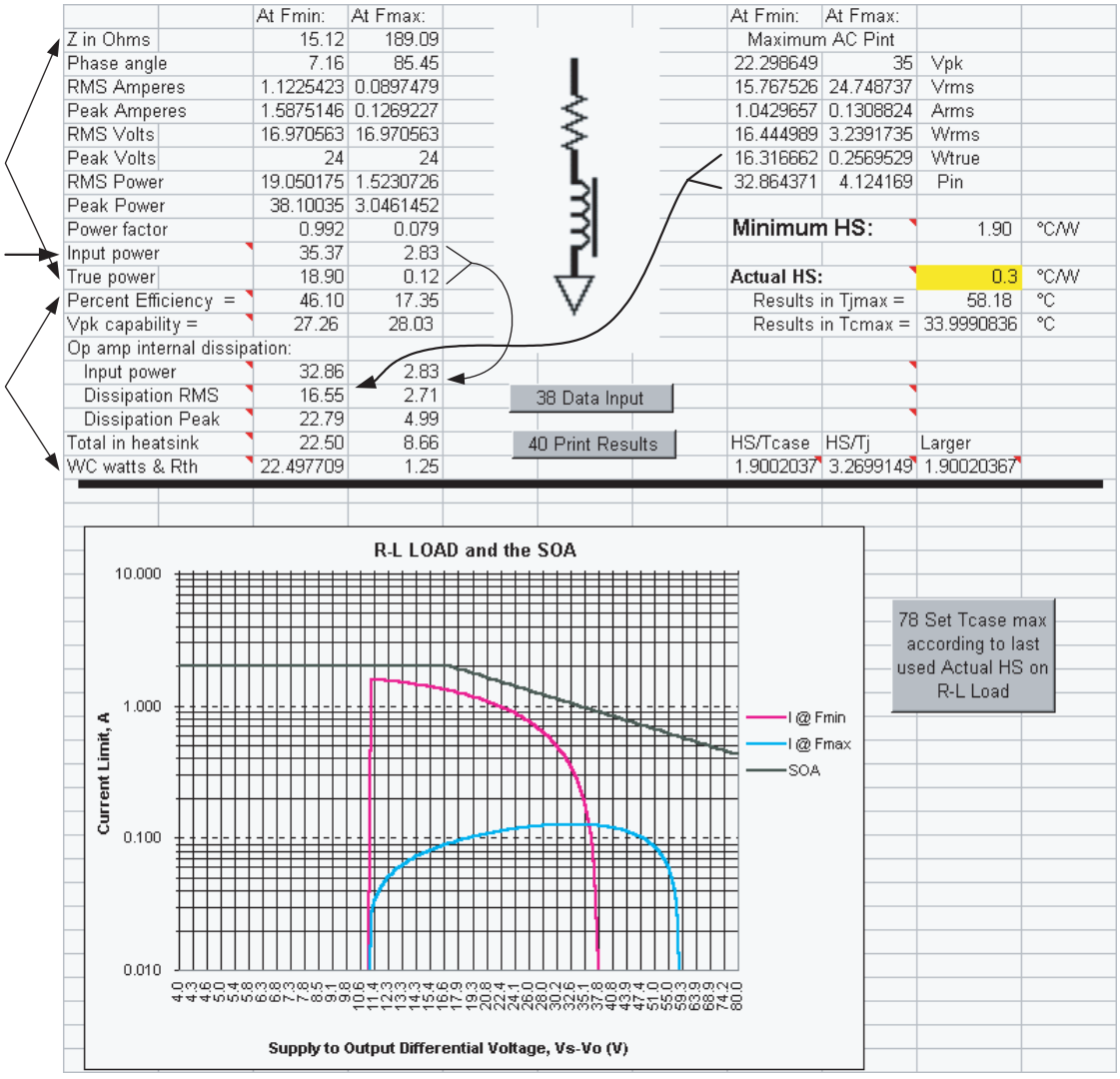


FIGURE 4. ALL THE POWER DATA

Selecting an Apex Heatsink See ACCESSORIES INFORMATION data sheet for specifications

Thermal Resistance		Package		Velocity Calculator:				Units of Measure:
1.96	°C/W	TO-3		15	CFM	2	Inch Width	English
		Update heatsink List		4	Inch Dia	3	Inch Length	
READ ME				171.8873	Ft/min	360	Ft/min	
				0.873198	M/sec	1.8288	M/sec	

Notes:

Beware: Flow rates change as you enter Thermal Resistance, but may be **wrong** until the Command Button is used!

Model	Fluid	Thermal resistance, free air, °C/W	Your rating requires FPM or GPM flow	Package(s) accepted	Style	Length, inches or cm	Width, inches or cm	Heigth, inches or cm	Weight, ounces or grams	Singles Price USD Domestic
HS02	Air	4.5	298.0982	TO-3	Cup	1.81	1.81	1.5	1.89	$16.85
HS03	Air	1.7	0	TO-3		3	4.75	1.25	5.6	$38.45
HS04	Air	0.95	0	TO-3		3	4.75	3	12	$74.85
HS05	Air	0.85	0	TO-3		5.5	4.75	2.63	18.3	$58.60
HS11	Air	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS11	H2O	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS13	Air	1.48	0	TO-3		5.5	4.81	1.312	13.9	$53.95
HS14	Air	2	100	TO-3		3	4.81	1.312	7.6	$33.95

FIGURE 5. HEATSINK SELECTION AND AIR VELOCITY CALCULATIONS

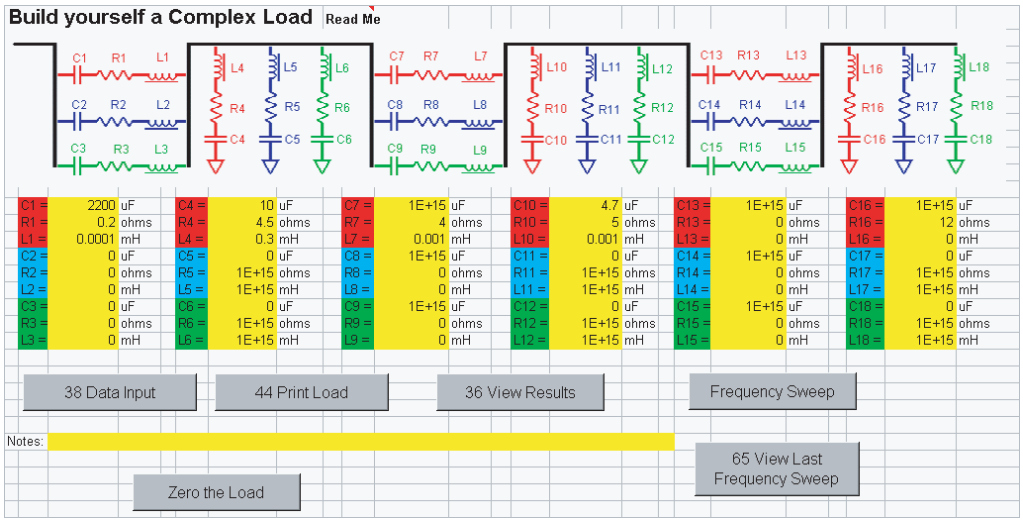


FIGURE 6. THE COMPLEX LOAD

grams keep going down, entering component values. Each load is computed independently so the previous entries other than the 15 ohms and 0.3mH of our current R-L load make no difference. If you have both an L and a C in your load and the resonant frequency is shown as lying between your min/max range, check the READ ME to see if you have a peak or a dip as far as internal power is concerned. If your load is more complicated, you will use the "Define" command button. More on this later. Just below the data entry cells, note the number of watts labeled "Piq." This is the standby power of the amplifier you entered as the Model when running on dual supplies of the value you specified. For hybrid op amps this will be the total quiescent current of the amplifier. For discrete designs, quiescent current would normally be set to the quiescent current of only the output transistors because the driver stages are not normally on the same heatsink as the output transistors.

Referring again to Figure 3, to the right of the signal magnitude entry cell is the pull-down bridge question cell. Make sure this cell contains "No." Below this is the cell specifying the number of amplifiers connected parallel. Make sure this cell contains "1." Below this, we need to specify "Bipolar" output current. From here, go up to enter the maximum ambient temperature your application will encounter. This is the starting point for the heatsink. To the right, enter the maximum junction temperature you wish to allow for the power transistors. 150° is acceptable for many commercial applications but in one respect transistors are just like cars: the hotter your run them, the shorter the life. Using lower temperatures should be considered when down time would be very costly. The last entry cell on this screen is that of maximum case temperature. In addition to life concerns, case temperature affects DC accuracy of the power op amp (check voltage offset and bias current drift) and often has significant affect on current limit values. In this example, a tight DC error budget mandates a maximum case temperature of 70°C.

To see power calculations use the "Results" button under the appropriate load diagram. The entire power data output is shown in Figure 4. Load lines based on voltage output from 90° to 270°. With purely resistive loads this produces one-quarter cycle of current output. With purely reactive loads one-half cycle of current is displayed. In this case the amplifier seems to be loafing at high frequency and is comfortably within SOA at low frequency.

The left side of both curves seems to indicate current drops to zero abruptly. This is not the electrical case, but is a function of Excel plotting routines. Note that at low frequency the load is mainly resistive (only ~7°) and the curve shows maximum current at minimum voltage stress across the conducting transistor (at the peak of the output voltage wave form). It drops to zero current (right end of the curve) at a stress voltage of just a little more than supply voltage or just a little after zero crossing of the output voltage. At high frequency, the load is mainly inductive (~85°) and peak current appears at a stress voltage approaching the supply voltage (near zero crossing of the output voltage). Current does not drop to zero until stress voltage is considerably more than supply voltage or until well after zero crossing of the output voltage. This explains why current drops better than 12:1 from low to high frequency but RMS internal dissipation drops only about 6:1 and peak drops less than 5:1.

This SOA graph is dynamic in that the constant power portion of the curve is drawn to meet the maximum case and junction temperatures you specified earlier. Data sheet graphs usually show one curve for a case temperature of 25°C plus others for

elevated temperatures. All these curves assume maximum junction temperature as published in the product data sheet (up to 200°C on some bipolar transistors) but this is not in the best interest of long-term reliability. Power Design draws only one constant power line according to the case and junction temperatures you specify. If you assign an actual heatsink more generous than the minimum for the application, the constant power curve will be artificially low until you use the "Set Tcase max according to last used Actual HS on..." button.

For details on the load, refer to upper left block of numbers. Just about all the electrical information you could want is detailed. Mixed in here is a line showing power delivered to the amplifier by the power supply (except for quiescent current). "Percent Efficiency =" is based on watts drawn from the supply (including quiescent) and VA delivered to the load. It does not include power factor of the load. "Vpk Capability" is supply voltage minus an estimate of the saturation voltage of the power amplifier at the peak load current.

Turn your attention to the upper right hand corner where the first line of numbers indicate the peak output voltage producing the maximum internal power dissipation. Below this are results of power calculations at these worst case signal levels. The bottom two are the most important:, true watts in the load and power delivered to the amplifier. At low frequency signals, peak internal power dissipation is at about 22.3Vpk, less than the maximum signal amplitude specified earlier. The Power Design assumes real signal amplitude does vary and the amplifier must be able to survive the lower signal level.

The 32.86W is then used on the left (long arrow) as well as the 16.31 true watts that is subtracted from input power to yield "Dissipation RMS" of 16.55W. "Dissipation Peak" is higher than the RMS value but is ignored because minimum frequency is well above 60Hz in this case. "Total in the heatsink" at low frequency is the addition of the 16.55W RMS and 5.25W calculated for quiescent earlier.

The same calculations are repeated for maximum frequency. In this case the very high phase angle demands the amplifier swing all the way to the supply rail (35V) to experience worst case internal heating. As our maximum signal amplitude is less, the input power (short arrow) and true load power are used from the user specified signal amplitude. Again, RMS and quiescent powers are added to find the heatsink total at maximum frequency (peak values are ignored). The last line picks the higher power level of the two frequencies and displays the DC thermal resistance if the frequency is below 60Hz or the AC thermal resistance.

To the right with bold face heading we find the minimum heatsink rating for this application. Your job is to find or design a heatsink and enter its actual thermal rating. Entering the 1.7°C/W rating causes display of case and junction temperatures for the amplifier. A little below this area are the actual calculations which include thermal interface resistance between the amplifier and the heatsink. Separate calculations are made to insure both case and junction limitations are met. In this example, case temperature is the limiting factor. If the heatsink had been sized according to junction temperature only, the case would have been running about 97°, outside the guaranteed performance range for drift with the commercial part.

In this general area you may also find up to three warning flags. The most common warning is for excessive temperatures. The other two warnings will pop up if your application is demanding more voltage or current output than the amplifier is specified to deliver. The voltage calculation takes into consideration the supply voltage and the output saturation characteristics of the amplifier.

If you're asking what's so magic about 1.7°C/W, refer to Figure 5 where an Apex Precision Power heatsink can be selected. To use this sheet, simply enter the desired heatsink rating and package type, then click on the command button. Even though our example used the HS03 without a fan, note that an HS02 inside a 2"x3" duct fed with a 15CFM fan would be more than adequate to produce the required thermal rating.

4.0 USING THE COMPLEX LOAD

Using the load shown in Figure 6 requires complex numbers which most Excel users do not automatically activate. You will probably need to use Tools, Add-Ins and Analysis ToolPak. Unless you have known good data already entered, use the "Zero the Load" button to place extremely high impedance components in all the vertical strings with a ground connection and extremely low impedance components in the horizontal strings.

Refer to the sample load diagram in Figure 7 to illustrate data entry. Let's start on the left at the amplifier connection. Use any one of the three strings for the capacitor. Note that we are also entering values for ESR and ESL for the capacitor. These may be found on the data sheet or measured with an impedance analyzer. R1 is used to model ESR of the 2200uF capacitor and L1 to model ESL. It is important to open the other two unused strings in parallel with our component model. The easiest way to achieve this is entering zero capacitance in each string. Our second group of components could again use any of the three strings with a ground termination. The resistor is actually a coil and parasitic inductance is also entered. Proceed through groups of components until finished.

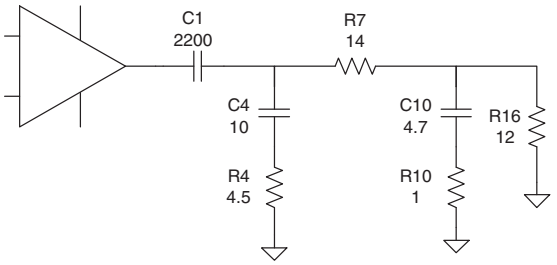


FIGURE 7. A SAMPLE COMPLEX LOAD (PARASITICS NOT SHOWN)

After entering your load data, the "View Results" button will show performance at the minimum and maximum frequencies. To see what's happening in between, press the "Frequency Sweep" button. Figure 8 illustrates typical results of a sweep. This specific load shows the need to analyze carefully in the low KHz area.

Setting the min/max frequencies to 2/4KHz and re-running the sweep as shown in Figure 9 will allow a more precise determination of the peak values for current output and internal power dissipation. Notice that peaks and dips do NOT coincide exactly. In this case set Fmin to 2.54KHz and Fmax to 2.84KHz and click "View Results" to see maximums in numerical form and select the heatsink rating.

5.0 NORMAL BRIDGE CIRCUITS ARE EASY

The master/slave approach shown in Figure 10 is an easy way to implement a bridge circuit. The master maybe be configured any way desired. The job of the slave is to invert the master's output such that the load is driven equally but opposite at its two terminals. The schematic suggests calculating internal power dissipation might be tricky, but not so when using Power

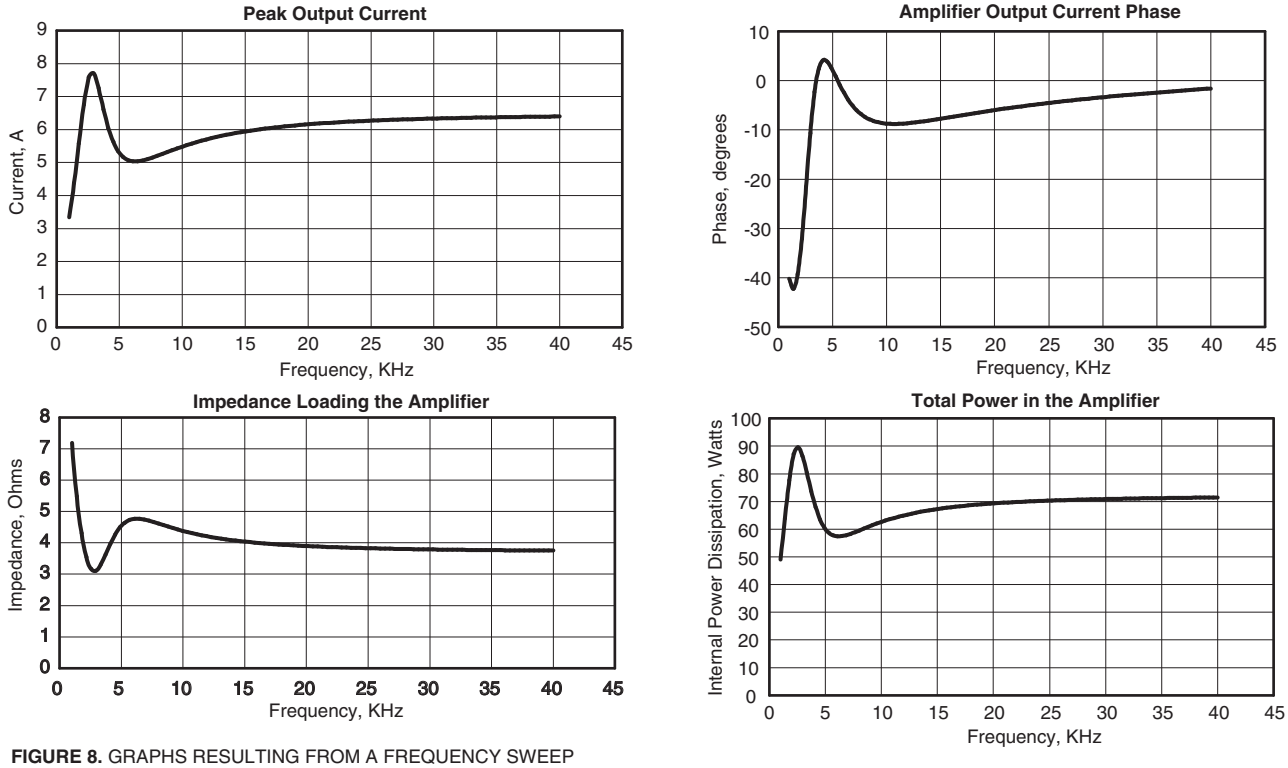


FIGURE 8. GRAPHS RESULTING FROM A FREQUENCY SWEEP

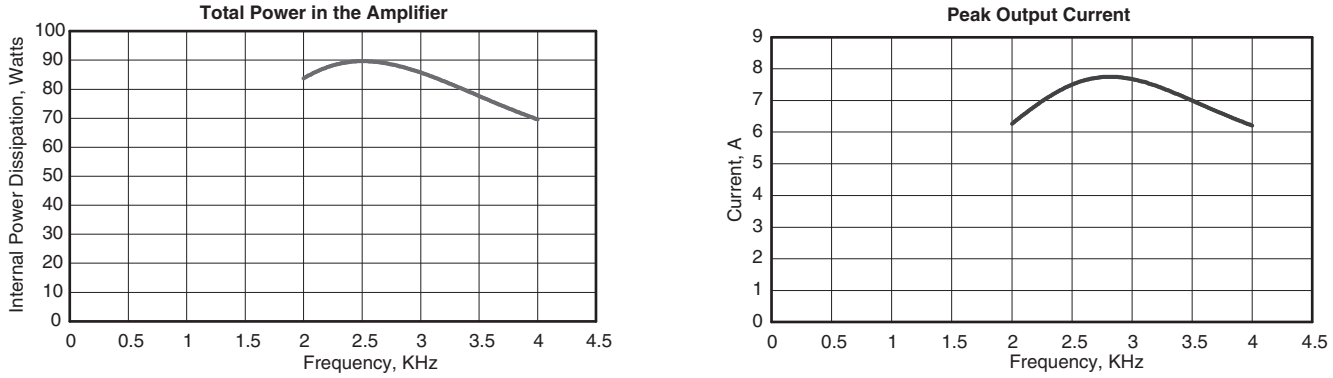


FIGURE 9. ZEROING IN ON THE PEAK VALUES OF A COMPLEX LOAD

Design. Enter signal amplitude applied to the total load, enter the total load components, enter "Yes" for the bridge question and all the modeling is taken care of automatically. Load impedance shown will be the total value, currents are for load and each amplifier. Voltages, wattages and heatsink ratings are for a single amplifier and are flagged as such.

6.0 SINGLE OR NON-SYMMETRIC SUPPLY BRIDGES REQUIRE A TRICK

The circuit shown in Figure 11 is often used to achieve bi-directional drive on a single supply or to double voltage swing capability when a single higher voltage amplifier is not cost effective or does not exist. To easily accommodate ground referenced small signal driver circuits, a small negative supply is often used to overcome common mode voltage restrictions.

Note that zero drive to the load requires both amplifier outputs to be equal to that of the voltage divider (two equal resistors). This forces the center of the load to be constant and at 50% of a true single supply or centered between the two supply voltages. If one algebraically subtracted the correct voltage from both the positive and negative supply pins of the amplifiers and the lower divider termination, you would end up with operation identical to the symmetric supply bridge of Figure 10.

For Power Design to analyze this circuit, enter a supply voltage equal to half the single supply or half the sum of the absolute values of both supplies. For 110V single supply, enter 55V. If an opposite polarity supply of 10V is added, enter 60V.

7.0 BIAS LEVELS ON AC ONLY LOADS

There are two bias voltages to determine with AC only loads; one affects internal power dissipation, the other does not. Refer to Figure 12, noting that neither bias level affects output current. The DC blocking property of the load capacitance means current demand is a function of only the load impedance and the applied AC signal. DC bias levels can be ignored, even if they result from the load being terminated at one of the amplifier power supplies or a separate supply. While constant load bias has no affect on internal power dissipation, output bias directly affects voltage across the conducting transistor and therefore power levels. Power Design always assumes output

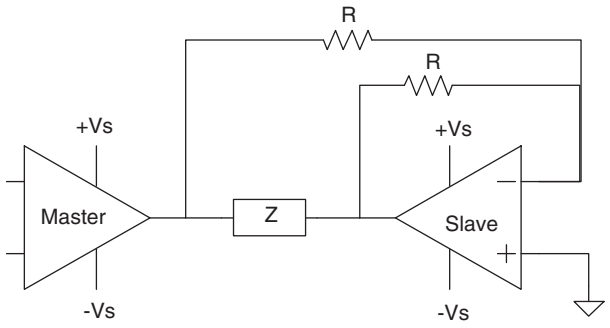


FIGURE 10. THE MOST COMMON METHOD USED TO IMPLEMENT A BRIDGE CIRCUIT

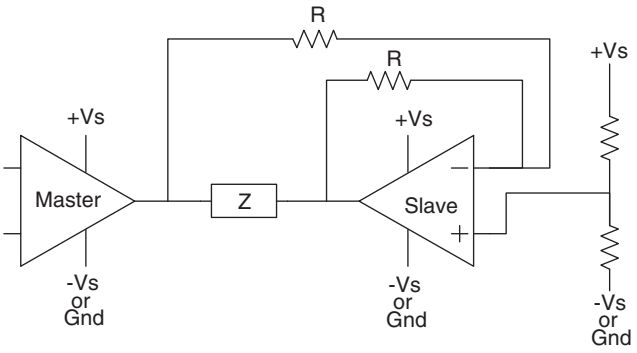


FIGURE 11. THE CLASSIC NON-SYMMETRIC BRIDGE CIRCUIT

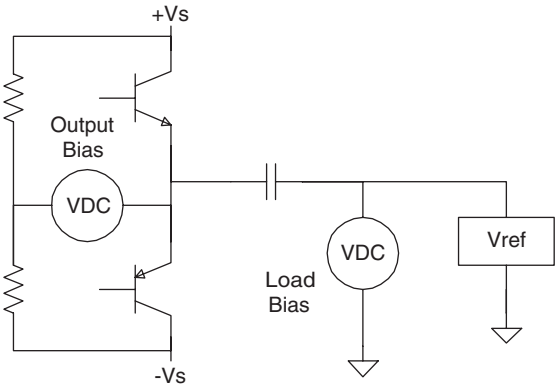


FIGURE 12. BIAS LEVELS FOR AC ONLY LOADS

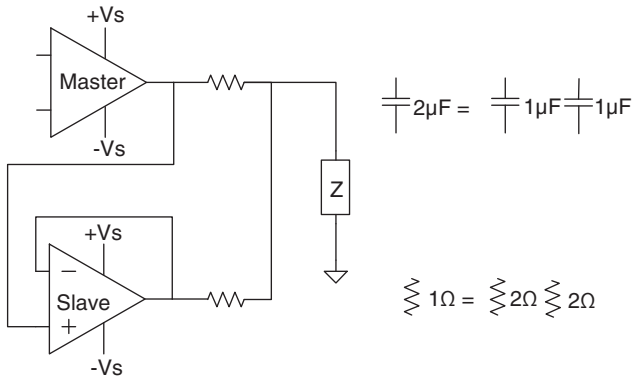


FIGURE 13. A COMMON PARALLEL CIRCUIT AND CIRCUIT ALGEBRA TO MODEL A SINGLE AMPLIFIER'S LOAD CURRENT

bias is zero meaning equal power dissipation in both transistors.

Given a requirement to drive a capacitive load at 7.07VAC riding on 100VDC, the least expensive op amp solution would be a 100V reference supply and a low voltage op amp. The catch is that this reference supply must sink and source current. If using an output filter capacitor 10 to 100 times the value of the Cload is acceptable, this type solution is likely to be lower cost overall. Remember that if these two capacitance values are constant, the resulting drive voltage errors due to the non-zero impedance of the reference supply can be compensated by increasing the drive signal.

Refer to TABLE 1 for a way to approximate power levels given the following assumption: +120V and -10V will be used to accommodate voltage saturation on the high side and common mode voltage on the low side. Calculate voltage stresses on each transistor from mid point of the sine wave to each supply. In this case, 20V to the positive supply and 110V to the negative supply. Run two calculations using each of these values. Select an arbitrarily large initial heatsink value. The numbers in TABLE 1 are a result of a PA88 driving 15 ohms and 0.04uF at 40kHz with Ta=25°, Tc max=70 and the actual heatsink 1.7°C/W. Subtract case temperatures from junction temperatures to find temerature rise. The 110V data tells us the hardest working transistor is 35.5° above case temperature. The 20V data tells us the other transistor is only 6.2° above case temperature. Now set supply voltage to 65V (the average of 110 and 20) to find a minimum heatsink rating of 10.3 °C/W is required. Enter an actual heatsink rating, such as 4.5°C/W corresponding to an Apex Precision Power HS02 with no fan. To find a case temperature of 44.8°C add to this the previously calculated temperature rises. To find the output transistors junction temperatures of 80.3° and 51°C. Iterate the last step if this is too hot.

Vs	Tj	Tc	Delta	Heatsink
110	73.2	38.2	35.5	6.1
20	33.5	27.3	6.2	

TABLE 1. MULTIPLE PASS METHOD OF DETERMINING TEMPERATURE WITH DC BIAS ON A CLOAD

8.0 TECHNIQUES FOR PARALLEL OPERATION

Calculation methods for parallel operation of power amplifiers is simple; however, getting two or more power amplifiers to cooperate rather than kill each other is often quite another matter. Power Design assumes all the precautions of Apex Precision Power Applications Note 26 PARALLEL CONNNECTION or some other authoritative reference have been followed. Potentially destructive currents between amplifiers are NOT modeled. Causes of these currents include voltage offset, common mode errors and violations, phase shift, and current limit sequence errors. If you have overcome all these, refer to Figure 13 for the most common approach to parallel operation along with a way to think about an equivalent load for the single amplifier.

To use Power Design for parallel operation, enter the number of amplifiers in parallel in the yellow cell below the bridge question. Total values are then calculated for the load results area and scaled by the number of amplifiers for the SOA graph and amplifier internal power dissipation results. The heatsink rating will then need to be applied to each amplifier.

9.0 UNIPOLAR OUTPUT CURRENT

Programmable Power Supplies (PPS), Thermo-Electric Coolers (TEC) and heaters are often configured for current

Uni-polar Current	At Fmin:	At Fmax:		At Fmin:	At Fmax:		
Z in Ohms	15.12	15.17		Maximum AC Pint			
Phase angle	7.16	8.58		22.298649	22.377096	Vpk	
RMS Amperes	1.1225423	1.1187227		15.767526	15.822997	Vrms	
Peak Amperes	1.5875146	1.5821128		1.0429657	1.0430736	Arms	
RMS Volts	16.970563	16.970563		16.444989	16.50455	Wrms	
Peak Volts	24	24		16.316662	16.320037	Wtrue	
RMS Power	19.050175	18.985354		32.864371	32.86777	Pin	
Peak Power	38.10035	37.970708					
Power factor	0.992	0.989		**Minimum HS:**		2.25	°C/W
Input power	35.37	35.25					
True power	18.90	18.77		**Actual HS:**		1.7	°C/W
Percent Efficiency =	50.14	50.12		Results in Tjmax =		88.23	°C
Vpk capability =	27.26	27.26		Results in Tcmax =		59.5109188	°C
Op amp internal dissipation:							
Input power	32.86	32.87					
Dissipation RMS	16.55	16.55	38 Data Input				
Dissipation Peak	22.79	23.24					
Total in heatsink	19.17	19.17	40 Print Results	HS/Tcase	HS/Tj	Larger	
WC watts & Rth	19.172733	1.6		2.2470833	3.6179691	2.24708327	

FIGURE 14. OUR CLASSIC EXAMPLE TURNED INTO A UNI-POLAR CURRENT OUTPUT AMPLIFIER

of only one polarity. This means only one output transistor is doing the work and therefore the DC thermal resistance specification of the amplifier must be used even if the signal frequency is quite high. Most op amp data sheets footnote the AC rating as applying if current alternates between the two output transistors are at a rate greater than 60Hz. The mechanism yielding an improved AC rating is simply a larger square area of the package materials used to conduct heat when two transistors are active.

All the previous examples assumed output current was bipolar. In cell D13 (under the parallel question), you can enter "Unipolar" to force all heatsink calculations to be based on DC thermal resistance and change the quiescent power calculation to reflect the supply voltage you entered as being a true single supply, plus change the supply problem flag.

A word of caution is in order here. Many loads will demand bipolar current even though the voltage is uni-polar. The easiest to visualize is the capacitive load: current flow is determined only by rate of change and direction of change. Both positive and negative direction changes can be achieved without changing polarity. A good rule of thumb is to not use this feature if the phase angle for your load is greater than 10°.

If your application uses a low voltage supply opposite a high voltage supply which is doing all the work, enter the high voltage supply ignoring the low one. This will result in an error in quiescent power by a factor of Iq*Vs low (usually negligible).

Returning to our classic example with the PA09, reducing the maximum frequency to 1.2KHz and setting cell D13 to "Uni-polar" results in data shown in Figure 14. The frequency change keeps us within the 10° limit. Note that neither peak nor RMS power dissipation has changed but total in the heatsink has come down 2.63W. This change is due to total supply voltage being reduced by 35V. Thermal resistance used has jumped from 1.25°C/W (AC rating) to 1.6 (DC rating). Just as before, the limitation of this application is case temperature rather than junction temperature. It is interesting to note that the same heatsink now produces a case temperature about 5° lower but the increased thermal resistance produces junction temperature only 1° lower.

10.0 A LITTLE 'WHAT IF?" GAME

You have a PA12A rated at +/-50V, 15A, 125°C case, 200°C junction. It can drive to within 5V of the rail at 5A and to within 6V at 15A. How much power can be delivered when mounted on a 0.5°C/W heatsink?

The first correct answer is: "that depends". Start with a sine wave driving a 225 ohm pure resistor which will be voltage limited. We need no help on this one; 45V peak output will drive .2Apk or 9W peak or 4.5W RMS. Yes, a ridiculous job for the PA12A but it shows the importance of impedance matching. Set up the PA12A as above, set the signal to 44Vpk and define the load as 4.4 ohms (0mH). This would be 10Apk, 440W peak and 220W RMS. Can it be done? Still "depends". If you have a frequency below 60Hz, no; if not, we are just barely over the limit. Assume we must operate below 60Hz. What can we do? Lower the peak output voltage and the supply voltage by equal amounts until the TOO HOT flag goes away. Did you arrive at something like 120W RMS and 240W peak?

Change the rules just a bit; stay below 60Hz, but you may vary the load resistor to achieve maximum output power. High power demands high efficiency which means saturation voltage loss (a relatively constant value) must be small compared to output voltage. This means maximum supplies and signal level should be used. Now enter increasing values of load resistance until the TOO HOT flag goes away. Did you get something like 7.35 ohms, 132W RMS and 263W peak?

This time I have looked up the specs on a high quality woofer: 8 ohms nominal impedance, 5.9 ohms resistive, 0.93mH inductance, 40Hz to 4KHz usable frequency range. The amplifier is too hot at maximum supply and signal levels, so bring them both down. How does 122W RMS at 40Hz but only 30W at 4KHz sound?

One last item: The circuit will use -5V and +95V, resistive load at DC. You tell me the rest of the story.

11.0 CONCLUSION

The Apex Precision Power Power Design Tool automates examination of sine wave power levels of both the load and the power amplifier. Gone is the need to remember or look up multiple formulas or even decide which ones to use. With almost instant plotting of load lines with plenty of resolution, the tendency to scrimp on this part of power design is eliminated. With frequency sweep capability, sweet points or hot spots of complex loads can be quickly located. While aimed at and containing a database of power amplifiers from Apex Precision Power, this tool is usable for just about any power amplifier application. It is available free of charge at www.Cirrus.com.

Please remember that answers to perfect calculations are only as accurate as the input data and assumptions they are based on. Do not let the bad news of poor assumptions ruin your day. Here are some things to consider: How good is the power supply regulation? Does load impedance change with temperature, current, voltage or mechanical loading? How well were all the parasitic values nailed down? What is the phase margin of the circuit? What is the reduction in airflow due to backpressure?

There is still no excuse to skip measurement of operating temperatures on your equipment under worst case operating conditions. With Power Design, these measurements are more likely to say “Job well done!” than “Oops”.

PS. About 303W (SOA graph will be fine when case temp is set to 77.5°C).

Other Application Notes in this “Power Design Tool” series are: Application Note 38: Loop Stability With Reactive Loads Application Note 39: Filters & Power Dissipation for PWMs

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Loop Stability With Reactive Loads

INTRODUCTION

One definition of an oscillator: A circuit with gain and a total phase shift of 360°. Usually 180° comes from the ideal amplifier being inverting. The remaining shift comes from feedback elements and the non-ideal portion of the amplifier.

A second definition of an oscillator: A circuit the power amplifier designer has nightmares about.

If you are looking for a l o n g and b o r i n g Application Note with lots of formulas you no longer remember how to deal with, this is not the document for you. This article works in conjunction with the Apex Precision Power Power Design CAD tool to remember and apply correctly all the rules and formulas, thus allowing concentration on the big picture. As a toddler, you probably had toys that gave you the "feel" that square pegs do not fit in round holes. The objective here is to give you a "feel" for what curve to bend in which direction allowing you to slay the evil dragon of power amplifiers, the oscillator.

WHY THE DRAGON APPEARS

By far and away, the most common cause of oscillation is lack of adequate supply bypassing! This is often true even of circuits having hundreds or even thousands of microfarads of bypass. It is all too easy to forget details such as:

1. The amplifier has gain into the MHz range even when used at DC.
2. In the MHz range, some capacitors have significant inductive reactance.
3. Even a straight piece of wire has inductance.
4. Resistance of PC traces and even wire makes a difference in power circuits.

Bypassing supplies for a power amplifier is such a broadband job that it often requires multiple sets of components and demands proper placement of each set. For the high frequency spectrum (this includes the frequency where the amplifier runs out of gain) the use of small value ceramic capacitors placed right at the pins of the amplifier is required. In the range of the signal frequency, capacitors will be larger in value and physical size so they will be further from the supply pins of the amplifier. Relying on the output capacitors of the power supply may be acceptable, but not if they are multiple feet from the amplifier.

The second most common cause of oscillation is the elusive ground loop. Refer to Figure 1 for an over-simplified picture of the problem. Load currents flowing through the parasitic impedances in the line back to the supply, develop voltages which are inserted as positive feedback. To break the loop, designate one physical point as the center of a star ground. Make sure every connection to ground has its own path to the center of the star. Do not forget the low side of the bypass capacitors. The best news about this problem is that the frequency of oscillation usually points to the cause by being right at the unity gain frequency of the amplifier.

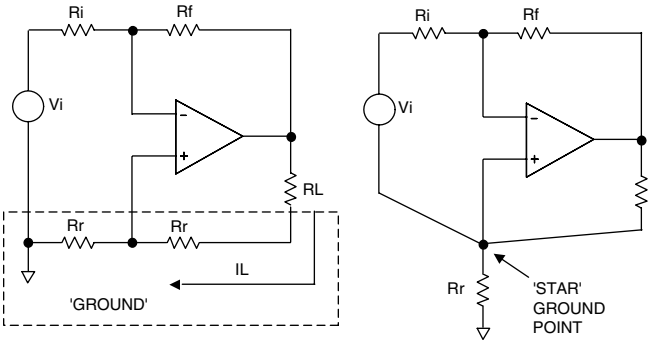


FIGURE 1. GROUND LOOPS AND THEIR SOLUTIONS SIMPLIFIED

The least common cause of oscillation is related to design of the output stage of the amplifier itself and also raises a flag to identify itself. If the oscillation is above the unity gain frequency of the overall amplifier (below 0db on the bode plot), we have a local feedback problem in the output stage. First, check supply bypass. Then try a snubber network (series R-C connected from the output to ground) in the range of 1 to 10 ohms and 0.1 to 1uF.

What about exceeding the capacitive load specification that appears on most op amp data sheets? This refers to Cload with the amplifier connected in a unity gain configuration. We will examine means to circumvent this limitation.

THE GROUND RULES DEFINING THE PLAYING FIELD

With the above out of the way, we can attack the real subject of this article-taming oscillations caused by the non-ideal characteristics of the amplifier and feedback elements. A few more definitions are in order:

Closed loop response is the relationship between the input and output signals of the total amplifier (including feedback). We will be looking at both the gain and the phase of this response.

Open loop response is the relationship between the input and output signals of the amplifier without feedback. This response does not go away when we close the loop. It is still the input to output pin relationship and it does affect closed loop response.

Loop gain is the difference between the open and closed loop gains. This is the magic of op amps allowing overall circuit function to be primarily a function of feedback elements. It allows an op amp to be a general purpose building block. More loop gain means the circuit will be more faithful to the ideal closed loop response.

Beta is the fraction of the output signal fed back to the negative input of the op amp. We refer more often to the reciprocal which is closely related to inverting signal gain. It is imperative to note that stability analysis is treated as a non-inverting circuit, just as when calculating the effects of voltage offset on the output signal. This means gain, or 1/beta can never go below one or 0db.

Intersection rate is the slope difference between the open and closed loop roll-off at the point where they cross.

Closure frequency is the frequency where open loop gain is 0db. Above this frequency the circuit can not meet the definition of an oscillator.

Phase margin is the difference between the 360°of the oscillator definition and the phase shift of the total circuit at closure frequency. In practical circuits, it is recommended that all frequencies below closure be examined as well. Note also that by using negative feedback to close the loop we have the first 180° of phase shift needed to oscillate simply from the inverting function of the op amp. The phase plots you will see do not reflect the inversion, only the change over frequency. This further means that on all the phase plots to follow, phase

margin will be the difference between the curve and 180°.

Phase margin is the buffer zone between the power amplifier and the power oscillator. 45° is desirable, more is better, never accept less than 30.

Straight line approximation is the technique used to plot most of the response curves to follow. While real performance would be represented by smooth curves, the straight segments make it much easier to pinpoint corner frequencies. The penalty in terms of phase accuracy is +/-6°.

SNAP SHOT OF A CLASSIC AMPLIFIER POWER DESIGN MECHANICS

The data entry screen of the Cload sheet is shown in Figure 2. Yellow cells are for data entry and their labels correspond to component labels of the schematic. Entering actual, extremely high or zero values can model the most common stabilization techniques. Comment cells will instruct you how to enter data for your own operational amplifier, but Apex Precision Power hopes you will use the pull down to select one of theirs from the built-in data base. The first thing Power Design should be able to do is duplicate the small signal response (or bode plot) and the open loop phase response of the given amplifier.

For amplifier models featuring external compensation, Power Design uses a three digit suffix to specify compensation capacitor values detailed on the product data sheet. The Rcl entry allows entry of the current limit setting used with most power amplifiers. Enter the remaining circuit values according to your application. Setting up the PA85 (compensated for unity gain) as a unity gain buffer (Rin=very high, Rf=very low) will produce the graphs shown in Figure 3. Open loop response should duplicate what is shown in the data sheet, or measured values of your own amplifier.

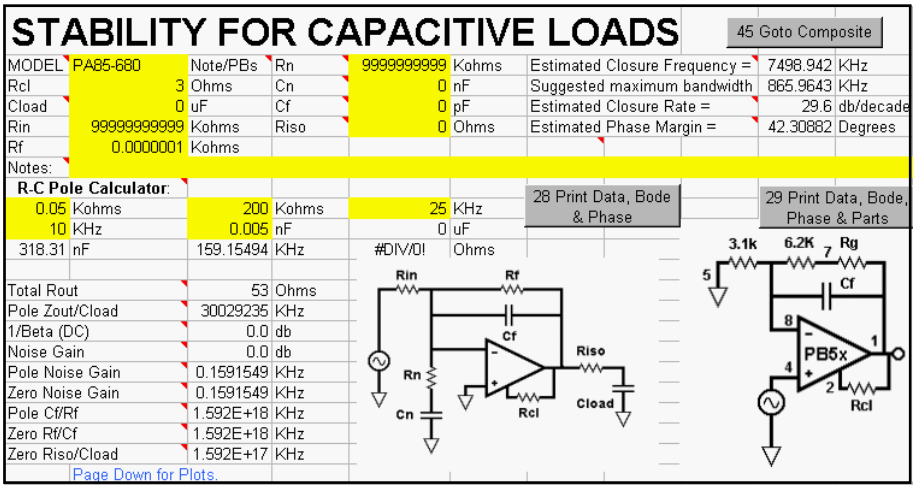


FIGURE 2. DATA ENTRY FOR CLOAD ANALYSIS

Notice the first smooth curves in the Phase Shift Graph. The right most curve plots the closed loop phase shift of the complete circuit. For example, phase shift at 40KHz is about 7°. For those times when phase shift at lower frequencies is of interest, factors of 10, 100 and 1000 scale the other three curves. Phase shift at 400Hz would be about 0.007°.

In the upper right corner of Figure 2, are some answers that illustrate what this whole exercise is about. The most important answer is phase margin where we like to see 45°. Closure (intersection) rate is a key indicator of health, where 20 is the desired number. The number is usually a multiple of 20 but as you see here, when the intersection and a corner

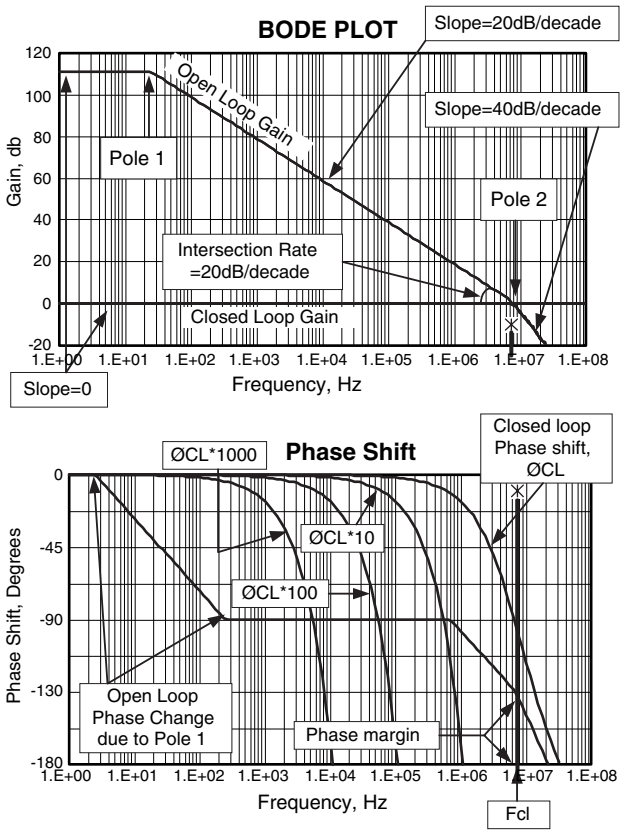


FIGURE 3. UNITY GAIN STABLE AMPLIFIER CURVES

frequency are nearly coincident, it may fall in between. The suggested maximum bandwidth is the frequency where loop gain is down to 20db. This is very much a judgement call and will be application dependent. Remember the basic op amp theory where various internal errors are reduced by the loop gain when the circuit is closed. For example, open loop output impedance (affecting gain accuracy) of 10 ohms would be a killer with a 1A output. If the circuit has 40db of loop gain, this error drops from 10V to 0.1V. Demanding this 40db would reduce the suggested maximum bandwidth by a decade.

The unity gain stable op amp will have its first pole at a low frequency and the second pole will not appear until open loop gain has crossed 0db. The horizontal line at 0db indicates closed loop unity gain operation. Notice that pole 1 of the open loop response is at roughly 25Hz, that phase started moving a decade before this and within 2 decades has moved 90*. We find the second pole at about 7MHz and again phase starts moving a decade before. While the third pole does not show on the bode plot, a corner in the phase plot around 7MHz tells us pole 3 is near 70MHz. The main point of interest for stability concerns is at Fcl where intersection rate is 20db per decade and open loop phase is about 135°. This means the phase margin is about 45°.

The R-C Pole Calculator is a convenience item having no effect on any of the results. However, it does make it easy to translate

graphic data to component values. Below this are listed many of the operating points of the circuit. As experience is gained using this tool, you will start using some of these numbers directly to eliminate paging down to the graphs.

In contrast, Figure 4 shows the same amplifier compensated for a gain of 100, but still configured for unity gain. Pole 1 has moved up in frequency giving us a greater gain-bandwidth product, but notice that pole 2 is now well above 0db and the intersection rate is 40db per decade. Our phase margin has disappeared. This example is a little radical, but it does show the dangers of improper compensation. There are also some op amps having a minimum gain specification which would fit this same general picture if used below the minimum gain spec.

In the following examples, we will first attempt to obtain an intersection rate of 20db per decade (a very good sign but not a guarantee) by visualizing line segments and then checking out the actual phase graph.

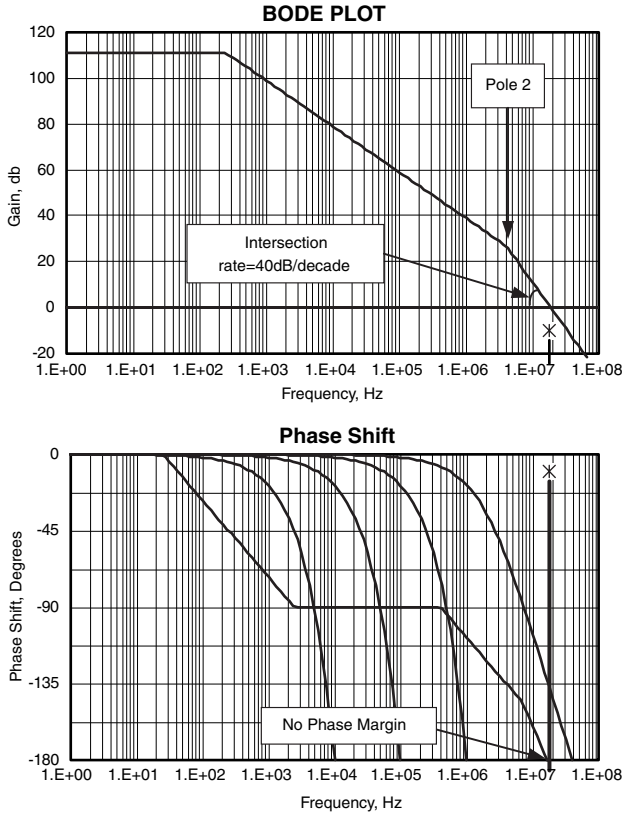


FIGURE 4. ATTEMPTING TO USE AN AMPLIFIER BELOW SPECIFIED MINIMUM GAIN

LARGE CAPACITIVE LOADS CAUSE PROBLEMS

Open loop output impedance of an amplifier forms a pole with a capacitive load, which is modeled as an additional pole in the small signal response as shown in Figure 5. This is our same amplifier (compensation recommended for gain=20), attempting to drive a heavy Cload with an inverting gain of 19. Note that this pole introduced with the addition of an external component is causing the same 90° shift of phase; 45° taking place below the pole frequency and the other half above. Any time the combination of Zout (sum of the amplifier output impedance and any other resistance inside the loop) and Cload is large enough to place this pole below closure frequency. The intersection rate will no longer be 20db per decade and stability will be in question.

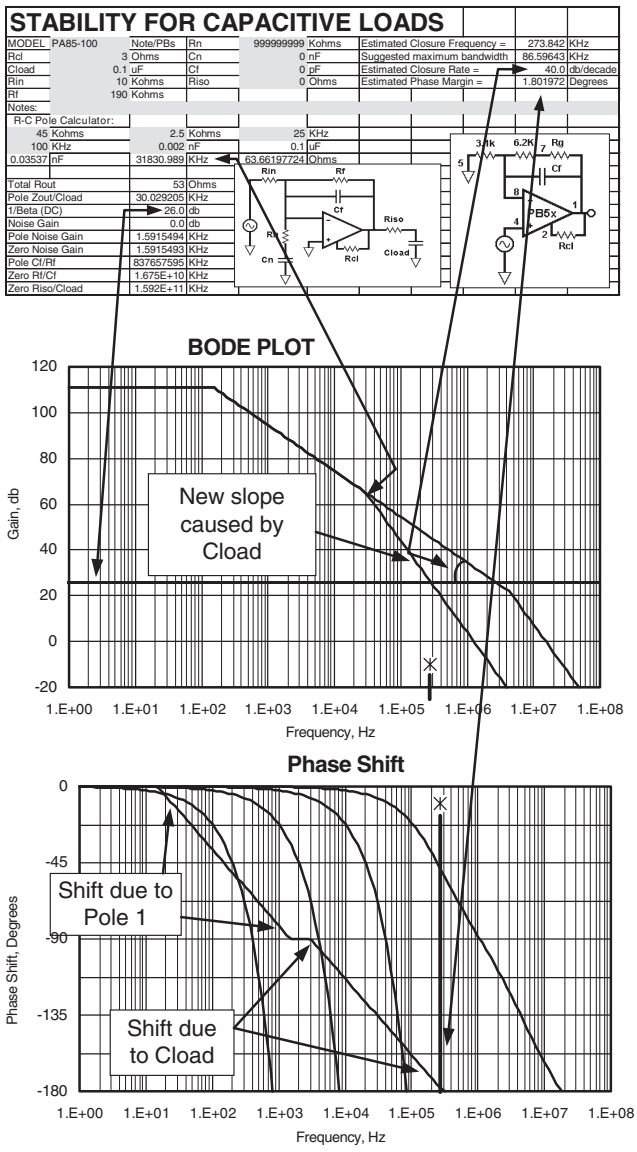


FIGURE 5. MODELING A LARGE CAPACITIVE LOAD

It is now time to start the process of visualizing potential solutions. We know good intersection rate is a key. Sometimes we can change amplifier compensation to move the open loop response, but usually not enough to cure this problem. One thing we might do is increase the closed loop gain to 66db. Entering Rin=.1 results in the data shown in Figure 6 (next page) where the stability problem now looks fine with a phase margin of ~45°. There are several problems associated with this solution. The most obvious is that we have changed the closed loop transfer function which now requires other system changes to compensate. Next, DC errors due to voltage offset and drift are up by a factor of 100! Also notice that if we demand the recommended 20db of loop gain, circuit bandwidth is only ~2.7KHz, about a factor of 30 reduction. This solution is rarely acceptable.

USING AN ISOLATION RESISTOR

Go back to Figure 5 and imagine we have the power to grab the segment modeling the effect of our Cload, just above the intersection point (about 200KHz & 30db) and bend it back to a minus 20db/decade slope. This would result in a new inter-

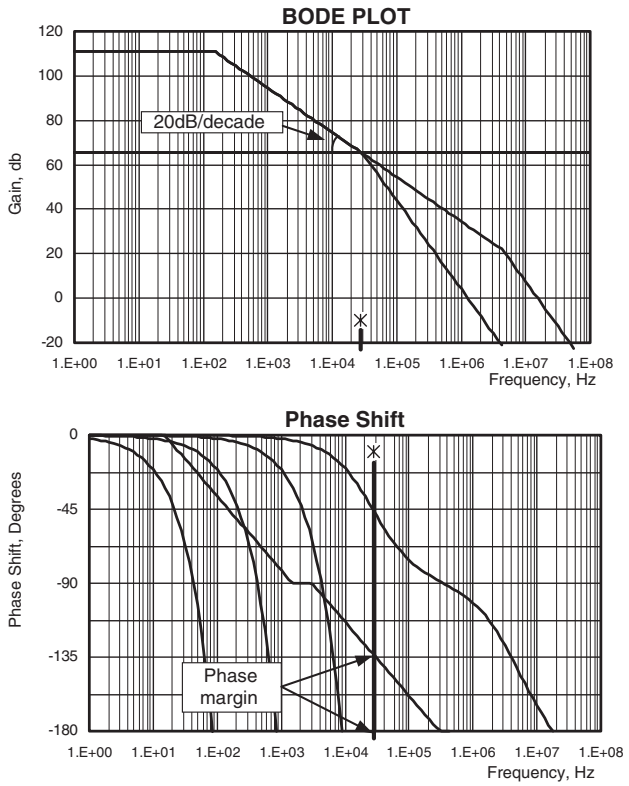


FIGURE 6. INCREASED GAIN YIELDS ACCEPTABLE PHASE MARGIN

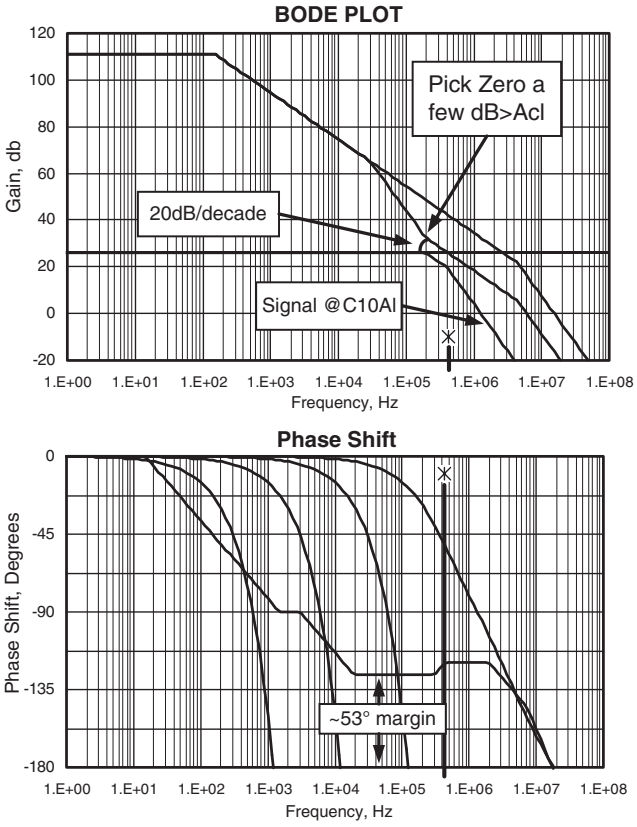


FIGURE 7. AN ISOLATION RESISTOR IS OFTEN THE BEST STABILIZATION METHOD

section rate of 20db/decade. This is exactly what an isolation resistor does for us! The R-C Pole calculator is pre-loaded with the Cload value and prescribes 8 ohms when we enter the corner frequency of 200KHz. Figure 7 shows the results of entering 8.2 ohms as Riso.

What about larger values of Riso? They will produce stable circuits but there are two things you need to know. Riso is outside the feedback loop where voltage drops and phase shifts are not corrected by loop gain. The curve labeled “Signal at Cload” shows roll off of the signal at the actual load. Check Figure 8 to see the effect of increasing Riso to 40 ohms. The load is now rolled off at 40KHz cutting usable bandwidth to about half that of the 8.2 ohm solution. The suggested maximum bandwidth cell does not take this into account. Also, phase shift outside the loop is not reported by Power Design.

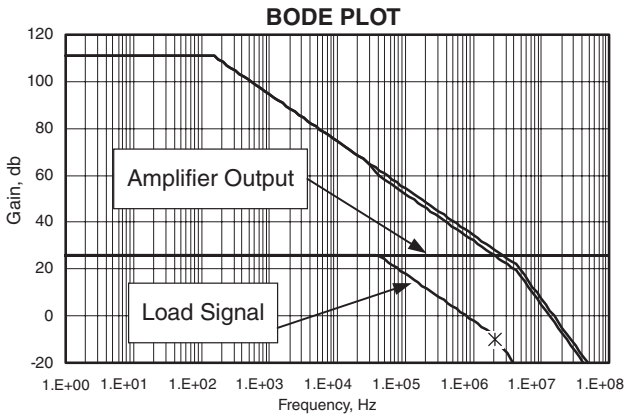


FIGURE 8. THE BANDWIDTH PENALTY IMPOSED BY LARGE ISOLATION RESISTORS

Do not let these drawbacks to the isolation resistor technique scare you off. It is the easest to visualize from the graph; generally not bothered by parasitics; works equally well for inverting and non-inverting circuits; and it is very tolerant of variations in Cload. This circuit remains stable even if the load capacitance increases several orders of magnitude. This is true because the singular value of Cload forms both a pole with the amplifier output impedance and a zero with Riso. These tend to cancel each other as they move up and down the frequency spectrum together with changes in Cload. Obviously, huge values of capacitance reduce bandwidth.

THE ROLL OFF CAPACITOR

We know a capacitor across the feedback resistor will attenuate high frequency gain or roll off the circuit, changing slope of the closed loop gain from zero to -20db/decade. If we position the pole of this roll off correctly, it will cross the open loop gain curve producing an intersection rate of 20db/decade giving a good shot at stability. We also know that 1/beta is the critical factor in stability analysis; it must be thought of as non-inverting; and non-inverting gain (or 1/beta) can never go below 0db. This means the desired segment of 1/beta will have a -20db/decade slope, starting at 26db and stopping at 0db. Here’s where the vision or feel of things comes in. Look again at the graph of Figure 5, our problem statement. Picture (maybe with the help of a straight edge) a line segment with a -20db/decade slope crossing the open loop gain curve at half the closed loop gain (13db in this case). At what frequency will this segment cross the closed loop gain (26db)? With a little practice, your vision will yield about 150KHz and the R-C

Pole Calculator will tell you 5.6pF across the 190K ohms is the place to be. See Figure 9 for the results.

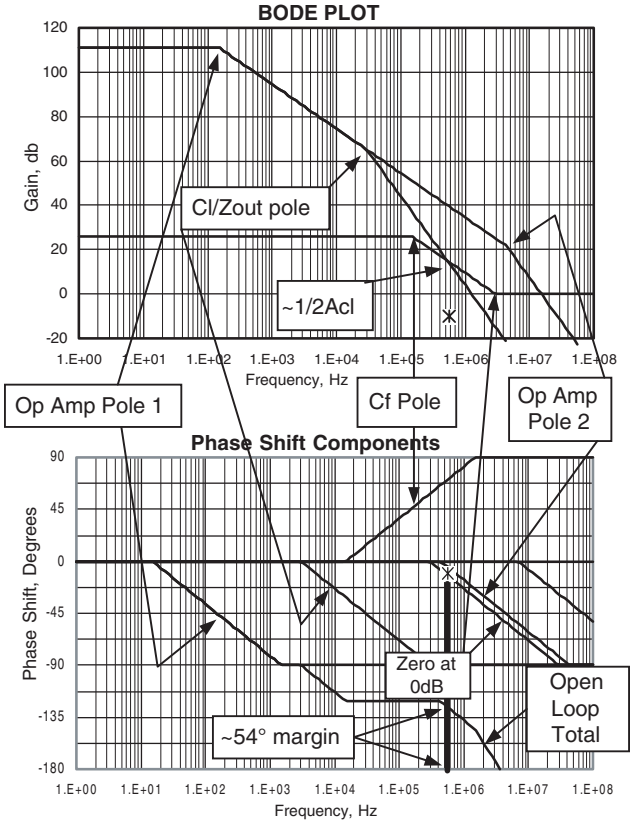


FIGURE 9. A CORRECTLY SIZED ROLL OFF CAPACITOR ACHIEVES STABILITY

We now have a paper circuit with ~54° phase margin, the desired gain, acceptable DC accuracy and a recommended bandwidth of 86KHz. The reason for the phrase "paper circuit" has to do with parasitic capacitance, which can vary wildly with quality of the physical layout. If the actual layout were to add 5pF to the feedback capacitor, we would loose almost 20° of our phase margin. In addition to careful layout, consider using lower values for the input and feedback resistors. Cutting the resistors in half will double the value of Cf, making errors due to parasitics less destructive.

Was this magic? No, just Power Design automation of Apex Precision Power Application Note 25 on Driving Capacitive Loads. Refer to this and Application Note 19 on Stability for Power Operational Amplifiers for theory and formulas. You will learn that the closed loop phase shift curves we have been looking at are the sum of effects of all the poles and zeros in the circuit. The bottom curve of Figure 9 shows graphically most of the individual phase shift components. Individual phase shift relating to pole 1 is hidden under the total curve. The only positive going curve is the result of the pole of the roll off capacitor. Note the zero associated with Cf (-45° at 3MHz) when 1/beta reaches 0db. Do not fall into the trap of thinking that if a small capacitor is good, a bigger one must be better. This capacitor will certainly roll off signal amplitude below 0db, but it does not take 1/beta below 0db. A larger capacitor would produce a flat high frequency 1/beta at 0db, a high intersection rate and oscillation.

The roll off capacitor technique is very effective when closed loop gain is 20db or more. With a slope of 20db/decade on this segment, the frequency spacing of the pole and zero are directly related to closed loop gain. As gain decreases the pole and zero become closer together and cancel each other.

THE NOISE GAIN COMPENSATION NETWORK

The last technique requires two components and requires the non-inverting input to be hard grounded. The hardware is a series connected R-C from the summing junction to ground. The Power Design schematic has them labeled Rn and Cn. With this network grounded, it does not change gain of the signal path. At high frequencies, where you would think of Cn as appearing as a short, the noise of this circuit will increase because it has two input resistors in parallel making the net gain higher. The real objective, however, is to increase 1/beta or to reduce the fraction of the output signal fed back to the inverting input.

Please: Visualize, "feel" and refer to Figure 10 with a modified problem statement. The capacitive load is only 5nF this time, but this is enough to yield a phase margin of ~8°. Step one is to imagine a new horizontal line located 20db above the original closed loop gain. Note the frequency where the new line crosses the open loop gain curve. Step two is dividing by something between 3 and 10. For now, let's pick 10 and hope your answer is somewhere in the area of 20KHz. ***This will be the pole location of the noise gain network.***

MODEL	PA85-100	Note/PBs	Rn	9999999999	Kohms
Rcl	3	Ohms	Cn	0	nF
Cload	0.005	uF	Cf	0	pF
Rin	10	Kohms	Riso	0	Ohms
Rf	190	Kohms			
Notes:					
R-C Pole Calculator:					
1	Kohms	2.5	Kohms	25	KHz
20	KHz	0.002	nF	0.005	uF
7.95775	nF	31830.989	KHz	1273.239545	Ohms

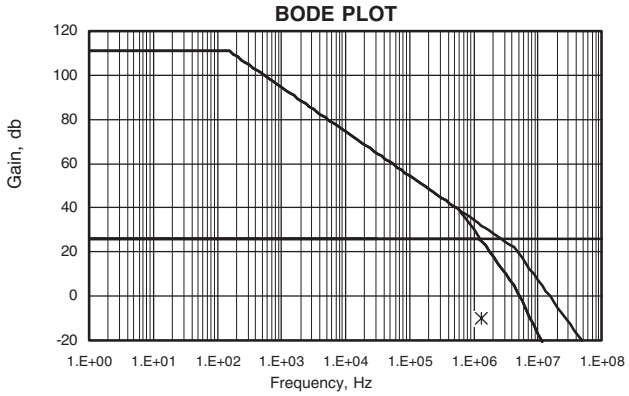


FIGURE 10. A NEW PROBLEM TO CONQUER

The 20db elevation of the new line segment is important; too little does not help enough, too much gets to be just as bad. Select the value of Rn such that when paralleled with Rin, the non-inverting gain goes up by a factor of 10. An approximation is simply Rin/10, which has already been entered in the R-C Pole Calculator. Power Design tells us this approximation yields 20.4db. Entering the desired pole frequency of 20KHz yields 8nF. We will use 8.2nF and proceed to Figure 11 (next page).

Noise gain compensation works best when the pole formed by output impedance and capacitive load is not more than 20db above the closed loop gain.

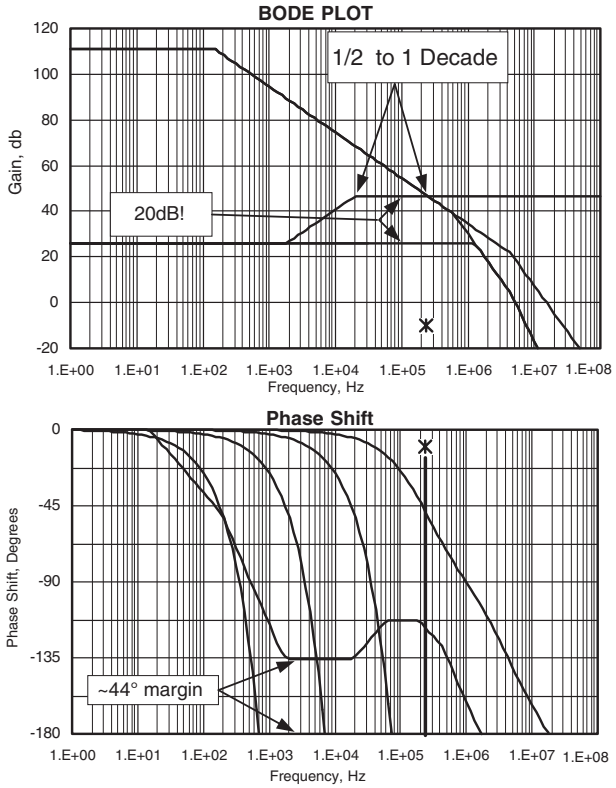


FIGURE 11. THE NOISE GAIN COMPENSATION NETWORK DOING ITS THING

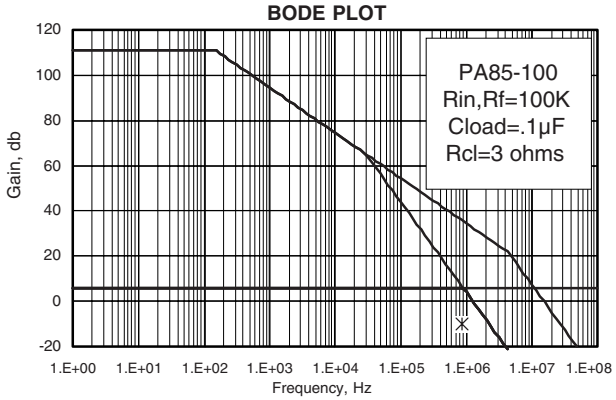


FIGURE 12. LOW GAIN AMPLIFIERS PRESENT THE BIGGEST CHALLENGE

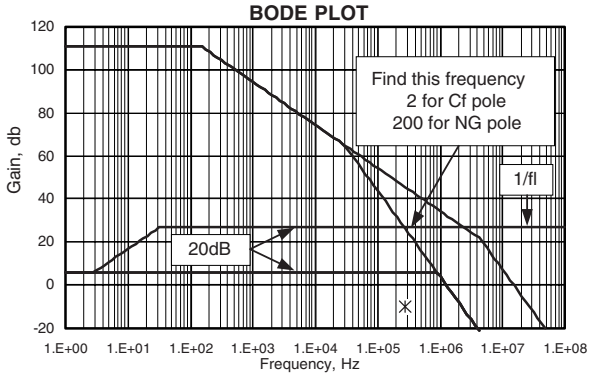


FIGURE 13. SETTING UP THE INITIAL NOISE GAIN CURVE

A COMBO DEAL IS NOT ALWAYS FAST FOOD

We found that a minimum closed loop gain of 20db is desirable for the roll off capacitor to do a good job. Also, for the noise gain compensation to produce good results, we want no more than 20db between closed loop gain and the pole produced by output impedance and the load capacitor. There are a fair number of applications requiring a signal gain of -1, which is a 1/beta of only 6db. See Figure 12 as our next problem statement. This circuit is an ideal candidate for a combination of both roll off capacitor and noise gain techniques.

As a first step, select Rn for a 20db increase of 1/beta or non-inverting gain (5K was used in this example). For a trial, enter 1000nF for Cn and refer to Figure 13 showing our new 1/beta. Divide the frequency where 1/beta crosses open loop gain (~250KH) by 2 and set the Cf pole accordingly. Set the noise gain pole two decades lower yet. The R-C Pole Calculator makes it easy to select 12pF for Cf and 27nF for Cn. Figure 14 shows the results.

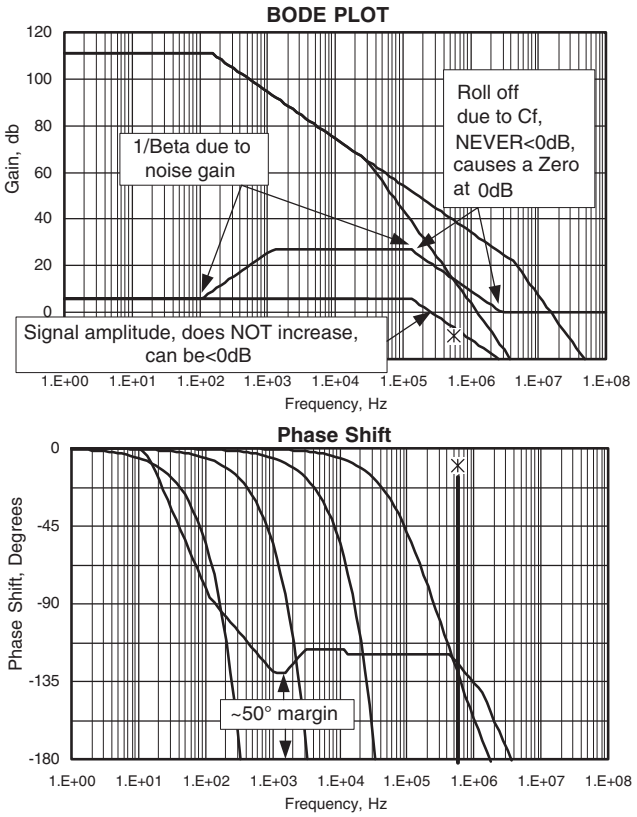


FIGURE 14. COMBINING NOISE GAIN WITH A ROLL OFF CAPACITOR

COMPARING THE METHODS

Your Daddy probably avoided using the isolation resistor technique because of the dreaded voltage drop outside the loop. But being of the enlightened age, you will look at the roll off error shown in Figure 15 and realize this error applies to any feedback capacitor inside the loop as well! This means that when pole frequencies are equal, gain errors introduced by either an isolation resistor or a feedback capacitor are identical.

We also need to look at the phase shift issue. The lower graph of Figure 15 shows the phase shift occurring outside the loop; an error to be added to the closed loop phase shift to find total phase shift applied to the actual load. Comparing

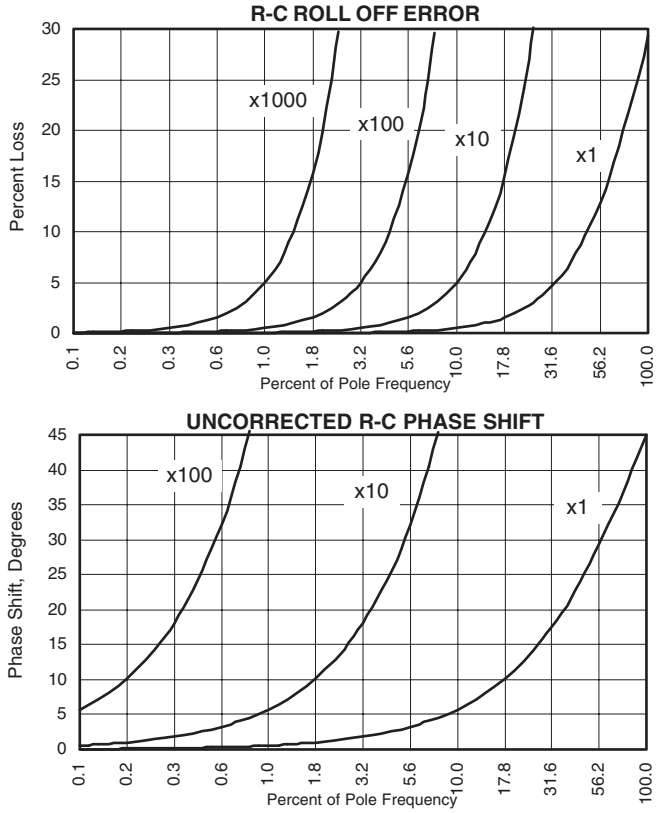


FIGURE 15. R-C ROLL OFF AMPLITUDE ERROR AND UNCORRECTED PHASE SHIFT

the closed loop phase shift of Figure 7 (the isolation resistor solution) to that of Figure 9 (the feedback capacitor solution) reveals much better phase performance when the isolation resistor is used. The key to this difference is that adding the feedback capacitor introduces both a positive and a negative component to open loop phase shift while adding an isolation resistor introduces only a positive component. This difference can be seen directly in the Phase Components graphs. For an indirect indicator, notice that open loop phase beyond the closure frequency falls off more rapidly with the Cf solution than with the Riso solution. Table 1 shows gain errors and total phase shift errors for the two circuits at the suggested maximum bandwidth and several points below. With the pole frequency of the isolation resistor solution a little higher than the pole of the feedback capacitor solution, both gain and phase performance of the isolation resistor solution is superior.

	865KHz	43KHz	22KHz	8.6KHz	860HZ
Cf Gain	12.8%	4%	1.1%	0.17%	0.002%
Riso Gain	8.7%	2.4%	0.62%	0.1%	0.001%
Cf Phase	40	21	11	4.3	0.43
Riso Phase	37	19	9.5	3.9	0.39

TABLE 1. TOTAL GAIN AND PHASE ERRORS FOR Cf AND RISO SOLUTIONS

WORKING WITH COMPOSITE AMPLIFIERS

Stability headaches seem to escalate exponentially with the number of amplifiers in the loop, so most designers tend to avoid them. However, the composite is often worth the extra trouble when large power levels and high DC accuracy are both required. The techniques to achieve stability with the composite are basically the same as we already covered; stabilize the power stage first, then repeat the job for the total circuit.

Figure 16 is the data entry screen for the second half of this work. The first half is represented by the Pwr symbol (accomplished as above), and those numerical results become input data for this half. The schematic is showing that the closed loop response of the power stage is in series with the host amplifier, or is being added to the open loop response of the host amplifier. Stability analysis for the composite performs exactly that addition and a typical result and the classic problem with the composite is shown in Figure 17 (next page).

The OP07 host amplifier has a well behaved open loop gain curve with its second pole near 0db gain. If the small signal amplifier you wish to use is not included in the built-in data base, Power Design comments tell how to enter data extracted from a data sheet. The model of the composite open loop gain features the poles of both the host amplifier and the closed loop power stage response. The pole at ~21KHz (due to the roll off capacitor in the power stage) causes an intersection rate of 40db/decade for any closed loop gain between 25db and 45db. Lower gains would yield 60db/decade because closure frequency in the power stage places pole just over 70KHz. It is quite possible to see this type stability problem even when not driving a capacitive load..

Power Design provides two techniques to stabilize the composite circuit. If an isolation resistor was used, it is modeled in the power stage only and its effects are included in the closed loop response data fed into the composite problem statement. You may use the roll off capacitor, the noise gain network or both as shown in Figure 18 (next page). The same basics on component selection apply here, but you may find a little more tweaking of component values is required. Final values for the solution shown are Rn=3.4K, Cn=10nF and Cf=22pF which yield a phase margin of 50°.

Composite Circuits

MODEL	OP07	READ ME				Estimated Closure Frequency =	86.59643	KHz
Aol =	135	dB	Pole 1 =	0.1	Hz	Suggested maximum bandwidth	27.3842	KHz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz	Estimated Closure Rate =	60.0	dB/decade
Rin	21	Kohms	Rn	99999999999	Kohms	Estimated Phase Margin =	-35.95021	Degrees
Rf	340	Kohms	Cn	0	nF			
Cf	0	pF	Using Look-Up data					
Notes:								
R-C Pole Calculator :								
3.4	Kohms	47	Kohms					
5	KHz	10	nF					
9.36206	nF	0.338627538	KHz					
1/Beta (DC)		24.7	dB					
Noise Gain		0.0	dB					
Pole Noise Gain		0.015915494	KHz					
Zero Noise Gain		0.015915494	KHz					
Pole Cf/Rf		4681027738	KHz					
Zero Rf/Cf		80469095893	KHz					

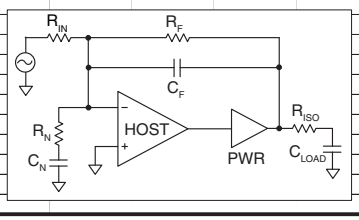


FIGURE 16. ENTERING HOST AMPLIFIER FOR THE COMPOSITE CIRCUIT

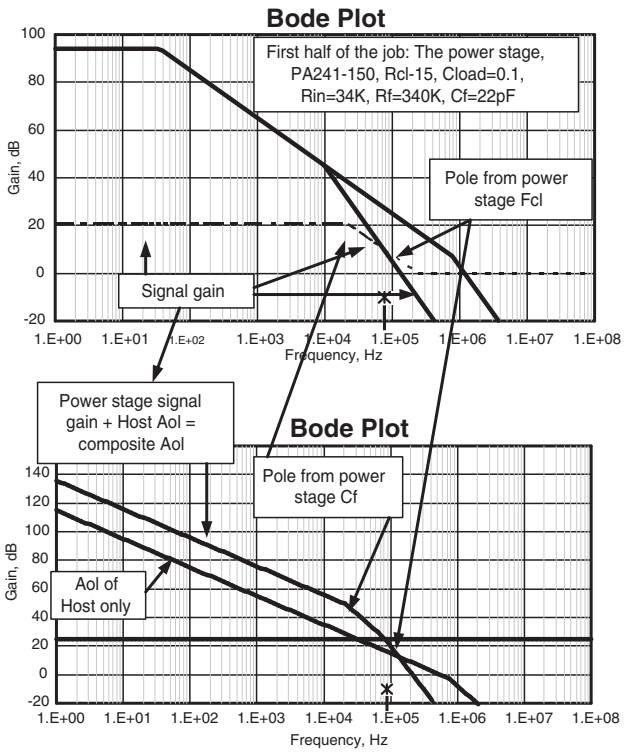


FIGURE 17. A POWER STAGE RESPONSE INCORPORATED INTO A COMPOSITE AMPLIFIER

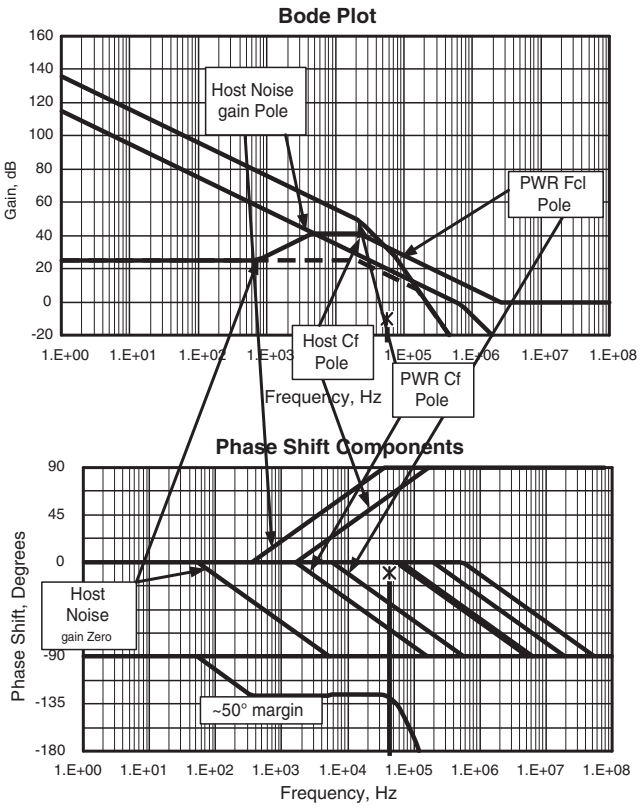


FIGURE 18. THE FINISHED COMPOSITE AMPLIFIER

DOES INDUCTANCE ALWAYS BRING STABILITY PROBLEMS?

The answer is no. You can drive inductance all day long in the voltage mode without waking the dragon. The problem is current mode drive where inductive V-to-I phase shift is inside the loop, courtesy of the current sense element. Figure 19 illustrates a combination of typical topologies on the data entry screen. We will address the numbered boxes later.

The most simple real topology is realized by applying the input signal to the non-inverting input and not using Rin. The power op amp drives the load in phase with the input signal to whatever amplitude is required to obtain voltage across Rs equal to the input signal. Adding Rin (grounded) to the circuit causes the voltage across Rs to be greater than the input signal.

To achieve an inverting circuit, ground the non-inverting pin and apply the signal to Rin. The op amp will drive the load out of phase at an amplitude large enough to develop a voltage on Rs equal to Rf/Rin. This inverting setup has dual advantages over the non-inverting circuit. Voltage on the sense resistor can be larger or smaller than the input signal, plus there is no common mode voltage on the amplifier.

Notice that in both circuits the load impedance is inside the feedback loop, meaning closed loop gain is partially a function of load impedance. This is exactly what we want for current control; load impedance goes up; gain goes up; output voltage goes up; and current remains constant. Refer to Figure 20 (next page) for a picture of the problem with "the gain goes up". Open loop gain is falling at 20db/deacade and closed loop gain is rising at 20db/decade to produce an intersection rate of 40db/decade; an event of which we've grown suspicious.

When it comes to adding all the phase shift elements to find open loop phase shift (and phase margin), notice that the first pole in the open loop response of the op amp is nearly coincident with a zero in the closed loop. This causes open loop phase to drop like a rock to 180° (zero phase margin) at 100Hz. The key to stabilizing this circuit will be to lower the frequency of the

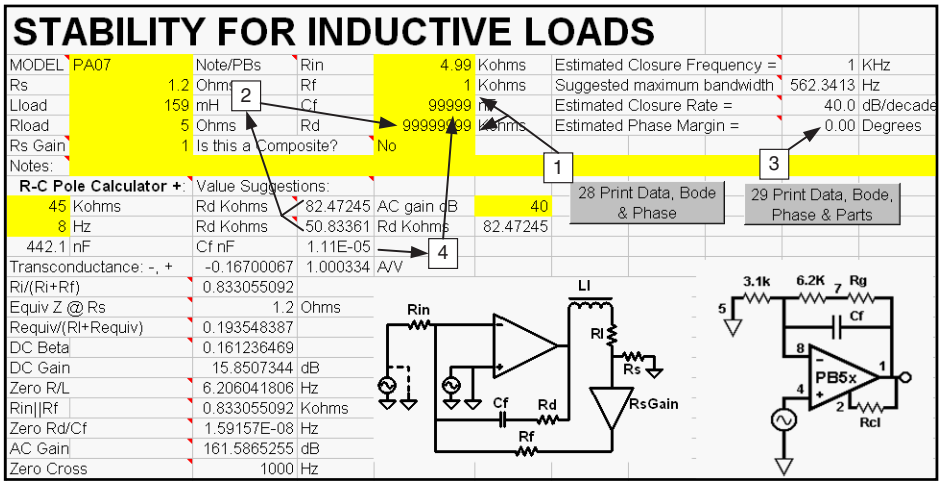


FIGURE 19. STEPS TO STABILITY FOR CURRENT CONTROL WITH INDUCTIVE LOADS

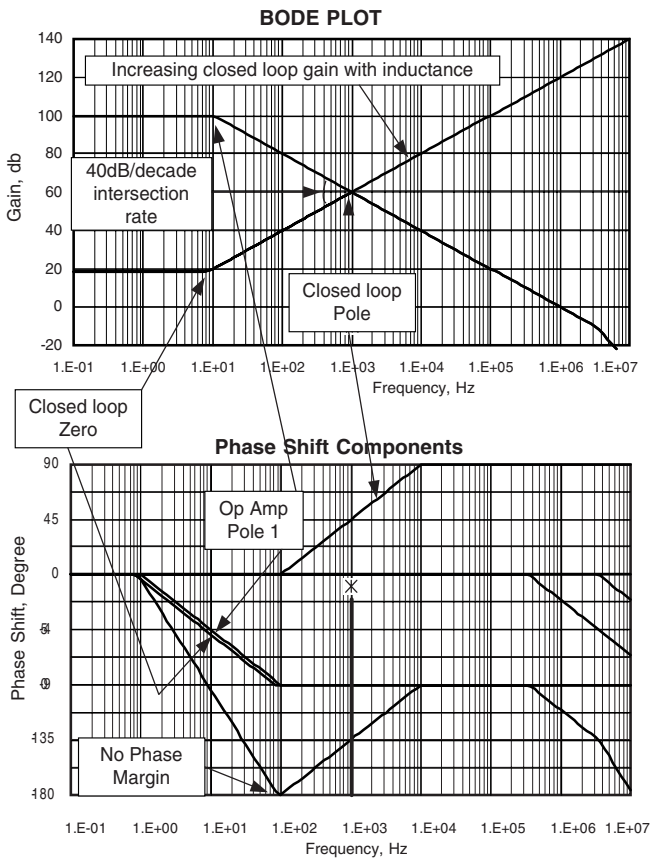


FIGURE 20. GAIN AND PHASE PROBLEMS CAUSED BY INDUCTANCE IN THE FEEDBACK LOOP

closed loop pole (currently at the intersection point) by using a second feedback path consisting of Cf and Rd.

This R-C network will introduce a second feedback path doing practically nothing at low frequencies but providing dominant voltage feedback at higher frequencies, without the additional V-to-I phase shift of the inductor. Figure 21 shows a typical solution where the flat portion of this feedback path is usually positioned at least 20db above DC gain or 20db below the intersection of open loop gain and the inductive feedback path. If there is a conflict between these to goals, start with the higher db level. The corner frequency of the R-C network is usually about 3/4 of a decade below the intersection of the two feedback paths.

The circuit function of our example is an inverting amplifier with an input signal of ±10V and a transfer function of 0.167A/V. At peak currents of 1.67A, power dissipation in the sense resistor seemed acceptable and values of Rin and Rf were convenient. Please note that these same component values could model a non-inverting amplifier with a transfer function of 1A/V.

Refer to Figure 19 again to see that Power Design calculates two values for Rd and then a value for Cf. To use these features:

1. Enter large values for both Cf and Rd.
2. Enter the larger recommendation for Rd.
3. If phase margin is well over 45°, raise Rd, if less, lower Rd.
4. When satisfied with phase margin, enter recommendation for Cf.

In this example, values of 82K ohms and 120nF were used.

As transfer functions and Q ratings of inductors change, the curves Power Design draws for you will vary a lot. As in this example, some will fall into place with suggested values; some

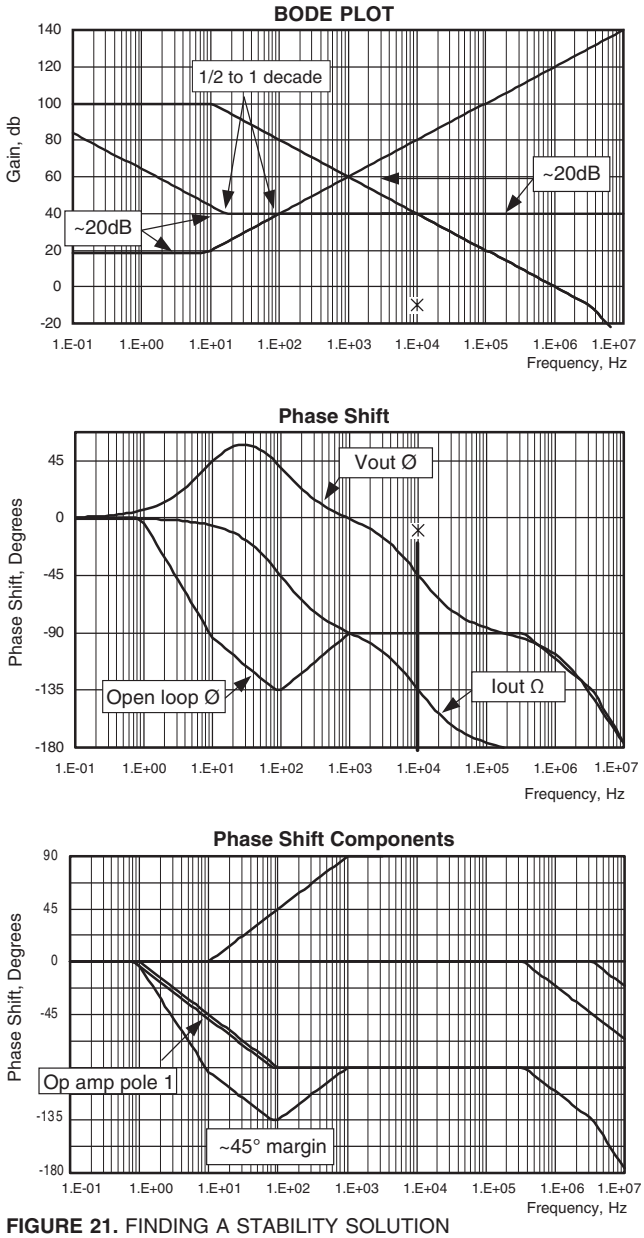


FIGURE 21. FINDING A STABILITY SOLUTION

will require playing with the value of Rd; and a few may require no network at all. When viewed as a single issue, stability for these amplifiers is simple. However, you will often find yourself fighting for bandwidth. The good news is that re-running the stability analysis for a dozen sets of gain and sense resistors is an easy task. As a general rule, large sense resistors and low gain settings will maximize bandwidth.

THEORY IS GREAT--------BUT

We have mentioned parasitics and layout concerns a couple of times. Please pull from your memory the old phrase, “too broad a subject to cover....” True, so we will get right to Figure 22 (next page) and say the job is positively not finished until the hardware is tested. Use all components as close to production version as possible; power supplies, cable harnesses, signal sources, loads and any thing else you can think of.

Watch the 1KHz output signal for over/under shoot while setting the very low frequency signal to exercise the amplifier output (plus the supplies, cables and the load) over the entire

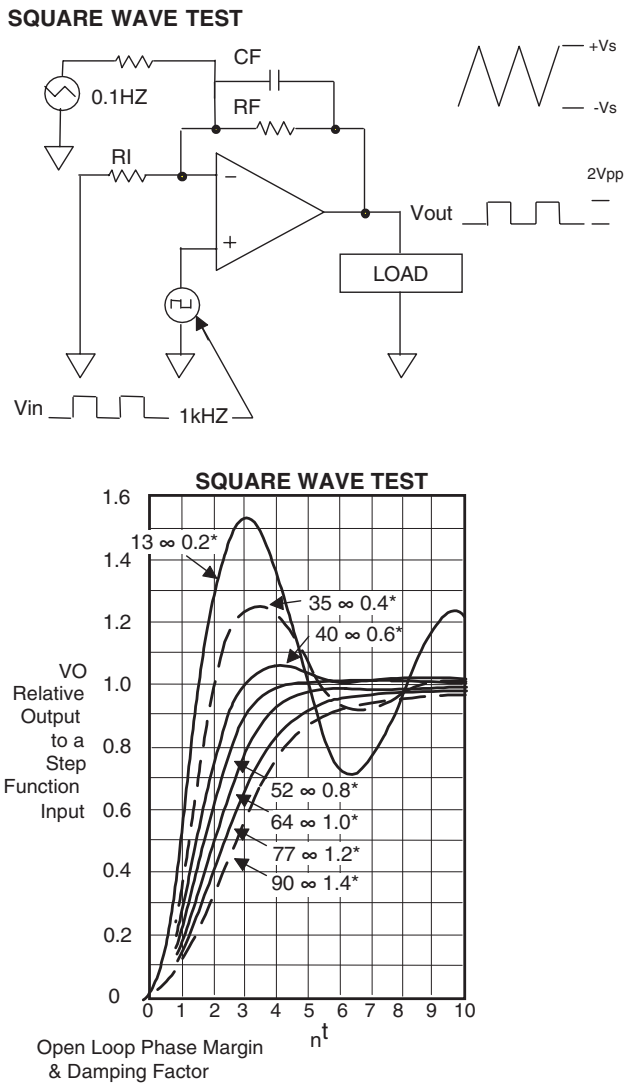


FIGURE 22. TESTING THE ENTIRE SYSTEM HARDWARE FOR PHASE MARGIN

dynamic range. Then estimate phase margin of the system using the graph. A little time spent here now may keep you off the production line in six months.

CONCLUSION

The next time you happen to be involved in a nightlong argument about whether stability is a science or a black art, just smile. You won't have to say anything, just keep smiling. It would be good though, if you have your laptop along loaded with Power Design. When you think the smiling is about to get you smacked, tell the crowd both arguments are correct; arithmetic is the science portion, but expecting anyone to remember all the rules and formulas is the black art. With almost instant calculations and graphic data presentation, arithmetic is a snap and a lot of the rules can remain hidden. Power Design's built-in documentation presents the most important procedures and rules at the command of your mouse. The entire process becomes so easy, tasks like checking worst case component tolerances become bearable.

You'll be the hit of the party.

Filters and Power Dissipation for PWMs

INTRODUCTION

Those of us who have ventured into high power linear circuits with their massive and sometimes liquid cooled heatsinks have a tendency to go ga-ga over the efficiency potentials of the Pulse Width Modulation (PWM) amplifiers. This is OK. But these little switching miracles do bring a new set of challenges to the table.

The PWM amplifier with no filtering is NOT capable of amplitude modulation. It can only change times and maybe polarity. We get lucky once in a while and get a load which will do the filtering for us. Much more often we must design the filter, a job many of us do not place at the top of our list of most cherished activities. In addition to this, the methods required to calculate internal power dissipation and the heatsink size are quite different than those used in the linear world.

The Power Design CAD tool automates Butterworth filter equations found in Apex Precision Power Applications Note 32 and expands on this base by graphing response with real world components. It then goes on to automate internal power dissipation equations, plus draw a wide variety of graphs on amplifier performance over frequency. As the overall process is usually iterative, the benefit of computer analysis is indispensable.

SOME PWM BASICS

PWM circuits achieve high efficiency compared to their linear counterparts in much the same manner as switching power supplies do versus linear supplies. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Figure 1 illustrates a typical PWM amplifier output stage employing four switches configured as an H-bridge providing bipolar output from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals.

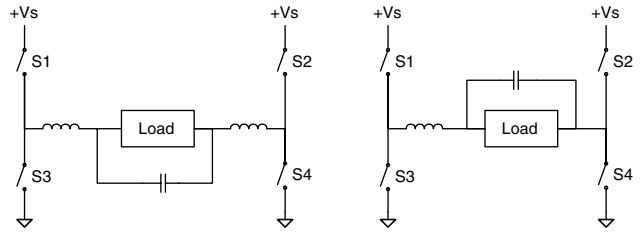


FIGURE 1. H-BRIDGE OUTPUTS WITH DIFFERENTIAL AND SINGLE-ENDED FILTERING

The H-bridge switches work in pairs to reverse polarity of the drive, even though only one polarity supply is used. Figure 2 shows waveforms of locked anti-phase modulation where S1 and S4 are on during one portion of each cycle, and S2 and S3 are on during the remainder of the cycle.

To help understand the conversion of the time modulated data to analog levels, visualize each waveform segment of Figure 2 run through a low pass filter whose cutoff frequency is at least 10 times lower than the switching frequency. The A and B voltages of the 50% duty cycle waveforms will both be equal to 50% of the supply voltage. With both terminals of the load connected to the same voltage, the load sees 0V across

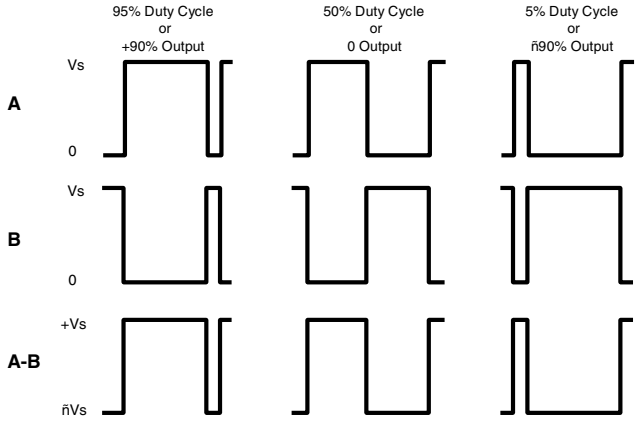


FIGURE 2. H-BRIDGE WAVEFORMS

itself. The A-B waveform represents this differential connection of the load, and the filtered voltage of this waveform equals zero. To examine the 95% duty cycle waveforms, lets assume a supply voltage of 100V. The filtered A value will be 95V, B will be 5V, and the load will see 90V; the same as the filtered value of the A-B waveform.

Note that if S1 and S3 were to turn on simultaneously, there is nothing to limit current. Self-destruction would be only microseconds away. The fact that these transistors turn on faster than they turn off, means a “dead time” needs to be programmed into the controller if doing your own design. When you buy the amplifier from Apex Precision Power, this is all inside the package.

Changing duty cycle through 50% is a continuous function, meaning there is no inherent discontinuity as exists in sign magnitude modulation. This is analogous to the much improved distortion levels of class AB linear stages versus class C linear stages where zero current crossing brings a discontinuity or dead spot usually referred to as crossover distortion.

National created their FAST and DAMN FAST buffers, but they can’t hold a candle to these guys. In fact, that’s the problem with switchers- -they move voltages and currents around so fast it’s difficult to keep the noise down. From the linear or analog world we borrow the equation relating slew rate to power bandwidth. If your PWM amplifier switches 50V in 25ns, the slew rate is 2000V/us. With a peak voltage of 50V, this equates to over 6MHz. With 5 or 10 amps flowing, those transitions contain RF energy similar to a moderate radio transmitter. Spending a few minutes thinking like an RF designer may be worthwhile.

Refer to Figure 3 (next page) for a pictorial of the filter’s job. The relatively flat portion of the curve is the pass band of the filter. The signal frequency of the power drive to the load must fit under this area. Desired attenuation in this area is 0db and the corner frequency is Fc, the cutoff frequency. We then go down the filter slope to the switching frequency, Fsw. Allowing one decade between these two frequencies is a good starting point. In this case, the graph tells us the worst case peak ripple voltage at the switching frequency will be a little under 1% of the supply voltage.

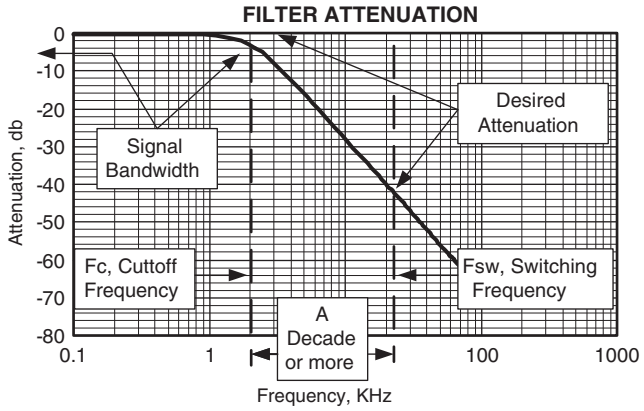


FIGURE 3. PWM FREQUENCY RELATIONSHIPS

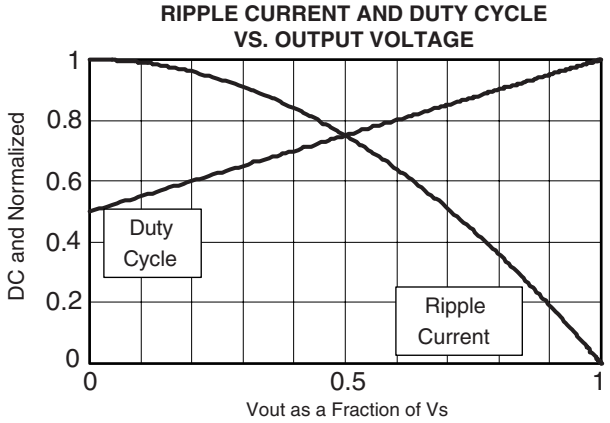


FIGURE 4. DUTY CYCLE AND RIPPLE CURRENT VARIATIONS WITHOUT OUTPUT VOLTAGE

Figure 4 (next page) illustrates how a zero output voltage corresponds to a 50% duty cycle and produces maximum ripple current. As expected, there is a linear relationship between increased output voltage and increased duty cycle. Not quite as obvious is the curve that indicates the ripple current is reduced all the way to zero if we push modulation all the way to steady state.

The need to squeeze the last ounce of bandwidth from our designs, along with the physics limitations on switching frequencies, makes it desirable to minimize the distance between signal and switching frequency. Pure theory says adding more poles can increase filter slope. This is true to a point. We would probably question an eight-pole filter in the small signal world. Do you really need that? Can you find high enough quality components to make it work? Can you afford it in terms of size and cost?

In the PWM world these questions are not only valid but are many orders of magnitude more important because power levels have gone from mW to KW! Rule of thumb: Allow at least a decade between switching and signal frequencies.

THE POWER DESIGN APPROACH TO SUCCESSFUL PWM AMPLIFICATION

The usual process is:

1. Select an amplifier model (possibly with the Part Selector sheet).
2. Load circuit data into the PWM Filters sheet.
3. Auto load components into the Filter/load model and sweep the frequency.
4. Tune components and parasitics plus check load variations and fault conditions.
5. Set sweep frequency band from Fmax to at least 10 times Fsw to check high frequency attenuation.
6. Use the graphs to select the heatsink.

The Power Design, PWM Filters sheet data entry screen for step 2 is shown in Figure 5. The pull down Model cell reads the built-in database containing specifications on supply voltage, maximum switching frequency, current levels, and internal resistance. Alternatively, comments in the database area provide instructions to enter data for your own design.

Switching frequency, Fsw, is required because some models are programmable, most can be run lower than the maximum and many can be driven with digital signals. Immediately to the right of this data entry cell is the maximum for the model selected. Enter minimum frequency to be amplified as Fmin. Use .001 for DC. Consider using .001 even if the application is a substantially higher fixed frequency, as this may simulate a "lost" input signal condition and some circuits will present their lowest impedance at DC. Enter the maximum frequency to be amplified in Fmax. Fmin and Fmax set the frequency end points of the sweep that will be run later. Fcutoff is the cutoff frequency of the filter and will be the -3db response point. The next three cells describe three series connected elements forming the load. Vripple is the maximum peak voltage on the load at the switching frequency, your way to specify the attenuation of the filter at

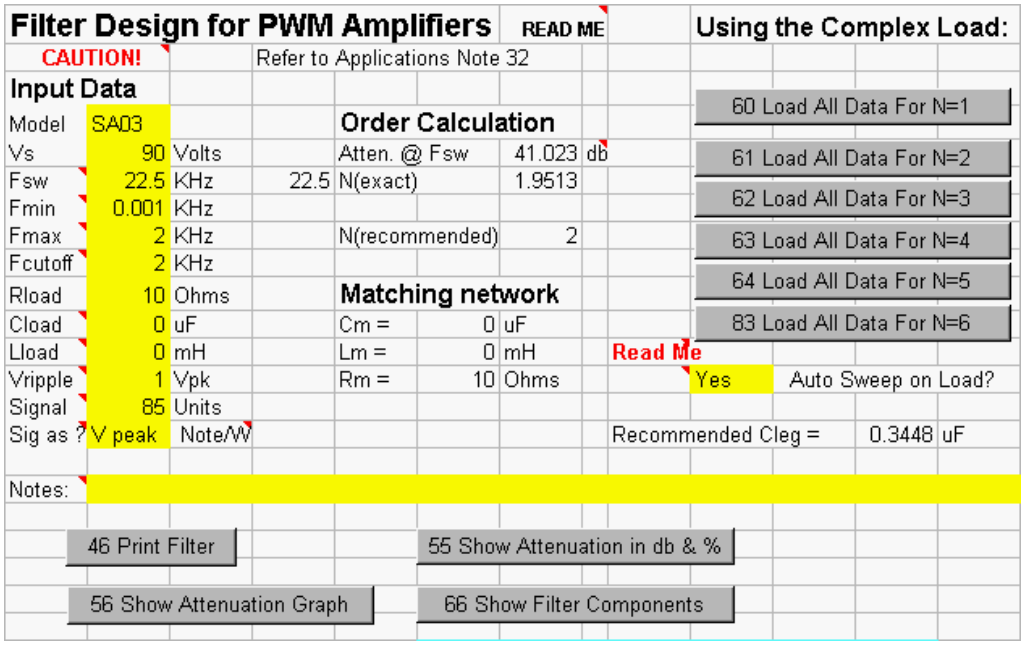


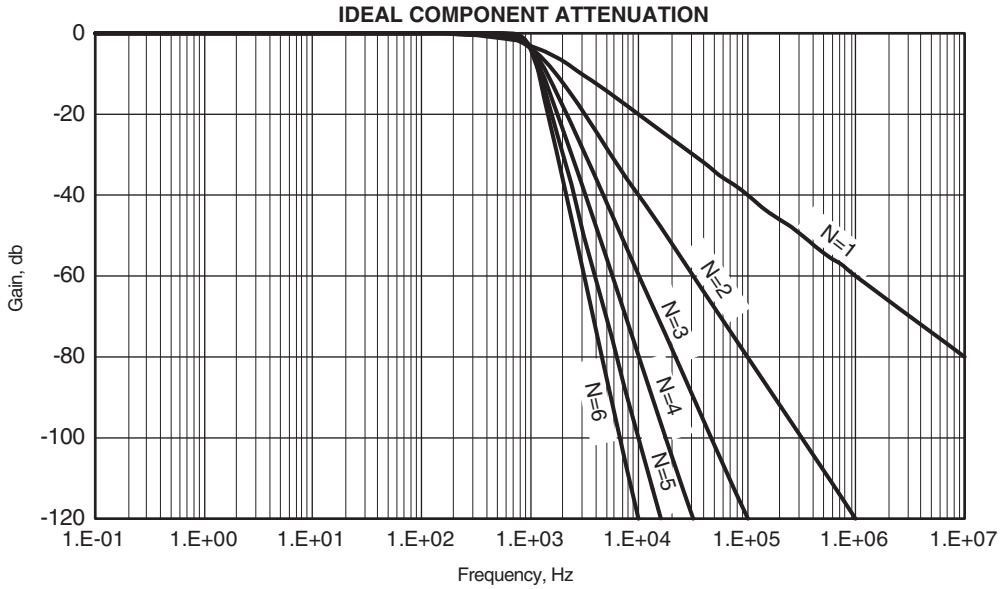
FIGURE 5. PWM FILTER DESIGN DATA ENTRY SCREEN

Component Calculations Shading indicates values for Split Inductor topology

		Dual Cap Filter	Single-ended Filter
N = 1	L =	0.3979 mH	0.7958 mH
	P-P Iripple =	2.5133 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.6283	
N = 3	L1 =	0.5968 mH	1.1937 mH
	C =	21.22 uF	10.61 uF
	L2 =	0.1989 mH	0.3979 mH
	P-P Iripple =	1.6755 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4189	
N = 5	L1 =	0.6148 mH	1.2296 mH
	C1 =	26.967 uF	13.484 uF
	L2 =	0.5499 mH	1.0998 mH
	C2 =	14.235 uF	7.1174 uF
	L3 =	0.1229 mH	0.2459 mH
	P-P Iripple =	1.6266 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4067	

		Dual Cap Filter	Single-ended Filter
N = 2	L =	0.5627 mH	1.1254 mH
	C =	11.254 uF	5.6269 uF
	P-P Iripple =	1.7772 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4443	
N = 4	L1 =	0.609 mH	1.2181 mH
	C1 =	25.102 uF	12.551 uF
	L2 =	0.4307 mH	0.8613 mH
	C2 =	6.0909 uF	3.0454 uF
	P-P Iripple =	1.6419 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4105	
N = 6	L1 =	0.6179 mH	1.2358 mH
	C1 =	28 uF	14 uF
	L2 =	0.6179 mH	1.2358 mH
	C2 =	19.124 uF	9.562 uF
	L3 =	0.3016 mH	0.6031 mH
	C3 =	4.1189 uF	2.0595 uF
	P-P Iripple =	1.6184 Amps out of the amplifier	
	Avg. Iout for thermal calculations =	0.4046	

FIGURE 6. COMPONENT VALUES FOR DIFFERENTIAL AND SINGLE ENDED FILTERS



Attenuation in db							Percent attenuation						
500	-9.7E-01	-2.6E-01	-6.7E-02	-1.7E-02	-4.2E-03	-1.1E-03	5.0E+02	10.55728	2.98575	0.772212	0.194742	0.048792	0.012205
750	-1.9E+00	-1.2E+00	-7.1E-01	-4.1E-01	-2.4E-01	-1.4E-01	7.5E+02	20	12.84245	7.863584	4.658634	2.702074	1.547157
22500	-2.7E+01	-5.4E+01	-8.1E+01	-1.1E+02	-1.4E+02	-1.6E+02	2.3E+04	95.55994	99.80247	99.99122	99.99961	99.99998	100
225000	-4.7E+01	-9.4E+01	-1.4E+02	-1.9E+02	-2.4E+02	-2.8E+02	2.3E+05	99.55556	99.99802	99.99999	100	100	100
Hertz	N=1	N=2	N=3	N=4	N=5	N=6	Hertz	N=1	N=2	N=3	N=4	N=5	N=6

FIGURE 7. THE IDEAL ATTENUATION GRAPH AND PRECISE CHECKING OF POINTS OF INTEREST

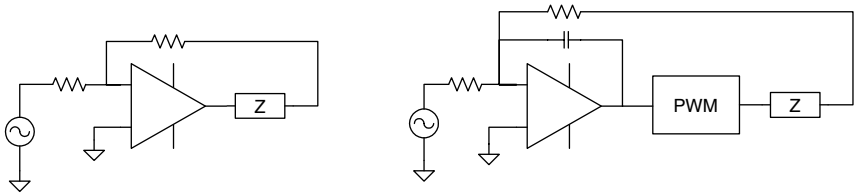


FIGURE 8. A PURE INTEGRATOR IS THE KEY TO ACCURACY

Fsw. The bottom two cells specify the magnitude and unit of measure for the output signal.

The Order Calculation section first converts your maximum ripple and power supply ratings into db attenuation. Then by examining the switching and cutoff frequencies, it calculates the order, or number of poles needed. The integer recommendation is rounded up. The matching network that is calculated will cause reactive loads to appear resistive to the output of the filter. Figure 6 shows the actual filter components for filter orders up to N=6, plus expected ripple current at the switching frequency. Figure 7 shows the ideal response graphed and an area where attenuation at specific frequencies can be checked in detail.

"Ideal" is a great word. Just as we use the concept to describe theoretical performance of the linear op amp, it will work equally well here. To achieve the performance shown in this graph, output impedance of the amplifier must be zero; the filter must contain perfect components; be terminated with the load described; and the specified matching network must be in place. If these conditions are not true, **ALL BETS ARE OFF**.

A quick look at PWM amplifier data sheets will tell us actual output impedance can cause small errors if left unchecked. Use your knowledge of op amp theory and Figure 8 to see how closed loop output impedance of the PWM amplifier is extremely low just as with a closed loop op amp. On the left circuit we know output impedance is reduced by the loop gain. As long as the op amp in the right circuit has no direct DC feedback, and the PWM block with its output impedance (typically ranging from 0.1Ω to 1Ω) is inside the feedback loop, closed loop output impedance will be reduced in the same fashion. With PWM amplifiers being relatively slow compared to op amps, it is easy to obtain high loop gains over the power signal bandwidth to achieve negligible errors in driving the filter. In actual PWM systems, the feed back loop is often much more complex than shown here.

Trying to approach the second "ideal" condition means most of the work still lies ahead in finding components which work as advertised in the MHz range and whose losses won't radically change the pretty graphs. An electrolytic capacitor may perform very well at 60Hz, but rather poorly at 6MHz. If temperatures allow, switching to tantalum should result in a noticeable high frequency improve-

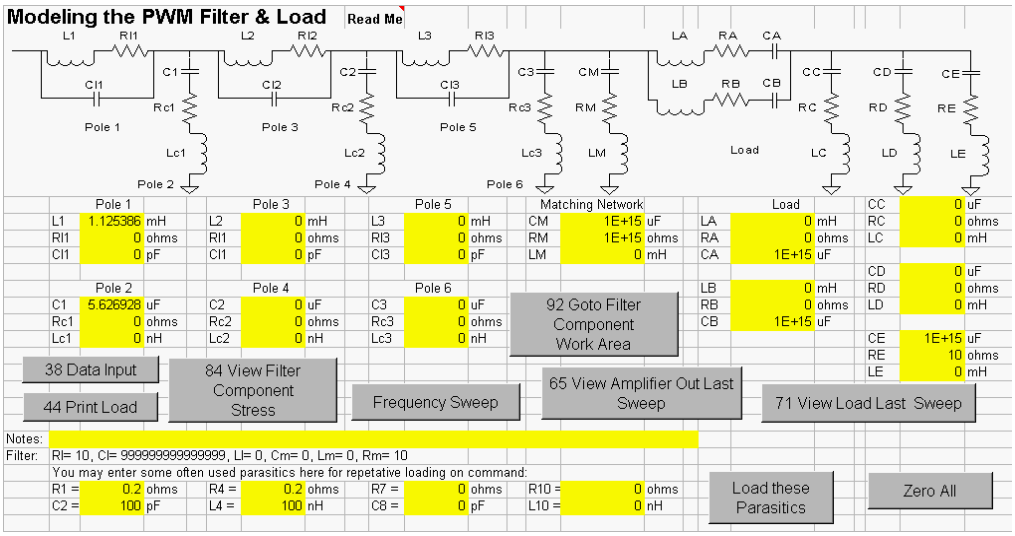


FIGURE 9. LOADING APPLICATION DATA FROM THE FILTER SHEET TO THE POWER SHEET

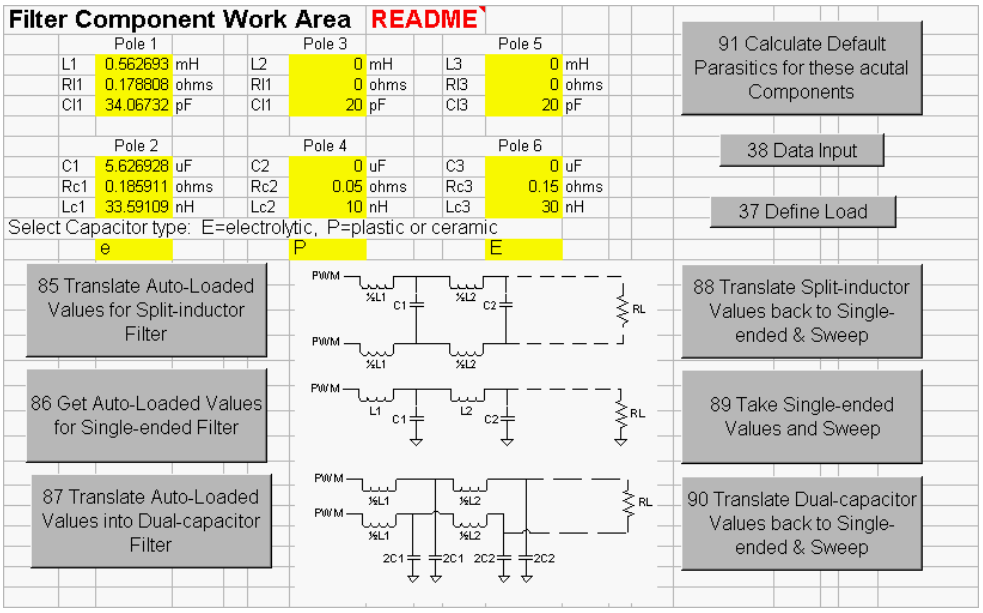


FIGURE 10. TRANSLATION BETWEEN FILTER TOPOLOGIES AND DEFAULT PARASITIC CALCULATION

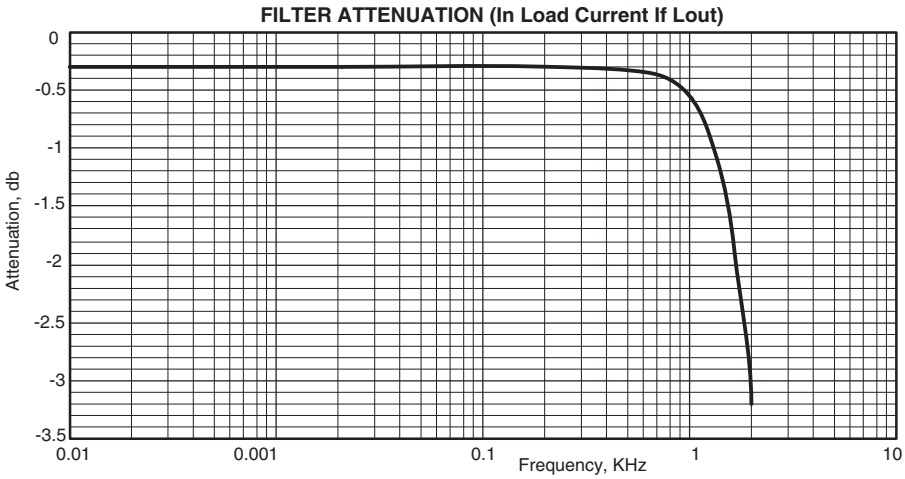


FIGURE 11. ATTENUATION WITHIN THE PASSBAND

ment. Moving to switching rated plastic capacitors or ceramic capacitors is usually an even better choice.

Not many of us would attempt using laminated steel core inductors here, but please note that not all "high frequency" coils are created equal. Air core inductors get away from the magnetic saturation problem and they have fewer tendencies to become dummy loads at high frequency. The down side will be more turns of wire and more copper losses. When adding a magnetic core, make sure the material can handle the high frequency components of the square wave (manufacturers often rate frequency capability for only sine waves) at the switching frequency and can accommodate the flux density of the peak currents to be delivered.

Pressing one of the "Load All Data" buttons on the PWM Filter sheet transfers your application to the PWM Power sheet. Starting on the left of Figure 9 we find single-ended components for up to a sixth order filter have been entered. Next we find the matching network. On the far right you will find the simple three-element load specified on the PWM Filters sheet plus space to model a more complex load. Parasitics for the filter components have all been zeroed.

The sweep function handles only single ended filters, but Figure 10 shows the area where these component values can be translated into values for either split-inductor or dual-capacitor designs. While there is absolutely no substitute for finding real parasitic values for filter components, button 91 provides a default parasitic calculator for first pass design efforts. Notice the cells where capacitor type can be selected individually for all three capacitors. Parasitics vary WILDLY from part to part. The default calculator is ONLY intended to get somewhere in the ballpark. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse. Consult manufacture's data sheets or measure

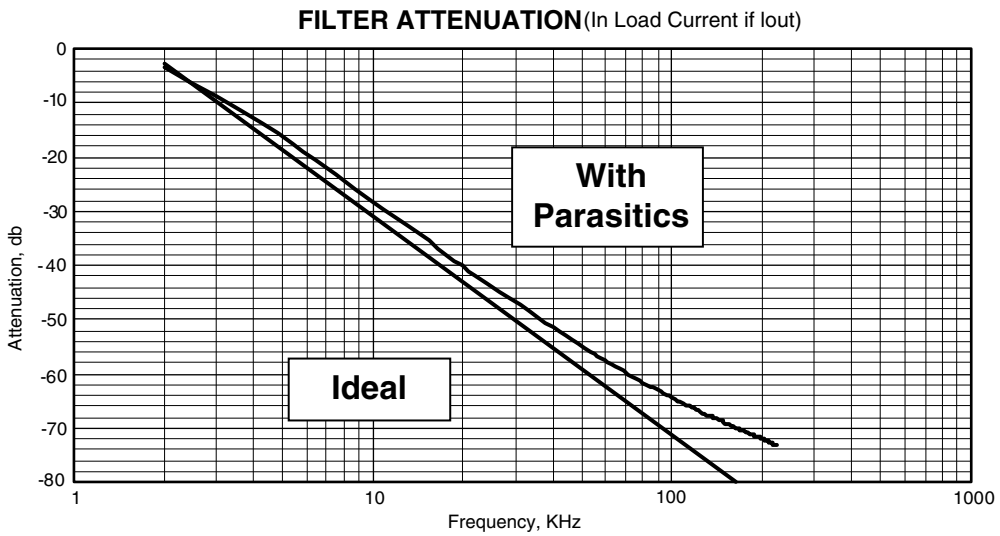


FIGURE 12. SMALL PARASITICS CAUSE A LARGE DEPARTURE FROM THE "IDEAL" PICTURE AT HIGHER FREQUENCIES

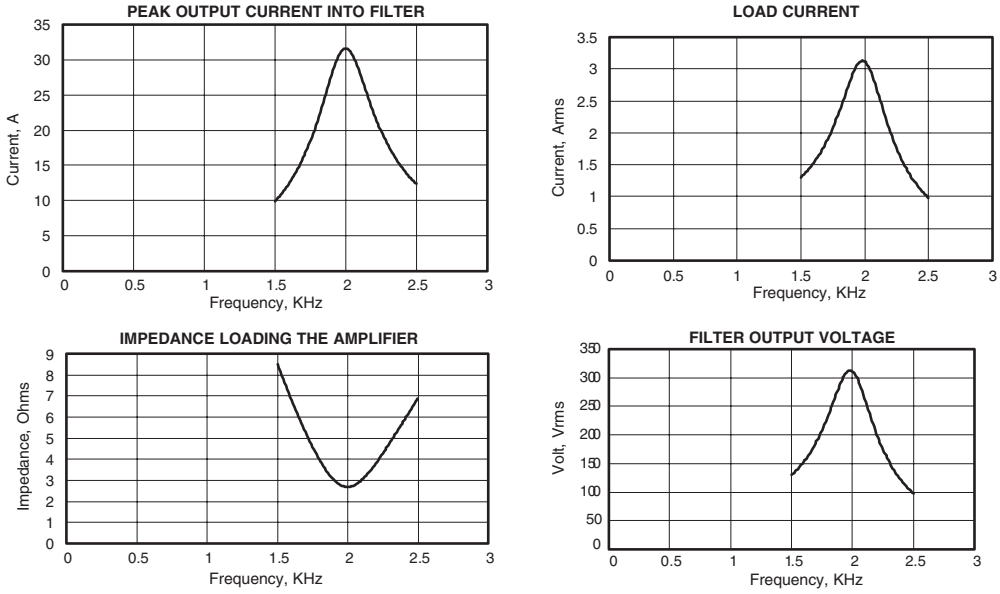


FIGURE 13. A GOOD PROCEDURE FROM THE LINEAR WORLD MAY BE DANGEROUS IN THE PWM WORLD

the parts to get accurate data for subsequent analysis. Values of purchased components and their real parasitics should be entered directly into the yellow cells and then be translated with button 88, 89, or 90.

This picture is part of the result of loading our sample application from the PWM Filter sheet (no auto sweep); going to the Filter Component Work Area with button 92; translating component values for a split-inductor design with button 85; and calculating default parasitics with button 91. Button 88 will translate prime component values and the parasitics back to single-ended equivalents and then run the frequency sweep to calculate critical voltages, currents, powers and phase angles over the frequency range we specified. 100 frequency points will be examined. If this takes less than 10 seconds, you should be proud of your computer. If it takes more than a minute ------. Frequency sweep requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then do the sweep.

Figure 11 shows attenuation of signal frequencies is close to the ideal except the entire curve is about 0.3db lower than expected. This drop is due to inductor resistance. We learned earlier that the extremely fast transition times of the PWM amplifiers means high frequency content is powerful well into the megahertz range. To check performance in this range; go to the data input screen; enter the cutoff frequency as Fmin; and at least the tenth harmonic of the switching frequency as Fmax; and rerun the sweep. The graph in Figure 12 tells us spike content at the filter output is far from ideal. An ideal second order filter for this example has about 82db attenuation at 225KHz, but parasitics reduce this figure to about 73db, or roughly a factor of 3 less attenuation with electrolytic capacitors in this dual-capacitor design. Is this OK? Or should we spend more time looking for better filter components? Or should we consider one of the other two topologies which will perform better at high frequencies?

So, you're an old hand with linear power circuits. You fire up the prototype with a light load to make sure everything is working before connecting the real load.

While this procedure is commendable for linear drives and may work fine for a PWM drive, watch out for tuned circuits in the filter/match network/load. Replacing a designed 10 ohm/1mH load with a 100 ohm purely resistive load (matching network removed), produces the graphs of Figure 13. At the 2KHz cutoff frequency, impedance presented to the amplifier drops to ~2.7 ohms, peak current tops 30A, load voltage is ~313V and load current is 3.1A. 970W delivered to the light 100 ohm load!

Be careful! Deadly voltages easily generated.

The second order filter driven at the designed cutoff frequency, with no load, is a series resonant circuit which presents a theoretical zero impedance to the amplifier and develops a theoretical infinite voltage at its center. Higher order filters generally produce lower amplitude peaks at lower frequencies relative to the cutoff frequency.

The very nature of PWM amplifiers demands reactive elements be driven. Inductance is mandatory and capacitance is very common, meaning resonance will exist. A properly designed and terminated filter will yield a response close to

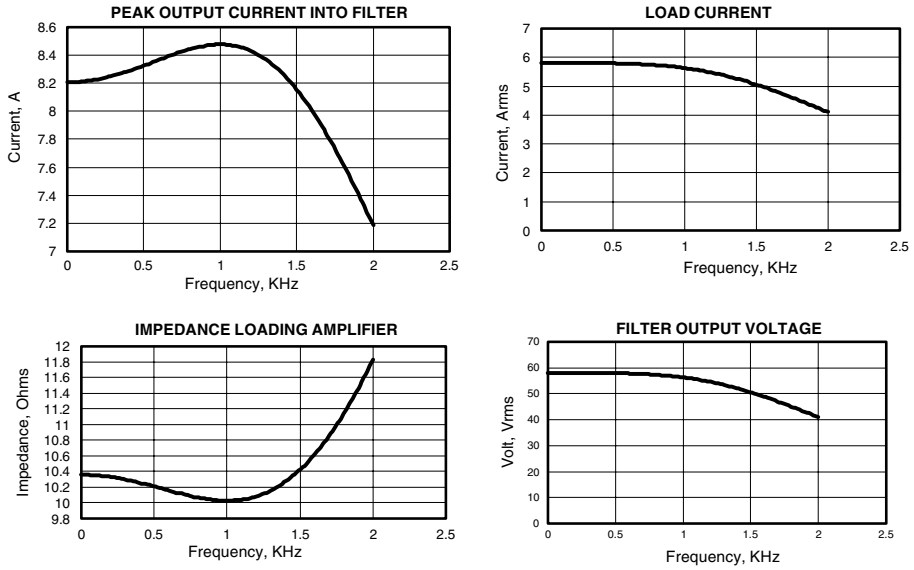


FIGURE 14. PERFORMANCE OF THE PROPERLY TERMINATED FILTER

the text book curve. The trick is to design the circuit to accommodate load variations and possibly certain fault conditions such that these conditions will not place undue stress on components or produce extreme high voltage hazards.

Figure 14 (next page) shows the well behaved performance of this example modified for a 10Ω purely resistive load. At DC, impedance loading the amplifier is the sum of the load and the parasitic 0.36 ohms of the filter inductor(s). The amplifier sees about a 3% impedance dip at mid-band and drives a corresponding peak output current. This is normal and Power Design will search for these peaks and dips when calculating heatsink requirements.

While this operation is proper, is it what you wanted? The cutoff frequency of the filter is where the load voltage is down 3db. Does -3db equal .707 or .5? Both, .707 applies to the voltage and the current ratio but .5 is correct for the power ratio. In this example output power drops form 337W at DC to 172W at 2KHz. Many times half power at maximum frequency is not acceptable. This is why some designers routinely start their filter calculations using a cutoff frequency twice the required maximum signal frequency of the application.

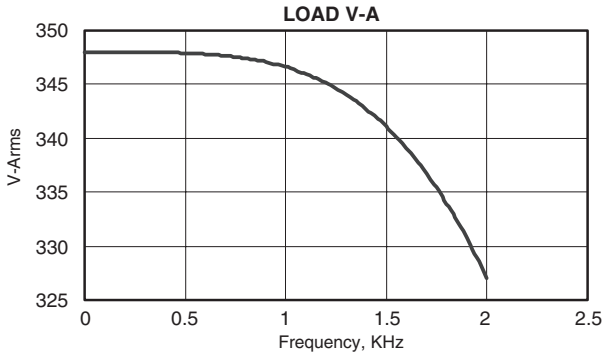


FIGURE 15. DOUBLING Fc YIELDS INCREASED OUTPUT POWER

Doubling the design cutoff frequency of the filter enables the circuit to deliver a lot more power at the desired 2KHz as shown in Figure 15. This is still a 2 pole filter and power loss is only about 6% at 2KHz. As an added benefit, inductors for a 4KHz filter are half the value of those for a 2KHz filter and likely will have substantially lower parasitic resistance.

Yes, you could double again to achieve an even flatter pass band. No, there is no free lunch. Every time you move cutoff frequency up, you allow more switching frequency power in the load. Yes, you can add more poles to the filter. Analyze as many combinations as you wish, it won't take long. The question becomes one of cost in terms of money, extra loss in the filter, size and weight.

Speaking of properly terminated filters, we need to look closely at the matching network. While the conjugate matching network performs almost like magic in terms of forcing the attenuation graph to approach text book shape, there is a cost involved. This cost is slight when the load is mostly resistive, but the power dissipated in this network approaches power delivered to the load as the load approaches pure reactance.

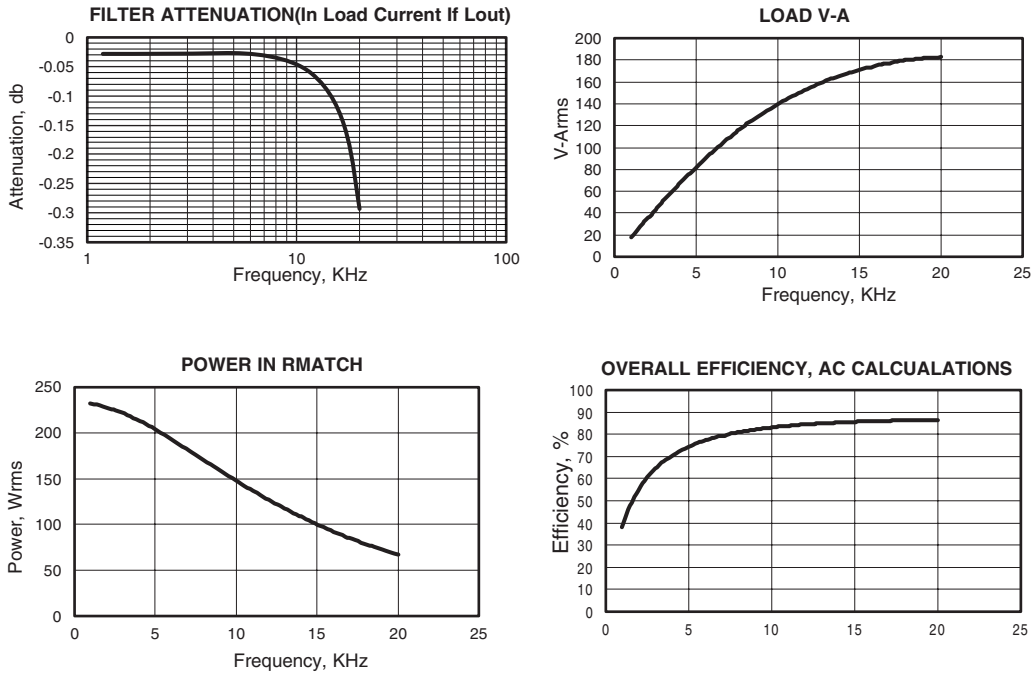


FIGURE 16. PERFORMANCE OF THE PROPERLY TERMINATED FILTER

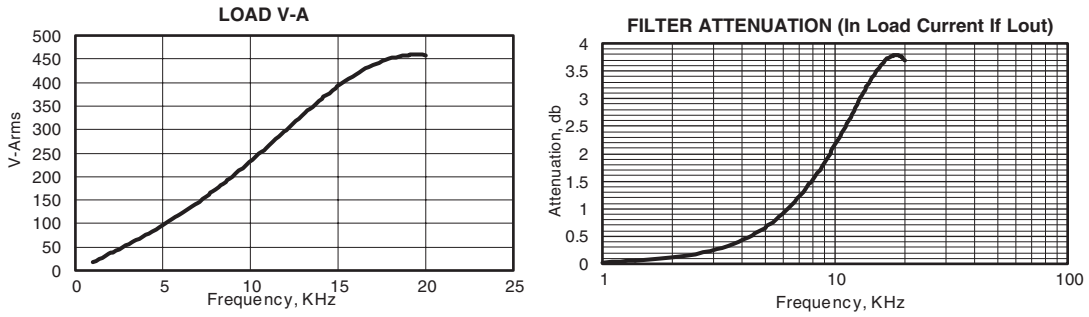


FIGURE 17. THE BAD NEWS IF THE MATCHING NETWORK IS OMITTED

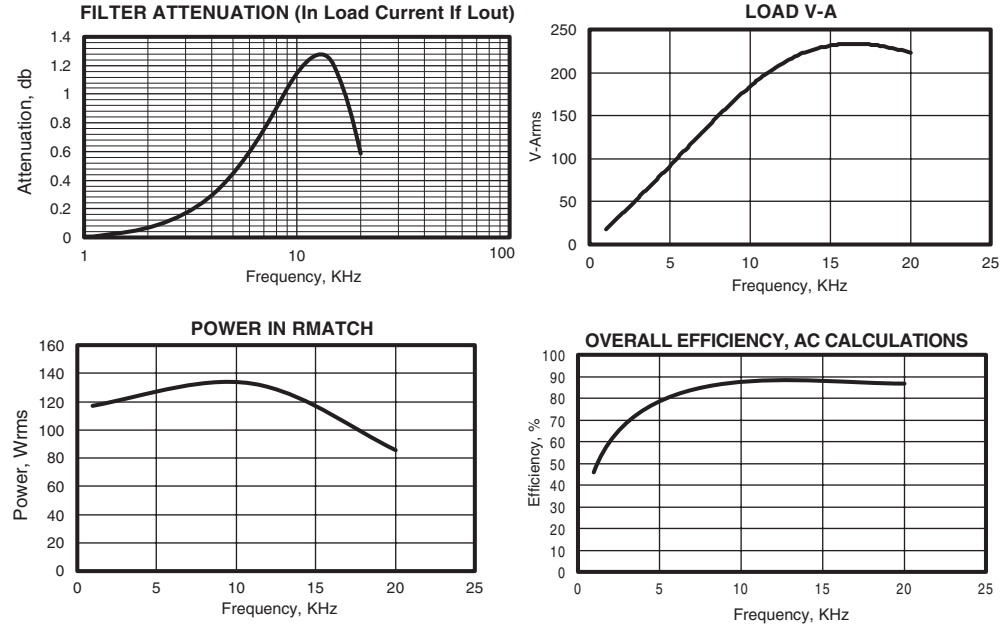


FIGURE 18. RESULTS OF A MODIFIED MATCHING NETWORK

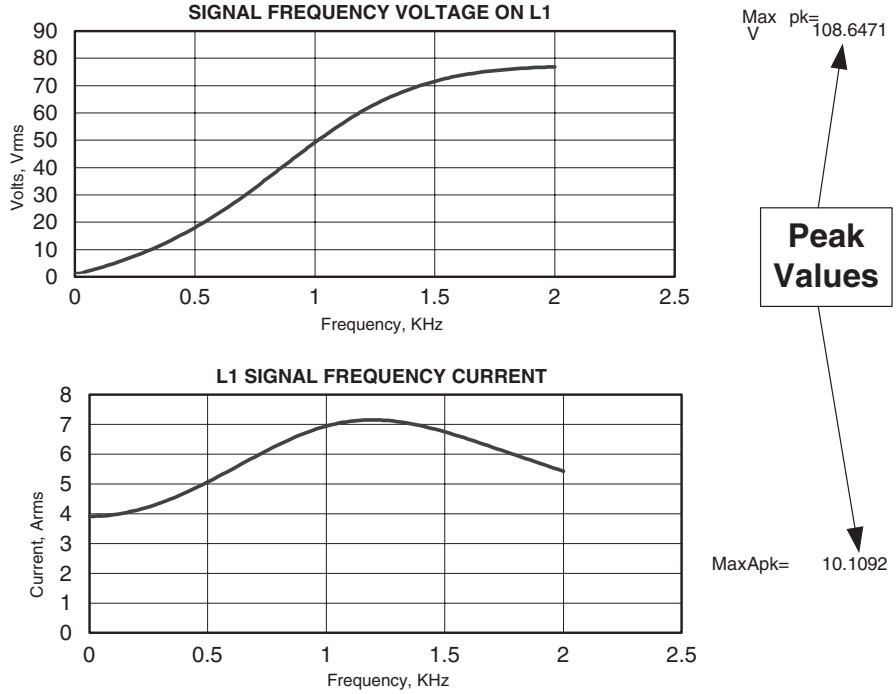


FIGURE 19. STRESS LEVELS ON L1

The graphs of Figure 16 are for an application driving a 1uF piezo stack with 12 ohms series resistance, to 75V peak from 1KHz to 20KHz. The second order filter cutoff frequency was designed for 40KHz providing a quite flat response. The V-A output falls at low frequency because the load impedance is increasing. To keep filter termination impedance flat, the matching network impedance moves in the opposite direction, giving rise to large power levels in the matching network resistor, especially at low frequencies. As this power is not delivered to the load, efficiency is far from the desired level.

Upon seeing this power loss, some designers immediately want to see what happens if they simply remove the matching network. With no matching network we cannot lose this power, but this leaves the filter with an improper termination. This would result in a unwanted resonant circuit causing almost 4db peaking as shown in Figure 17 (next page). In terms of V-A in the load near the upper end of the band, power goes from ~180 to over 450V-A. If you wish to see more on this subject, use the Filter Hazard on the Power Design Examples sheet. Comments explain each situation and a macro sets up and runs the analysis.

Here lies part of the beauty of the Power Design tool; investigating possible compromise circuits is a snap. See Figure 18 for results of doubling the resistor value in the matching network which may provide a workable compromise. Peaking at the load is down substantially from not using any network and wasted power is down substantially from using the ideal network.

DETERMINING FILTER COMPONENT STRESS LEVELS

This section uses the original coil driver example, with the second order filter designed for cutoff frequency=2KHz; load resistance=10Ω; and load inductance=1mH. However, we are assuming the load has gotten hot and the resistance has gone up to 15Ω.

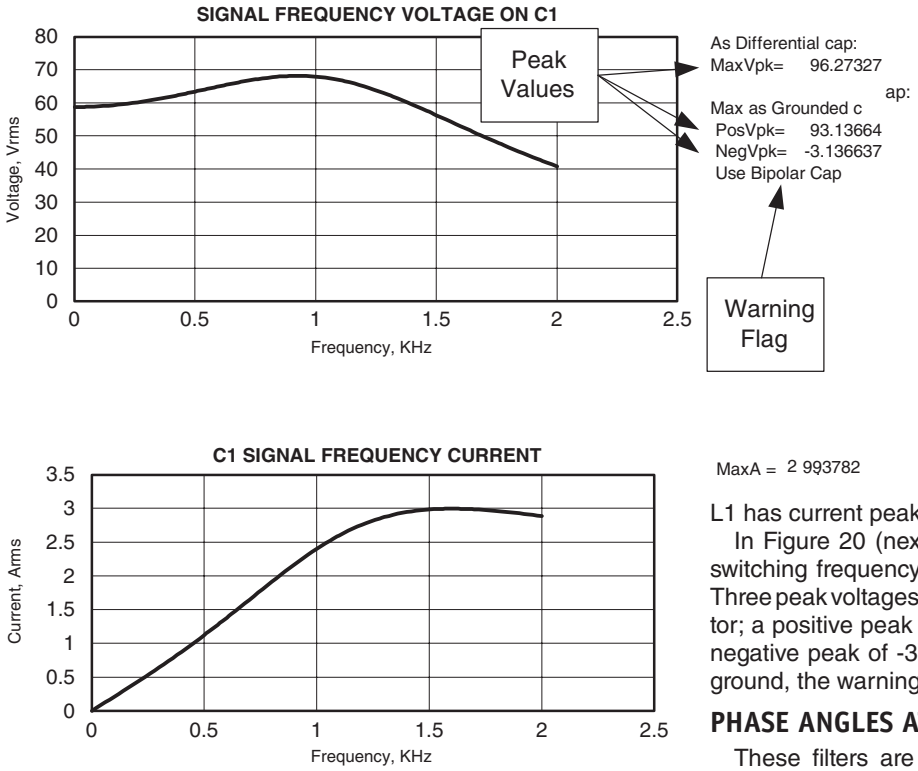


FIGURE 20. STRESS LEVELS ON C1

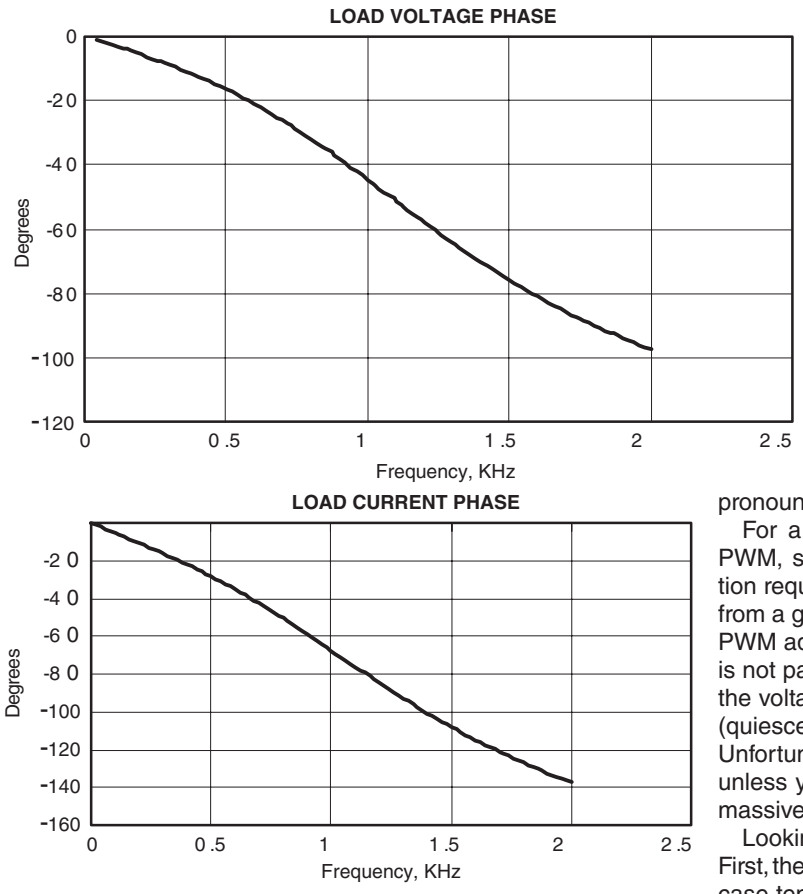


FIGURE 21. VOLTAGE AND CURRENT PHASE IN THE LOAD

This change affects all the performance graphs covered so far and they should be checked. Power Design calculates voltage and current stress levels on L1 and L2, plus C1 and C2 for all designs. Resonance of these filters can produce voltages and currents larger than the load levels. Button 84 will place the first graph on the screen, then scroll up and to the right to view other graphs. The currents shown in Figure 19 can be used directly for all filter topologies. If L1 is actually two inductors, half the voltage shown will be across each individual inductor. Note that our circuit example only has a 90V supply; the drive signal is only 85Vpk; the load resistance is 15Ω; but L1 has current peaks of 10.1A and voltage peaks of 108V.

In Figure 20 (next page), we find that in addition to the switching frequency current, C1 has 3A flowing at 1.6KHz. Three peak voltages are given; 96Vpk for a differential capacitor; a positive peak of 93V for a grounded capacitor; and a negative peak of -3V. Any time the negative peak is below ground, the warning to use bipolar capacitors also appears.

PHASE ANGLES AT THE LOAD

These filters are notorious for introducing large phase shifts. This is usually not a problem when feedback is taken directly at the output of the PWM amplifier. In applications such a servo loops, feedback is taken after the filter and any phase shift introduced here affects system phase margin. Figure 21 shows both voltage and current phase in the load for this example. This phase shift is reduced as the ratio between Fmax and Fcutoff frequencies widens, and is lower with lower order filters.

CALCULATING INTERNAL POWER DISSIPATION FOR PWM AMPLIFIERS

Heatsink selection for most PWM amplifiers is more complex than for a linear amplifier because FET ON resistance (and hence voltage drop, internal power and dissipation) increases roughly 2:1 as junction temperature goes from 25°C to 150°C. PWMs have the same concern over temperature vs. life expectancy as linears, but changes of circuit performance over temperature are much more pronounced than with linear amplifiers.

For a first order estimation of power dissipation in the PWM, simply multiply the output current (a given application requirement) and the voltage drop at that current (read from a graph on the product data sheet). This points out the PWM advantage over linear power delivery; supply voltage is not part of the equation. With a first order approximation, the voltage drop divided by supply voltage yields efficiency (quiescent current of both Vcc and Vs will reduce this a little). Unfortunately, first order approximation is not good enough unless you have the luxury of using overkill amplifiers and massive heatsinks.

Looking a little deeper, there are two points of confusion. First, the voltage graph offers multiple curves based on various case temperatures. We know cooler is better for life expec-

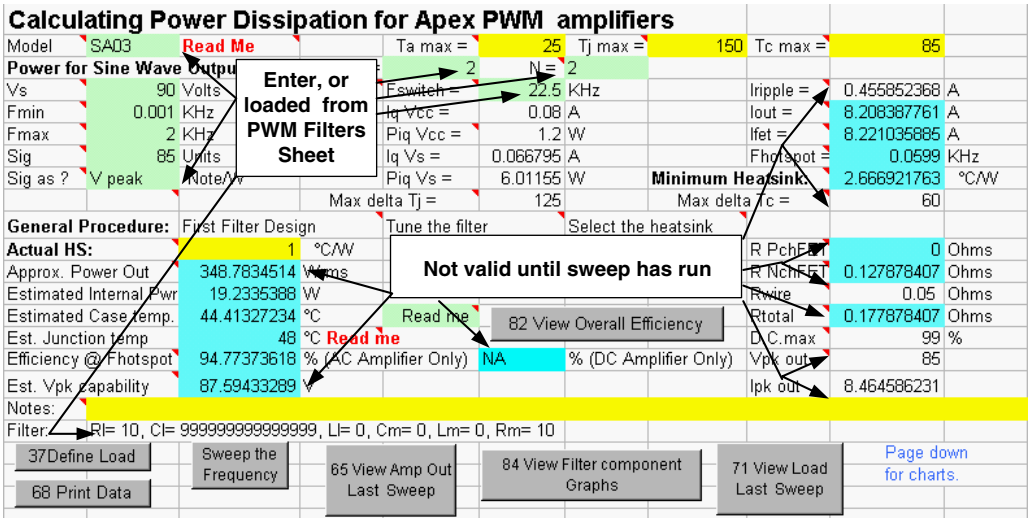


FIGURE 22. THE PWM POWER SHEET DATA INPUT SCREEN

tancy and efficiency, but there are no rules regarding which one to choose. Something not presented in any direct way is the second problem: methods to calculate junction temperature are not given. This is a parameter every power designer should know and it is often specified by contract.

While the linear Power sheet simply provides you with a minimum heatsink rating, the PWM Power sheet gives you graphs of junction temperature, internal dissipation and efficiency. With this data, you can make intelligent tradeoffs concerning circuit operation vs. investment in the heat removal system.

Our exercises on filter design have already taken us to the PWM Power sheet. From numerous locations you can use command button 38 to see the Data Input screen as shown in Figure 22. The green input cells are normally filled in with one of the Load Data command buttons on the PWM Filter sheet. These values may be changed at will but neither the graphs nor circuit parameters in the blue cells will necessarily be valid until a Frequency Sweep has been run.

In the center area, find data on quiescent current and resulting power dissipation. Data for these calculations comes from application parameters and the built-in database containing information on quiescent current variations with supply and switching frequency. In the upper right, applying a sine wave at the switching frequency and using a correction factor have approximated ripple current. If the filter and load are close to those entered in the Filter sheet, this ripple approximation will be close to ripple predicted by the Filter sheet. Hotspot frequency is the frequency where load current is producing the highest junction temperature. This is not necessarily coincident with the frequency producing the highest peak current. Consider the case of a DC current of 10A rising to 11A peak at 1KHz. At 1KHz heat generation is alternating between pairs of transistors fast enough to find them running cooler than at a steady state level of 10A.

The Iout cell will report amplifier output current at signal frequencies using peak values for hotspot frequencies below 60Hz or RMS values at higher frequencies. The Ifet cell is the RMS addition of the ripple current (at the switching frequency) and the output current. If hotspot frequency is 60Hz or more, ripple current is reduced 30% because ripple decreases as duty cycle increases (there is no ripple at 100%). The Minimum Heatsink is the thermal rating which will keep both the case temperature and the junction temperature within the boundaries entered at the top of the screen.

Continuing down on the right side are On resistances of the H-bridge switches at the hotspot frequency. The P channel number will be for one FET if P channel devices are used in the amplifier. If this is the case, the N channel number will also be for one FET. When only N channel FETs are used, this number will be for two FETs. If you specify a heatsink that will not keep junction temperatures below the specified maximum, both FET resistances will be forced to 10 ohms. Rwire represents internal conductor losses in the amplifier and Rtotal adds it all up. For amplifiers using IGBTs, all resistance cells will be blank.

Most PWM amplifiers can hold their output switches in one state. To rephrase, PWM amplifiers can be driven to zero or 100% duty cycle; however, propagation delays and dead time requirements limit the linear modulation range to less than these levels. D.C.max is the maximum percentage of the power supply voltage delivered before encountering the non-linear jump to being latched in one state. Vpk out and Ipk out are from anywhere between Fmin and Fmax.

Back on the left side under Actual HS, Approx. Power Out is the power factor corrected VA output directly at the amplifier at the hotspot frequency. If you really intend to look at DC or want a peak value, multiply by two. Estimated Internal Pwr includes losses due to driving the load and the quiescent power.

Efficiency of a DC power supply would compare DC, or peak power out, to input power. Efficiency of an audio amplifier would likely compare RMS power out to input power. These two approaches to efficiency will produce different answers for the same amplifier, driving the same peak current from the same power supply. Power Design always calculates an efficiency based on the AC thought process but will give you a DC based answer only if both Fmin and Fmax are less than 0.003 (remember to Sweep before reading the answer). In both cases, the numbers appearing here do not include filter loss. Est. Vpk capability subtracts internal losses and duty cycle limitations from the supply voltage.

Not shown in Figure 22 are four data dependent red warning flags. The first warning appears if the Actual HS is too small to maintain either specified case temperature or junction temperature. If Est. Vpk capability is less than the signal voltage, the next flag will become visible. The third flag warns of output current beyond the peak rating of the amplifier. The last flag concerns application supply voltage compared to amplifier ratings.

We know many of these numbers are a moving target relative to selection of the actual heatsink rating. Refer to Figure 23 (next page) for this important step. All heatsink references assume fresh thermal grease has been properly applied or an Apex Precision Power thermal washer has been used.

In the upper left graph it looks like a quite small heatsink will keep junction temperatures below the maximum of 150°C

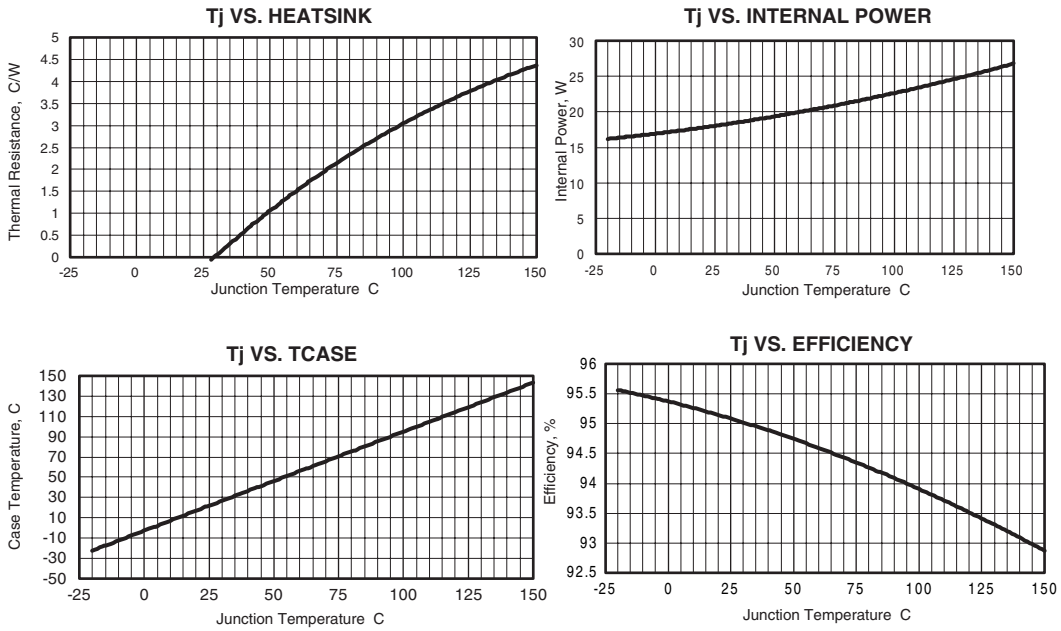


FIGURE 23. SELECTING A MAXIMUM JUNCTION TEMPERATURE IS THE KEY STEP

specified by almost all PWM amplifiers. However the graph below says there is little difference between junction and case temperature and we surely want to keep case temperature much lower than 150°C.

On the top right we see that internal power dissipation of the amplifier changes with junction temperature. Settling for the minimum heatsink size instead of investing in a 1°C/W heatsink (easy to do without a fan) will increase internal power almost 8W or nearly 40%. Below we see this same effect expressed in terms of efficiency. At first, moving only a few percentage points may not seem like much, but remember these points are relative to a quite large power level. Enter 100 as the Actual HS if you plan to not use a heatsink. More likely, a rating will come from the Heatsink sheet of Power Design, a manufacturer's data sheet, or your own design efforts.

The efficiency graphs above refer to performance only at the hotspot frequency and do not include filter losses. Figure 24 however, includes losses in the filter and matching network and provides frequency data. The curve is based on the AC thought pattern discussed earlier, input power compared to RMS power delivered. If there is a glitch at 60Hz, it is due to the instant change (mathematically) from peak power heating effect to RMS power heating effect. Fig. 24. Including filter losses in the big picture.

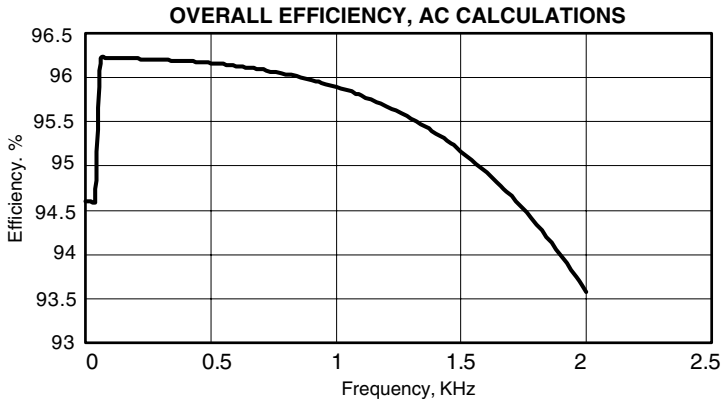


FIGURE 24. INCLUDING FILLER LOSSES IN THE BIG PICTURE

CONCLUSION

The Power Design tool is even more important to the PWM designer than the linear designer. PWMs are not as widely understood and worse yet, literature is not as widely available. The comments and automated examples built into this spreadsheet serve well as a text on the subject. PWMs also tend to require more iteration to approach an optimum design and are more frequency sensitive than linears. Again, tackling all this with computer aided design is the only way to go and the tasks of filtering and heatsinking are better handled by Power Design than by many Spice machines.

Not to harp on it, but do not let all this quick and easy data lead you into the trap of accepting theory with a smile while sticking your head in the sand when it comes to the hardware world and parasitics. And one more time: Without case temperature measurements, your design effort is NOT complete!

Stability and Biasing for PWM Amplifiers

1.0 INTRODUCTION

PWM applications are complex systems with a highly non-linear modulation/demodulation system at the heart of things. This mandates a collection of poles and zeros plus high harmonic and sub-harmonic content. This is further complicated by the fact that gain of the PWM block varies with supply voltage. These factors can make stability considerations a confusing issue without a plan of attack, that includes test criteria and some tools to obtain data. The successful design will arrange all the break points in a manner to avoid oscillation while maximizing bandwidth.

2.0 THE BASIC SYSTEM AND ITS CHALLENGES

Refer to Figure 1 showing the basic elements of a PWM amplifier circuit. The integrator will drive the PWM block where ever required to force feedback current to be equal and opposite of the input current. We will discuss only analog implementations, but computerized systems will function in a similar fashion. The PWM block translates its input to time modulated pulses of full supply amplitude. As of May 2001, all Apex Precision Power PWM full-bridge amplifiers utilize locked anti-phase modulation (when one output is high, the other is always low; 50% modulation means equal times high and low for each cycle of switching frequency and after demodulation, 0V at the load). For more detail, see APPLICATION NOTE 30, PWM BASICS. The low pass power filter demodulates the PWM signal so the load sees little of the switching frequency carrier. It is in these modulation and demodulation stages that signal and carrier frequencies are mixed, as well as sums and differences are generated. The low pass signal filter has multiple input connection options; however, in all options, it reduces the carrier content that the feedback gain amplifier must deal with.

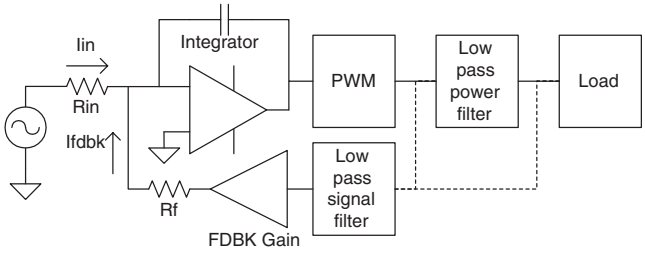


FIGURE 1. A TYPICAL PWM SYSTEM

Notice that the low pass function in the feedback loop will tend to make closed loop gain of the total system INCREASE above its corner frequency. Or we could say the pole in the feedback loop is going to cause the same stability problem as a zero in the closed loop gain of the system. To better understand the system, we will examine the various poles and zeros plus other problem areas.

Knowing the gain of the PWM block will be critical to analyzing this system. Finding the exact gain of the PWM block, including the effects of dead time, internal voltage loss and reverse currents in the catch diodes would be a formidable task. A suitable approximation is to compare full scale input with ideal full scale output. Product data sheets will give analog input voltages needed to generate modulation percentages. Modulation extremes will correspond to the upper and lower peaks of the ramp. Full scale input is then = VRAMPp-p. Full scale output on a single pin is the voltage change from 0 to 100% modulation, which equals supply voltage. In the case of a full bridge, we need to multiply this by two, because the load is connected differentially, seeing two equal and opposite drive voltages.

Gain of the PWM block = Vout p-p / Vramp p-p (1)

Where Vout p-p = Vs for half bridges and Vs * 2 for full bridges and Vramp p-p is set by the specific amplifier model, generally between 2.5 and 5V p-p. A full bridge PWM with a 4V ramp, running on 40V, has a gain of 20.

As the ratio between ramp voltage and supply voltage increases, the gain increases. Note that some PWM amplifiers, such as the SA50 and SA60, vary the modulation ramp voltage as Vcc varies. It would be acceptable to think of this changing gain as a changing gain-bandwidth product in an op amp circuit. The integrator and the PWM block are in series, so when viewed together, the gains of the two stages are added. Just as in linear circuits, achieving stable operation will be easier when all gain blocks are low compared to a system having higher gain blocks. In all cases, phase margin of the circuit will decrease as PWM gain increases. This means stability must be checked at maximum Vs, and minimum Vcc if appropriate. On the other side of the coin, check bandwidth at minimum Vs and maximum Vcc.

The job of the power filter is to attenuate the square, time modulated carrier and deliver only (ideally) the low frequency signal to the load. If the filter does a very good job, feedback must be taken ahead of the filter. If the filter is designed to have a minimum effect, feedback may be taken after the filter. In either case, the feedback signal will contain significant amounts of high frequency energy.

Taking voltage feedback after the power filter can put a PWM circuit well on the way to being a power oscillator. These filters contain a minimum of one series inductor and often some large capacitors on the load side of the inductor(s). If the filter design is not proper, or the load impedance has shifted after the filter was designed, the series L-C section(s) of the filter can produce serious peaking at the output. Even properly designed and terminated filters produce wild phase shift near their cutoff frequency. The technique of taking voltage feedback after the power filter is usually reserved for very special cases, the filter will be first order (inductor only) and the load is doing most of the filtering.

The low pass signal filter is used to attenuate the high frequency content of square PWM wave forms which have very short rise and fall times. Without this roll off, feedback gain amplifiers would need unrealistic bandwidth capability. The down side here is that a pole in the feedback path equates to a zero in the closed loop gain, a red flag for possible stability concerns.

Even with this filter, op amps picked for this job should exhibit superior high frequency common mode rejection. The non-linear response of feedback amplifiers can add extraneous signals to the feedback. The problem comes from the fact that feeding an op amp signals well above its bandwidth capability will often force the input stage into non-linear operation, resulting in what appears to be an offset error. This is compounded by the fact

the high frequency content (spikes) of PWM signals varies with modulation percentage. Imagine trying to drive a sine wave when an extra pulse is inserted every cycle between 150° and 180° and again between 330° and 360°! This is a path to distortion and in severe cases, to oscillation.

Along with R_F, the feedback voltage provides current to charge the integrator capacitor to the proper level. This capacitor should be the dominant frequency limiting element of the entire system. So, just where is the pole created by the integrator capacitor? As there is no resistor directly in parallel with this capacitor, the traditional calculation for an op amp roll off capacitor will not work. However, if such a resistor were in place (rather than our complex feedback loop), what would its value be? This fictitious value would result in the same change of integrator output voltage for a given change of input voltage, as occurs in the real system. To re-phrase, if we know Δinput current to the integrator, and output voltage of the integrator, then Ohms law dictates the effective feedback resistance must be ΔVOUT/ΔIIN. To answer these questions we need to know the input signal, the input resistor and how much the output of the integrator will move in response to the input signal.

To find this fictitious feedback resistor, refer to Figure 2, and assume a convenient input and use the given transfer function to find the PWM output voltage. Now divide by PWM gain (equation 1) to find the movement of the integrator voltage.

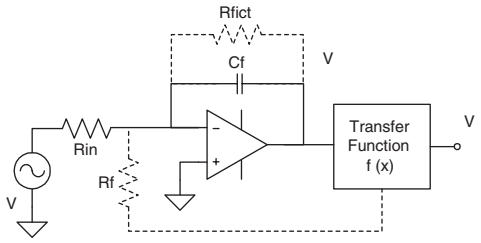


FIGURE 2. REPLACING THE REAL FEEDBACK SYSTEM WITH A FICTITIOUS RESISTOR

$$R_{FICTITIOUS} = R_{IN} * \Delta integrator / \Delta input \quad (2)$$

Using this fictitious feedback resistor, the pole frequency can be calculated just as if it were an op amp with parallel R-C feedback. When powering the SA01 (full-bridge and 5V p-p ramp) on 75V, gain of the PWM block is 30. If the circuit is configured for a gain of 10 (say, ±5Vin, ±50Vout) and the input resistor is 5K, Δ out =100, Δ integrator =3.333, Δinput = 10, and Δthe fictitious resistor is 1.67K. Even though the real RF maybe 5KΩ, a 0.1µF capacitor produces a pole at 953Hz.

If the overall system is controlling current rather than voltage, the foregoing is still true, and we have a new concern. The load is always inside the feedback loop for current control. Given a constant output current, output voltage will be a function of load impedance. This also means that load impedance is a factor in the integrator output swing, thus affecting the value of our fictitious feedback resistor, the pole frequency set with the integrating capacitor, system bandwidth, and stability. If load impedance changes only with factors other than frequency, such as resistor element thermal variation, the circuit can usually be checked at the two extremes and no special measures are required.

More often the load contains significant inductance which demands output voltage increase with frequency and it adds the V-to-I phase shift of the inductor to the feedback loop. In these cases, an additional voltage feedback path is usually added. The objective is to have this path come into play at a low enough frequency to avoid a stability problem, but high enough to achieve desired bandwidth.

The most common topology for current control is to use a differential amplifier, monitoring sense resistors in both the lower legs of the H-bridge. This leads to non-textbook filter design for current output circuits, especially when the load is inductive. This current sense yields a combination of load current, matching network current, plus filter capacitor current. To minimize errors in the load current, the filter and matching network need to be very light handed in the input signal frequency band. Filters will often be first order and matching network impedance will be increased as high as voltage peaking concerns will allow.

Servo loops are even more complex in that feedback is usually taken from position or velocity sensors. In these cases, power filtering is at an absolute minimum and additional compensation networks are sometimes applied with or between sensors, signal conditioners and the integrator.

Before proceeding, lets take notice of two items not included in this list of problem areas: frequency domain performance of the PWM block and the op amps used for feedback gain and for the integrator. With the frequency relationships discussed below, it can be demonstrated how the PWM block response is an insignificant problem. Op amps selected to meet the common mode rejection requirement at FSW, will automatically have enough gain-bandwidth product to not cause problems at the lower frequencies to be amplified.

3.0 FREQUENCY RELATIONSHIPS

The PWM F_{SW}, and required attenuation of F_{SW} at the load limit power filter the cutoff frequency, F_C. A reasonable starting place is to allow at least a decade between these two frequencies. A second way to look at this is to say you will allow at least ten segments or pulses to approximate the waveform delivered to the load. If the load is sensitive to high frequency components in the drive voltage, a larger ratio between these two frequencies will help and adding more poles to the filter will help. See APPLICATION NOTE 32 PWM LOW PASS FILTERING for additional information.

The low pass signal filter consists of one or more R-C pairs. The corner frequency is usually a decade or more below F_{SW}. The common mode capability of op amps, Vs , and system bandwidth requirements all factor into the design. If feedback is taken directly at the PWM output (by far the most common method), this filter sees a square wave input with peak-to-peak amplitude nearly equal to Vs. If feedback is taken after the power filter, phase shift of the power filter is added to the loop response. For this reason, a power filter inside the loop will be low Q and low attenuation.

The integrator pole frequency will be a fraction of the feedback pole(s). The higher the supply voltage, the smaller the fraction that should be used.

4.0 THE TECHNIQUE: PLOT 1/SSETA AVOID PEAKING

While the final filtered output is the objective of the PWM application, the best observation point is the integrator output. This approach allows borrowing some software analysis techniques from the op amp world. Even in the hardware world, it is often easier to monitor the integrator output (non switching and usually in the range of 0 to 10V) than monitor the output (switching, often differential, and centered at half the supply voltage).

The process of calculating the feedback factor of the inte-

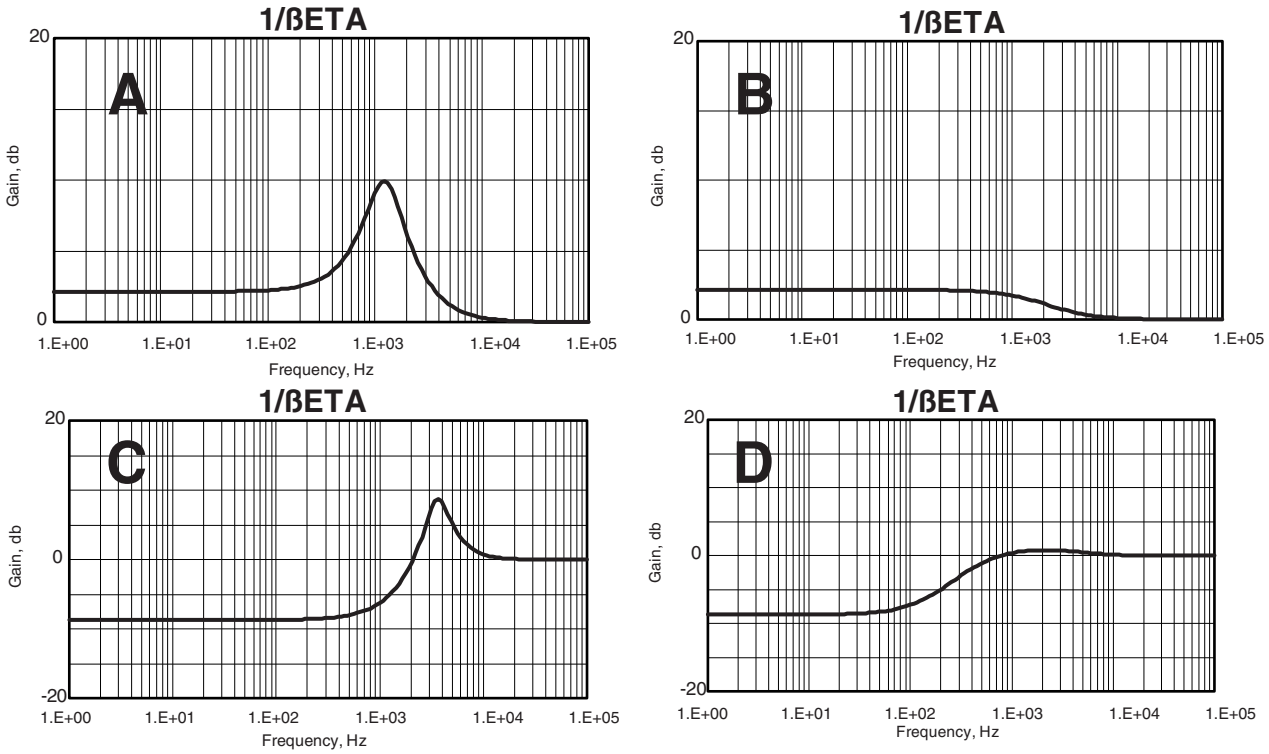


FIGURE 3. BASIC POSSIBILITIES FOR SHAPE OF THE 1/ßETA CURVE

grator is similar to that for a more traditional op amp circuit. First, assign a value of 1V to the integrator swing, and then calculate through all feedback paths back to the input(s). To finish the job, combine positive feedback (if it exists) with the negative; invert the feedback factor to obtain 1/ßeta, convert to dB, and plot the results. The objective will be to minimize or avoid peaking in this curve to assure a stable circuit.

There is one major point we learned for op amps that we must discard: "Feedback factor is always between 0 and 1, meaning feedback is limited from nothing to 100%." Because the PWM circuit has a gain block between the integrator and the feedback, it is possible to feed back more than 100% at low frequencies! At high frequencies, the integrator capacitors force 1/ßeta to 0dB, meaning there will be an increase in 1ßeta.

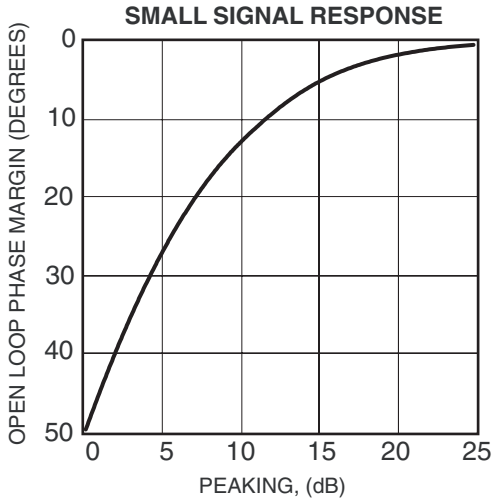


FIGURE 4. CONVERTING SYSTEM RESPONSE TO PHASE MARGIN

Refer to Figure 3 for examples of both peaking and non-peaking performance. Plot A resembles an op amp circuit with problems; low frequency 1/ßeta is positive, the peak spells trouble, and 0dB is approached at high frequency. Plot B is more what we want to see to insure stability. If bandwidth is not a concern, no peaking is desirable. When speed is a significant concern, some peaking will help, but at the expense of phase margin. For this case, peaking is defined as rise above the low frequency value.

Plots C and D are again bad and good, except for the case where low frequency 1/ßeta is negative. This will occur more often with the higher voltage amplifiers and it will be more difficult to eliminate all peaking without a severe penalty in bandwidth. The rise from the initial negative value to 0dB at high frequency is not part of the peaking we are looking for. For this case, peaking is defined as just the rise above 0dB.

Judgment criteria for PWM circuit stability will be taken from hardware tests often used in the linear world. The system response peaking curve as shown in Figure 4 is the first criteria used. This test can be applied to the 1/ßeta curve mentioned earlier, to Spice simulations, or to actual hardware. With the system running closed loop, plot the frequency response of the integrator output. Then extract the amount of peaking, using the above definitions. Note that this test is not defined over 50°.

The square wave peaking test as shown in Figure 5 (next page) can be applied to either Spice simulations or to hardware. Sum two input signals to produce a small square wave riding on a much slower triangle (or sine). If a nominal 2Vp-p square wave displays a step peaking at 2.5V, phase margin is about 35°.

5.0 GENERAL TOPOLOGY SELECTION

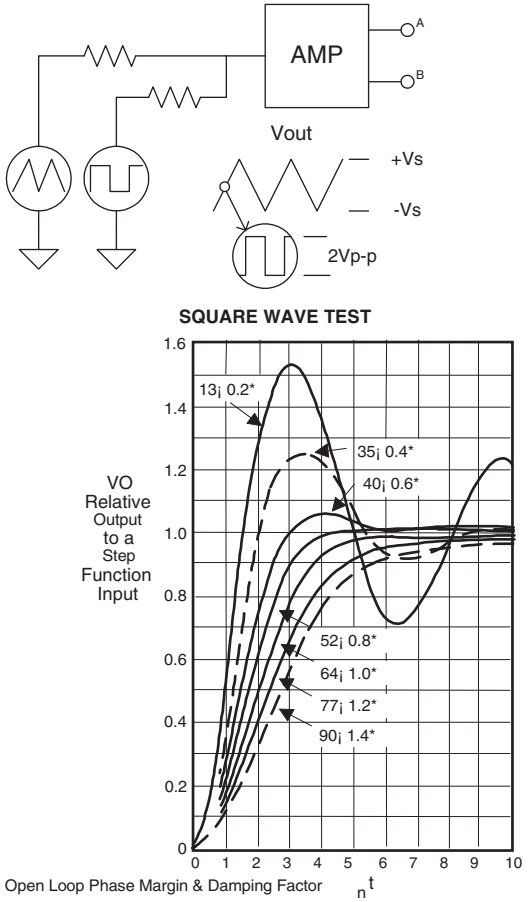


FIGURE 5. THE SQUARE WAVE STABILITY TEST AND RESULTS INTERPRETATION

Figure 6 illustrates the two most common topologies for controlling output voltage. While the filter and load are part of the system, they are outside the feedback loop in most voltage control systems and can be ignored for the most basic analysis. Type V1 requires an additional amplifier, but this topology lends itself well to level shifting input signals (unipolar input producing bipolar output) with a single resistor because the summing junction does not move as the input signal varies.

Type V2 is simpler, but does not go well with single resistor level shifting because the summing junction moves as the input signal varies. To level the shift, a reference capable of sinking and sourcing current should be applied to the opposite input signal location. This circuit then functions similar to a four resistor difference amplifier, except a T-network of two resistors and a capacitor replaces each single R_F (add the two resistors for DC gain calculations), and the pin normally labeled reference is connected to the inverting PWM output. The output is now differential rather than single ended and DC circuit gain is simply R_{Ftotal}/R_{IN}. Extra components may be required to meet common mode voltage restrictions of the integrator op amp.

For common current control options, refer to Figure 7. This time the load is central to stability issues because it is inside the feedback loop. Load and filter must be specified right up front.

Type I1 mandates the PWM amplifier to have 2 Isense pins (some models have only 1). This topology does not require high voltage capability for the differential amplifier. For supply voltages above 200V, this is probably the best choice.

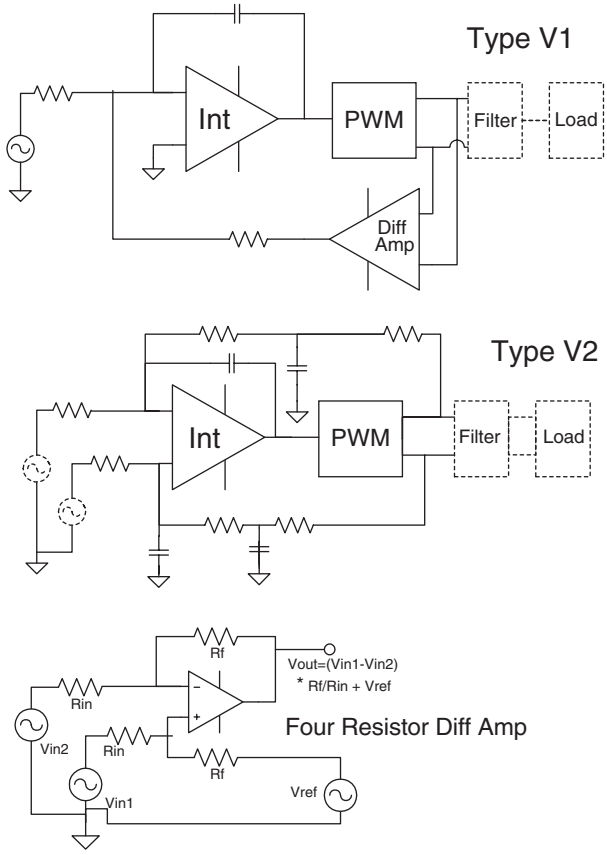


FIGURE 6. BASIC VOLTAGE CONTROL TOPOLOGIES

Type I2 is required for PWM amplifiers with only one sense pin. This type should also be considered if the filter contains a matching network (type I1 assumes matching network current is delivered to the load). Note a MAJOR change for the diff amp from type I1:

Differential voltage is still usually a volt or less, but Common Mode Voltage (we need to reject this) is up to supply voltage!

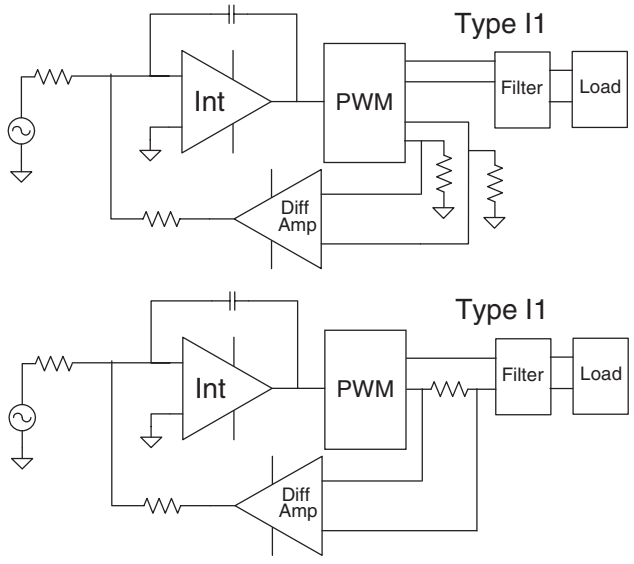
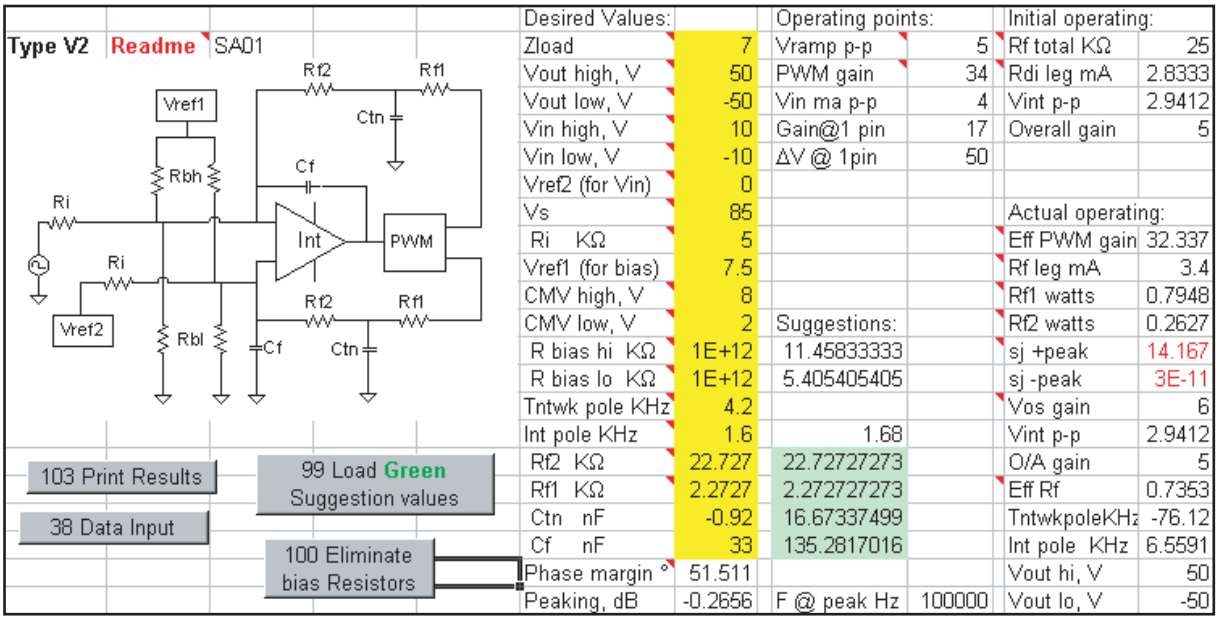


FIGURE 7. BASIC CURRENT CONTROL TOPOLOGIES



Desired Values:		Operating points:		Initial operating:	
Zload	7	Vramp p-p	5	Rf total KΩ	25
Vout high, V	50	PWM gain	34	Rdi leg mA	2.8333
Vout low, V	-50	Vin ma p-p	4	Vint p-p	2.9412
Vin high, V	10	Gain@1 pin	17	Overall gain	5
Vin low, V	-10	ΔV @ 1pin	50		
Vref2 (for Vin)	0				
Vs	85			Actual operating:	
Ri KΩ	5			Eff PWM gain	32.337
Vref1 (for bias)	7.5			Rf leg mA	3.4
CMV high, V	8			Rf1 watts	0.7948
CMV low, V	2	Suggestions:		Rf2 watts	0.2627
R bias hi KΩ	1E+12	11.45833333		sj +peak	14.167
R bias lo KΩ	1E+12	5.405405405		sj -peak	3E-11
Tntwk pole KHz	4.2			Vos gain	6
Int pole KHz	1.6	1.68		Vint p-p	2.9412
Rf2 KΩ	22.727	22.72727273		O/A gain	5
Rf1 KΩ	2.2727	2.272727273		Eff Rf	0.7353
Ctn nF	-0.92	16.67337499		TntwkpoleKHz	-76.12
Cf nF	33	135.2817016		Int pole KHz	6.5591
Phase margin °	51.511			Vout hi, V	50
Peaking, dB	-0.2656	F @ peak Hz	100000	Vout lo, V	-50

FIGURE 8. INITIAL DATA ENTRY AND PRELIMINARY CHECKS FOR TYPE V2 CIRCUITS

This means CMRR is VERY important and buying a packaged instrumentation amplifier is almost always superior to making one. Remember that the basic four-resistor differential amplifier exhibits a common mode rejection error voltage of common mode voltage times the ratio mismatch between the two resistors on the plus input and the two on the minus input. To achieve 80dB CMRR (even with a prefect op amp), resistor mismatch between the plus and minus sides needs to be limited to .01%!

6.0 TOOLS FOR DESIGN

PowerDesign.exe is a self-extracting spreadsheet for Excel 97 or later. The PWM Stability sheet automates much of this application note, plus includes diagrams and macros for fast execution of common tasks. The liberal use of comments (place cursor in cells with the red triangles) helps the user with both spreadsheet use and with hints and facts on PWM operation. It is the fastest of all the design tools. Its limitations include dedicated topologies, no square wave test, as well as minimal data on maximum bandwidth.

Spice state average models are available for both Berkeley based and Pspice based simulators. With no PWM switching, these models run many times faster than the pulse by pulse models and they can run an AC sweep, making the optimizing of feedback loops very quick once a schematic has been captured. With a Spice platform, topologies are wide open.

Spice macro models are the closest to the hardware of all the tools. Pulse by pulse switching will show some distortion elements the faster tools cannot. They may also show you some capacitors are working harder than you ever imagined, but these additional capabilities may boost simulation time more than two orders of magnitude. Also, these models are not capable of an AC sweep.

So, all three of these software tools agree to your design. This does NOT mean the design is done. There are some things to check which should only be trusted to bench work with real hardware. Significant problems may still exist relating to a mix of high current, high voltage and high frequency all at the same time. When using the fastest PWM amplifiers, one inch of wire in the wrong location can destroy performance. Most readily available op amp models do a poor job of predicting real errors when the input is overloaded with high frequency garbage. While a pulse by pulse model, along with modeling EVERY parasitic would be impressive (and maybe even correct), who has the time and ability to figure size and location of each one?

Before going to the bench, here are a couple of cautions:

1. Even though years of op amp experience may have taught you to start with a reduced load, this can be dangerous with PWM circuits. A reduced load means the filter you designed is improperly terminated, and may produce output voltages far in excess of the supply voltage.
2. Starting with a reduced power supply is fine, as long as you realize bandwidth will increase and phase margin will decrease when the higher design value is applied.

7.0 SIMPLE R-C VOLTAGE CONTROL

EXAMPLE 1

This first example adds to Example 1 from APPLICATIONS NOTE 32, PWM LOW PASS FILTERING. The design critera:

SA01 operating on a 70 to 85V supply
$V_{RAMPp-p}$ = 5V
CMV limits = 2V and 8V
Reference output = 7.5V
Op amp Vos = 10mV
Switching frequency = 42KHz
Output = up to ±50V, from 10Hz to 2KHz
Input signal = ±10V

As the drive system has ±10V available, type V2 topology will be used to yield a simple, low part count circuit. Figure 8 shows the PowerDesign screen after entering SA01, selecting the topology, and the initial data entry. Use command button 100 to eliminate bias resistors and then enter known data in the column of yellow input cells. The first pass selection for R_{IN} was 5KΩ, yielding a ±2mA loading of the drive signal. Suggestions for pole frequencies were used and the Load Green Suggestion Values button was clicked.

The two feedback resistor suggestions are a convenient split totaling the value (appears in the upper right corner)

required to meet overall gain specified, with the 5KΩ input resistor. The 1/11 split means the loading effects of the larger resistor on the pole, created by the smaller resistor and the capacitor, will be at a minimum. After a standard value is entered for R_{F2}, the suggestion for R_{F1} is recalculated as the ideal total minus R_{F2}. The feedback pole frequency reported here, is calculated as though the larger resistor did not exist. It is perfectly acceptable to use both resistors equal to half the R_F total value given. The 1/ßeta plot, the peaking, and phase margin will still be correct. Now is the time for two preliminary checks.

First check the will be power ratings for the two feedback resistors. The resistor connected directly to the PWM outputs must be checked for AC power. With the associated pole frequency being substantially less than the F_{SW}, the impedance of the capacitor will be much less than that of the resistor. Assume a square wave of ±Vs/2 is applied to approximate the reported power for this resistor. The second resistor power rating is reported as a DC function, assuming the PWM output pin is being held at Vs. Notice that with a 5KΩ input resistor, there is nearly 3/4W in the smaller resistor. It was decided to change R_{IN} = 15KΩ, which will allow a 1/2W resistor to handle the job with some margin. New values for R_{F2} and R_{F1} will be 68.1KΩ and 6.9KΩ. The second check to be made is to see if the suggested capacitor values are in a convenient range. Increasing R_{IN} will decrease capacitor values.

After entering the new input resistor value and loading suggestions, we need to turn our attention to biasing and CMV. Refer to Figure 9A for the most important new numbers. With no bias resistors, we have problems on both ends of the CMV window. Lets attack the lower side by entering roughly the suggested value, 33K for the high side bias resistor. This suggestion is a DC calculation of the resistor required to pull the combination of R_F (assuming V_{OUT} = 0) and R_{IN} up to the lower CMV limit when connected to VREF. In Figure 9B, the lower CMV limit has been met but the upper is still too high. The second suggestion appears and is 33KΩ *ΔCMV / Δsj peak. To rephrase, the 19.1KΩ is the 33KΩ lowered by the amount that the $V_{SJ\ p\text{-}p}$ is still too high. When the 19.1KΩ is entered as in section C, the reported VSJ peaks are both too high. The 17KΩ suggestion for the lower bias resistor is a DC calculation of the resistor needed to pull down the combination of R_F (assumes $V_{OUT} = V_S$), $R_{BIAS\ HI}$ and R_{IN}, to the upper CMV limit. In section D, the 16.9KΩ has been entered, the summing junction voltages meet the CMV limits, and voltage offset gain is ~14.3. Use this gain to calculate Vos, NOT signal gain.

CMV low, V	2	Suggestions:			Rf2 watts	0.0875
R bias hi K	1E+12	34.375			sj +peak	14.167
R bias lo K	1E+12	16.21621622			sj -peak	9E-11

A

CMV low, V	2	Suggestions:			Rf2 watts	0.0875
R bias hi K	33	34.375	19.2706		sj +peak	12.335
R bias lo K	1E+12	16.73003802			sj -peak	2.0604

B

CMV low, V	2	Suggestions:			Rf2 watts	0.0875
R bias hi K	19.1	34.375	13.3835		sj +peak	11.53
R bias lo K	1E+12	17.12492528			sj -peak	2.9668

C

CMV low, V	2	Suggestions:			Rf2 watts	0.0875
R bias hi K	19.1	34.375	19.3668		sj +peak	7.9675
R bias lo K	16.9	-1861.9363			sj -peak	2.0502
Tntwk pole KHz	4				Vos gain	14.365

D

FIGURE 9. CHANGES DUE TO THE 15KΩ INPUT RESISTOR

The process varies with application, but basics of selecting bias resistors are:

The high bias resistor has the most affect on V_{SJ} -peak.

The low bias resistor has the most affect on V_{SJ} +peak.

Selection assumes PWM outputs reach 0 & V_S (a safety margin).

Selection is an iterative process.

A near perfect selection results in:

High bias actual = second suggestion (19KΩ here).

Low bias suggestion = a large number of either polarity.

Summing junction voltages close to specified limits.

Less than perfect selection results in increased Vos gain.

1/ßeta plot may change quite a bit at low frequencies.

With feedback resistor power levels and DC biasing out of the way, we can turn to stability. There are only two decisions to be made here, the T-network pole and the integrator pole frequencies. The T-network pole placement relative to F_{SW} determines what fraction of the square wave output is fed back to the integrator. A good place to be is 1/10 of F_{SW}, where coincidentally, the fraction is about 1/10. The second decision is picking a fraction of the T-network pole to assign to the integrator pole. The rule of thumb is 0.4. Smaller fractions tend to yield more stable circuits at the expense of system bandwidth. Capacitor values for the frequencies entered are suggested automatically. Initial results of entering 4.2KHz for the T-network and 2KHz for the integrator (this is our system requirement), are shown in Figure 10.

Ctn nF	5.4919		5.491888996	
Cf nF	36.075		36.07512043	
Phase margin	39.438			
Peaking, dB	2.0357		F @ peak Hz	3651.74

FIGURE 10. INITIAL STABILITY CHECK ON THE SHAKER TABLE DRIVE.

The job now is to find standard values, which will maintain or improve phase margin without reducing the integrator pole below 2KHz. Figure 11 shows our choices.

Ctn nF	4.7		5.491888996	
Cf nF	33		36.07512043	
Phase margin	39.935			
Peaking, dB	1.9317		F @ peak Hz	4216.97

FIGURE 11. FITTING THE CIRCUIT TO STANDARD VALUE COMPONENTS

Additional steps used to verify this design are shown in Figures 12-14 (next page) . The first two utilize the state average spice models with each analysis requiring only a few seconds simulation time. The AC sweep indicates the circuit is only 0.85dB down at 2KHz. The square wave test agrees with Power Design in saying we have adequate phase margin. This model could also show us that supply current is substantially less than the ~7A delivered to the load. Next is the pulse by pulse simulation which required 4 minutes simulation time on a 750MHz PC. This model could also provide vast quantities of switching waveform data. Last is the hardware square wave test. This is the only test verifying that the op amp is not getting into trouble with high frequency common mode voltage.

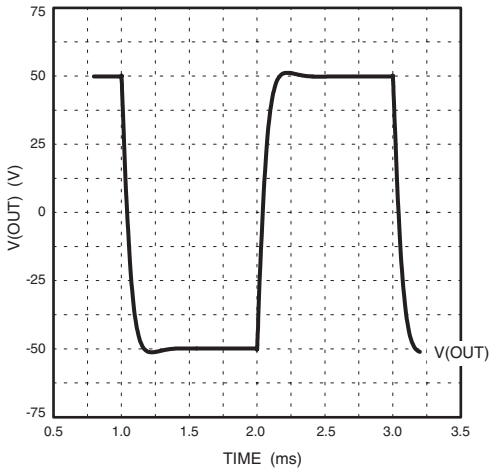


FIGURE 12. STAGE AVERAGE SPICE MODEL SQUARE WAVE TEST

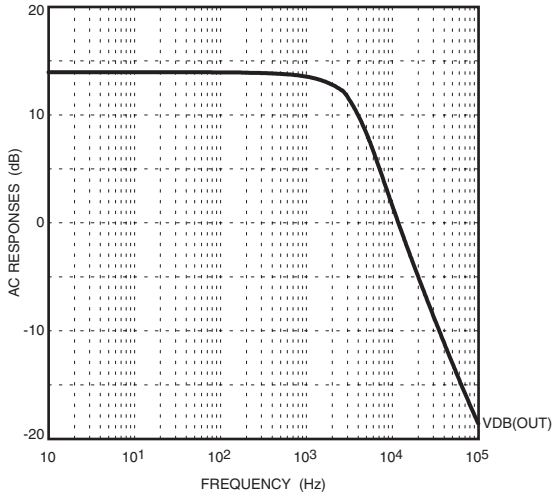


FIGURE 13. STATE AVERAGE SPICE MODEL AC SWEEP TEST

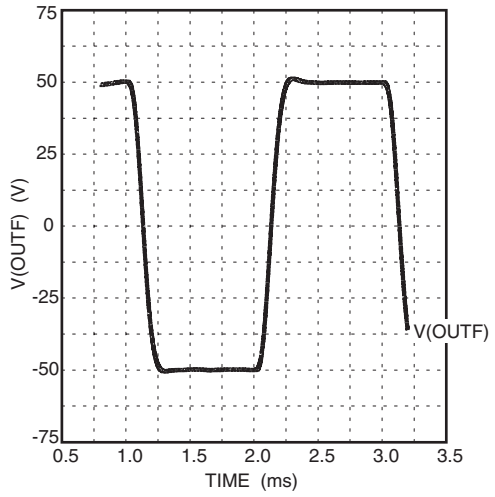


FIGURE 14. PULSE BY PULSE SPICE MODEL SQUARE WAVE TEST

EXAMPLE 2

Here's the given data for this example:
MSA260, half bridge mode operation
Vcc = 15V, Vs ranges from 156V to 178V
Switching frequency = 20KHz
Output = 10.2 to 53V, basically a DC amplifier
Load resistance = 3.7Ω at low output, 5.2Ω at high output
Makes use of the onboard error amplifier and voltage reference

This example is extracted from Power Design, PWM Examples sheet where details of product selection, filter and inductor design and heatsink selection are also covered. The topology of Figure 15 will be used in this example. While the filter and load are part of the system, the first order stability analysis is not affected by their values and you will enter only load resistance which is used to approximate internal voltage loss.

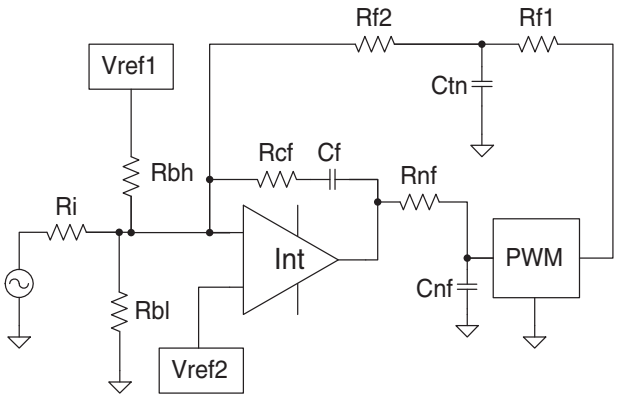


FIGURE 15. The simplest of all closed loop PWM systems is Type V3.

Type V3 is limited to half bridge operation and is easiest to understand with non-inverting PWM operation from the PWM input to the output (the percentage of time the output is high increases as the analog input increases). Alternately, the integrator can be used upside down (ground the -input and connect the passive component to the +input) with an inverting PWM function. Some applications may require Rbh, some Rbl, and some do not require either bias resistor.

Initial data entry into Power Design is shown in Figure 16. Here are some entries that may not be obvious:

1. Zload is the mid range of the load impedance.
2. Vref2 must be within the common mode range of the integrator (0 to 4V for the MSA260), usually positive, and a lower amplitude than Vref1.
3. Setting Ri to 5K just seemed a reasonable starting point.
4. The MSA260 provides a 5V reference.
5. The high bias resistor was left open because the suggested value was negative.
6. The suggested value for the low bias resistor was entered.
7. Pole frequencies were more conservative than the suggestions in the comments because we have virtually no bandwidth concerns.
8. The command button to Load Green Suggestions was used.
9. Rcf is normally only used in servo loops.
10. Rnf and Cnf put a noise filter pole at 15.9KHz, a good design practice.

While the values in Figure 16 would produce a working

circuit, please check the 4W rating for Rf1 on the right and the large Cf on the left. All component values in the lower half for Figure 16 are scaled to the specified value of Ri. Figure 17 shows all the rescaled values and operating parameters when Rin is increased to 20K.

Desired Values:		Operating points:		Initial operating:	
Zload	4.5	PWM gain	89	Rf total KW	21.4
Vout high, V	53	Vin ma p-p	2	Rf leg mA	6.7424
Vout low, V	10.2	Gain@1 pin	89	Vint p-p	0.4809
Vin high, V	0	DV @ 1pin	42.8	Overall gain	4.28
Vin low, V	10			I FDBK High	2.3598
Vref2 (for Vin)	2.5	Rcf KW	0	I In High	-0.5
Vs	178	Rnf KW	1	Delta Isj	1.8598
Ri KW	5	Cnf nF	10	Actual operating:	
Vref1 (for bias)	5			Eff PWM gain	85.486
				Rf leg mA	8.3178
		Suggestions:		Rf1 watts	4.0715
R bias hi KW	1E+12	-1.34422111		Rf2 watts	1.346
R bias lo KW	1.344	1.344221106		Vos gain	21.203
Tntwk pole KHz	1			Vint p-p	0.5007
Int pole KHz	0.3	0.4		O/A gain	4.28
Rf2 KW	19.455	19.45454545		Eff Rf	0.2503
Rf1 KW	1.9455	1.945454545		Rcf zero KHz	#DIV/0!
Ctn nF	81.809	81.80861561		NoisepoleKHz	15.915
Cf nF	2119.2	2119.229685		TntwkpoleKHz	1
Phase margin °	41.941			Int pole KHz	0.3
Peaking, dB	1.5211	F @ peak Hz	749.894	Vout hi, V	53.007
				Vout lo, V	10.207

FIGURE 16. Is this a complete design?

Desired Values:		Operating points:		Initial operating:	
Zload	4.5	PWM gain	89	Rf total KW	85.6
Vout high, V	53	Vin ma p-p	0.5	Rf leg mA	1.6856
Vout low, V	10.2	Gain@1 pin	89	Vint p-p	0.4809
Vin high, V	0	DV @ 1pin	42.8	Overall gain	4.28
Vin low, V	10			I FDBK High	0.59
Vref2 (for Vin)	2.5	Rcf KW	0	I In High	-0.125
Vs	178	Rnf KW	1	Delta Isj	0.465
Ri KW	20	Cnf nF	10	Actual operating:	
Vref1 (for bias)	5			Eff PWM gain	85.486
				Rf leg mA	2.0777
		Suggestions:		Rf1 watts	0.893
R bias hi KW	1E+12	-5.37688442		Rf2 watts	0.3315
R bias lo KW	5.36	5.376884422		Vos gain	21.267
Tntwk pole KHz	1			Vint p-p	0.5011
Int pole KHz	0.3	0.4		O/A gain	4.2835
Rf2 KW	76.8	77.81818182		Eff Rf	1.0022
Rf1 KW	8.87	8.8		Rcf zero KHz	#DIV/0!
Ctn nF	18	17.9430601		NoisepoleKHz	15.915
Cf nF	470	529.3745216		TntwkpoleKHz	0.9968
Phase margin °	41.242			Int pole KHz	0.3379
Peaking, dB	1.6625	F @ peak Hz	805.842	Vout hi, V	53.167
				Vout lo, V	10.332

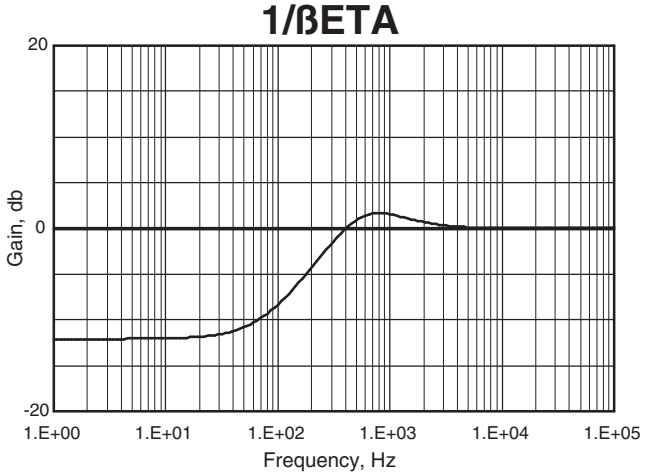


FIGURE 17. The final design values and operating parameters.

Power Design makes it easy to check component tolerances for both DC and dynamic performance, as shown in Figure 18. The top group indicates our choice of standard values places the output voltages within 167mV of nominal. In the second group, reference voltage divider accuracy is altered 1% (integrator voltage offset is also in series with the reference voltage) to find maximum error to be 0.7V. The next group pegs error at 0.45V for a 1% change in Ri. The next two groups show similar errors for variations of the bias resistor and the larger feedback resistor. As phase margin decreases when the two pole frequencies get closer

Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	53.1668
R bias lo KW	5.36	Vout lo, V	10.3318
Rf2 KW	76.8		
Vref2 (for Vin)	2.525		
Ri KW	20	Vout hi, V	53.6984
R bias lo KW	5.36	Vout lo, V	10.8634
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20.2	Vout hi, V	53.0607
R bias lo KW	5.36	Vout lo, V	10.6499
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	52.7682
R bias lo KW	5.414	Vout lo, V	9.93323
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	53.6222
R bias lo KW	5.36	Vout lo, V	10.4022
Rf2 KW	77.57		

Ctn nF	18	Ctn nF	18.18
Cf nF	470	Cf nF	423
Phase margin °	41.242	Phase margin °	40.488
Peaking, dB	1.6625	Peaking, dB	1.8171

FIGURE 18. Checking component tolerances.

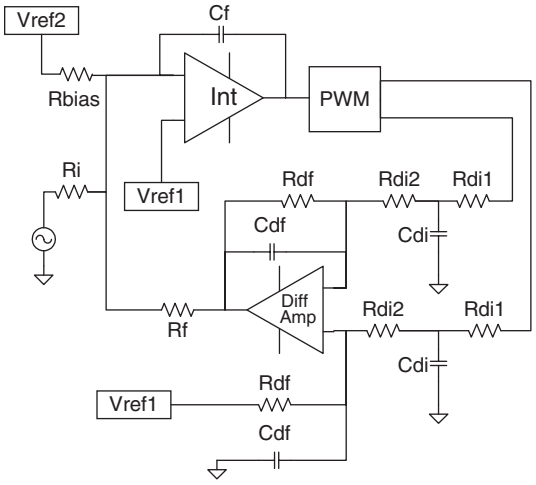


FIGURE 19. "ONE SIZE FITS ALL" VERSIONS OF CONTROLLING VOLTAGE WITH A DIFF AMP.

together, the last group shows that the worst 10% changes in capacitance have very little effect.

8.0 VOLTAGE CONTROL WITH A DIFFERENCE AMPLIFIER

Refer to Figure 19 (last page) for the general type V1 topology while various options are covered. The schematic shown here may contain more parts than you actually need because there are three options to cover.

Option 1: As drawn, this is a full-bridge PWM with the diff Amp. For half-bridge applications, the diff amp becomes a simple inverting op amp circuit with Vref1 tied to the non-inverting input.

Option 2: Op amp supplies may be single or dual. If dual supplies are used (usually only done when already available in the system), Vref1 becomes ground. This makes for a "clean" circuit where voltages out of the diff amp and into the integrator are proportional to and not level shifted from the actual output voltage. If a single supply is used, Vref1 as shown will allow the diff amp output to swing negative with respect to Vref1 (required to close the feedback loop).

Option 3: If the input signal needs shifting, Vref2 can be assigned a value higher than Vref1, or below ground, so that Rbias will provide the proper shift. Consider:

A. The half- bridge output never goes negative, but the input signal is bipolar with respect to Vref1. This would be the case with bipolar input signals (single or dual supplies, Vref1=ground or above) or when input signals range from 0 to a positive level and the op amps are on a single supply (Vref1 is above ground). If Vref2 is more positive than Vref1, Rbias is capable of providing the shift. See Figure 20 for the half-bridge version of this circuit

B. The full-bridge output swing is bipolar, but the input signal range is not spread equally above and below Vref1.

I. This could happen with bipolar input signals and single supply operation (Vref1 is above ground). If Vref2 is more positive than Vref1, Rbias is capable of providing the shift.

II. This could also occur when the input signal ranges from 0 to a positive value and the op amps are running on dual supplies (Vref1 = ground). If Vref2 is below ground, Rbias is capable of providing the shift.

C. With this general technique, even a voltage derived from a 4/20mA loop could be shifted to program a symmetric bipolar output or a unipolar output including zero. The idea is to compute input current for an input signal voltage where no current flows through R_F, and make current provided by RBIAS equal and opposite. For full bridges, this input voltage corresponds to 0V output. For half bridges, this input voltage corresponds to an output voltage equal to Vref1.

This circuit in Figure 20 could be implemented using dual supplies for the op amps, but additional circuitry must be added to prevent integrator output swing below ground. Such an event would be in violation of the Absolute Maximum Input Voltage range of the PWM amplifier. Even if this caused no damage, a swing below the lower ramp peak does not result in any further voltage change at the output. It merely puts a big non-linearity in the system.

9.0 WHAT'S DIFFERENT ABOUT CURRENT CONTROL?

It's already been mentioned that the filter and the load are inside the loop for a current control application, but here are a few more handy-to-know details. In applications where the load does most of the filtering, such as servos, the "filter" is often far from that described in Application Note 32. Instead, the filter only knocks off the sharp edges of the raw output, and the load mainly does the job of demodulating the signal from the carrier. The tricky part lies in the load that usually contains moving parts and the mechanical factors need to be equated to electrical parameters for a complete analysis of the system.

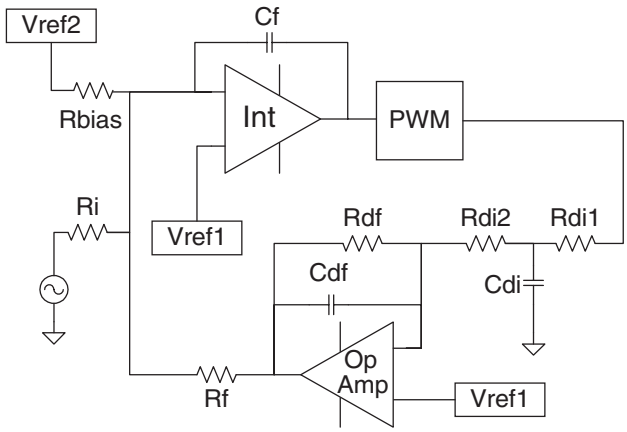


FIGURE 20. THE HALF-BRIDGE VERSION IS SIMPLER THAN THE FULL BRIDGE

Even when there is a filter in the more normal sense, it often diverges from textbook design when it comes to the matching network. The textbook filter includes this network if the load has any reactive elements because a flat pass band requires the load to appear resistive to the filter. One way to think of the network/load relationship is that any frequency change induced decrease of load current is accompanied by an equal increase of network current making the total impedance appear constant. A second way to view this situation is the amplifier output current is never equal to load current. Because monitoring amplifier output current is the easiest way to implement current control, the network impedance is often larger than ideal, the filter is not ideally terminated, and the output voltage at the load peaks near F_C. It would be a good idea to keep this voltage mode peaking down to no more than 10dB.

10.0 CURRENT CONTROL USING THE ISENSE PINS

EXAMPLE 3

This application provides current drive for a coil. Bandwidth of the circuit needs to be DC to 2.5KHz. Here's the rest of the given data for this example:

SA12 full bridge amplifier
Vcc = 15V
$V_{RAMPp\text{-}p}$ = 4V
Switching frequency = 200KHz
Input signal = 2.5 to 7.5V
Load impedance = 0.3mH, 9Ω
Load current = ±10.2Apk
System does not have a negative supply

For a quick way to find required voltage drive, use the Power Design, Power sheet. For this load to reach the required current at maximum frequency, it will need 103.5V peak swing. The answer explaining why a PWM was selected is also on this sheet; a perfect linear solution for this drive will need to

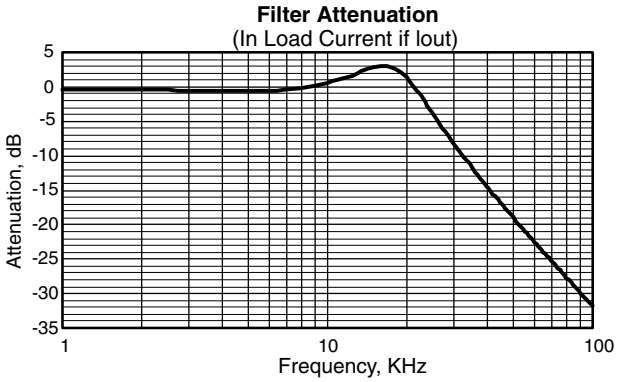


FIGURE 21. TESTING THE FILTER/LOAD FOR PEAKING IN THE VOLTAGE MODE

dissipate 312W and most real op amps weigh in at 350 or more watts. The next stop will be the PWM Filters sheet. F_C was set at 20KHz, second order component values were rounded off, except the resistive component of the matching network was doubled. In the PWM Power sheet, signal drive was set to voltage control for a peaking test. See Figure 21 for the results.

With all the preliminaries out of the way, (including selection of a 120V for the main supply), the next stop is the PWM Stability sheet. In the top left corner of this sheet, SA12 in entered and the Type I1 configuration is selected. Figure 22 (next page) shows the area where the filter, matching network and load can be entered manually or extracted from our previous work. For first pass analysis, leave the inductance of the load equal to zero. If you started with the PWM Filters sheet, this inductance will be the lower right cell.

Figure 23 illustrates more circuit set up. Given data is entered and the first circuit choice is a value for the input resistor. A range between 1 and 10KΩ usually avoids both excessive loading of the signal source and high impedance nodes that tend to either kill bandwidth, pick up noise or oscillate.

There are two logical choices for sense resistor values; the one that will develop the voltage required for activation of the SA12 current limit function (100mV) and the value to develop about 1V (a safe level which will not affect the switching action of the lower MOSFETs). From both the accuracy and bandwidth points of view, a higher voltage is better. Choices of value for R_{DF} cover a wide range and this choice will scale values for the input resistors and the roll off capacitors. Very low values can demand capacitors larger than practical and very high values can bring on problems with op amp offset current errors (bipolar input types) or can allow circuit parasitics too much influence on pole frequencies. A good goal would be make sure all capacitors used are at least 100pF. The recommendation of $F_{SW}/10$ was used for the diff amp pole placement and a slightly more conservative entry for the integrator pole was made. The diff amp will be LF353, running on the 15V required for the SA12 Vcc supply and the appropriate swing limitations were entered for Diff V high and low. Vref1 was set at half the op amp supply to allow the diff amp to swing symmetrically.

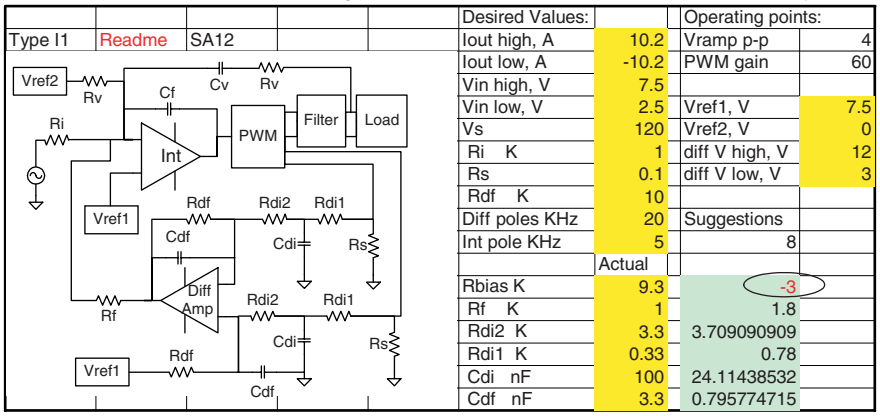


FIGURE 23. CIRCUIT SET UP FOR CURRENT CONTROL USING THE PWM ISENSE PINS.

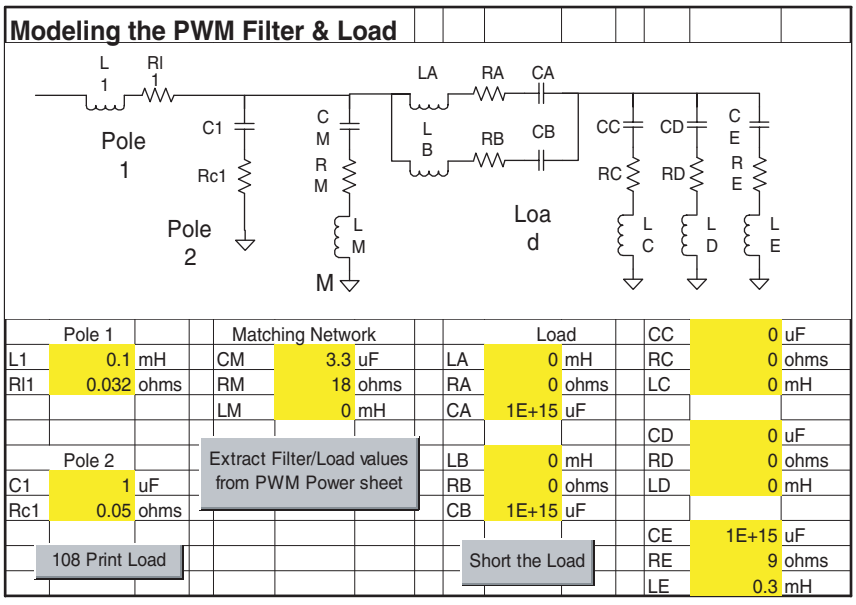


FIGURE 22. SETTING UP THE FILTER, MATCHING NETWORK AND LOAD FOR STABILITY

At this point, Vref2, the rest of the Actuals and the suggestions are all left over from the last circuit development. Even so, we have useful information in the suggestion for Rbias; it is negative and printed in red. This means the bias reference, Vref2 is the wrong polarity with respect to Vref1. The spreadsheet has followed the guidelines above for level shifting: find Vin (5V) for zero current out (no current in R_F); find input current at Vin=5V (Δ2.5V/1KΩ), and calculated the resistor needed to provide an equal but opposite current from Vref2 (Δ7.5V/-2.5mA). Entering an easily obtained 10V for Vref2, results in a new Rbias suggestion of 1KΩ.

The suggestion for R_F will place diff amp swing exactly at the limits specified above. Entering an Actual value higher than the suggestion will demand greater diff amp swing. The suggestion for Rdi2 will be 10/11 of the total required to meet diff gain for the overall transfer function. Entering a close standard value will recalculate the suggestion for Rdi1

making up the remainder of the total input resistance. This decade relationship between the two input resistors is not mandatory, but is clean in that Rdi2 will have very little effect on the pole of Rdi1 and Cdi. If you are happy with the high and low output values in the lower right of Figure 24, this completes setup of gain and biasing. If this is not the case, check for standard values of better tolerance resistors (0.1% instead of 1% or 5%), or consider adding adjustment networks for offset and gain. While thinking of DC error budgets, move up this column to find output current errors corresponding to the voltage offset of the integrator and diff amp op amps.

Stabilizing the circuit will be an iterative process. The first step is to set up the circuit for about 10dB peaking with NO inductive load. In Figure 24, note that Actuals have been entered for the first three capacitors using standard values similar to the suggestions. It is important that Cv and Rv

	Actual				
Rbias K	1	1		Int Vos, A/V	10.419
Rf K	1.8	1.8		Diff Vos, A/V	12.265
Rdi2 K	2.05	2.060606061		Iout p-p	20.385
Rdi1 K	0.215	0.216666667		O/A Xfer, A/V	4.077
Cdi nF	33	37.01277746		Eff Rf @.01Hz	0.6552
Cdf nF	1	0.795774715		Diff pole i KHz	22.432
Cf nF	47	48.58403031		Diff pole f KHz	15.915
Cv nF	999	1.28652E-05		Int pole KHz	5.1685
Rv K	1E+07	64.86209964		RvCvpoleKHz	2E-08
Phase margin °	18.379	7.826086957		Beta @.01Hz	0.5973
Peaking, dB	7.7364	F @ peak Hz	8659.64	Iout high, A	10.193
				Iout low, A	-10.19

FIGURE 24. CHECK THE DC ERROR BUDGET AND START STABILIZING THE CIRCUIT

have large values for this first phase. Note that our entries result in a little under 8dB peaking at about 8.7KHz. Peaking below 10dB will not endanger the final stability solution but will lower bandwidth. Higher values of peaking will make the final stability solution very elusive. Increasing the integrator capacitor, Cf will decrease peaking. Increasing the diff amp capacitors will increase peaking. Another way to put all this is that peaking will decrease as the ratio between integrator and diff amp pole frequencies widens. Beware: decreasing diff amp capacitors allows more high frequency energy to reach the op amp. When satisfied with this step, use the command button to Define the Filter/Load, and reinsert the correct value for load inductance. If your specific application has no load inductance, adjust Cf for a phase margin of at least 30° (more is better, if you can afford the bandwidth), and you are finished.

Figure 25 shows the results of re-entering the load inductance value; peaking is too high, phase margin is too low. Start with the higher suggestion given for Rv and zero in on a value range yielding 1 to 4dB peaking, and then enter the suggested value for Cv. The upper suggestion is designed to limit 1/ßeta to 10dB above the value calculated at 0.01Hz. The lower suggestion is designed to limit to 3dB. Figure 25 shows our final component selection and the 1/ßeta plot results. The circled area in both plots is the result of the voltage mode peaking in the filter/load because the matching network impedance was doubled from design value. Figure 21 shows this peaking in the load. See Figure 26 for square wave test results with both state average and macro models.

11.0 CURRENT CONTROL USING A SERIES LOAD SENSE

EXAMPLE 4

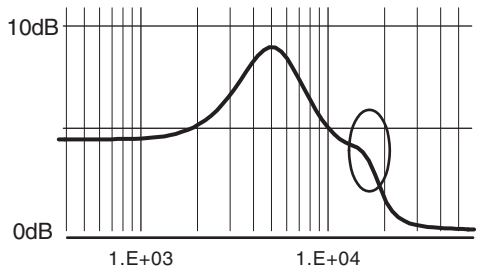
This application provides current drive for a motor. Bandwidth of the circuit needs to be DC to 100Hz. This circuit is part of a DSP based system controlling elevation and azimuth of an antenna. Here's the rest of the given data for this example:

SA01 operating on 48VDC.
$V_{RAMPp-p}$ = 5V
Switching frequency = 42KHz
Input signal = ±4.2V
Load impedance = 0.3mH, 1.5Ω
Load current = ±16.7Apk
Diff amp is INA117 running on ±15V
Op amp is LT1013 running on ±15V

To avoid significant phase shift in the filter, its design approach was very different from the normal design for a voltage output circuit. The objective is to knock off the square edges of the PWM waveform and reduce the peak to peak amplitude to roughly a third of the 48V supply. At F_C, motor impedance will be very high, leaving the matching network as the prime termination of the filter, and the prime factor in determination of ripple current. It was decided that 1.5Ap-p ripple current would be acceptable. With ripple voltage being roughly 16Vp-p, 10Ω would be a reasonable impedance for

Cv nF	999	2.2878E-05	
Rv K	1E+07	64.86209964	
Phase margin °	28.966	7.826086957	
Peaking, dB	4.4834	F @ peak Hz	4869.68

A



Cv nF	3.3	3.614914215	
Rv K	51	64.8622161	
Phase margin °	40.046	7.826086957	
Peaking, dB	1.9085	F @ peak Hz	6042.96

B

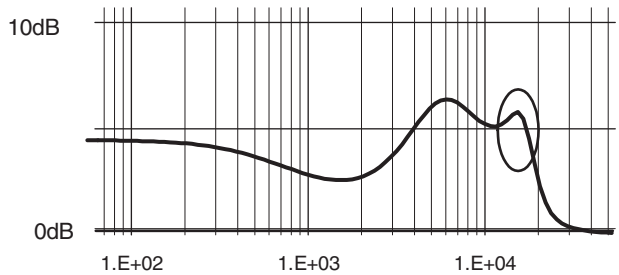


FIGURE 25. FINAL STEPS OF COMPONENT SELECTION FOR TYPE I1 CIRCUITS

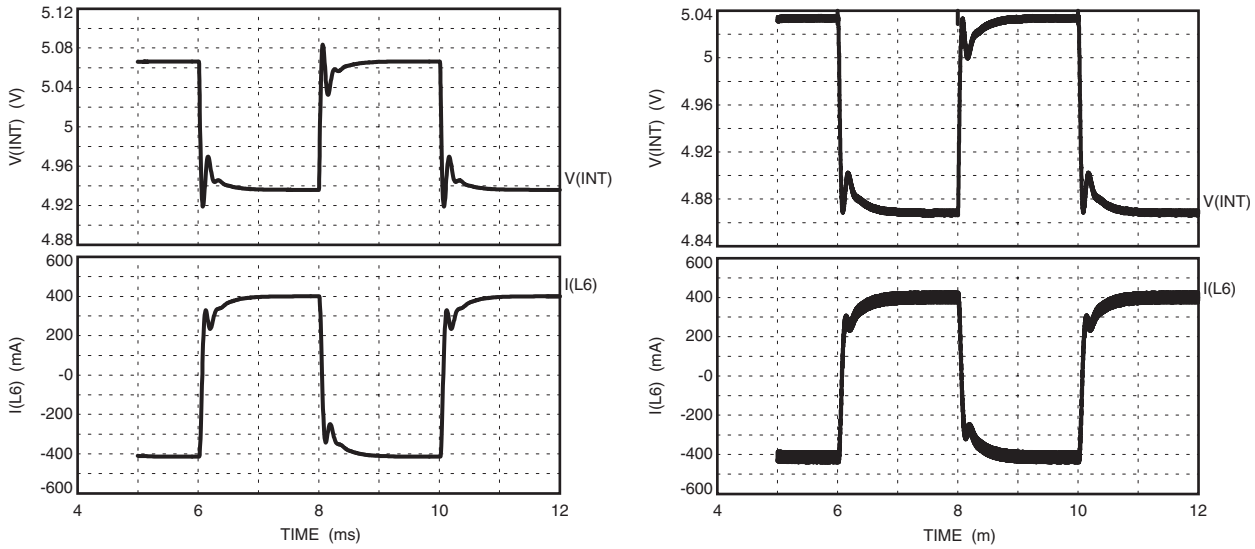


FIGURE 26. SQUARE WAVE TESTING EXAMPLE 3

the matching network. Examination of ideal attenuation graphs indicates a second order filter set at 1/2 F_{SW} should yield a -10dB response (about a third). Loading 21KHz, 10Ω and 300µH into the PWM Filters sheet yielded (adjusted to standard components) 47µH and 1µF to ground for each output, plus a matching network of 3.3µF and 10Ω. A check with the PWM Power sheet (voltage drive mode and the real 1.5Ω motor resistance) reveals -10.5dB at 42KHz and no peaking.

Refer to Figure 27 for data input in the PWM Stability sheet. Parasitic values for pole 1 and 2 elements were defaults calculated. Note that for the first pass stability calculations, the load inductance was set to zero. At the second pass this will be re-entered as 0.3mH. All the given data is entered below this and some circuit choices will be made. The input resistor choice was arbitrary. The sense resistor value was a trade off between voltage loss at high currents and accuracy errors caused by the voltage offset of the INA117.

Rbias K	10	1E+12	
Rf K	3.97	3.966274789	
Cdi nF	33	39.78873577	
Cfilt nF	100		
Copf nF	3.3	3.978873577	
Cf nF	27	25.01684876	
Cv nF	999	0.000673238	
Rv K	999999	125.9623149	
Phase margin ∞	19.101	14.16276477	
Peaking, dB	7.4752	F @ peak Hz	1654.8

LE	0.3	mH

Don't forget me!

Cv nF	22	19.10162495	
Rv K	47	125.9658199	
Phase margin ∞	32.422	14.16276477	
Peaking, dB	3.6139	F @ peak Hz	1240.9

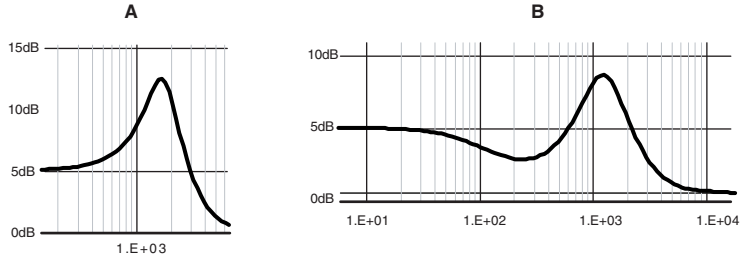
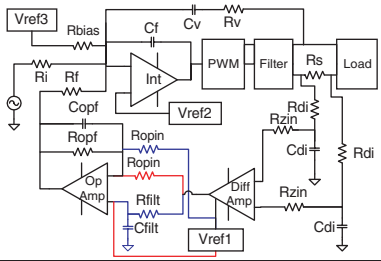


FIGURE 28. STABILIZING THE TYPE I2 CURRENT OUTPUT CIRCUIT

Pole 1		Matching Network		Load		CC	0 uF
L1	0.094 mH	CM	3.3 uF	LA	0 mH	RC	0 ohms
Rl1	0.0482 ohms	RM	10 ohms	RA	0 ohms	LC	0 mH
		LM	0 mH	CA	1E+15 uF		
Pole 2						CD	0 uF
C1	0.5 uF			LB	0 mH	RD	0 ohms
Rc1	0.1 ohms			RB	0 ohms	LD	0 mH
				CB	1E+15 uF		
						CE	1E+15 uF
						RE	1.5 ohms
						LE	0 mH

Type I2 Read me SA01



Desired Values:		Operating points:	
Iout high, A	16.7	Vramp p-p	5
Iout low, A	-16.7	PWM gain	19.2
Vin high, V	4.2	Vref1, V	0
Vin low, V	-4.2	Vref2, V	0
Vs	48	Vref3, V	0
Ri K	10	o/a gain: +/-	-
Rs	0.01	Ropin K	1
Diff amp gain	1	Ropf K	10
Rdi K	1	Rfilt K	10
Rzin K	400		
fdbk poles KHz	4	Suggestions	
Int pole KHz	1.6	1.6	
	Actual		
Rbias K	1E+12	1E+12	

FIGURE 27. SETTING UP EXAMPLE 4 FOR STABILITY ANALYSIS

The INA117 data sheet also indicates 1KΩ in series with its inputs will not seriously degrade performance, and this value will allow reasonable filter capacitor values in the few KHertz range. The 400KΩ input impedance was also extracted from this data sheet. Pole frequency for the feedback poles are set at 1/10 F_{SW} and the suggestion for the integrator pole frequency was used.

As no level shifting was required for this circuit, all references were set to zero. Again, arbitrarily, inverting gain for the op amp was entered. This could be changed to non-inverting as long as the two inputs to the diff amp were also reversed. The 1K/10KΩ gain setting for the op amp seemed convenient. The possibilities for specific component values have great latitude in several areas as long as related components are scaled in a similar fashion. When making specific choices, check effects of amplifier bias currents, voltage offset effects on current output, and keep impedances low enough such that a stray capacitance of 10pF will have negligible effect on the circuit.

The A side of Figure 28 (last page) shows suggestions, standard values entered and results for Step 1 where inductance has been removed from the load.

Note that a bias resistor of 10KΩ was entered. Rather than biasing, this resistor serves as an auxiliary input for offset adjust and a velocity loop input. As entered, this resistor has no effect on DC output but it does change the feedback factor, and consequently the stability solution. The 7.5dB peaking level is a little on the conservative side. The first choice for Rv in the second step (inductance re-entered) was 39Ω. After running the square wave test with a state average model, it was decided to change Rv to 47KΩ as shown in the B side.

By now, some of you have realized there are significant details missing in the presentation of this circuit. The integrator was set up for ±15V, the SA01 on-board op amp is normally used as the integrator, and it is single supply only and requires a reference voltage to avoid common mode voltage violation. Refer to Figure 29 to see the actual implementation. Here are some reasons for this approach:

1. The INA117 data sheet does not mention single supply operation.
2. Reference voltage for the INA117 needs to be zero impedance (requiring an op amp rather than a simple voltage divider).
3. Voltage offset of the SA01 op amp is 10mV; drift is not specified.
4. Driving an SA01 input pin directly with negative voltage violates Absolute Maximums.

With the INA117 on dual supplies and using ground as the reference voltage, items 1 and 2 above are no problem. By using the SA01 op amp as a level shifter, item 4 above is taken care of. As long as the level shift function has a gain of one, there will be no changes in AC performance. This also places the offset and drift of the SA01 op amp inside the loop of the actual LT1013 integrator with much better accuracy (item 3).

During circuit development, several variations of the filter and matching network system were evaluated. In addition to the 1/ßeta plot and square wave test, voltages at the input to the diff amp, on the wires leading to the motor and across the motor, were analyzed with an input of 0V. Refer to Figures 30 through 34 for the following points:

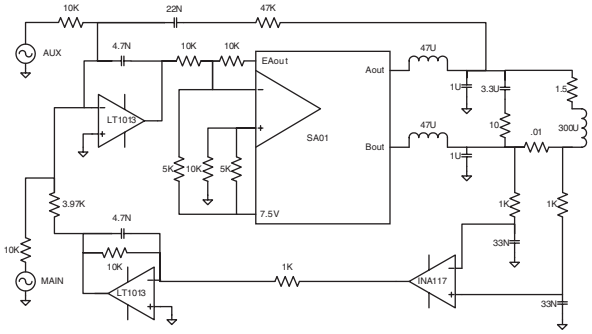


FIGURE 29. SOLVING SEVERAL CIRCUIT LIMITATIONS WITH UNUSUAL TOPOLOGY

1. The only option causing a significant change in the 1/ßeta plot or the square wave test is the use of large filter capacitors and no matching network. The reason for the dip below 0dB at 27KHz is very high voltage mode peaking as shown in Figure 34. We already knew this was something to avoid, but read on for other reasons to stick with the original design.

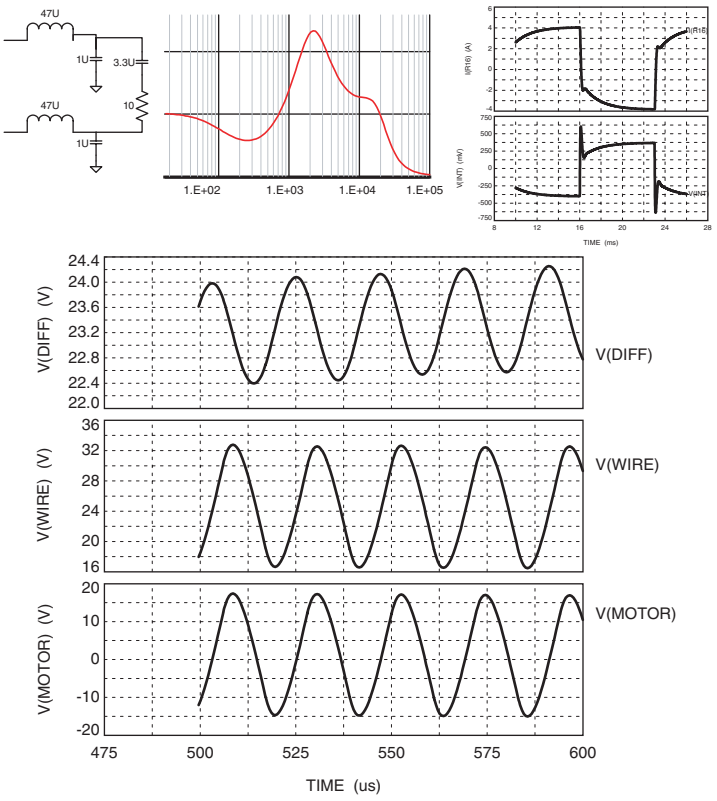


FIGURE 30. RESPONSE AND WAVEFORMS

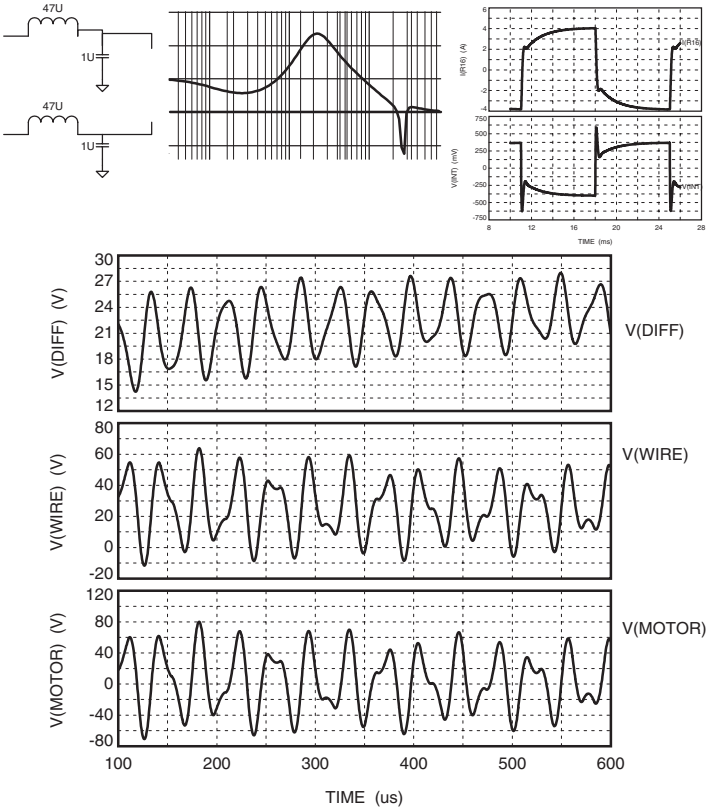


FIGURE 31. RESPONSE AND WAVEFORMS WITHOUT THE MATCHING NETWORK

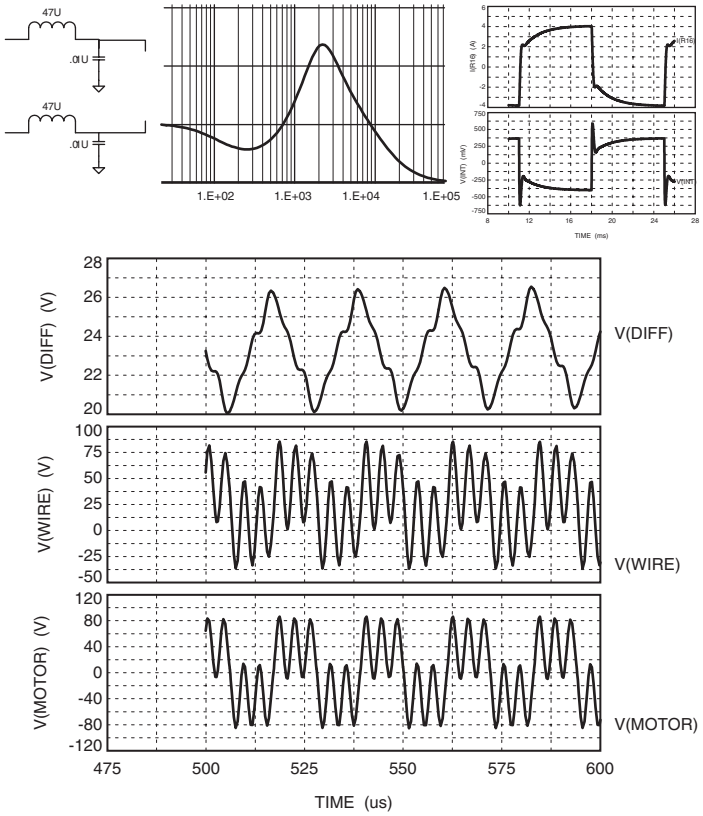


FIGURE 32. THE EFFECT OF SMALL CAPACITORS AND NO MATCHING NETWORK

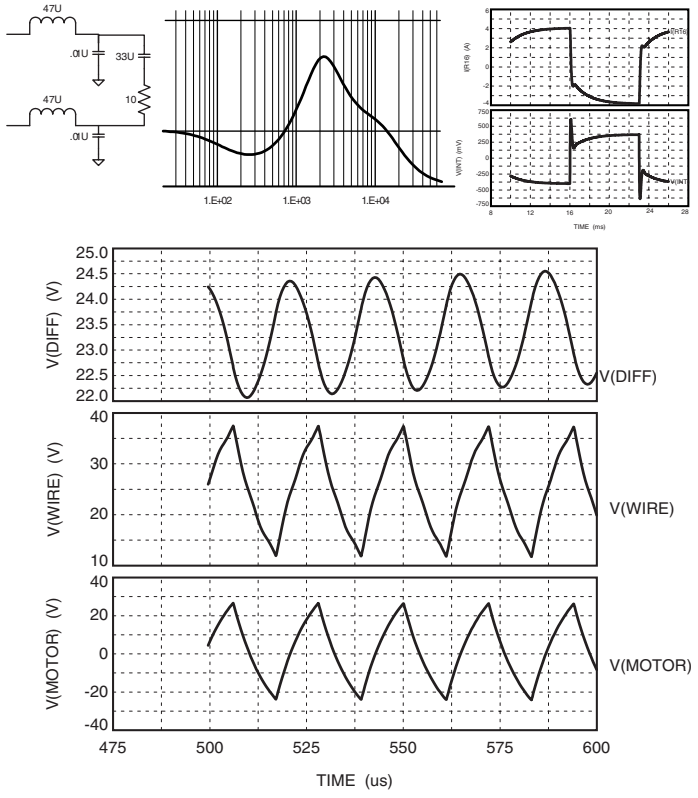


FIGURE 33. THE EFFECT OF SMALL CAPACITORS WITH THE MATCHING NETWORK

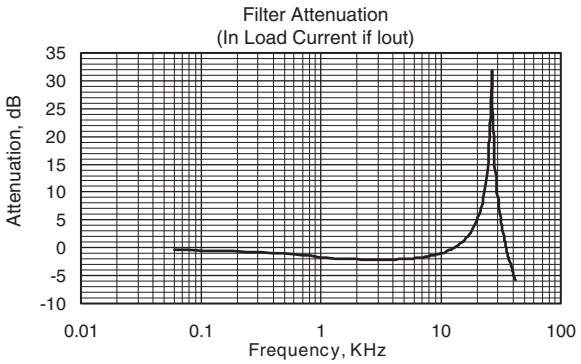


FIGURE 34. THE CAUSE OF THE FEEDBACK FACTOR DIP IN FIGURE 31

2. Omission of the matching network brings on high harmonic content in both the motor waveform and on the wires leading to the motor, plus it increases the peak-to-peak amplitude of these two waveforms about 2.5 times. Note the time scale difference on the motor waveforms in Figure 31. A major frequency seen here is around 25KHz as opposed to the 42KHz of the other figures. If peak voltage across the motor is 50V, ~0.75A will flow in the motor. This means power loss and heating will be above optimum.
3. Using an undersized filter capacitor with the matching network results in wire and motor waveforms with higher than optimum amplitude and worse yet, they contain considerable high frequency energy (read this as a radiation problem).

12.0 CONCLUSION

While the typical PWM application is more involved (read this as more work) than the typical power op amp application, the additional steps required are in line with the additional power the PWM can deliver to the load. Using the tools and procedures presented here will bring out the best from the very compact and cost effective PWM amplifier. These tools are available free at www.Cirrus.com.

13.0 ADDENDUM-THE OP AMP INTEGRATOR

Any one for a slow comparator? That's what we find in Figure 35, where the feedback capacitor slows down the transition time. During the transition, the op amp is likely operating in a linear closed loop fashion. The input signal sets a current in R_{IN} because of the virtual ground property of the inverting input. With no current in or out of the op amp input pins, the input current path is through the feedback capacitor to the op amp output. Voltage is developed across a given capacitor, governed by the time and magnitude of the input. Linear operation ceases when the output of the op amp cannot meet the current requirement. This happens when the op amp slew rate, current capability or most

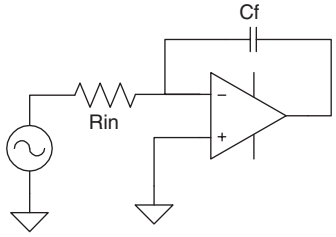


FIGURE 35. WHY WOULD ANYONE WANT A SLOW COMPARATOR?

often, voltage swing capability is exceeded. This is fine, the comparator has done its job of switching, with a controlled transition rate.

With a little modification, we can transform this switching circuit into a very useful linear tool. What is required is a form of feedback to maintain operation in the transition area, or the linear area. Figure 36 shows a generalized form of this idea where $f(x)$ is non-inverting. This function is often non-linear, but seldom contains step junctions. Confining our analysis to linear operation, there is no current in the op amp input pins. Looking at the summing junction with three connections, current in any given path must equal the sum of the other two paths. Therefore, capacitor current will be the algebraic sum of the input and feedback currents:

If I_{IN} and I_{FDBK} are equal and opposite, the output does not move.

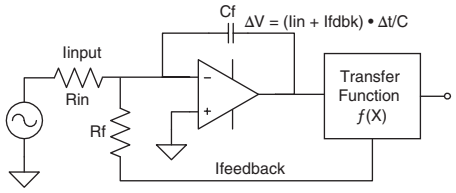


FIGURE 36. THE INTEGRATOR IN A SYSTEM

Notice that our rule on movement of the output does NOT predict absolute level, only direction and rate of movement. This can be a magical elixir for many $f(x)$ functions. Assume a simple $f(x)$ of $V_{OUT} = V_{IN}$ - 3V as shown in Figure 37. Apply +1V as an input signal and mentally apply power. Start the analysis with the op amp output at zero, the non-powered state. The battery provides a -3V feedback signal, meaning 2mA will flow through the capacitor, causing the op amp to slew positive. Positive slew will continue, though at a decreasing rate, until input and feedback currents to the summing junction are equal and opposite. This condition will be reached when the $f(x)$ output = -1V and the op amp output = +2V.

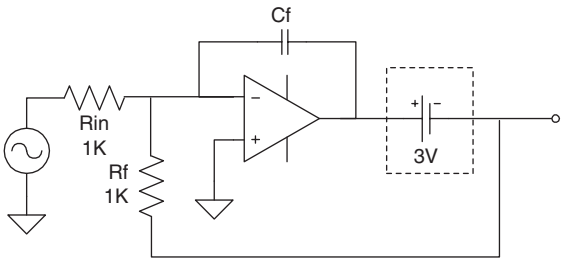


FIGURE 37. INCLUDING A SIMPLE TRANSFER FUNCTION

That was simple and may not qualify as magic, but we get closer if we replace the battery with threshold voltage of a power MOSFET (moves around part to part and over temperature) and add a resistor to sense output current (which we may have very little control over). As long as our modifications of $f(x)$ do not take the circuit out of the linear operating range, the op amp still views its job as driving its output where ever needed to make the sum of all currents into the summing junction = zero.

Refer now to Figure 38 and assume the op amp output saturation is 3V from the rails, and common mode voltage is limited to 3V from the rails. Op amp output range is further that the input signal = ±5V (10Vp-p), R_{IN} = 1K, and our 15V supply is reference quality. Two resistors with a 2:1 ratio will yield a convenient 5V reference for the op amp +IN, giving a good safety margin on common mode voltage. Next, set overall gain according to $V_{OUTp\text{-}p}$ /$V_{INp\text{-}p}$.

$$R_F = R_{IN} * 9Vp\text{-}p / 10Vp\text{-}p = 900\Omega$$

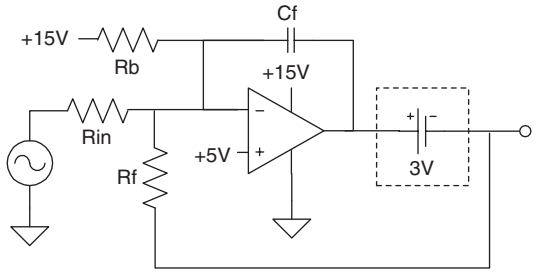


FIGURE 38. MOVING TO SINGLE SUPPLY OPERATION

Pick a convenient input voltage to compute the bias resistor needed to satisfy the requirement of zero net current to the summing junction. With the input signal = 5V, the circuit output will be zero (the overall transfer function = -0.9V/V). At this assumed point, current through R_{IN} = 0 and current through R_F = 5.556mA. We need 5.556mA bias from a reference of the opposite polarity of the feedback voltage with respect to the summing junction. This may seem a waste of words, but if $f(x)$ were +30V, the bias resistor would need to go to ground instead of the 15V reference.

$$R_{BIAS} = 10V / 5.556mA = 1.8K\Omega$$

If you care to check out operation at -5V input, current through R_{IN} = 10mA from a source negative with respect to the summing junction and current through R_{BIAS} = 5.556mA from a source positive with respect to the summing junction. For a net zero, current through R_F must be from a source positive (opposite that of the larger current) with respect to the summing junction and be equal to the difference of our first two currents. Start with the summing junction voltage and add I * R.

$$VOUT = 5V + (10mA - 5.556mA) * R_F = 9V$$

Basic operation of the circuit shown in side A of Figure 39 (next page) is identical to the common op amp four-resistor difference amplifier shown on the side B. Note that on the difference amplifier, the voltage difference between the output and Vref is always Vin (combined value) times the gain. Circuit A is doing the same thing, except the B output connection has been substituted for the reference input, meaning the voltage difference between the A output and B output is always Vin times the gain.

Next, assign circuit A input resistors of 1KΩ and feedback resistors of 10KΩ, providing an overall gain of 10, and a maximum supply voltage in the output stage of 50V. At 0V in, both outputs will be at 25V; at either input extreme, one output will move to 50V and the other will move to 0V. Assume the same op amp limitations and +15V supply as above. Starting with the non-inverting input, we know the pin needs to be pulled up at least 3V at all times; worst case is when the B output is 0V. The 1KΩ and the 10KΩ are effectively in parallel so we need enough current to pull 909Ω up to 3V or 3.3mA. With 12V across R_{BIAS}, its value should be 3.64KΩ. As this is a balanced circuit; the two bias resistors MUST be equal. A mismatch in these two resistors results in an offset.

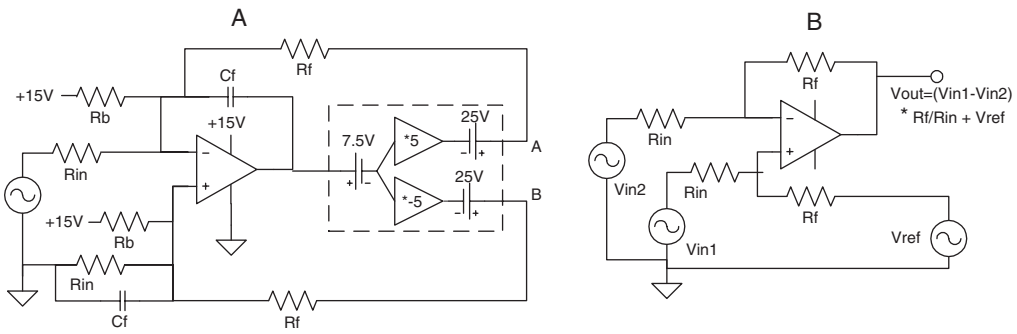


FIGURE 39. WHY WOULD ANYONE THINK UP THIS?

Our last step is to check common mode voltage when the B output is 50V.

Many of us could quickly find a node voltage fed with two sources, through two resistors, but would be slowed down considerably when three legs feed the node. Refer to Figure 40 for a simple way to solve this circuit question with iteration. Start with the two legs having fixed voltage; find an equivalent voltage and resistance doing the same job as the original pair. V_{EQ} will be the voltage present if you removed the 10KΩ resistor, or 3.23V. R_{EQ} will be the parallel value of 3.64KΩ and 1KΩ, or 785Ω. The equivalent circuit for the +input can now be quickly used for any value of B output. With the B output = 50V,

V+IN = 46.77V / 10.785KΩ * 785Ω + 3.23V = 6.7V

This solution finds common mode voltage very safe with respect to the 12V specification on the upper end.

Congratulations! You have set up an integrator to drive a rudimentary stage average model of an SA60 running on Vcc = 15V (7.5V battery) and Vs = 50V (the 25V batteries).

Biasing integrators for common mode voltage, or to level shift the input signal, is neither magic nor difficult. The overall transfer function must be known and linear operating limits must not be exceeded. The objective is then to reduce the sum of all currents to the summing junction to zero. When this is done, the charging rate of the capacitor is zero, and the op amp does not move. We have a stable operating point.

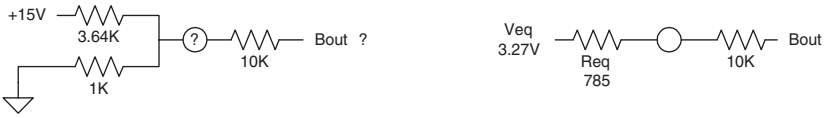


FIGURE 40. EQUIVALENT ELEMENTS HELP SOLVE FOR NODE VOLTAGE

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

Heatsinks, Mating Sockets, Washers, Vendors

RECOMMENDATIONS FOR THERMALLY CONDUCTIVE WASHERS

Apex Precision Power thermal washers are also available from Power Devices. "Thermstrate" is the material trade name for these washers unless the model specification states otherwise. These washers are pre-coated aluminum stampings which provide better thermal conductivity than thermal grease, easier use and freedom from application variables. Electrical conductivity of these washers makes sleeving of at least two opposing pins a requirement to achieve correct alignment. A small number of Apex Precision Power washers are noted to be electrically insulating or made of Kapton. These are made of "Isostrate" material, type MT Kapton with over twice the thermal conductivity of type HN Kapton. Thermal performance is similar to a mica washer with thermal grease. Both types are 3 mils thick and NON-COMPRESSIBLE.

HEATSINK THRU-HOLES

Custom heatsink manufacture or mounting of the Apex Precision Power power amplifier to a bulkhead for heatsinking, requires the use of individual heatsink thru-holes for the external connection pins. For the 8-pin TO-3 package the main path for heat flow occurs inside the circumference of 8 pins. (Refer to Figure 1)

Therefore, a single large hole, (to allow the 8 pins to pass through), will remove the critical heatsink material from where it is most needed. Instead, 8 separate holes must be drilled. Refer to Table 1 for recommended drill sizes for heatsink thru-holes for Apex Precision Power power amplifier packages.

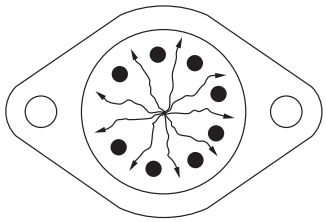


Fig. 1: Main heat flow path, 8-pin to TO-3 package.

PIN DIAMETER	RECOMMENDED DRILL SIZE	HOLE DIAMETER INCHES	HOLE DIAMETER mm
.025"	#50	.070±.002	1.781±.051
.040"	#46	.081±.002	2.057±.051
.060"	#37	.104±.002	2.642±.051

Table 1: Heatsink thru-hole sizes.

TEFLON TUBING

Anodized heatsinks can be easily nicked or scratched, exposing bare aluminum, which is an excellent electrical conductor. When mounting the Apex Precision Power power amplifier using a socket, it is recommended to sleeve, with Teflon tubing, a minimum of two opposite pins. This centers the external connection pins in the heatsink thru-holes and prevents electrical shorts when tightening the power amplifier down on a heatsink. When soldering directly to external connection pins it is recommended to sleeve, with Teflon tubing, all pins. Table 2 lists the recommended Teflon tubing and some suggested manufacturers (for manufacturers' phone numbers, see "Vendors for Power Op Amp Accessories").

TUBING DIMENSIONS						
PIN DIAMETER	Nominal I.D. Inches	Nominal I.D. mm	Nominal O.D. Inches	Nominal O.D. mm	MFG.	MFG. PART NO.
.025"	.028	.711	.052	1.321	★	TSI-S22
					★★	TFT-250-22
.040"	.042	1.067	.074	1.88	★	TSI-S18
					★★	TFT-250-18
.060"	.056	1.676	.098	2.489	★	TSI-S14
					★★	TFT-250-14

Table 2: Teflon tubing. ★ SPC Technology ★★ Alpha Wire Corp.

Teflon meets all known requirements but many other materials will work fine in some applications if three requirements are met. The tubing must fit the pin and the heatsink hole, it must be rated for the maximum voltage of the application and it must be rated for the temperature extremes of the application. Simply stripping the insulation from #14, #18 or #22 wire may be a viable tubing source.

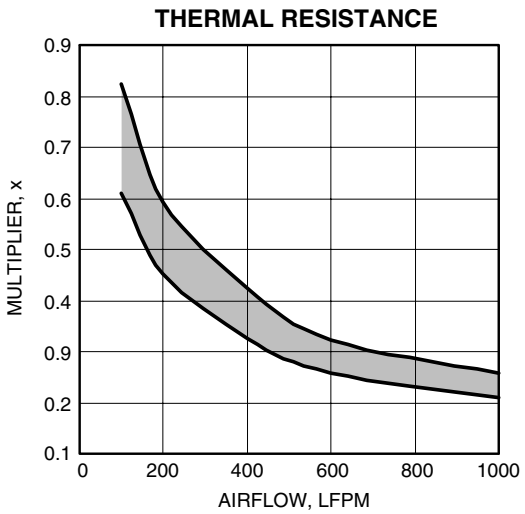
HEATSINKS

A wide spectrum of applications can be satisfied with the heatsinks stocked as accessories for Apex Precision Power power amplifiers. All are made of aluminum to provide high levels of conduction. HS01 clamps over the TO-3 case using virtually no additional space on a printed circuit board. Some are suitable for chassis or printed circuit mounting. Some are designed for chassis mounting only. The HS11 provides the most protection for prototyping or for production of high power products. All heatsinks are pre-drilled with hole patterns as shown. Conservative calculations are recommended for prototype work while performance graphs are included to enable optimization for production runs. Due to calculation complexity of thermal circuits and of power dissipation levels where reactive loads are driven, it is often helpful to utilize temperature measurements after the electrical design has been completed.

Heatsink ratings seen in the Apex Precision Power Application Notes are thermal resistance from ambient fluid (usually air) to the mounting area in the center of the hole pattern. Do not forget to add the thermal resistance of the interface between the heatsink and the amplifier (see model specific Application Notes). These ratings are for the heatsink with unobstructed air flow with optimum mounting orientation (extrusions would be suspended in mid-air with fins running vertically) and dissipating enough power to raise the heatsink mounting surface 75°C above ambient. While this convention seems to be common among heatsink manufacturers, making it easy to compare offerings, it often leaves the designer of an amplifier circuit with considerable work to do.

Let us first consider the 75°C rise above ambient condition. Apex Precision Power experience indicates this is a quite large number. Our research has found substantially different graphs for correcting thermal ratings for different temperature rises. A conservative approach is to increase thermal resistance 0. 8%/°C for lower temperature rise applications. A heatsink rated at 1°C but required to limit temperature rise to only 60°C would be expected to perform at about 1.12°C/W.

The conditions of optimum orientation and unobstructed air flow are also elusive in many power amplifier applications. Orientation and PC boards or cabinets obstructing air flow sometimes reduce thermal performance; fans sometimes enhance it. Calculating the improvement of adding a fan is not a single step job. When a graph is provided for a heatsink, the air flow is given in velocity, but most fans are rated in cubic delivery, and this rating varies with pressure. The Heatsinks sheet of the Apex Precision Power Power Design spreadsheet (Excel) will help with the cubic to velocity conversion. The degree of improvement in thermal performance achieved with forced air cooling varies with physical features of the heatsink. The following graph is a composite of known performance and can be used as an approximation of improvement possible with the addition of a fan when the specific heatsink does not have its own graph.



THERMAL INTERFACE

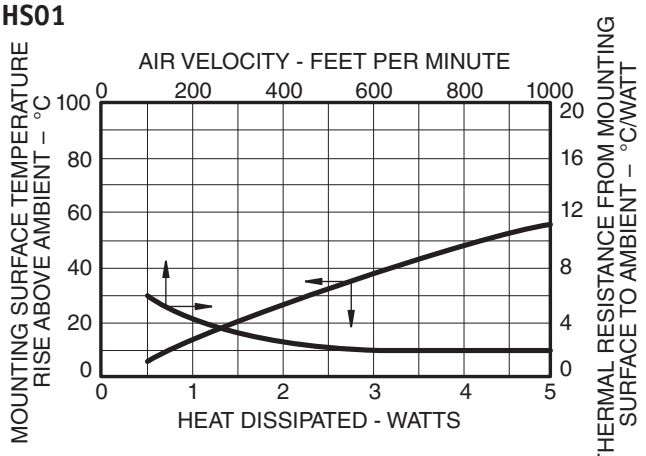
Both mounting surfaces of the heatsink and the amplifier are rough and non-flat to a degree where thermal performance will be compromised if a medium to fill voids is not included in between these surfaces. Silicone based thermal compound has a long track record of satisfactory performance when the fluid base and the filler have not been allowed to separate and are applied in a thin, even and complete layer. Apex Precision Power thermal washers also have a proven track record showing advantages of much lower process variability than manually applied thermal grease. When using aluminum based washers, installation must insure the washer does not touch the pins of the amplifier. See the TEFLON TUBING paragraph above.

DO NOT USE COMPRESSIBLE THERMAL WASHERS. The Apex Precision Power failure analysis team has seen many cases where compressible pads lead to cracked ceramic inside the amplifier when mounting screws are torqued down. Many Apex Precision Power data sheets proclaim the product warranty is void if these products are used.

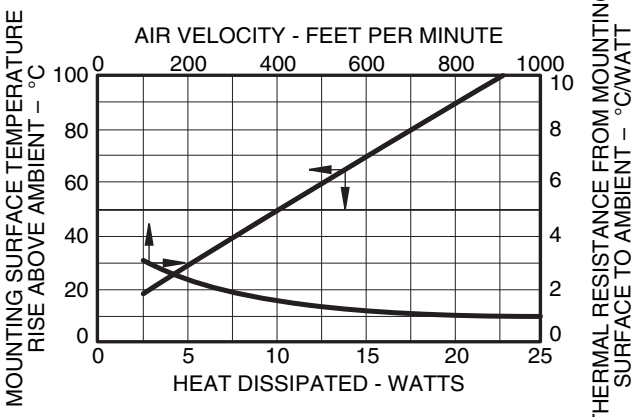
CAGE JACKS AND MATING SOCKETS

In addition to allowing amplifiers to be replaced without soldering (and potential PC board damage), cage jacks and mating sockets prevent solder joint stress when the amplifier/ heatsink assembly is rigidly fastened to the PC board and is subjected to wide temperature variations. Cage jacks are inserted and soldered into PC boards for each individual pin of an amplifier. The MS06 mating socket is used in the same manner as cage jacks. Other mating sockets can be inserted into PC boards, but also have turret terminals for direct wiring.

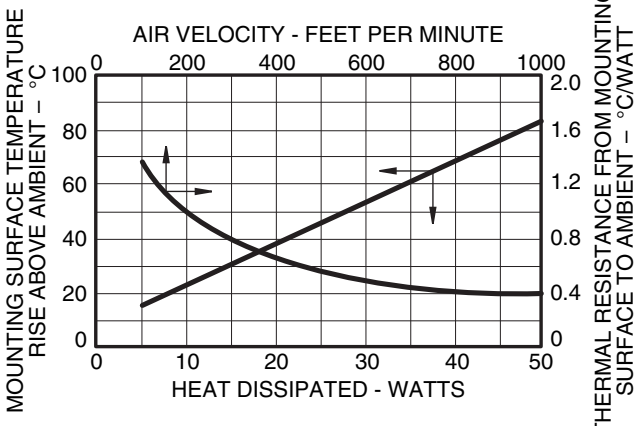
HS01



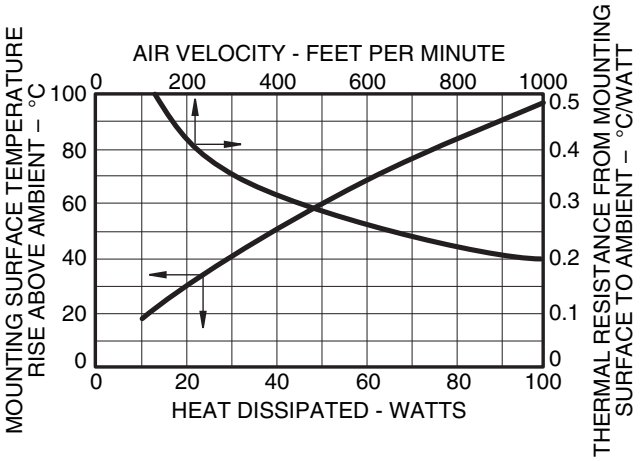
HS02



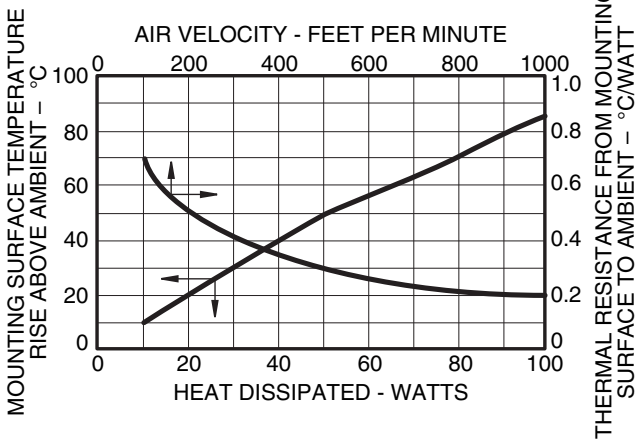
HS03



HS04

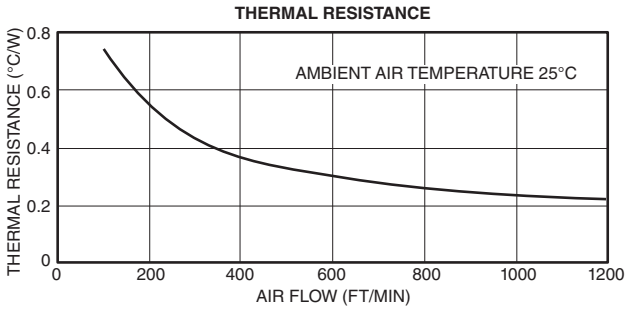


HS05

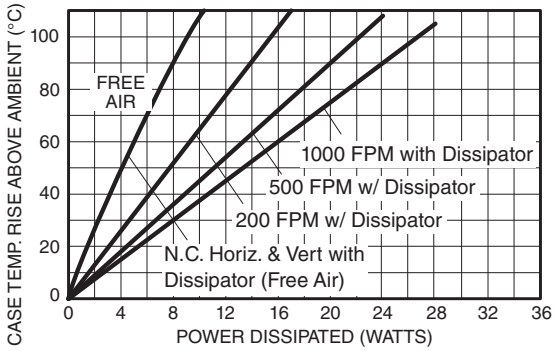


HS06

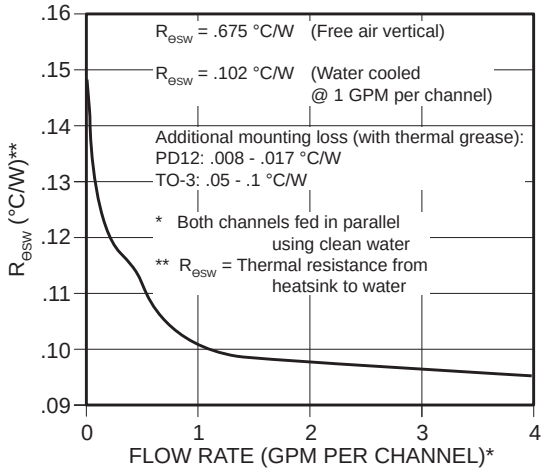
Thermal Resistance: ≈ .96°C/W



HS09

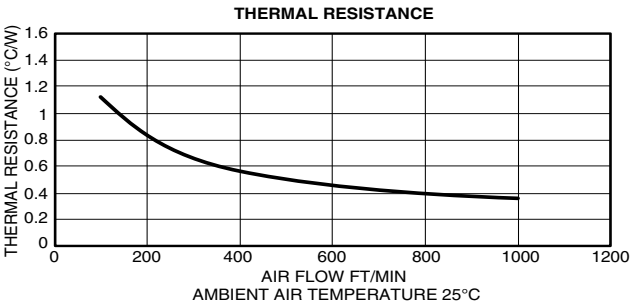


HS11



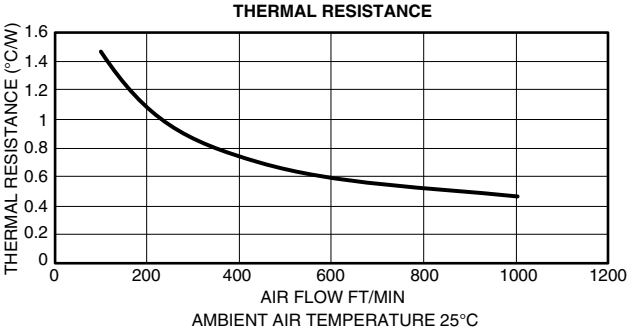
HS13

Thermal Resistance: 1.48°C/W



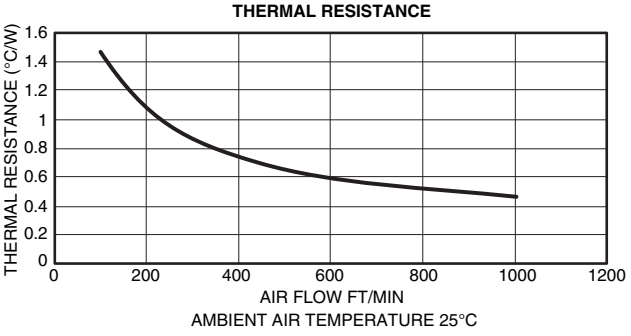
HS14

Thermal Resistance: 2°C/W



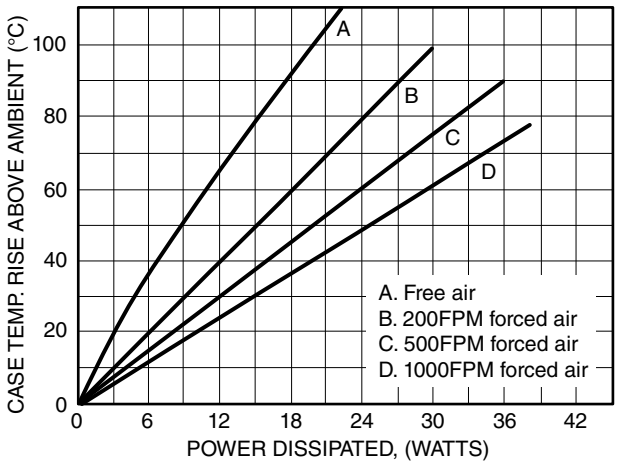
HS16

Thermal Resistance: 2°C/W



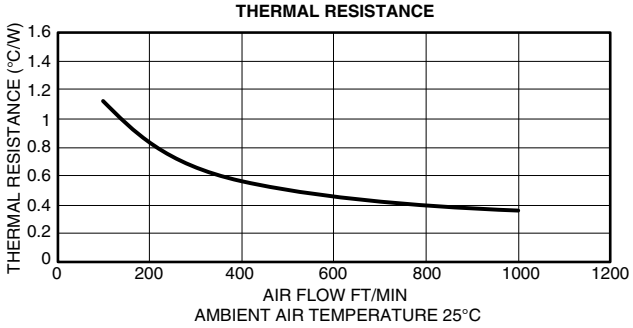
HS21

$R_{\theta SA}$ = 5.6°C/W



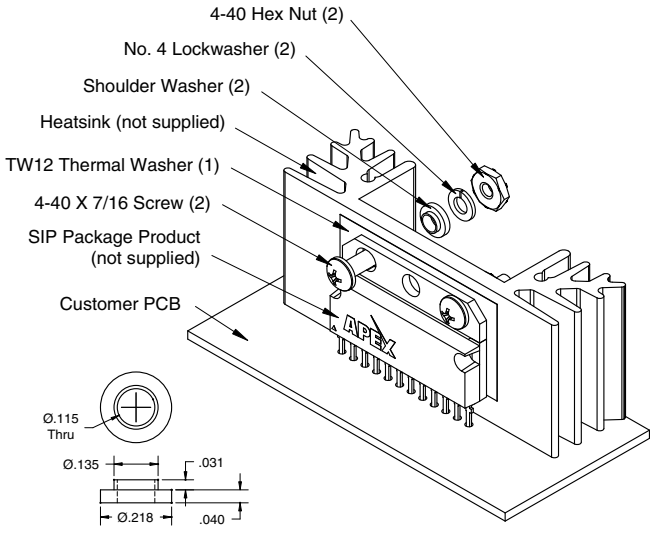
HS31

Thermal Resistance: 1.48°C/W



HK26/HARDWARE KIT

FOR DX (SIP12) PACKAGE



Shoulder Washer Dimensions

Keystone Part No. 3049
Nylon 6/6 per ASTM D4066

ACCESSORIES VENDORS FOR POWER AMPLIFIER

The following list answers the most common requests received on the Apex Precision Power Design Support Request. It is by no means a complete list of sources, but can save you valuable time locating requirements not found in the Apex Precision Power data book.

CAGE JACKS

Mill-Max Manfacturing Corp.
516-922-6000 Fax 516-922-9253
http://www.mill-max.com

CHIP CAPACITORS

NOVACAP
800-227-2447 Fax 661-295-5928
http://www.novacap.com

CORES

Magnetics
800-245-3984 Fax 412-696-0333
http://www.mag-inc.com

Micrometals, Inc.
714-970-9400, 800-356-5977 Fax 714-970-0400
http://www.micrometals.com

FAST DIODES

Intersil Corp.
888-468-3774 Fax 321-724-7000
http://www.intersil.com

MicroSemi
800-713-4113 Fax 949-756-0308
http://www.microsemi.com

Philips Components
800-447-1500
http://www.semiconductors.philips.com

Semtech
805-498-2111 Fax 805-498-3804
http://www.semtech.com

Vishay
610-407-4800 Fax 610-640-9081
http://www.vishay.com

HEATSINKS

AAVID Thermalloy Technologies, Inc
603-224-9988 Fax 603-223-1790
http://www.aavidthermalloy.com

Wakefield Engineering
603-635-2800 Fax 603-635-1900
http://www.wakefield.com

International Electronic Research Corp.
818-842-7277 Fax 818-848-8872

HIGH VOLTAGE SUPPLIES

International Power
805-981-1188 Fax 805-981-1184
http://www.internationalpower.com

Power-One Inc.
805-987-8741 Fax 805-388-0476
http://www.power-one.com

UltraVolt, Inc. DC/DC Converters
800-876-7693 Fax 631-471-4696
http://www.ultravolt.com

Emco High Voltage
209-223-3626 Fax 209-223-2779
http://www.emcohighvoltage.com

HIGH WATTAGE SUPPLIES

DYNA Power Corp.
248-471-1800
http://www.dynapower.com

Elgar Electornics Corp.
800-733-5427 Fax 858-458-0267
http://www.elgar.com

LOW VALUE RESISTORS

Caddock Electronics, Inc.
951-788-1700 Fax 951-369-1151
http://www.caddock.com

ISOTEK
800-569-6467 Fax 508-676-0855
http://www.isotekcorp.com

Vishay Dale Electronics
402-564-3131 Fax 402-563-6418
http://www.vishay.com

Riedon, Inc.
626-284-9901 Fax 626-282-1704
http://www.riedon.com

Vishay
610-407-4800 Fax 610-640-9081
http://www.vishay.com

RESISTANCE WIRE

MWS Wire Industries
818-991-8553 Fax 818-706-0911
http://www.mwswire.com

TEFLON TUBING

Alpha Wire Corp.
800-522-5742 Fax 908-925-6923
http://www.alphawire.com

THERMAL GREASE

AAVID Thermalloy Technologies, Inc
603-224-9988 Fax 603-223-1790
http://www.aavidthermalloy.com

VOLTAGE TRANSIENT SUPPRESSORS

MicroSemi Corp./Santa Ana Division
800-713-4113 Fax 949-756-0308
http://www.microsemi.com

Semtech Corp.
805-498-2111 Fax 805-498-3804
http://www.semtech.com

Vishay
610-407-4800 Fax 610-640-9081
http://www.vishay.com

NOTE:

Many of the above items can be purchased in small quantities through distributors such as:

Allied Electronics
800-433-5700
http://www.alliedelec.com

DigiKey Corporation
800-344-4539 Fax 218-681-3380
http://www.digikey.com

Mouser Electronics
800-346-6873 Fax 817-804-3899
http://www.mouser.com

Newark InOne
800-463-9275 Fax 773-907-5339
http://www.newark.com

Driving Piezoelectric Actuators

1.1 INTRODUCTION

The word *Piezoelectricity* is derived from the Greek and means 'electricity by pressure'. Piezoelectricity is a classical discipline dating back to the research of Jacques and Pierre Curie in the 1880s. The phenomenon, piezoelectricity, describes the interrelationship between mechanical strain upon a solid and its electrical behavior. One can create an electrical output by applying a force to the material sometimes called *the direct piezoelectric effect*, thereby transforming mechanical energy into electrical energy. Conversely, a distortion can be developed by applying an electric field, *the reverse electric effect*, which transforms electrical energy into mechanical energy. If the applied voltage is an alternating field, then it will cause the substance to vibrate, thereby generating mechanical waves at the same frequency as the applied field.

From this classical discipline an extraordinary number of applications have been developed, particularly, over the last 20 years. A list, by no means complete, appears in Table 1.

The piezoelectric phenomenon is relatively complex and the reader is referred to the book listed in the 'References' for a more rigorous treatment[1]. However, in this Application Note we shall confine ourselves to information relating to piezoelectric actuators and to the electronics that is essential to drive them.

1.2 PIEZOELECTRIC CRYSTALS

Piezoelectric actuators are fabricated from materials that exhibit the piezoelectric effect. These include a number of naturally-occurring crystals such as quartz, tourmaline and sodium potassium tartrate. In addition there are piezoelectric ceramics which include lead titanate and lead zirconate which are often identified as PZT. These materials exhibit certain advantages over single-crystal quartz including higher piezoelectric coefficients, ease of fabrication into components of any size and shape, mechanically hard and robust, as well as chemically inert. PZT devices are manufactured from their respective oxides and carbonates of Pb, Zr, Ti, rare earths, and alkaline metals.

Above what is known as the Curie Temperature (T_C) piezoelectric materials exhibit a simple cubic symmetry as shown in Figure 1a, and the unit cell contains a central cation, denoted by the black dot, which has no dipole moment — or in other words, the negative and positive charge sites coincide so there are no dipoles present in the material. However, below T_C, these lattice structures shift to a tetragonal symmetry, as illustrated in Figure 1b, in which the positive and negative charge sites are no longer coincident. This is denoted by the fact that the central cation is displaced from the center of the unit cell. These materials are now termed ferroelectric because their behavior is analogous to the behavior of ferromagnetic materials. As depicted in Figure 2a, the dipoles are randomly oriented in each of the various Weiss Domains (see glossary, pg. 13) in the material above T_C.

A ferroelectric material can be transformed into a piezoelectric material if it is subjected to a strong electric field at a temperature slightly below T_C along any chosen axis, as depicted in Figure 2b. This is called *Poling*. The influence of the field will also elongate the material along the poling axis.

When the field is removed, the dipoles remain locked in an approximate alignment, as shown in Figure 2c. It is this alignment of the dipole moments within the various Weiss Domains that enables the crystal to behave as a piezoelectric material.

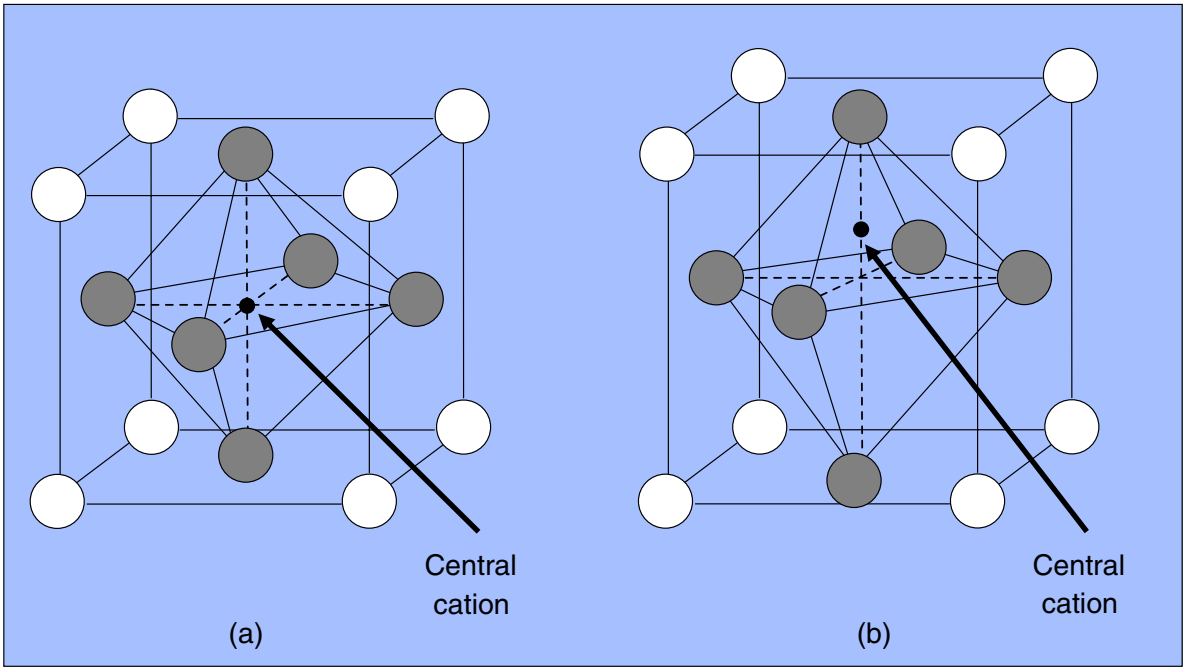


Figure 1. (a) A PZT elementary cell showing the cubic lattice above the Curie temperature; (b) The cell becomes a tetragonal lattice below the Curie temperature, after it has been poled. Note that the central cation has shifted upwards.

TABLE 1. PIEZOELECTRIC ACTUATORS — BENEFITS AND APPLICATIONS

Their benefits

- **No moving parts** – makes motion in the sub-nanometer range possible. Because there are no moving parts in contact, there is virtually no limit on resolution.
- **Fast response** - piezoelectric actuators respond in a matter of microseconds. Acceleration rates of more than 10,000 g can be realized.
- **High force generation** - capable of moving loads of several tons. Piezoelectric actuators can cover travel ranges of several 100 µm with resolutions in the sub-nanometer range.
- **No magnetic fields** - because the piezoelectric effect is related to electric fields, piezoelectric actuators produce no magnetic fields nor are they affected by them. Therefore such devices are especially well suited for applications where magnetic fields cannot be tolerated.
- **Low power consumption** - static operation, even holding heavy loads for long periods, consumes virtually no power. A piezoelectric actuator behaves very much like an electrical capacitor. When at rest, no heat is generated.
- **No wear** - no moving parts such as gears or bearings. The displacement is based upon solid-state dynamics and therefore exhibits no wear. Endurance tests have been conducted on piezoelectric actuators that have exhibited no measurable change in performance over several billion cycles.
- **Vacuum and clean room compatible** - piezoelectric actuators cause no wear nor require lubricants.
- **Operates at cryogenic temperatures** - the piezoelectric effect continues to operate even at temperatures approaching zero degrees Kelvin.

Their applications

Data Storage
- Magnetic recording head testing
- Spin stands
- Disk testing
- Active vibration cancellation
- Pole-tip recession test

Semiconductors, Microelectronics
- Nano & Microlithography
- Ultrasonic soldering
- Wafer and mask positioning
- Ultrasonic wirebonders
- Inspection systems
- Active vibration cancellation

Precision Mechanics
- Fast tool servos
- Ultrasonic drilling
- Active vibration cancellation
- Structural deformation
- Tool adjustment
- Wear compensation
- Needle-valve actuation
- Micropumps
- Linear drives
- Knife-edge control in extrusion tools
- Micro-engraving systems

Medical and Dental Technologies
- Brain scanners
- Ultrasonic cataract removal
- Ultrasonic scalpels
- Plaque scalers
- Lithotripters
- Cell penetration
- Microdispensers

Optics, Photonics
- Scanning mirrors
- Image stabilization, pixel multiplication
- Scanning microscopy
- Auto-focus systems
- Fiber-optic alignment
- Fiber-optic switching
- Adaptive and active optics
- Laser tuning
- Vibration stimulation

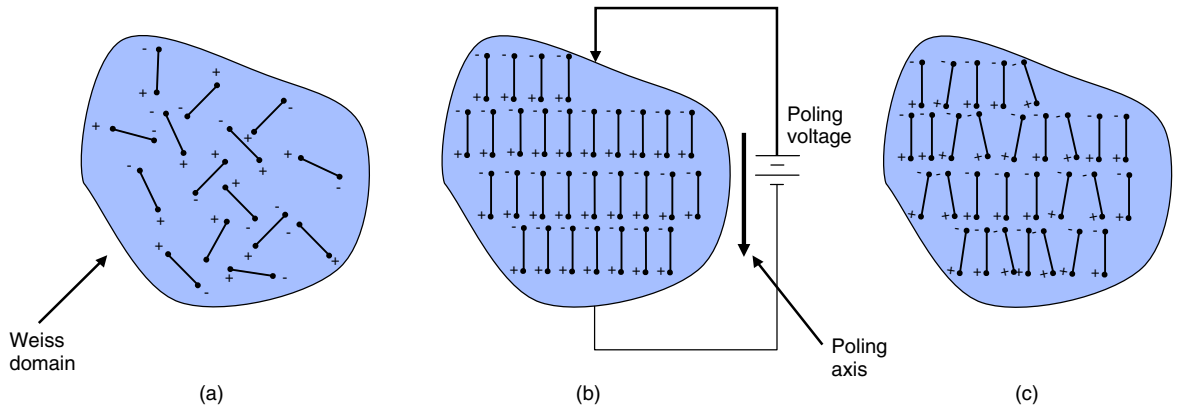


Figure 2. How the electric dipole moments align before polarization (a), during polarization (b) and after polarization (c).

1.3 PIEZOELECTRICS ACTUATORS — SOME BASICS

Within the cylindrical piezoelectric actuator illustrated in Figure 3a, when a voltage is applied longitudinally, a deformation occurs along the axis of the device causing a displacement ΔL, as depicted in the illustration. Typically a piezoelectric material can withstand a strain, or change in length, of 0.1%. This means that an actuator that is 100-millimeters long that is poled (energized) along its axis can be expanded by 0.1 mm.

The displacement, or change in length of an unloaded single-layer piezoelectric actuator can be closely approximated by:

$$\Delta L = SL_O \approx Ed_{33}L_O \quad (1)$$

Where:

ΔL = the change in length (meters)
S = strain-per-unit length or relative length change (meters/meter, and therefore, dimensionless)
E = the electric field strength (volts/meter)
L_O = the length of the actuator (meters)
d_{33} = piezoelectric coefficient (meters-per-volt) where the first subscript identities the axis of the field and the second subscript identifies the axis of the displacement.

The maximum electric field that most ceramic piezoelectric actuators can withstand is on the order of 1 to 2 kV/millimeter. To extend the travel beyond the approximately 0.1% maximum of a single slice and to avoid applying too large an applied field, a multilayer piezoelectric actuator can be fabricated by gluing thin layers of the piezo material together to form a stack. A voltage is then applied to each layer individually, as depicted in Figure 3b, so that each is powered, independently.

Now the applied voltage applied to each slice is still the same, but the total displacement is simply the sum of the individual displacements, or:

$$\Delta L_{TOT} = N\Delta L \quad (2)$$

1.4 DRIVING AT FREQUENCIES BELOW RESONANCE

When a piezoelectric actuator is driven by an AC voltage, the equivalent circuit is quite complex[2]. However, when a piezoelectric actuator is driven by a periodic voltage source with a frequency below the resonant frequency of the piezoelectric actuator, which is often the case in inkjet applications, then the device can be modeled by a single capacitor. In this case the impedance presented to the driving source is, to a close approximation, simply:

$$Z_{LOAD} = \frac{1}{2\pi f C_{PA}} \quad (3)$$

Where: f = the frequency of the driving source
C_{PA} = the equivalent capacitance of the piezoelectric actuator

2.1 GUIDELINES FOR DESIGNING DRIVER CIRCUITS

Some essentials to keep in mind when designing systems that employ piezoelectric actuators are these:

- Limited strength in tension - The tensile strength of a cylindrical piezoelectric actuator is approximately 10% of its strength in compression. It is essential to abide by these values to avoid fracturing the piezoelectric actuator. Specific values can be obtained from data sheets supplied by piezoelectric actuator manufacturers.
- Boundaries on acceleration - When driven by a periodic waveform the acceleration will increase exponentially with frequency. So it is important to identify the upper limit of the device's ability to withstand high acceleration forces. In particular, multilayer piezoelectric actuators are vulnerable to delamination should their acceleration limits be exceeded.
- Driver circuits do consume power - Piezoelectric actuators consume virtually no power when static, other than the quiescent power consumed by the electronics. However, the power dissipation demands upon the operational power amplifier circuits when the actuator is driven are significant, indeed.
- Follow sound principles in designing the driving circuits – Make sure the driving power operational amplifiers are operating in their safe operating region and current limiting is provided to protect the circuitry from an inadvertent short circuit. Other essential design tasks include selecting a satisfactory heatsink, flyback diodes and compensation capacitors. Many of these issues are covered in the discussion of the sample circuits described in the following sections.

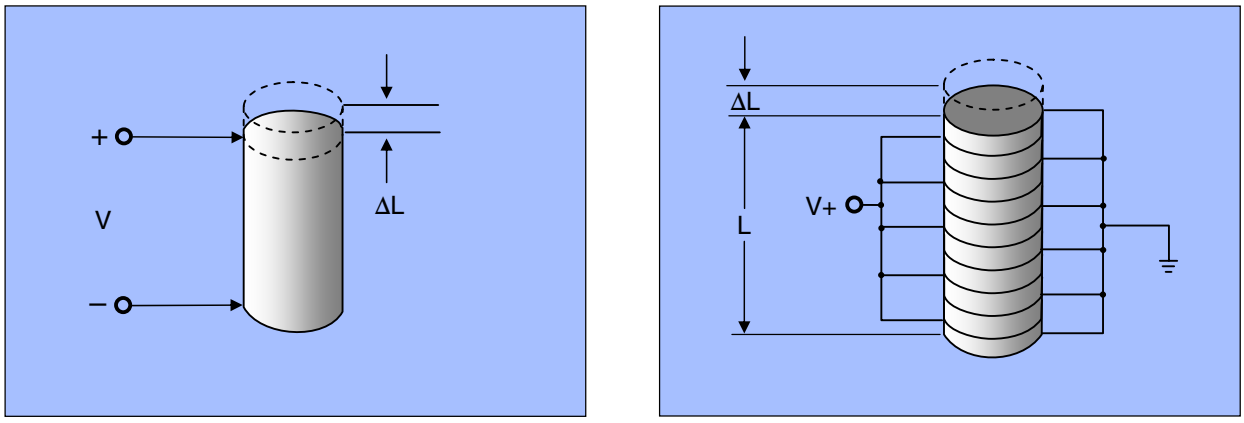


Figure 3. Two Linear Piezoelectric Actuators — A single stack in (a) and a multilayer (b) in which the displacement is amplified by the number of slices.

2.2 A BRIDGE-CONNECTED DRIVER CIRCUIT

The circuit that appears in Figure 4 was developed to drive a piezoelectric actuator that requires 300 Vp-p at 80 kHz. However, it will function at any frequency down to and including DC. The sinusoidal source applies 15 Vp-p at 80 kHz to drive the amplifier pair which, in turn, drives the piezoelectric actuator. In this case the actuator can be represented by a 1-nanofarad capacitance in series with a 1-Ohm resistance, as depicted in the figure.

Two PA78 power operational amplifiers are configured in this bridge circuit[3]. In this configuration the amplifiers provide an output voltage swing that is twice that of a single power operational amp. This configuration also doubles the slew rate of a single device. Any nonlinearities become symmetrical, thereby reducing second-harmonic distortion when compared with a single-ended amplifier circuit.

A Floating Load - In this application, the load is floating, which is to say it is not ground-connected at all. When the left output V_{OUTA} swings from 10 to 160V (Figure 5a) and the right output V_{OUTB} descends from 160V to 10V (Figure 5b), a voltage swing of 300V (-150V to +150V) develops across the load, as depicted in Figure 5c.

The outputs of the two amplifiers are now out of phase. The overall gain of the bridge-configured PA78s is +20 so that 300 Vp-p is delivered to the piezoelectric actuator, as required. The feedback circuit comprising resistors R3 and R4 center the outputs of both of the PA78 amplifiers at about 85V. As shown in Figure 4, a dual-source, asymmetric power supply delivers +175V and -5V to the two amplifier modules[4].

Establishing the $+V_S$ and $-V_S$ headroom - The values of $+V_S$ and $-V_S$ must be chosen so there will be sufficient headroom during the positive and negative excursions of both V_{OUTA} and V_{OUTB}. Though the output ($V_{OUTA} - V_{OUTB}$) shown in Figure 5c, will swing from +150V to -150V, it is actually the Common Mode Input Range (CMR) positive and negative values of the amplifier and specified in the PA78 data sheet that will play a significant role in governing the values of $+V_S$ and $-V_S$ employed in this asymmetrical sourcing arrangement.

In the case of the PA78, the specified value of the CMR negative is $-V_S + 3V$. This means the input should approach the negative rail no closer than 3V. So by choosing $-V_S$ equal to -5V, both V_{OUTA} and V_{OUTB}, will exhibit negative excursions of 10V and will thereby approach the negative rail no closer than 15V.

The CMR positive is $+V_S$ - 2V. This means the most positive-going excursion of both V_{OUTA} and V_{OUTB} must stay at least 2V below $+V_S$. A second issue with regard to the $+V_S$ rail is the voltage drop at the output when the amplifiers are delivering peak current — and in this application the peak current is approximately 75mA. There is a graph in the PA78 data sheet called "Output Voltage Swing" which discloses that the drive current is 75mA, the loss will be approximately 8 volts. The sum of the two, 2V and 8V, is 10V, which means that the $+V_S$ must be at least 10V above the maximum voltage swing of 150V. By choosing a $+V_S$ of 175V an additional headroom margin of 15V is established.

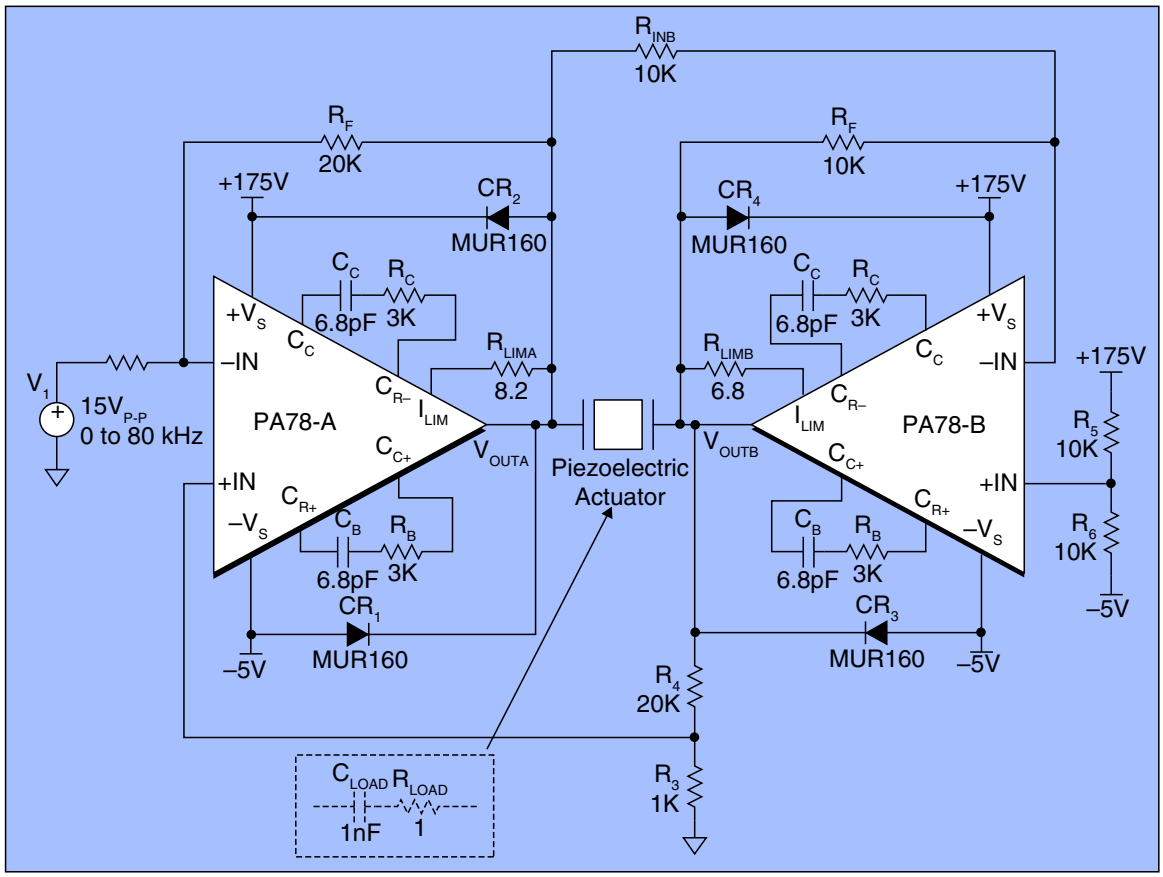


Figure 4. Bridge Connected – A pair of PA78s drive the piezoelectric actuator and are powered by asymmetric power supplies at +175V and -5V.

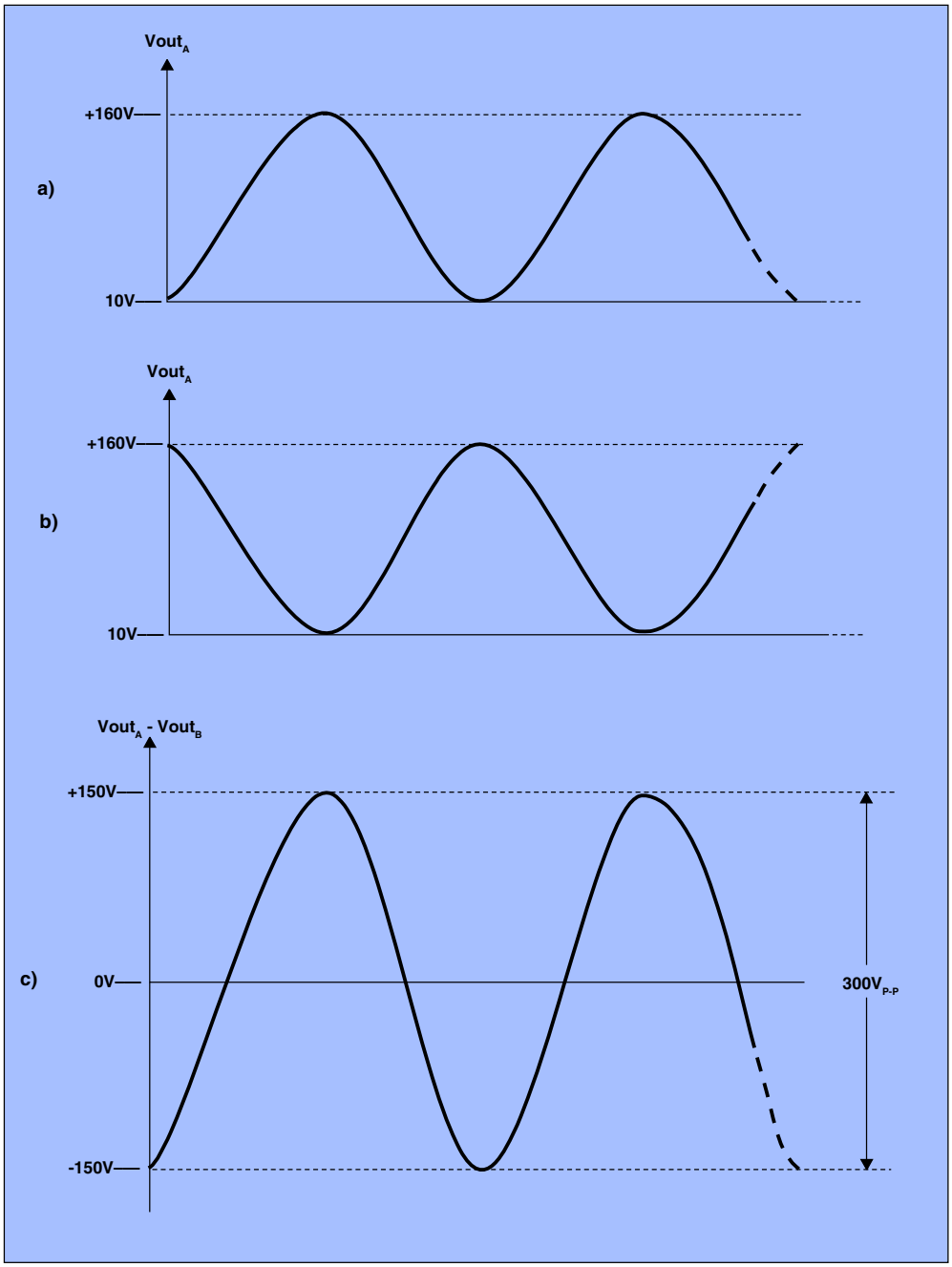


Figure 5. Output Waveforms – a) Left module output; b) Right module output; C) Waveform appearing across the piezoelectric actuator.

In any piezoelectric actuator circuit it is essential to prevent signals from inadvertently feeding back to the amplifier. A piezoelectric transducer can just as easily convert mechanical into electrical energy and vice-versa. So if something were to inadvertently bump the transducer, it could create a lot of energy that would travel backwards into the output of the amplifier. This could be destructive. However, by simply connecting several ultra-fast, MUR160 diodes (CR_1 – CR_4) from the output of each amplifier to its corresponding power supply rails, as shown in Figure 4, each amplifier is protected.

Computing the maximum dissipated power per module - The load impedance of the piezoelectric cartridge is given by the expression:

$$R + \frac{1}{j\omega C} = 1 + \frac{1}{j2\pi(80x10^{3})(1x10^{-9})} \qquad (4)$$

$$= 1 - j1989 \approx -j1989 \text{ Ohms}$$

To compute the maximum power per module we can devise the equivalent circuit shown in Figure 6. This is done by splitting Figure 4 into two parts with each part comprising a 2-nF capacitor and a 0.5-Ohm resistor, while assuming a

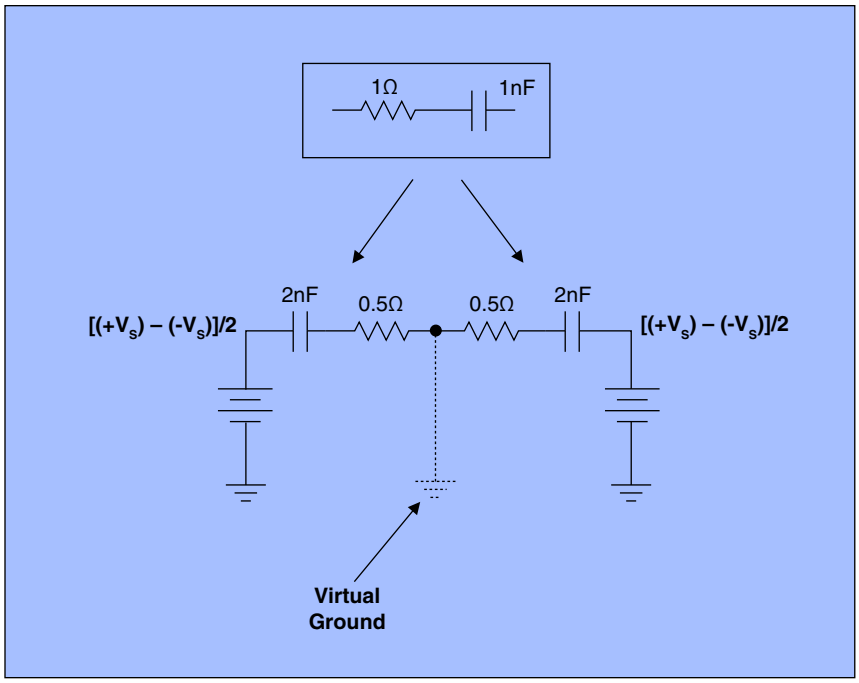


Figure 6. Equivalent circuit for computing the maximum power dissipation

virtual ground denoted by the dotted line and symbol. Since the real part of the impedance (1 Ohm) is negligible compared with the total capacitive reactance of 1989 Ohms, it can be neglected.

In the equivalent circuit the applied voltage will be one half the total potential applied to each module:

$$0.5[(+V_S) - (-V_S)] = 0.5[(175V) - (-5V)] = 90V \quad (5)$$

The circuit for each half will drive half the capacitive reactance which is 1989 divided by 2 — or 994.5 ohms.

The key to determining power dissipation begins with knowing the phase difference between V & I in the load. In this case it is quite simple because we have modeled our load as a pure capacitor, so the phase angle Φ is simply 90 degrees. The formula for determining the maximum power dissipated in the case of a reactive load for a phase angle greater than 40° is given by[5]:

$$P_D(MAX) = \frac{2V_S^2}{\pi Z_L} \quad (6)$$

Where: V_S = the magnitude of each supply
Z_L = the magnitude of the load impedance magnitude

So: $$P_D(MAX) = \frac{2(90)^2}{\pi(994.5)} = 5.18 \text{ watts}$$

Since the load is totally reactive, the 5.18 watts is dissipated by each of the PA78 amplifiers and none by the load. We can then go on to select a heatsink and confirm that the maximum allowable junction temperature of each PA78 will not be exceeded.

Dealing with the heat - An Apex Precision Power HS27 heatsink has been selected for mounting each PA78. The thermal resistance of each amplifier is 5.5°C/W and as previously determined, the dissipation of each amplifier will be 5.18 watts.

It is essential to confirm that the junction temperatures of the MOSFET devices in the PA78 amplifiers will not exceed a safe value.

The familiar thermal resistance equation is:

$$\begin{aligned} P\Theta_{JA} &= T_J - T_A \\ P(\Theta_{JC} + \Theta_{CA}) &= T_J - T_A \end{aligned} \quad (7)$$

This equation can be modified by substituting the thermal resistance of the heatsink Θ_{HS} for Θ_{CA}:

$$P(\Theta_{JC} + \Theta_{HS}) = T_J - T_A \quad (8)$$

Next the equation is solved to confirm that the anticipated junction temperature (T_J) will not exceed the maximum allowable junction temperature.

By rearranging the terms equation (8) becomes:

$$T_J = P(\Theta_{JC} + \Theta_{HS}) + T_A \quad (9)$$

In this design the power per device is 5.18 watts and the Θ_{JC} according to the PA78 data sheet, is 5.5°C/W. The Θ_{HS} for the heatsink is 7.8°C/W, as determined from Figure 7a, and the rise in temperature above the ambient is determined from figure 7b is 40.4°C.

So the maximum junction temperature will be:

$$\begin{aligned} T_J &= P(\Theta_{JC} + \Theta_{HS}) + T_A \\ &= 5.18(5.5 + 7.8) + 25°C \\ &= 68.9°C + 25°C = 93.9°C \end{aligned} \quad (10)$$

Therefore the actual T_J will never rise above 93.9°C. This is far below the maximum permissible value of 150 °C specified in the PA78 data sheet.

Finally, it is essential when applying high power to a highly-reactive load, such as a piezoelectric actuator, to check the device's power dissipation rating and the safe operating area. The former is discussed in reference 5 and the latter is covered in the PA78 data sheet.

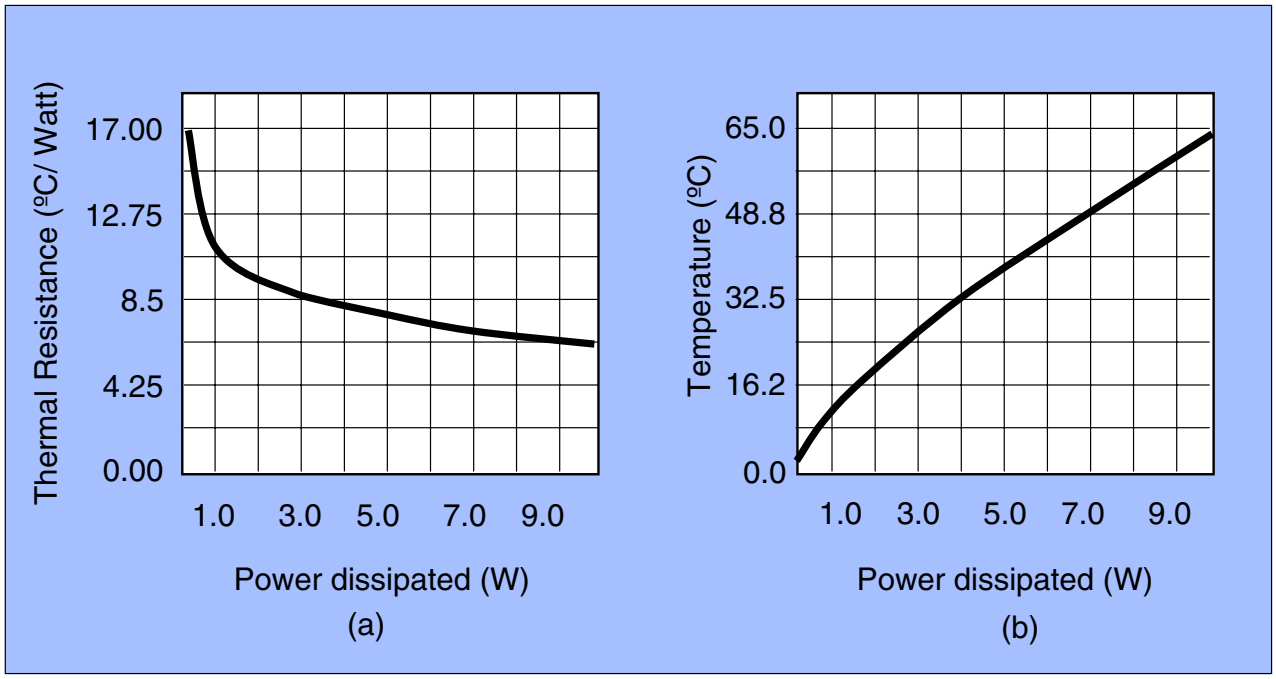


Figure 7. Heatsink Behavior – for the Apex Precision Power HS27 heatsink. The thermal resistance as a function of power dissipated is shown in (a); the temperature rise at the interface with the power module is plotted in (b).

2.3 MULTIPLEXING PRINTHEAD ACTUATORS

Piezoelectric nozzle assemblies for drop-on-demand printing look very much like an old-fashion hair comb where each of set of tines is an ensemble of jet nozzles. These nozzles are very thin and can therefore be stacked quite close together, one above the other.

A representative drop-on-demand printing head configuration might employ a single power operational amplifier to drive 128 nozzles. A variation of time-division multiplexing is employed. It departs from a conventional system of time-division multiplexing which normally connects to just one node at a time. Because in this case the power amplifier may be connected to any number of ports at any one instant — from 0 to 128.

Depicted in Figure 8 is a simplified diagram illustrating 128 MOSFET switches which connect each piezoelectric jet nozzle in the printhead to the power operational amplifier. Consequently, at any instant, the voltage on each piezoelectric driver is either zero volts or full voltage, depending on whether that nozzle is on or off. As shown in the figure, each nozzle is turned on by grounding the piezoelectric transducer via the MOSFET switch element corresponding to the nozzle it drives.

However, the high-voltage piezoelectric driver remains connected at all times to all of the high sides of the 128 nozzles via a bus.

The MOSFET switches enable controlling the entire ensemble, digitally. The switches allow the negative return of each piezo transducer to either float — in which case the companion nozzle does not dispense a droplet of ink — or to be grounded, so as to dispense a droplet of ink. At any instant, the printhead carrying all 128 nozzles is emitting anywhere from 0 to 128 ink droplets as governed by the program instructions delivered to the bank of MOSFET switches. Perhaps numbers 12, 84 and 128 nozzles are selected, at any instant. If so, they are all driven at once by the piezo transducer.

Different Waveforms for Different Inks - To successfully develop the inkjet printer just described requires that electrical, mechanical, and chemical expertise be brought together to achieve the right combination of parameters for each specific inkjet printing requirement.

In early, large-scale ink jet printers, the high-voltage signal was simply a huge square wave — such as a 48-volt drive signal — which was either on or off. That was fine up to a point, but it did not provide satisfactory control over the size and shape of the droplets dispensed by the jet nozzle. Also, the square corners of the waveform caused ringing and hindered the delivery of well-formed ink droplets.

At lower resolutions such aberrations seldom matter. However, at higher resolutions, precise control of the size and shape of the ink droplet becomes essential. Based on this, various waveforms have been devised for printing various kinds of inks.

The simplest is a trapezoidal waveform which exhibits a controlled ramp on the up slope and a ramp with a slightly different slope on the down sideas depicted in Figure 9. Though these slopes are well controlled, they are not necessarily symmetric. The rise on the up slope is likely to be faster. Whereas on the down slope a longer fall time is necessary to make sure ink will have sufficient time to flow from the ink magazine to the nozzle chamber.

The slower speed also ensures sufficient ink will be available when the next droplet is dispensed. A representative wave form is shown in Figure 9. For some inks it may be necessary to double-pulse the piezo transducer to overcome oscillations which might hinder satisfactory ink delivery. Depending on the ink employed, such double-pulsing can counteract oscillations that would otherwise occur when the droplet leaves the jet.

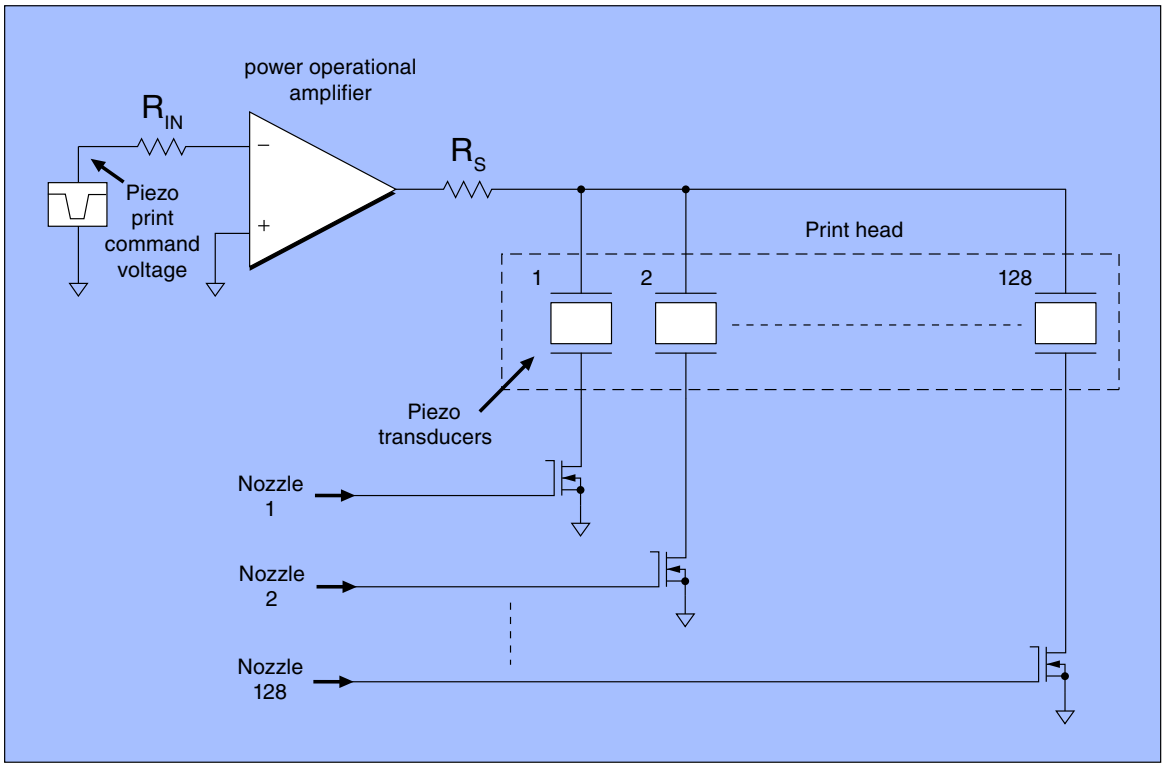


Figure 8. Simplified diagram using MOSFETs to multiplex the piezo transducers which form the printhead and is fabricated from a single piece ceramic endowed with piezoelectric characteristics.

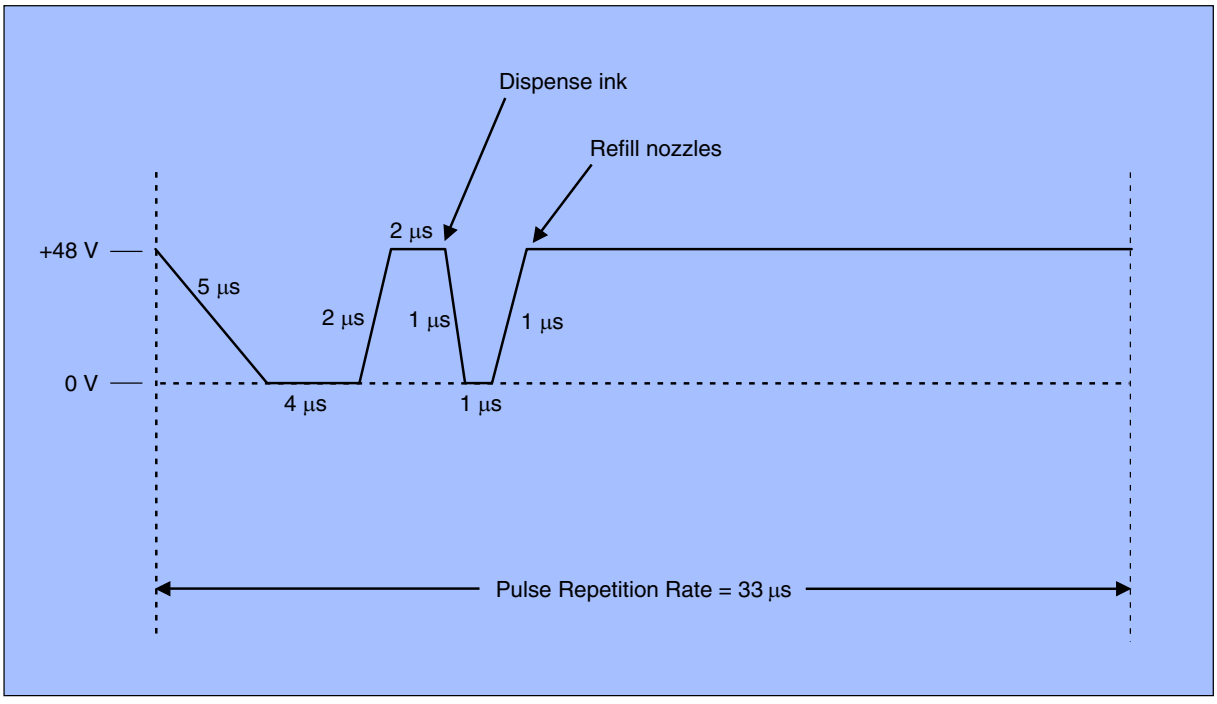


Figure 9. This tailored waveform was devised to optimize performance for a specific printhead.

Avoiding Pitfalls - Because piezoelectric elements are almost purely capacitive and therefore dissipate virtually no power, disposing of the heat is of paramount importance. Almost all the build-up of power is dissipated in the power amplifier module. This must be safely transferred from the power operational amplifier module via thermally-efficient heatsinking in such a way that the operating temperatures within the power operational amplifier remain safely below its rated safe operating temperature.

There is no single circuit which will fulfill all piezoelectric, ink-driver design objectives. That is why understanding all the design issues is so essential to developing driver circuits.

In one application a user intended to drive four piezoelectric printheads in parallel with each head driving 256 nozzles. In this case the pulse currents were fairly high because of the need to drive 1000 nozzles in parallel.

Assuming that the individual piezoelectric tranducers exhibit a capacitance of one nanofarad, 1000 nozzles present a capacitance of approximately 1 microfarad as the load for the power operational amplifier. That is a lot of capacitance. Now let's say you want to apply a 50 volt, 1 microsecond pulse. Given that $I = C \times dV/dt$, then $I = 10^{-6} \times 50/10^{-6} = 50$ amps. This design will require a power amplifier that will be able to deliver 50 amps — such as the Apex Precision Power Logic MP111FD.

This calculation assumes the worst case when the load is 100 percent capacitive. However, this is never going to be true since there will always be some stray resistances including the wiring. In some cases there may be a discrete resistor in series with each channel. This would completely change the assumption above, thereby reducing the current to a level much less than this calculation would indicate.

In another application a design group wanted to employ a 50 volt pulse and was planning to apply +/-100 volts to the amplifier. Whenever current is applied to a capacitor, of course, there will be a reverse current flow during each pulse cycle, which discharges the capacitor. While the capacitor is charged, one side of the amplifier delivers the entire current pulse, but the capacitor will momentarily have a 100 volt potential across it. However, the voltage will never go below zero. So there is no reason to have a ±100 volt symetrical supply. Having one would raise power dissipation within the amplifier, while serving no useful purpose.

Tailoring waveforms - Common to all designs is a waveform tailored to the specific characteristics of the ink to be dispensed. Principal governing factors are the viscosity of the ink and the shape and size of the droplet to be delivered to the printing surface and the mechanism of the printhead itself.

In some cases a double pulse is the optimal wave shape. The rise and decay of each pulse may have to be different. These wave shapes are developed empirically and are then stored in a computer so that the optimal waveshape for each ink and its specific application can be retrieved at a later time. The power amplifier must be designed to deal with any arbitrary wave shape that may be required for a given printing solution.

Here are some of the essential steps in designing the piezo transducer circuit:

- Determining design parameters - The Apex Precision Power MP111FD power operational amplifier is particularly well suited for driving piezoelectric transducer arrays. It is a 100 volt device with a 500 KHz power bandwidth and a 50 amp pulse capability. Shown in Figure 10 is a simplified drawing of the MP111FD power operational amplifier in an inkjet transducer application with the companion passive components identified.

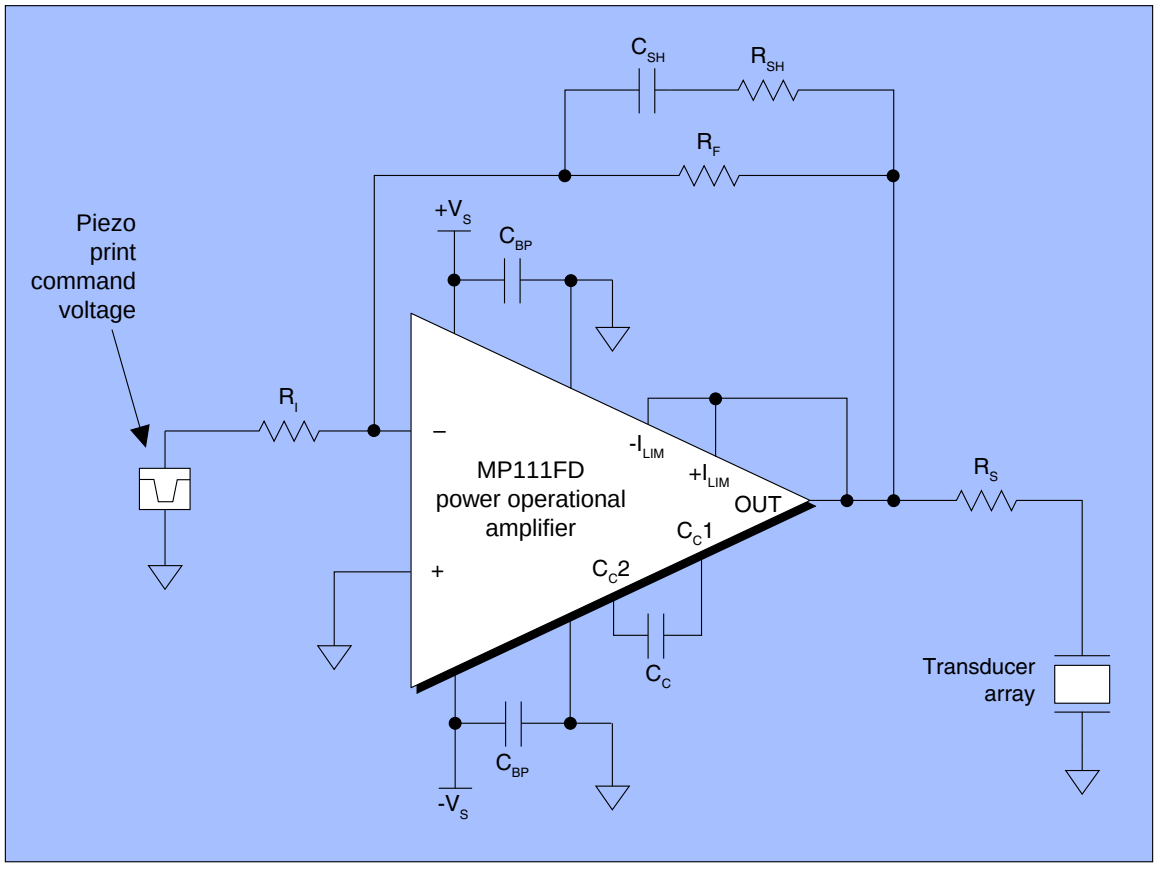


Figure 10. A simplified diagram using a power amplifier and companion passive components.

- Choosing power supply voltages – An unbalanced source voltage would be best. Assume that a 50 volt pulse is to be delivered by the power amplifier. Then a +62 volt and a –12 volt source would be appropriate. This will assist the charge-discharge cycle because the capacitive load presented by the array of tranducers must be driven back to zero volts during each pulse cycle. As the capacitor approaches zero volts, the –12 volt potential will make sure that the output transistor of the power amplifier will still have sufficient potential to drive the capacitor back to zero volts. This minimizes the power dissipation in the amplifier and also contributes to signal fidelity.
- Selecting passive component values – Assuming a gain of 10, the value of R_I would be 100 ohms, R_F is 1 kilohm and capacitor C_C is 33 to 47pF.
- Dealing with stability issues – Because the load is highly capacitive, a resistance R_S may need to be placed in series with the transducer array to improve the stability of the amplifier circuit. It may be necessary to experiment, but typical values for R_S will range from 0.1 to 0.5 ohms depending on the capacitance of the printhead. Without R_S there may be considerable overshoot in the output waveform that could adversely affect the droplet shape and the overall performance of the system.
- Bypassing the power supply terminals – Because the slew rate of the power amplifier is quite high, there would be a tendency for the power supply to droop if no precautions are taken. It is recommended that two, 1 microfarad ceramic capacitors of the leadless, surface-mount type, CBP, be connected directly to the $+V_S$ and $–V_S$ pins of the power amplifier.
- Enhancing dynamic response – This is achieved by connecting a series network comprising a 10pf capacitor C_{SH} and a 1kilohm R_{SH} in shunt with resistor R_F, as shown in Figure 10. This will improve the dynamic response of the power amplifier. Adjust these values slightly to optimize the response.
- Minimizing distortion - As the amplifier slews, it forces energy back into the signal source (the piezo print commad voltage). To minimize distortion that might otherwise occur, it is essential the signal source exhibit a low dynamic impedance of 1 ohm or less.
- Determining power dissipation - Once the waveform for a particular ink is determined, a simplified circuit can be devised to perform a SPICE simulation and thereby determine the power that will be dissipated within the amplifier.
- Selecting a heatsink - It is essential to hold the junction temperatures within the power amplifier module below 175°C. Determining the proper heatsink is a three-step procedure. First, the average power consumption is determined. Then the thermal resistivity in degrees C per watt of the heatsink is calculated. Finally, the thermal resistivity of the heatsink selected is checked to make sure it provides sufficient margin, holding the junction temperatures to a value well below 175 °C.

Shown in Figure 11 is a simplified SPICE circuit that represents the MP111FD power operational amplifier circuit. In this example the amplifier is assumed to be driving four inkjet printheads simultaneously. Each printhead will be assumed to have 256 nozzles for a total of 1024 nozzles. The total capacitance of the four heads is 1µF. If we assume only every third nozzle is driven at any instant, then the maximum capacitance in this analysis is reduced to 0.33µF. This is the load capacitance identified as C1 in Figure 11. A piece-wise linear waveform is developed by V8 that duplicates the selected waveform, as illustrated in Figure 9. The results of the SPICE simulation are depicted by the three graphs in Figure 12.

Plot (1) depicts the amplified output voltage waveform V(1). Plot (2) is the current pulse train I(C1) applied to the load capacitor C1. Whereas Plot (3) shows the average power dissipated in the amplifier vs. time:

$$\text{AVG } \{[(V1)-V(6)] \bullet [I(V6)]+[(V(1)-V(4)] \bullet [I(V7)]\} \quad (11)$$

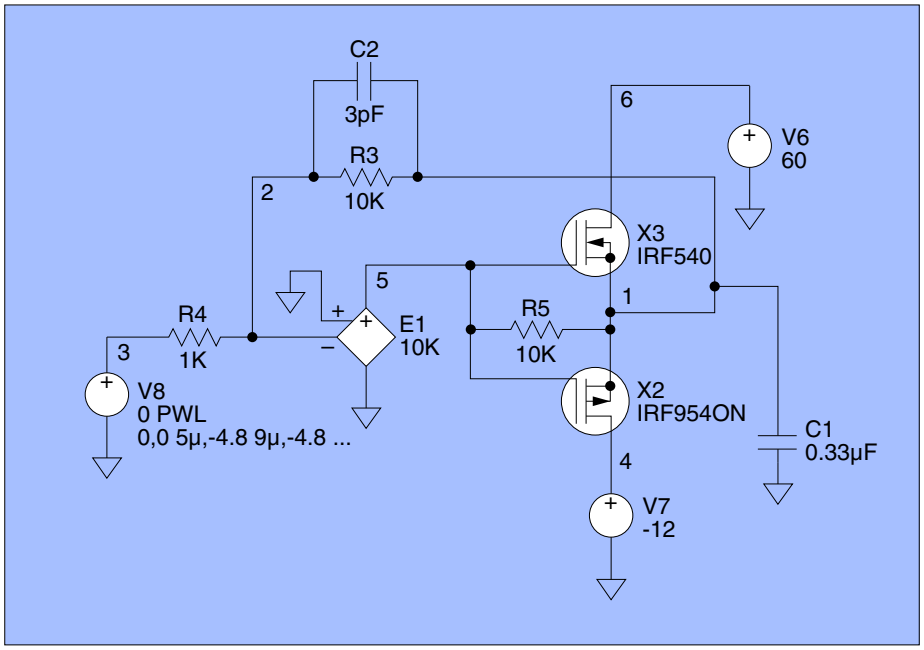


Figure 11. Spice representation of the transducer drive circuit. Note that capacitor C1 represents the printhead transducer.

Plot (3), as governed by this equation, is the average of the voltage across each output transistor multiplied by the current through each transistor at each instant in time. The result at the end of the period is the average power that the heatsink must dissipate due to the load. It is this average power, 68 watts, that is of interest in determining the heatsink requirement.

- The pulse rate frequency is 30 kHz and the period of the pulse is 33.33 microseconds. Notice that in Plot (2) in Figure 12 the current pulses end after 16 microseconds. The remainder of the period is dead time. Therefore the time interval for the average is greater than the time over which instantaneous energy is being delivered. Consequently, 68 watts is indeed the average power that must be dissipated by the amplifier over the full period.
- Determining heatsink requirements - By referring to the data sheet for the MP111FD, the AC thermal resistance is determined to be 0.65°C /W. To calculate the temperature rise of the junctions of the output transistors above the case temperature multiply the thermal resistance of the MP111FD by the average power dissipated:

$$0.65°C/W \bullet 68W = 44.2°C \qquad (12)$$

- To determine the permissible case temperature assume that a normal ambient temperature within the printer will be 30°C. The maximum operating case temperature of the MP111FD is 85°C. Therefore subtract the ambient from the maximum operating temperature to determine the permissible case temperature rise:

$$85°C - 30°C = 55°C \qquad (13)$$

- Therefore the permissible case temperature rise is 55°C.
- Though the load, C1, dissipates 68W of power in the amplifier, the heatsink will have to dissipate the quiescent power dissipation of the amplifier, as well as the power delivered by the pulse. The quiescent power dissipation of the MP111FD with the operating conditions given is approximately 11W. The quiescent power is due to the operating power supply voltages and the quiescent current in the amplifier.
- Therefore the actual amount of power that must be dissipated is the sum of the two – or 79 watts. The thermal resistance of the heatsink required is then:

$$X°C/W \bullet 79W = 55°C \qquad (14)$$

Where:
X = the required heatsink thermal resistance in °C /W
79 = the total amplifier dissipation in watts
55 °C = the permitted temperature rise of the amplifier

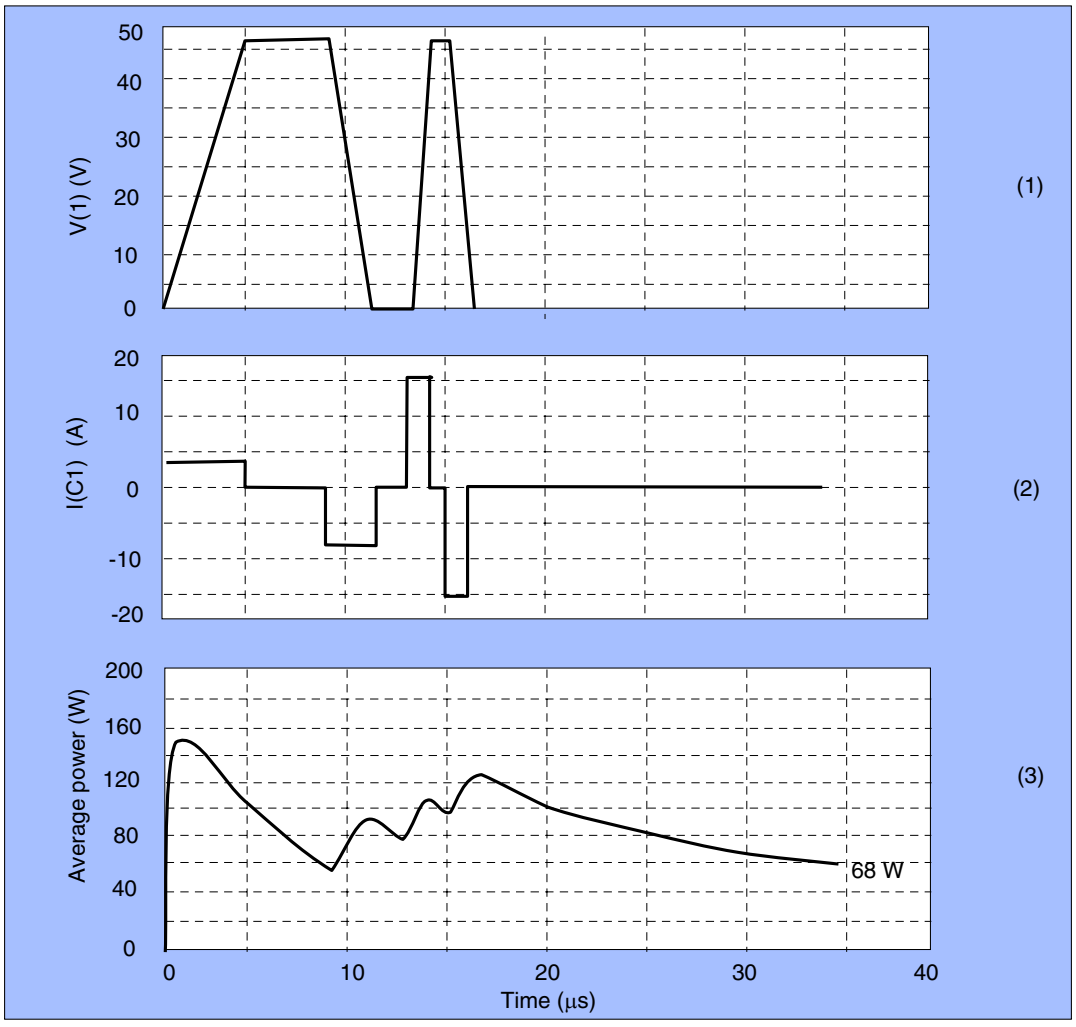


Figure 12. Spice (1) amplified output voltage V(1), (2) Current pulses I(C1) applied to capacitor C1, (3) average power dissipated in the amplifier versus time.

- Solving equation 14 for X yields a thermal resistance of 0.696 °C/W. Therefore, any heatsink that exhibits a thermal resistance of 0.696 °C/W or less will be acceptable in this application.
- Confirming the maximum junction temperature - Although a maximum junction temperature of 175°C is allowed, for long-term reliability a lower temperature would be better. Check that a heatsink with a thermal resistance of 0.696 °C/W will hold the junction temperature of the output transistors below 175°C:
- As previously mentioned, the 68 watts of power dissipation due to the load causes a temperature rise of 44.2°C in the output transistors. The total junction temperature with the selected heatsink is then the sum of the maximum case temperature and the temperature rise in the output transistors:

$$85°C + 44.2°C = 129.2°C \quad (15)$$

  Where:
  85°C = the case temperature with the selected heatsink
  44.2°C = the temperature rise of the output transistors due to the load.

- Since a junction temperature of 175°C is allowed, there will be a margin of 45.8°C – acceptable for the heatsink in this application.
- If the power module is to be located near the printhead and the ink is heated, the operating ambient will be well above room temperature of the traditional 25°C. In this case liquid cooling or forced air may be required.
- Note that for illustration purposes the quiescent current in the output stage and some other fine details have been neglected. However, Apex Precision Power has an online Power Design spread sheet software tool which can easily help you with all the details of arriving at a heatsink thermal resistance for your particular application. Log on to www.Cirrus.com and look for "Circuit Design Software" under the "Support" icon.

Conclusions - As we have shown, devising a driver circuit for inkjet circuits requires tailoring a waveform that will optimize the delivery of the ink droplets by a particular printhead. Then by following the sequence of steps described, the designer will be able to configure a driver circuit that will provide the necessary current pulse train and preserve the fidelity of the waveform delivered to the printhead, while addressing the resulting thermal issues.

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4. Cirrus Logic Corp, Application Note 21, Section 3.1 – Single Supply Operation of Power Operational Amplifiers, www.Cirrus.com
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GLOSSARY

Cation – An atom or a group of atoms carrying a positive charge. The charge results because there are more protons than electrons in the cation.

Curie Temperature – The Curie temperature (T_C) is the temperature below which a ferroelectric material can be transformed into a piezoelectric material. In the disordered state above the Curie temperature, thermal energy overrides any interactions between the local moments of ions. However, below the Curie temperature, these interactions are predominant and enable the electric dipole moments to align so that the piezoelectric transformation occurs.

Ferroelectric materials – So called because their behavior is analogous to the behavior of ferromagnetic materials.

Poling – The transformation of a ferroelectric material into the piezoelectric state by applying a strong electric field along a chosen axis at a temperature slightly below the Curie temperature (T_C). The material will also become elongated along the axis of the field.

Weiss Domains – Regions in a ferroelectric material, with spans on the order of 0.1 to several mm, in which the electric-dipole moments, upon being poled, align so they all face in the same direction.

Driving 3-Phase Brushless Motors

1.1 INTRODUCTION

NOTE: Apex Precision Power has developed a MCU program with a soft start algorithm for driving motors with the Apex Precision Power SA305. Download it free from the SA305 product page at www.Cirrus.com.

When comparing the attributes of a brushless motor with those of its brush motor equivalent, the most notable difference is the reduction in size and weight for the brushless motor offering the same horsepower. What is less obvious is the absence of the familiar brush–commutator arrangement that has been at the heart of single-phase DC brush motors for over a century. The lack of a brush-commutator interface means brushless motors also exhibit lower acoustic noise, are virtually maintenance free and they simply last longer.

Despite their many advantages, price points for brushless motors have been the single greatest detractor from their gaining wide-spread acceptance. That is until recently. Like all new technology, it was only a matter of time until gradual price reductions reached a level where demand would begin to increase. Today the price differential between brushless versus brush can be as little as 10 percent.

Adding to the appeal of the brushless motor is the widening availability of microcontrollers with the special functions (routines) necessary to control the three-phase operation of brushless motors. Equally important, and more readily available, are IC drivers that deliver power to the motor and form the interface between the microcontroller and the brushless motor itself.

This application note is intended to help guide the development of brushless motor drive boxes and motor drive cards. These specialized designs include the microcontroller, the programmability and the driver – all in a single assembly.

Let's begin this discussion by looking at the primary difference between motors with brushes and those without – the use of commutation. *Commutation* refers to an on-going sequence of steps that specifies the application of voltages to the proper motor phases and imparts the desired motor rotation throughout each successive 360-degree revolution.

Brush-type DC motors use electromechanical commutation that is achieved via graphite brushes that contact a circular commutator mounted on the rotor. The motor is designed so that torque is maximized as the motor shaft rotates throughout each full 360-degree rotation. However, in a brushless motor, although there is sensorless commutation, it is usually performed by switching electronics that rely on devices such as Hall sensors. This arrangement is depicted in Figures 1 and 2. The Hall sensors feed back the position of the rotor at known instants to the control electronics.

Brushless motors use what is commonly referred to as "inside out" commutation because their design is essentially that of a brush motor turned inside out. Although the stators in the motor are wound, the rotor is not. Instead it employs a permanent magnet rotor. The magnetic attraction of the rotor to the revolving magnetic field is induced in the wound stator poles and develops the torque necessary to rotate the motor and drive the attached load. This scenario is depicted in Figure 1.

Also brushless motors are synchronous in behavior because the rotor rotates at the same frequency as the magnetic field developed by the stator windings. Thus they differ from single-phase, AC squirrel-cage motors in which 'slip' develops, causing the rotor to rotate at a slightly lower frequency than the rotating AC field, depending on the load.

Thanks to the Hall sensors, the control circuitry always knows the exact moment to commutate. Most brushless motor manufacturers supply motors with three Hall-effect position sensors. Each sensor delivers an alternating binary high and a binary low as the rotor turns. The three sensors are offset, as illustrated in Figure 1. Each sensor aligns with one of the fields developed by one of the wound stator poles. Note that as depicted in Figure 3, two windings are always energized while one winding is not.

1.2 A BRIEF OVERVIEW OF PWM

The first Pulse Width Modulation (PWM) ICs appeared on the market some 40 years ago, so the concept of switching electronics is at least as old. Though the earliest applications were in switching power supplies, it was not much later that the technique was employed in brushless motors.

The principal benefit of PWM as a control technique becomes clear by examining Figure 4. The traditional linear power delivery technique for limiting power simply employs a variable resistance as depicted in Figure 4a. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded, the pass element resistance again approaches infinity and losses again approach zero.

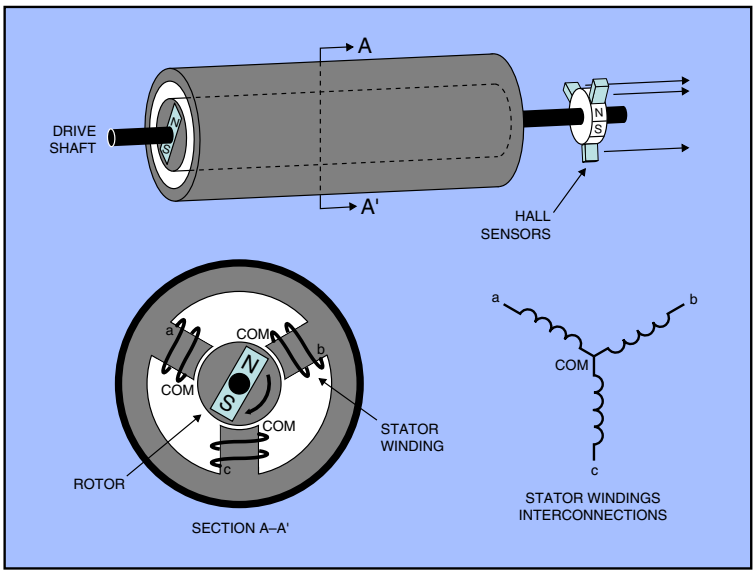

Figure 1. A Brushless Motor – Differs from a motor with brushes in that commutation is provided by sensors rather than the familiar bush-commutator arrangement found in a conventional DC motor with brushes.

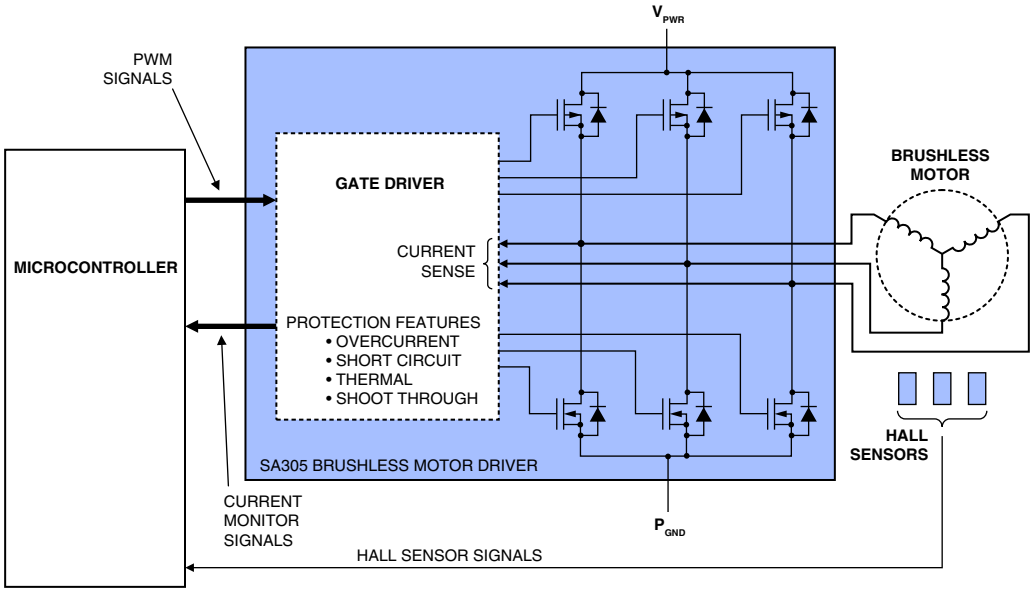

Figure 2. Block Diagram – A microcontroller and an Apex Precision Power SA305 Brushless Motor Driver provide the necessary functions to drive a brushless motor.

The disadvantage of the linear circuit becomes clear in the midrange when the output level is in the vicinity of 50%. At these levels the resistance of the pass element is equal to the load resistance which means the heat generated in the amplifier is equal to the power delivered to the load! In other words, a linear control circuit exhibits a worst case efficiency of 50% when driving resistive loads at midrange power levels. What's more, when the load is reactive, this efficiency drops even further.

Now consider the efficiencies of the switching PWM operation as illustrated in Figure 4b. In a PWM control system, an analog input level is converted into a variable-duty-cycle switch drive signal, as depicted in the figure. The process of switching from one electrical state to another, which in this case is simply between OFF and ON, is called “modulation” – thus the phrase *Pulse Width Modulation* or PWM.

Beginning at zero duty cycle, which is to say OFF all the time, the duty cycle is often advanced as the motor begins to rotate until it is running at the speed and/or the torque required by the application.

In the case of a PWM control circuit, the losses are primarily due to the ON resistance of the switching FET and the flyback diode which is why efficiencies as high as 80% to 95% are routine. However, at high switching frequencies, the energy required to turn the FETs on and off can become significant.

In addition to enhanced efficiency, PWM can provide additional benefits which include limiting the start-up current, controlling speed and controlling torque. The optimum switching frequency will depend on inertia and inductance of the brushless motor chosen, as well as the application.

The choice of switching frequency affects both the losses and the magnitude of the ripple current. A good rule of thumb is that in general, raising the switching frequency increases the PWM losses. On the other hand, lowering the switching frequency limits the bandwidth of the system and can raise the heights of the ripple current pulses to the point they become

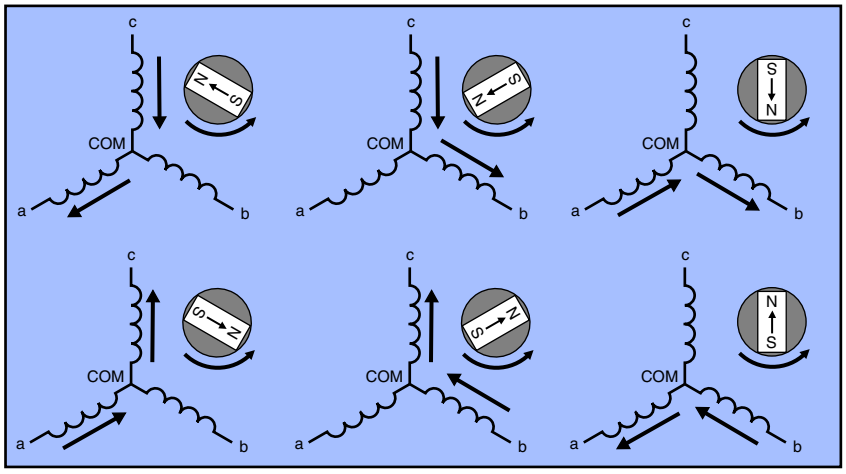

Figure 3. Six Connections – By monitoring the Hall sensors, the stator winding fields can be made to rotate so that the resultant field of the two energized stator windings and the pole of the permanent magnet rotor remain at right angles, thereby maximizing the instantaneous torque.

destructive or shut down the brushless motor driver IC. The ripple current pulses are depicted in Figure 5 and discussed in more detail later.

1.3 INTEGRATED DRIVERS

Until the introduction of off-the-shelf brushless motor drivers, such as the Apex Precision Power SA305, the development of three-phase driver circuits had to be configured discretely using three gate drivers and six FETs. Devices like the SA305 provide an integrated, fully-protected, three-phase brushless motor IC solution capable of delivering power levels of up to 300 watts[1]. The SA305 is fabricated using a multi-technology process that employs CMOS logic control together with DMOS output power devices. This brushless motor driver includes protection features such as overcurrent, short-circuit and thermal shutdown. For instance, the SA305 will shut down if the instantaneous current reaches approximately 12 amperes.

Operation of the SA305 is shown in Figure 2. The device features three independent, DMOS FET half bridges that provide up to 10 amperes PEAK output current under microcontroller or DSP control. As the motor rotor revolves in operation, the controller causes one motor terminal to be driven high, a second low and the third to float, as depicted in Figure 3. Proper synchronization of this sequence is assured by the feedback from the Hall sensors which keeps the microcontroller informed of the position of the rotor with regard to the stator windings at known instants.

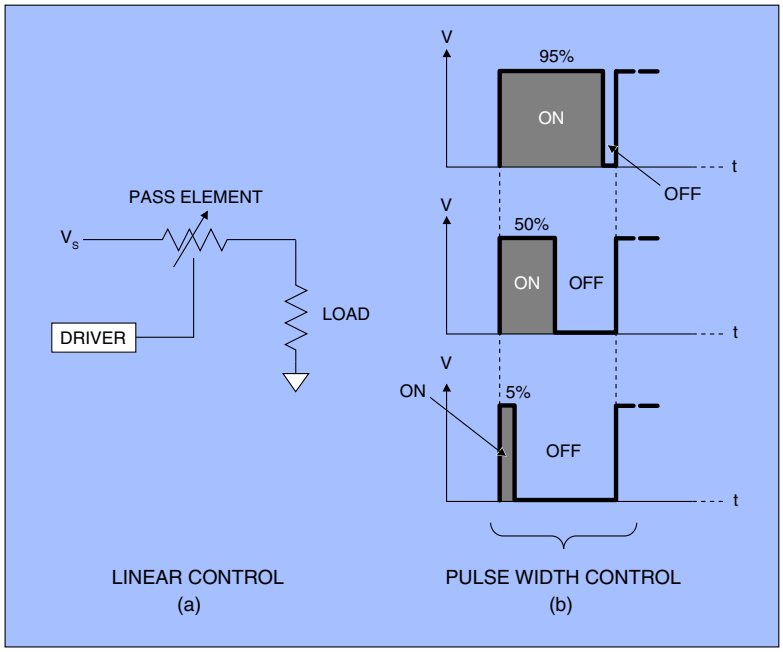

Figure 4. PWM versus Linear Control – PWM control in (b) exhibits far lower losses than the traditional linear control technique in (a).

"Shoot through" protection is included in this brushless motor driver IC. Shoot through identifies the state in which both the upper and lower portions of two half bridges are on at the same time. This must be avoided, for if it were to occur, it would overload the circuit and destroy the FETs. Consequently, a "dead time" is programmed to allow the FETs to fully commutate to the next state before power is applied to the ON FETs.

Fault status indication and current level monitors are provided directly to the SA305 controller. Output currents are measured using an innovative low-loss technique. The SA305 also offers superior thermal performance with a flexible footprint.

All brushless motors are driven by microcontrollers or some other intelligent system. A number of manufacturers including Analog Devices, Freescale, Microchip, and Texas Instruments market microcontrollers for motion control – and more specifically for driving brushless motors. For example, the Microchip PIC18F2331 includes a 14-bit resolution power control PWM module with programmable dead-time insertion to prevent shoot through. A brushless motor control algorithm employing this IC appears in Figure 6.

Although there are a number of sources which you can turn to for assistance in choosing a motor, brushless or otherwise, a good starting point is shared in Reference 2. As the author points out, choosing a motor requires looking at a whole list of issues including efficiency, torque, power reliability, and cost. (We also add motor inductance to this check list. As we shall examine shortly, it plays a vital role in how the motor will perform.)

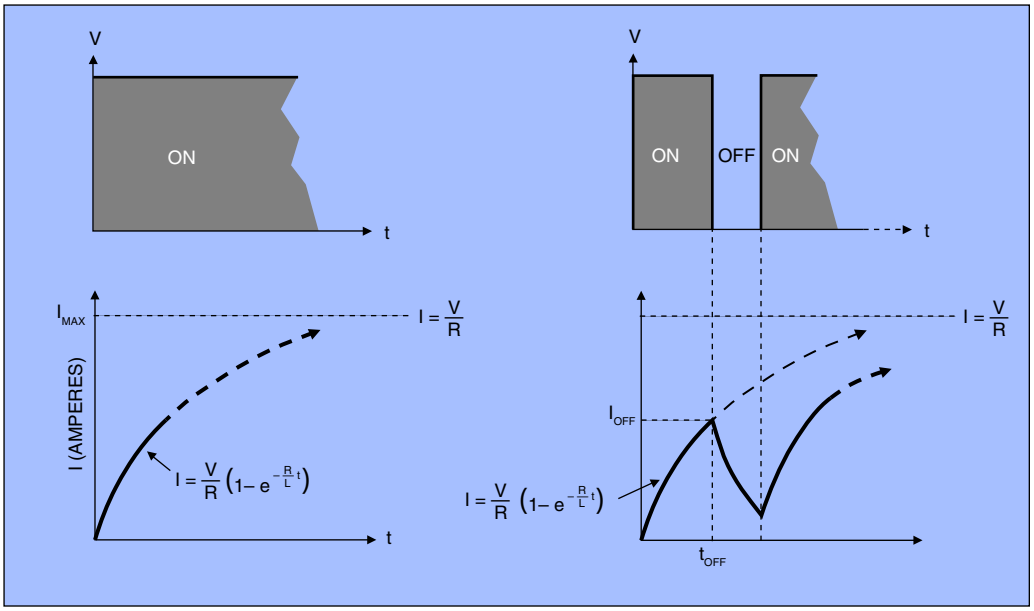

Figure 5. a) Current behavior with a steady-state excitation
b) Current behavior with PWM excitation

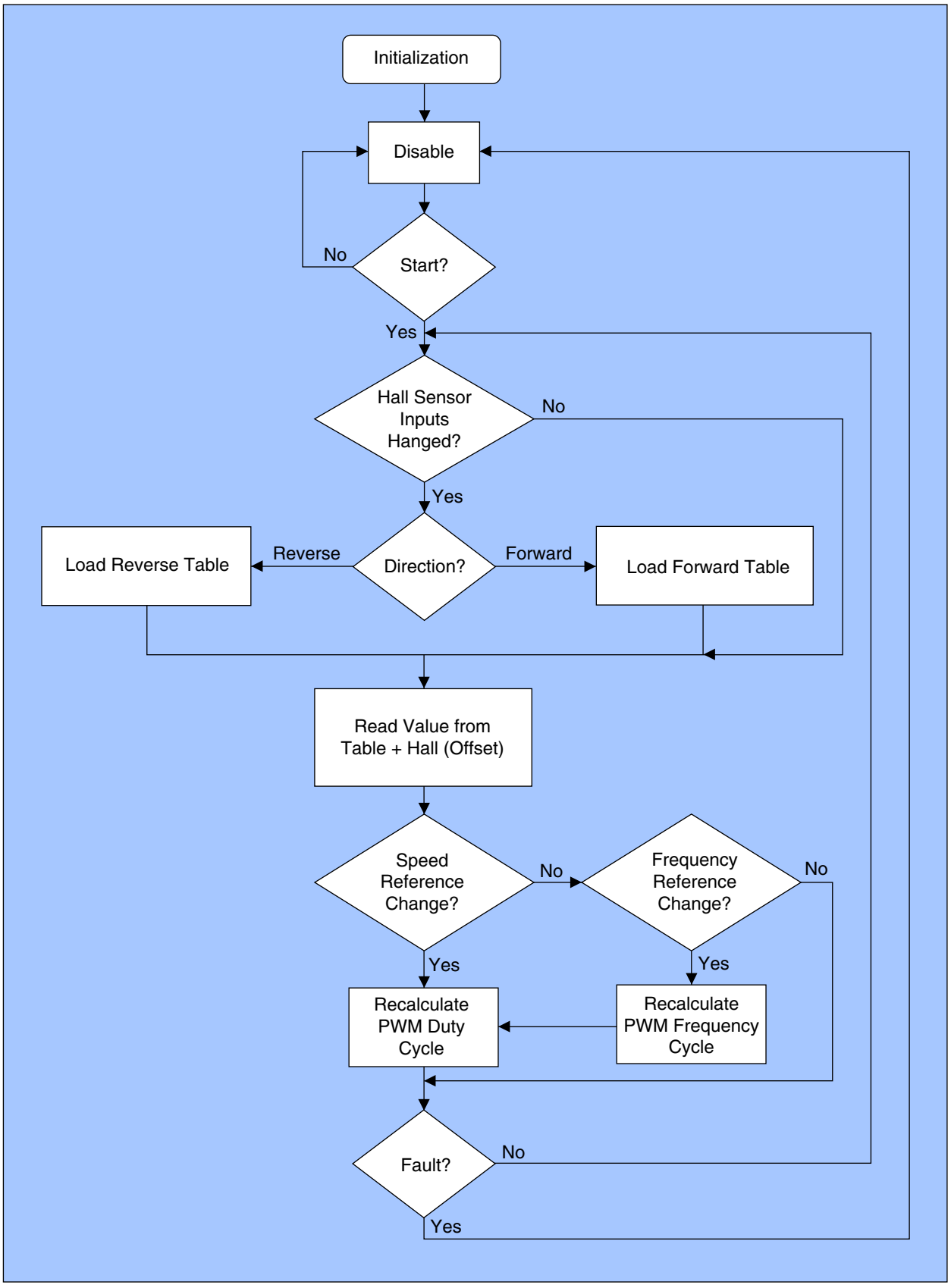

Figure 6. Brushless Motor Microcontroller Algorithm

What can be said categorically is that a brushless permanent magnet motor is the highest performing motor in terms of torque versus efficiency. Brushless motors allow you to consider a wide variety of performance options in designing your application. As we have explained prior, with a brushless motor you have control of all three stator windings, which is not the case with a traditional DC motor and its brush commutation. If your decision is to follow the brushless route, some important guidelines are outlined below.

2.1 BRUSHLESS MOTOR BEHAVIOR — AN OVERVIEW

One of the most critical operations for a brushless motor — also true for a brush motor — is when power is first applied to the motor while at rest. At that time the rotor is stationary and is delivering no "back EMF" or V_{BEMF}. V_{BEMF} can be expressed as:

$$V_{BEMF} = (K_b)(\text{Speed}) \qquad (1)$$

Where:

K_b = voltage constant (volts/1000 RPM)
Speed = revolutions per minute (expressed in thousands)

Once a voltage is applied to the motor, the rotor begins turning, generating a V_{BEMF} governed by Equation (1).

If we ignore for the moment that we plan to drive the motor with a PWM source and assume the motor is driven by a steady-state voltage, then we can express the current by this equation:

$$I = [(V-V_{BEMF})/R_m][1-e^{-Rt/Lm}] \qquad (2)$$

Where:

V = the applied voltage
V_{BEMF} = back EMF
R_m = stator resistance (winding pair)
L_m = stator inductance (winding pair)

Note that in Equation (2) the current (I) at any moment is a function of both the back EMF (V_{BEMF}) and the time (t). The current when the motor is stopped ($V_{BEMF} = 0$) is illustrated in Figure 5a and is a familiar waveform for characterizing the current in any L-R circuit with its rise time governed by the time constant L/R.

Now let's exchange the steady-state excitation voltage for a PWM source, as shown in Figure 5b. The current rises until the first ON pulse ends. When the voltage abruptly falls to zero at the end of the first applied voltage pulse, the current begins to decay towards zero. However, the next pulse will again drive the current upwards, and so forth, so that the current continues to rise. As the motor accelerates, the current waveform will exhibit a sawtooth profile. This sawtooth characteristic is also known as ripple. Because torque is directly proportional to current, the sequence of rising current pulses drives the motor and develops a corresponding torque that accelerates the motor.

The applied voltage, the switching frequency and the PWM duty cycle are three crucial parameters that can be programmed independently. How these variables are selected will effect the behavior of the motor with regard to how fast it will accelerate, and how fast its speed and torque will develop.

2.2 A SPECIFIC EXAMPLE

This example begins by choosing a motor that will exhibit the mechanical performance required — which is to say the torque, the efficiency and the other specifications already discussed, are sufficient to meet the motor drive requirements of the end system. For this example a low-inertia, brushless motor will be used that delivers 55 oz-in of torque at 5000 rpm. The selected motor is a Galil Motion Control BLM-N23-50-1000-B (www.galilmc.com). The winding characteristics of this motor include a stator-winding pair that exhibits a resistance (Rm) of 1.2 ohms and an inductance (Lm) of 2.6 millihenries. The torque constant (Kt) of the motor is 12.1 oz-in/A and the voltage constant Kb of the motor is 8.9 volts/1000 RPM.

First make certain that the maximum current capability of the IC driver – in this case the SA305 with an output of 12 amperes -- is not reached. Should this happen, the drive circuit will shut down.

If V/R ≤ 12 amperes, then regardless of the other parameters, the current can never reach this value. This can be seen in figures 5a and 5b where both the first and all succeeding pulses approach the value of V/R. Another way of looking at it is the current in any L-R circuit can never exceed V/R. Consequently, voltage which includes any instantaneous ripple will never shut down the SA305.

If V/R > 12 amperes, then consideration must be given to several factors in the design. In this example, the Rm is 1.2 ohms. Assuming a 60 volt drive voltage, then V/R = 60/1.2 = 50 amperes. When the initial voltage is applied to the motor, the current ramps up as explained in equation (2). As the back EMF builds up, the current will taper off as shown in Figure 7. Maximum current may never be reached in normal operation because of the back EMF. The torque constant of the motor and the inertial load will govern the rate at which the motor comes up to speed. If the motor has a particularly low L/R time constant relative to the mechanical time constant, the current can reach the maximum well before the motor builds any back EMF.

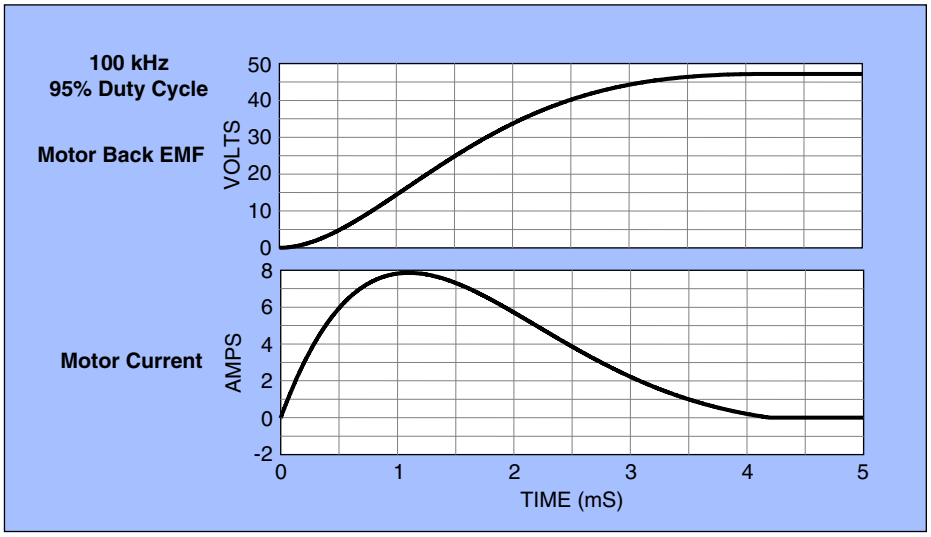

Figure 7. A graphical approach to determining maximum motor current – here the dynamic simulation of the Galil BLM-N23-50-1000-B brushless motor is illustrated.

Note that in this example the simulation depicted in Figure 7 discloses that the current will never rise above 8 amperes — well below the 12 amperes limit. If the current were to exceed the limit of the driver, adding external series resistance or inductance would limit the peak current and di/dt respectively, but each will adversely effect the performance of the system. If the start-up current is controlled with a PWM drive by limiting the duty cycle of each pulse and not to exceed the maximum peak current rating of the driver, the motor can safely accelerate. The current monitor feature of the SA305 makes this type of feedback relatively simple to implement.

By employing a microcontroller and monitoring the instantaneous currents in all three phases, a closed-loop algorithm can be developed for start-up purposes which would hold the peak current near 12 amperes without actually exceeding it. A small amount of headroom makes good sense so programming for an 11 ampere motor current would be best. The advantage of this approach is that it optimizes the run up and keeps the current and the acceleration as high as possible. In this approach the duty cycle would be modulated, based upon the current sensed in the three phases, as depicted in Figure 2. Further discussion on the use of microcontrollers to drive brushless motors is available in References 3, 4, and 5.

A "soft-start" algorithm can be developed as an open loop software solution to maintain a low duty cycle, as well as slowly up the required speed. Programming the start-up duty also ensures that the overcurrent limit of the SA305 is not exceeded. A soft-start algorithm is covered in Section 3 of this Application Note.

3.1 GUIDELINES FOR DESIGNING A MOTOR DRIVE CONTROL PROTOTYPE

The use of the Apex Precision Power DB62 Demonstration Board is recommended as the first step in assembling a prototype. The DB62 is designed to demonstrate the capabilities of the SA305 as a three phase brushless DC motor driver IC.

The PWM inputs to the SA305 are controlled by an on-board microcontroller. The supporting document is the DB62U data sheet, "Demonstration Board for SA305EX". The EVAL49 board which is described in DB62 is pre-wired for all required and recommended external components. The Microchip PIC18F2332 which has been selected to control the SA305 is pre-programmed for motor control applications. It is covered in Reference 6.

By utilizing the on-board Microchip PIC18F2331 microcontroller with the SA305, PWM input control is achieved. The resulting circuit of the DB62 can be easily converted into the circuit shown in Figure 9 and serve as the base circuit for a production version. The sequence table for commutation (obtained from the motor data sheet) is entered in the program memory of the microcontroller.

Hall Sensors – Hall sensors A, B and C are connected to the IC pins of the Input Capture (IC) module in the PIC18F2331. This module interrupts on every transition on any of the IC pins. Upon interrupt, the interrupt service routine reads all three inputs and loads the correct sequence for commutation.

Soft Start Algorithm – The use of a soft start algorithm enables controlling the rate of acceleration and consequently the maximum current. As depicted in Figure 8, there are two parameters to be programmed: the increment and the delay. The delay is the time interval between the successive incremental changes in the duty cycle. Whereas the increment is the percent increase in duty cycle which is implemented at the end of each delay.

After each increase in duty cycle that is slightly higher than the last one, there is a delay, or time interval, until the next incremental change occurs. The effect of the soft start is to ramp up the motor speed without exceeding the maximum allowable current until the specified speed is reached. This also serves to hold the speed until the motor is shut off.

NOTE: Apex Precision Power has developed a MCU program with a soft start algorithm for driving motors with the SA305. Download it free from the SA305 product page at www.Cirrus.com.

Handling Reversals – When the motor is to be reversed, it is essential that the soft start algorithm is once again initiated, causing the motor to gradually accelerate in the opposite direction. Likewise, during development, it is essential to reduce the duty cycle, holding the duty-cycle start-up current before attempting to rotate the motor in the opposite direction. Once the motor begins to rotate in the opposite direction, and the back EMF begins to build up, the duty cycle may be increased

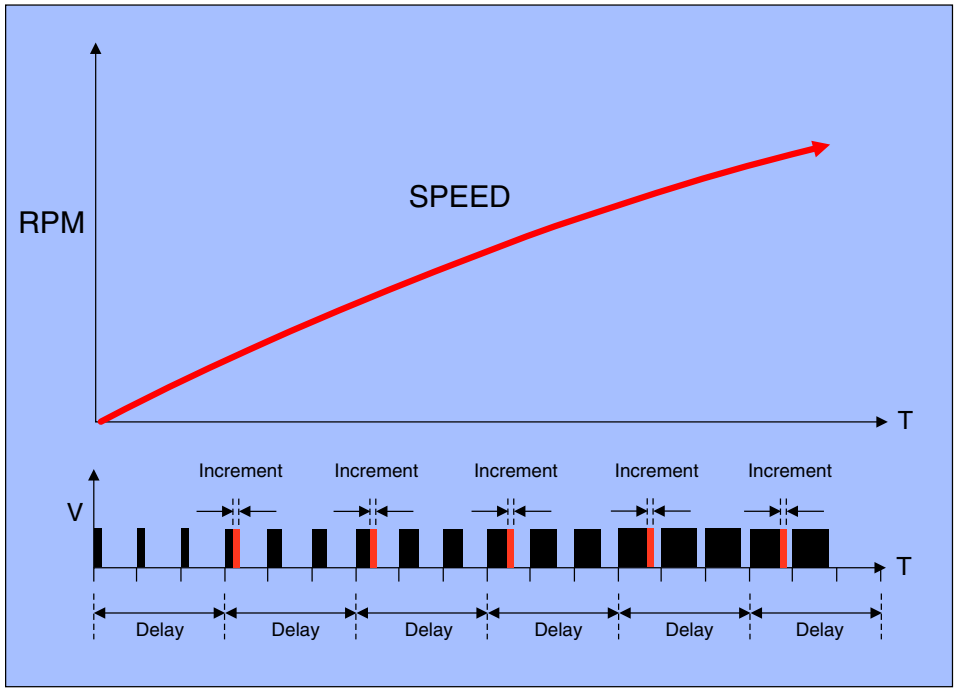

Figure 8. Increment and Delay – Principal parameters in the slow start algorithm.

3.2 PARAMETERS APPLIED TO THE MICROCONTROLLER

Here are parameters to address as they apply to the operation of the microcontroller:

- V_{FREQ} - The PWM frequency can be varied from 4 KHz to 118 KHz by varying the voltage applied between V_{FREQ} and microcontroller ground.
- V_{DUC} - The duty cycle can be varied from 0 % to 98 % by varying the applied voltage between V_{DD} and ground.
- Forward/Reverse - The Forward (High)/Reverse (Low) pin is provided to control the direction of the motor. Depending upon the direction, the corresponding Hall sensor commutation sequence shown in the DB62 document is used and the PWM signals are generated accordingly.
- Run/Stop - The Run(Low)/Stop(High) enables starting and stopping the motor by shifting the applied binary voltage between V_{DD} and ground.
- Monitoring Current – The SA305 data sheet specifies the ratio of the sensed current to output (motor) current for each of the three outputs.

3.3 SPECIFIC DESIGN TIPS

The following is a discussion of key design tips that will assist in prototype design:

Maximum Current – If the current exceeds 12 amperes, the SA305 will shutdown at start. Consequently, it is essential to determine the maximum current which the motor and the SA305 Drive IC will carry during the start up cycle. If the L and R are low, the current will ramp up quickly. The use of back EMF to counteract a high current will not be able to ramp up so quickly due to the inertia of the rotor. This is discussed in detail in Section 2.2 of this Application Note. The maximum start up current can be easily determined by using Cadence's PSpice simulator which has a built-in brushless motor simulation program. Also refer back to the soft start algorithm discussion in Section 3.1.

Three Separate Ground Planes – As discussed in detail in the DB62 document, noise immunity can be enhanced by three separate ground planes tooled in a multilayer board: DGND (microcontroller ground), SGND and PGND. The DGND ground is the most sensitive. The ground planes should be inter-connected by jumpers as depicted in Figure 9, so that no current flows between the three independent grounds. These jumpers are located in the center of the evaluation board at the right of the SA305.

Do NOT connect grounds at any other points. Make sure there is no direct connection between the P ground and the S ground. The connections must be made in a manner that keeps current from flowing through one ground plane to another via the jumpers.

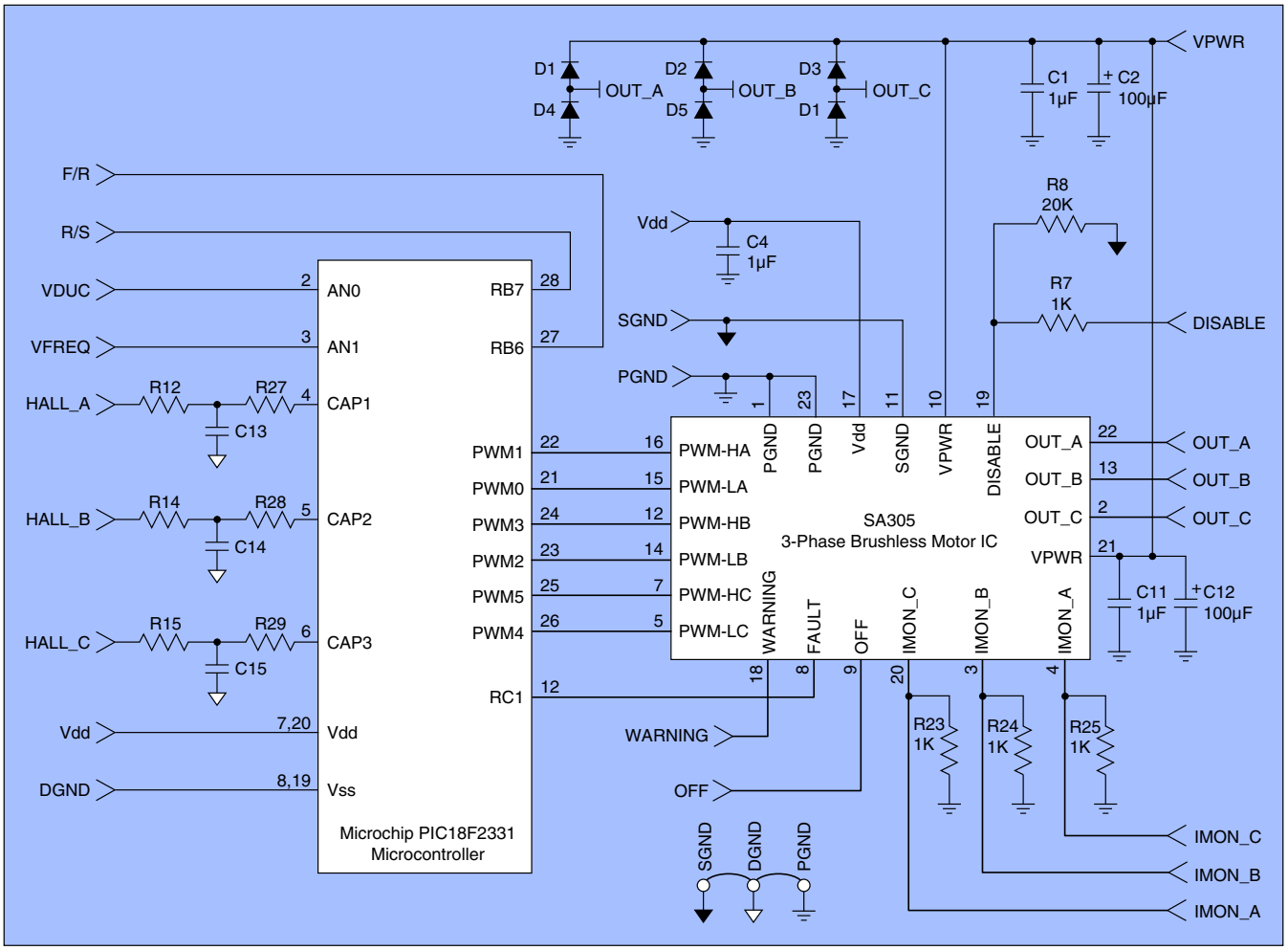

Figure 9. A specific example – Combining the SA305 brushless motor IC with a Microchip PIC18F2331 microcontroller

Heat Sinking – Refer to the SA305U datasheet for maximum power dissipation and power derating specifications. Heat sinking requirements can be determined based upon the power calculations. If a heatsink is required, please refer to the Apex Precision Power website for available options. References 7 and 8 provide information on power dissipation and thermal calculations. Incidentally, the DB62 demonstration board comes with an HS32 heatsink.

External Flyback Diodes – In high current applications it is recommended that external flyback diodes be connected as shown in Figure 9. This is because the internal body diodes cannot sustain high currents for long periods of time. Low voltage drop, high current Schottky diodes, such as International Rectifier's part number 50SQ100, are recommended.

Bypass Capacitors – The 1-µF ceramic capacitors supplied with the DB62 kit are for high frequency bypassing of the V_S and V_{DD} supplies (C1, C11, C4 and C7 on the EVAL49 schematic). Two additional 100-µF bypass capacitors are provided with the kit for the V_S supplies (C2 and C12 on the EVAL49 schematic). Please refer to Application Note 30 for guidelines on power supply terminal bypassing.

Hall Sensor Filters – In order to make sure that the MCU is receiving a clean signal from the Hall sensors enclosed within the noisy motor environment, RC filters must be connected in each of the three Hall sensor leads, as depicted in Figure 8. A Schmitt trigger circuit can also be added to each leg to provide additional noise immunity.

Resistors R12 and R27, in conjunction with capacitor C13 and the comparable components of the other two Hall diodes, comprise low pass filters that can suppress the noise.

The values of these components will depend on the switching frequency of the PWM source and how fast the Hall sensors respond. The filter time constant should be much smaller than the rise times of the Hall sensors to make sure that the switching of the sensors is not affected. Please refer to Application Note 32.

Optional External RC Snubber Circuits – (for high switching noise scenarios) R13 and C5, R16 and C8, R19 and C10 in the EVAL49 schematic in DB62 can provide noise immunity — especially in high-load-current scenarios. With the DB62 Evaluation Kit a 4.7 nanofarad, 100 volt capacitor in series with a 50 ohm 5W resistor is provided for each OUT-A, OUT-B and OUT-C line, and they should be connected in series between the SA305 outputs and P_{GND}. Depending on the PWM frequency and the resistances and inductance of the motor being driven, other values may be more effective.

The power dissipated in the snubber components can be estimated by:

$$P = V^2 C(F_{SW}) \qquad (3)$$

Where:

P = power dissipated
$V = V_S$ supply voltage
C = Snubber capacitor value
F_{SW} = Switching frequency

4.1 OPEN AND CLOSED LOOP OPTIONS

The motor may be operated in an open-loop configuration with a specified speed reference. As depicted in Figure 10a, a voltage can be applied to the V_{DUC} input of the PIC18F2331 microcontroller that is set to a value that will maintain the motor rotation at the required number of RPMs for the load it is driving – once the soft start algorithm has brought the rotor up to full speed. Though not shown in Figure 10a, the Hall sensors are still employed to make sure that the applied rotating magnetic field is always positioned so as to maximize the torque applied to the rotor of the brushless motor.

However, this open-loop method of speed control is not recommended. Instead, it is best that the motor be operated in a closed-loop configuration as depicted in Figure 10b, for reasons explained immediately below.

Closed-loop speed control is the preferred method for speed control because the microcontroller is actually measuring the true RPM based upon input from the Hall sensors and minimizing the error from the speed reference — using PID control in real time. As shown in Figure 10b, the designer needs to determine the voltage corresponding to the speed and apply it to the A/D pin 2 or 3. (Employing Hall sensors in closed-loop speed control configuration is also discussed on page 12 of Reference 4.)

Closed-loop torque control is depicted in Figure 10c. The outputs of the three current sense pins IMON_A, IMON_B and IMON_C of the SA305 Driver IC are added as voltages in an operational amplifier and then fed to one of the A/D inputs – pins 2 or 3 of the microcontroller. Note that the SA305 data sheet (Reference 2) supplies the information as to the current sense outputs. It is important to note that the current sense ratios (I_{LOAD}/I_{SENSE}) are not the same for the three outputs. So it is important to scale each of them properly by selecting the appropriate summing resistors so as to obtain an output from the op amp that is a true representation of the instantaneous current flow to the brushless motor.

The two values within the microcontroller — one receiving the reference value of the torque and the other the measured value obtained from the SA305 current sense outputs — are compared and applied to an PID control algorithm. This serves to change the duty cycle of the PWM outputs as necessary, to maintain a constant brushless motor torque. (This is discussed in more detail on page 13 of Reference 4.) PIC controllers are discussed in the Appendix of this document.

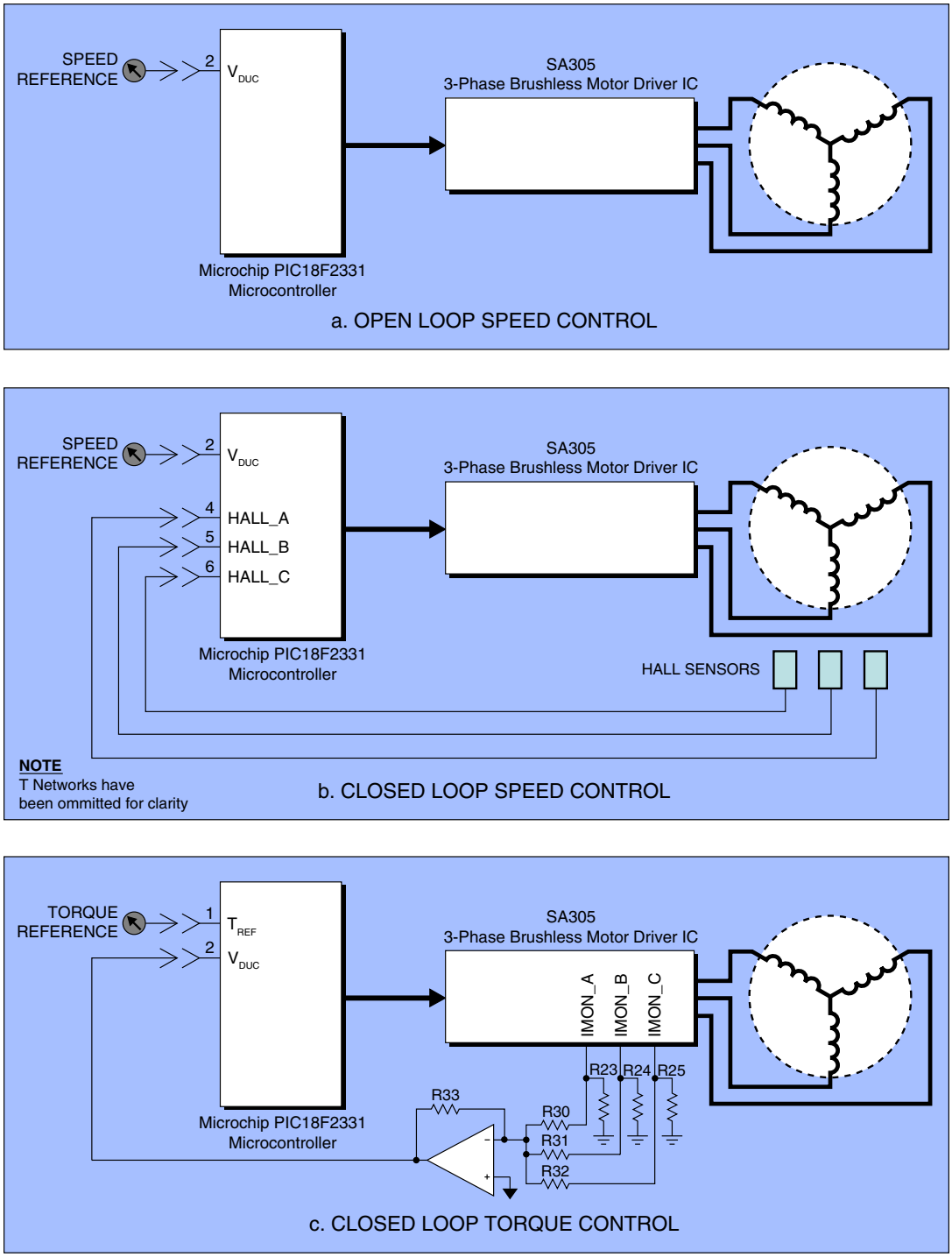

Figure 10. Open and Closed Loop Control Options

5. APPENDIX

Proportional integral derivative controller – A Proportional-integral-derivative controller (PID controller) is a feedback loop technique employed in control systems. It can be thought of as an extreme form of a phase lead-lag compensator. A PID controller has one pole at the origin and the other at infinity[9]. It is used to compare a measured value with a reference value. As employed in motor control the values may be either speed or torque. The difference value is then employed to calculate a new value to restore the value – be it speed or torque to the setpoint value. A PID loop produces accurate, stable control in cases, whereas a simple proportional control would be likely to induce a steady-state error or would induce oscillation. Unlike more complicated control algorithms based on optimal control theory, PID controllers do not require advanced mathematics to develop a design.

A standard PID controller is also known as a "three-term" controller and can be expressed in the “parallel form” by Equation (4) or the "ideal form" by Equation (5):

$$G(s) = K_P + K_I \frac{1}{s} + K_D s \qquad (4)$$

$$= K_P \left(1 + \frac{1}{T_I s} + T_D s\right) \qquad (5)$$

Where:

K_P is the proportional gain
K_I the integral gain
K_D the derivative gain
T_I the integral time constant
T_D the derivative time constant.

- The proportional term provides an overall control response that is proportional to the error signal through the all-pass gain factor.
- The integral term reduces steady-state errors through low-frequency compensation by an integrator.
- The derivative term improves the transient response through high-frequency compensation by a differentiator.

The effects of each of these three terms on closed-loop performance are summarized in Table 1.

Table 1. The Effects of Independent P, I and D Tuning

Closed-Loop Response	Rise Time	Overshoot	Settling Time	Steady-State Error	Stability
Increasing K_P	Decrease	Increase	Small Increase	Decrease	Degrade
Increasing K_I	Small Decrease	Increase	Increase	Large Decrease	Degrade
Increasing K_D	Small Decrease	Decrease	Decrease	Minor Change	Improve

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3-Phase Switching Amplifier - SA306-IHZ

INTRODUCTION

The SA306-IHZ is a fully-integrated switching amplifier designed primarily to drive three-phase brushless DC (BLDC) motors. Three independent half bridges, each comprising a P-FET and a N-FET in a configuration, provide more than 15 A of PEAK output current under digital control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram of this IC is provided in Figure 1.

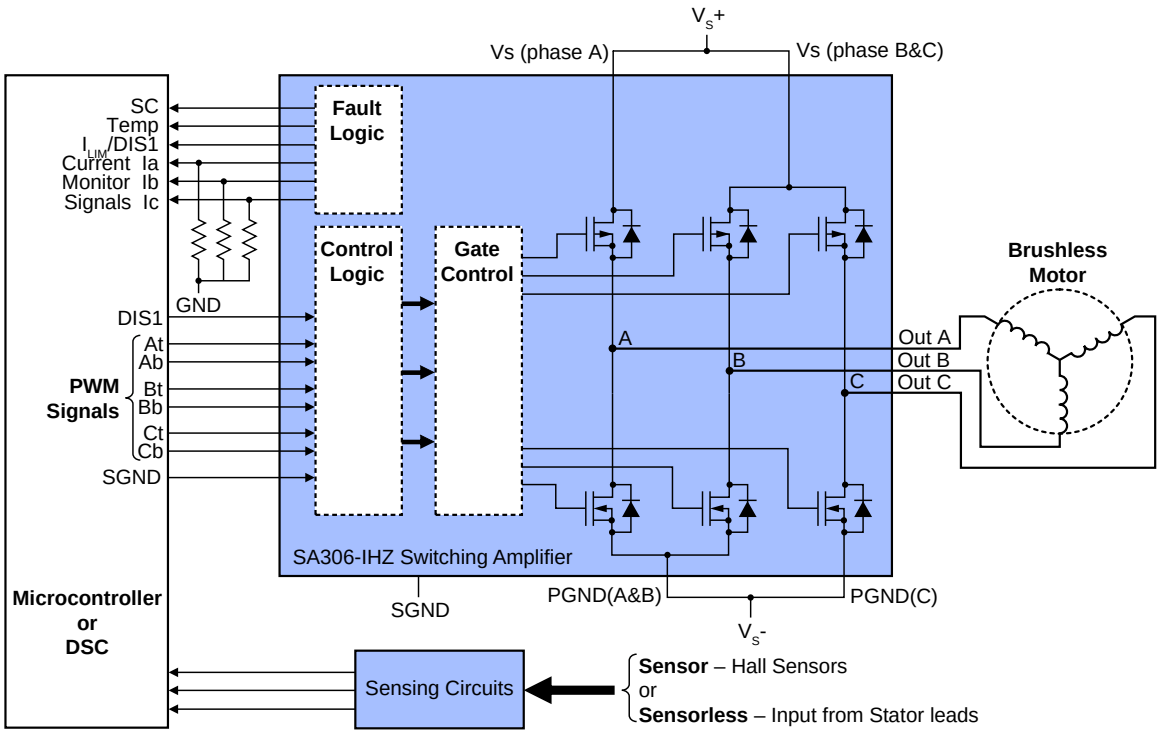


Figure 1. Polarity is Easily Switched – DC-to-DC converter, three terminal module can be switched from a positive to a negative converter by simply interchanging the jumpers identified by Note 2.

DRIVING BRUSHLESS MOTORS

Brushless motors of the same horsepower as their brush counterparts are smaller and lighter. What is absent in the former is the familiar brush–commutator arrangement that has been at the heart of single-phase DC brush motors for more than a century. Because they lack this brush-commutator interface, brushless motors exhibit lower acoustic noise; are virtually maintenance free; and a brushless motor will exhibit a longer life cycle. As recently as 2004, brushless motors were considered to be significantly more expensive than brush motors. At the time of this writing in 2008, brushless motors have benefited from a decrease in cost so that today the price differential is as little as a 10% when shopped against an equivalent brush motor.

CYCLE-BY-CYCLE CURRENT LIMIT – THE BENEFITS

Traditionally, in applications where the current flow to a brushless motor is not otherwise directly controlled, the inrush current had to be considered when selecting a proper driver amplifier. This is in addition to the average current that will flow. As an example, a 1 A continuous motor might require a drive that can deliver well over 10 A PEAK in order to deliver the initial inrush current that flows during startup. Many discrete motor drives use over-sized FETs to withstand startup conditions which results in higher system costs and larger package sizes.

However with the unique and robust cycle-by-cycle current limit scheme designed into the SA306-IHZ, the inrush current requirements of the motor are no longer an issue when selecting the drive. Current limit schemes inherently reduce acceleration of the motor; however, the average current delivered by the SA306-IHZ during start up is higher

than would be delivered by other current limit schemes. By using the SA306-IHZ, the motor will reach its operating RPM faster. Thus the SA306-IHZ is able to safely and easily drive virtually any brushless motor which requires 5 A continuously or less, through its startup interval — without regard to what its in-rush requirements are. (Up to 8 A continuously in the case of the SA306A-FHZ).

SA306-IHZ APPLICATIONS

The SA306-IHZ is designed primarily to drive three-phase motors. However, it can be used for any application requiring three high current outputs. The signal set of the SA306-IHZ is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in Figure 1. As explained below, over-temperature, short-circuit and current limit fault signals provide important feedback to the system controller that can safely disable the output drivers in the presence of a fault condition. High-side current sensors monitor the output current of all three phases, providing performance information that can be used to regulate or limit torque.

A SYSTEM OVERVIEW OF THE SA306-IHZ

With the introduction of the SA306-IHZ, designers now have an off-the-shelf solution for driving BLDC motors versus developing driver circuits by configuring three discrete gate drivers and six FETs. The performance specifications for the SA306-IHZ are unusual in that it can deliver over 15 A PEAK with up to 60 V applied to its FETs[1].

Imparting Rotation – Three independent DMOS FET half bridges pro¬vide the output current. In operation, as the motor rotor revolves, the controller causes one motor terminal to be driven HIGH, a second LOW and the third to FLOAT in a high impedance state, as depicted in Figure 2. This causes the magnetic field to rotate in six steps per electrical revolution in the simplest case, imparting rotation to the permanent magnets in the rotor. Proper synchronization of this sequence is assured by the feedback from either Hall sensors or a sensorless control system that keeps the microcontroller continuously informed of the position of the rotor with regard to the stator windings.

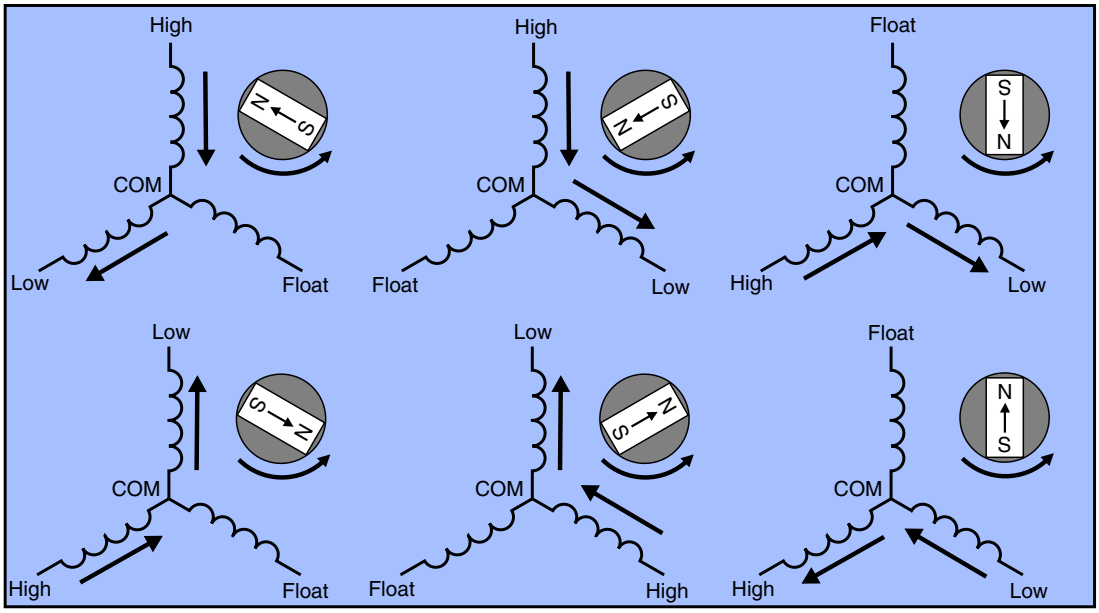


Figure 2. Imparting Rotation – By monitoring the Hall sensors – or by monitoring Back EMF in a sensorless configuration – the stator winding fields can be made to rotate so that the resultant field of the two energized stator windings and the pole of the permanent magnet rotor remain at right angles, thereby maximizing the instantaneous torque.

Shoot-Through Protection – The shoot-through protection feature of this IC identifies the state in which both the upper and lower portions of a half bridge are ON at the same time. Shoot through must be avoided, for if it were to occur, it would short the supply to ground, overload the circuit and destroy the FETs. Consequently, a ‘dead time’ is programmed to allow a FET to turn fully off before its companion FET is turned on. During dead time, inductive winding currents continue to flow, or commutate, through internal or external reverse biased diodes. Fault status

indication and current level monitors are provided directly to the controller. Output currents are measured using an innovative low-loss technique discussed in a later section. The SA306-IHZ also offers superior thermal performance with a flexible footprint.

Controlling Brushless Motor Drivers – Most brushless motor drivers are controlled by microcontrollers or some other intelligent system. A number of manufacturers including Analog Devices, Freescale, Microchip and Texas Instruments market microcontrollers for motion control – and more specifically for driving brushless motors.

Choosing a Brushless Motor – Although there are a number of sources for assistance in choosing a motor, brushless or otherwise, a good starting point is Reference 2. As the author points out, choosing a motor requires looking at a whole list of issues including efficiency, torque, power reliability and cost.

What can be said categorically is that a brushless permanent magnet motor is the highest performing motor in terms of torque versus efficiency. Also all three stator windings can be controlled which is not the case in a traditional DC motor where commutation relies on brushes.

SENSOR VERSUS SENSORLESS COMMUTATION

Hall Sensors are not required in sensorless commutation. Instead the instantaneous position of the rotor relative to the stator is determined by the Back EMF (BEMF) developed in the stator windings. The absence of both the Hall Sensors and the attendant wiring lowers the motor's cost and increases reliability, though deriving the lost information from the BEMF requires somewhat more complex control. This approach is attractive in applications such as refrigeration or HVAC systems which generate heat that could accelerate failures of the Hall Sensors.

On the other hand, starting presents a problem in sensorless commutation simply because there is no BEMF when the motor is at rest. Secondly, abrupt changes in the motor load can cause a BEMF drive loop to go out of synchronization. Central to both sensorless- and sensor-based control systems is the presence of pulse width modulation (PWM) which is discussed in the Appendix.

CYCLE BY CYCLE CURRENT LIMITING – THE FUNDAMENTALS

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the in-rush current must be considered when selecting a proper drive. For example, a motor that requires 1 A when running at constant speed, might require a drive that can deliver well over 10 A PEAK in order to survive the inrush condition at startup. But as this discussion will make clear, this is not the case when using the SA306-IHZ.

Depicted in Figure 3a is the behavior in a traditional motor where there is no cycle-by-cycle current limit. (This is discussed in more detail in the Appendix)

In this case, when the rotor is not turning (no BEMF), the current is limited only by the resistance of the rotor of the motor plus any series resistance that may be present. As the motor accelerates, the back EMF builds up, gradually reducing the current so that it diminishes to the steady-state current.

Figure 3 illustrates motor behavior when cycle-by-cycle current limit is applied at start-up. In this case, the current is limited by circuitry within the SA306-IHZ – not by the impedance of the rotor. As the motor reaches its steady-state speed, the current tails off.

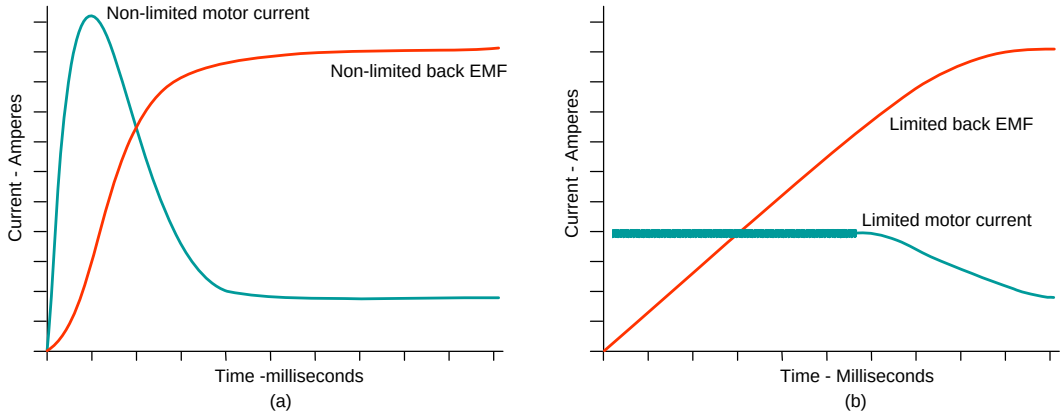


Figure 3. Motor Current Behavior at Startup – (a) Without cycle-by-cycle current limit. (b) With cycle-by-cycle current limit.

CYCLE-BY-CYCLE CURRENT LIMIT BEHAVIOR

Shown along the top of Figure 4 is the cycle-by-cycle behavior of the PWM pulse train applied to the SA306-IHZ by the microcontroller. The motor current is shown in blue at the bottom of the illustration. Outlined in red, and superimposed over the current waveform, is the actual PWM pulse train ('PWM output') delivered by the FETs which has, in effect, been modulated by the current flow. It shuts off the output pulse should the current exceed the 'current limit' set externally by the user.

1st Pulse – In the case of the 1st PWM pulse, no current limiting occurs because the pulse ends before the rising current reaches the current limit threshold. At the end of the 1st pulse there is a short decay before the PWM pulse turns on once more and the current resumes its rise. Note that because current cannot change instantaneously in an inductive reactance, which is, in fact, what the rotor of the brushless motor is, the current value, unlike the PWM voltage, is always continuous.

2nd Pulse – In the case of the second PWM pulse, the current reaches the limit value before the PWM input pulse ends. Consequently, the PWM output pulse is shut off early in its cycle. Then the motor current decays until the third pulse is applied which once again causes the current to rise.

Subsequent pulses – The behavior just described continues until the back EMF rises to the point where the current falls below the current limit threshold. This occurs as the motor approaches its operating speed and the current descends to its steady state value, as depicted in Figure 3b. The ratio of the peak-to-average motor current depends on the inductance of the motor winding, the back EMF developed in the motor, mechanical loading of the systems and the width of the pulse.

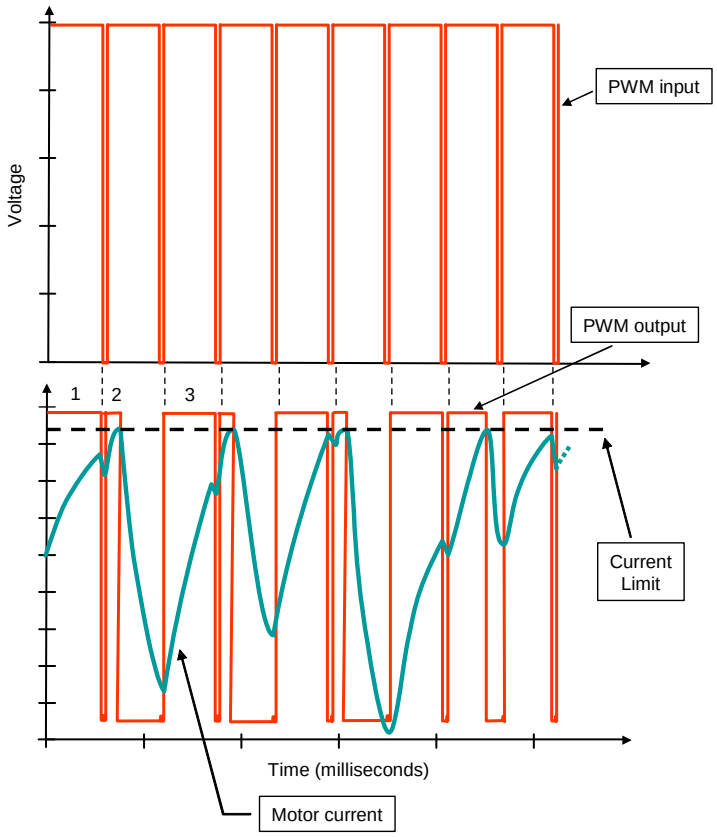


Figure 4. Cycle by Cycle Current Limit

CONTROL AND SENSE ARCHITECTURE

As depicted in Figure 5, the output current of the upper output FET U14 for OUT A is continually measured, (The same occurs for the corresponding output FETs for OUT B and OUT C). The output of the current sense circuit is applied to a current mirror comprising U1, U2 and U3 which develops a voltage across the external current limit resistor. This voltage is compared with the current limit threshold by Comparator U6.

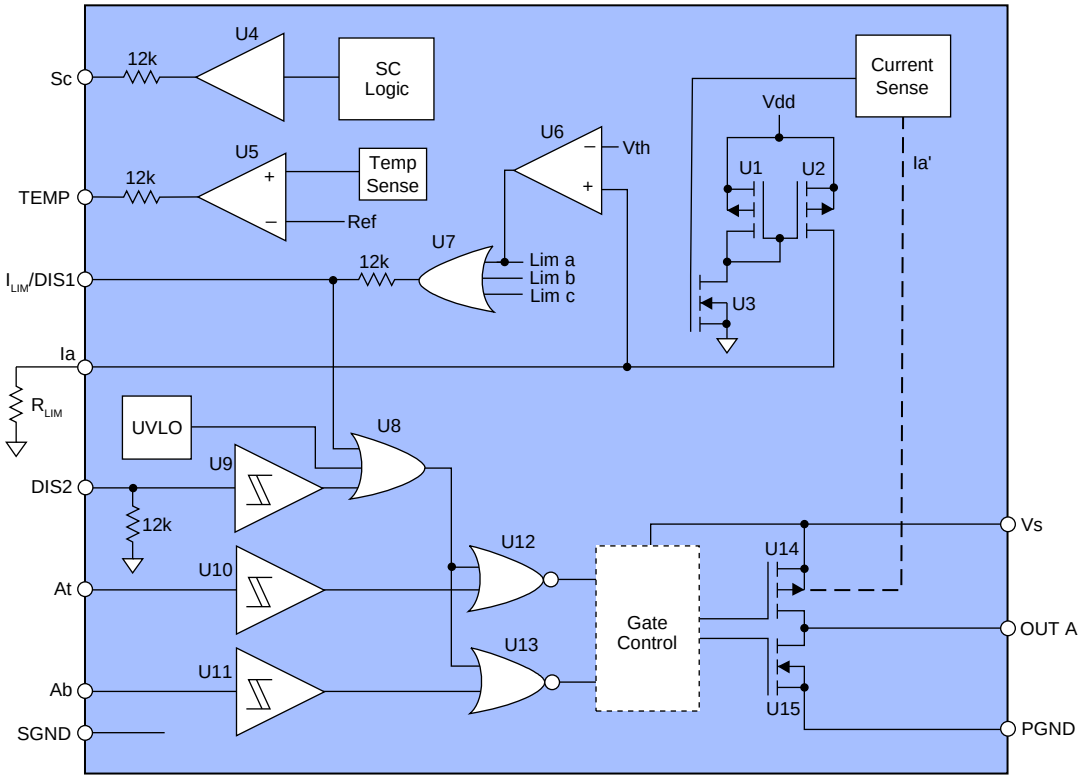


Figure 5. Control and Sense Architecture

Disabling Circuitry – If the voltage applied to the plus terminal of comparator U6 exceeds the current limit threshold voltage (Vth), all three outputs OUT A, OUT B and OUT C are disabled. The disabling path is via gates U7 and U8 and gates U12 and U13. Once the voltage applied to Comparator U6 falls below the Vth threshold voltage, and the disabled top side input to the gate control goes low, the output stage will return to an active state on the rising edge of any top side input command signal (At, Bt, or Ct). Note that the corresponding disable signals from phases B and C are also applied via gate U7 and their behavior is exactly the same as is the case for OUT A. Also the ILIM/DIS1 goes HIGH when any of the three current sense circuits detects an overcurrent situation. The cycle-by-cycle current limit feature of the SA306-IHZ will reset each PWM cycle. Thus the PEAK current is limited in each phase during each PWM cycle, as illustrated in Figure 4. Notice also that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal because this event is governed by the intersection of the rising current with the current limit – not the PWM duty cycle. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a 'sub-cycle oscillation'. This oscillation can be viewed with an oscilloscope by applying a probe to pin 7, I_{LIM}/DIS1.

Undervoltage Lockout – See Table 1 and Page 7.

Limitations at High and Low Speeds – Input signals applied to the PWM and commanding a 0%- or a 100%-duty cycle, may be incompatible with the current limit feature due to the absence of rising edges of At, Bt, and Ct – except at instances when the rotation of the motor requires the output FETs to change states. At high motor speeds, this may result in poor performance and significantly increased torque ripple. Whereas at low motor speeds the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge that would change the state of the output FETs and normally reset the current limit latch.

Disabling Cycle-by-Cycle Current Limit – The current limit feature may be disabled by pulling the I_{LIM}/DIS1 pin to GND. The current sense circuitry identified in Figure 5, will continue to provide top FET output current information.
External Current Control Options – Typically the current sense pins source current into grounded resistors which provide voltages to the current limit comparators, as shown in Figure 1. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically by the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when a low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection. This is discussed in detail under 'Current Sense – An Advantage'.
Three Degrees of Freedom – The applied voltage, the switching frequency and the PWM duty cycle are three crucial parameters that can be programmed independently. How these variables are selected will affect the behavior of the motor with regard to how fast it will accelerate, and consequently how fast its speed and torque will rise.

CONTROL AND SENSE PINS

A summary of the control and sense pins, and their functions, is supplied in Table 1.

Table 1. Control and Sense Features

Nomenclature	Pin #	Function	Description	Remarks
DIS2	23	Control	When a HIGH is applied to this Schmitt triggered logic level, it places OUT A, OUT B, and OUT C in a high impedance state.	Pin DIS2 (23) has an internal 12kΩ pull-down resistor connected to ground and therefore may be left unconnected. (See Figure 5.)
I_{LIM}/DIS1	7	Control/Sense	Control: Pulling this pin to logic HIGH places OUT A, OUT B, and OUT C in a high impedance state. Pulling this pin to a logic LOW effectively disables the cycle-by-cycle current limit feature. Sense: This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature.	
SC	3	Sense	Goes HIGH if a short circuit is detected or an output occurs that is not in accordance with the input commands,	The SC signal is blanked for approximately 200 ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor, as shown in Figure 5.
TEMP	25	Sense	Goes HIGH if the SA306 die temperature reaches approximately 135ºC.	This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor. See Figure 5.

Nomenclature	Pin #	Function	Description	Remarks
UVLO (Under-voltage Lock Out)	None	Control/Sense	Disables all output FETs until V_S is above the UVLO threshold voltage which is typically 8.3 V.	See discussion in Section 3.4.
Vth	None	Control	If the voltage of any of the three current sense pins exceeds the current limit threshold voltage (Vth),which is typically 3.75 volts, all outputs are disabled. After all current sense pins fall below the Vth threshold voltage and the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (At, Bt, or Ct).	

FAULT INDICATIONS

In the case of either an over-temperature or short-circuit fault, the SA306-IHZ will take no action to disable the outputs. However, the SC and TEMP signals can be fed to an external controller, as depicted in Figure 6, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA306-IHZ. Figure 6 depicts an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the DIS2 pin HIGH. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead. In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent I_{LIM}/DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA306-IHZ will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations that can greatly reduce the life of the device.

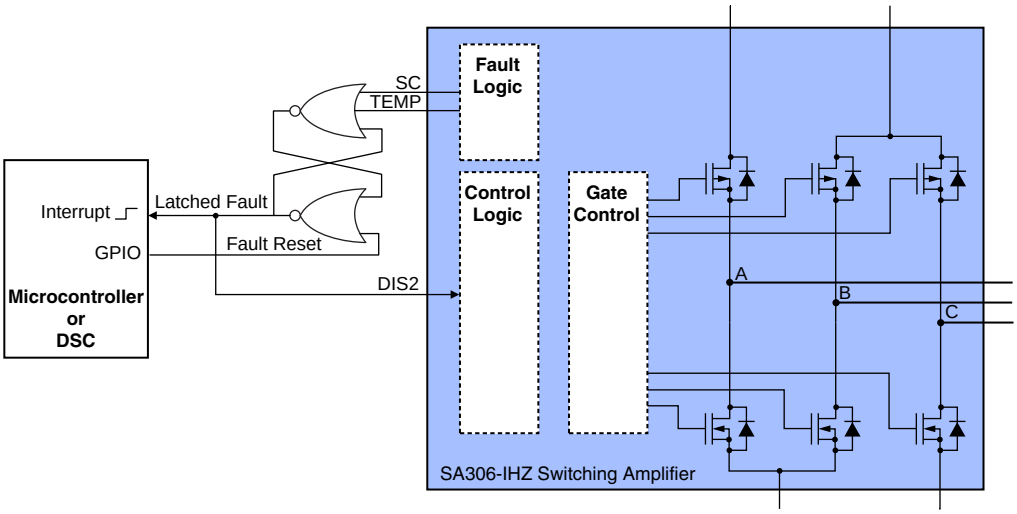


Figure 6. External Latch Circuit

UNDER-VOLTAGE LOCKOUT

Without sufficient supply voltage, the SA306-IHZ control circuit cannot sufficiently drive the gates of the output FETs. The undervoltage lockout condition results in the SA306-IHZ unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the specification table in the Data Sheet[1]. There is no external signal indicating that an undervoltage lock-out condition is in progress. The SA306-IHZ has two V_S connections: one for phase A, and another for phases B & C. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

CURRENT SENSE — AN ALTERNATIVE

External power shunt resistors are not required with the SA306-IHZ. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic, as depicted in Figures 1 and 5. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. As an alternative the currents Ia, Ib, and Ic can be fed to a single resistor and the voltage developed monitored by a high-impedance A/D converter, as shown in Figure 7.

As depicted in the 'Current Sense' plot on page 4 of the SA306-IHZ product data sheet, the maximum current per phase is slightly less than 2 milliamperes. Consequently, choose a resistor that will develop the voltage appropriate for the A/D Converter chosen. The full scale voltage will be the voltage developed across the resistor by the sum of the three currents — 6 milliamperes. Also allow a headroom of approximately 0.5 V.

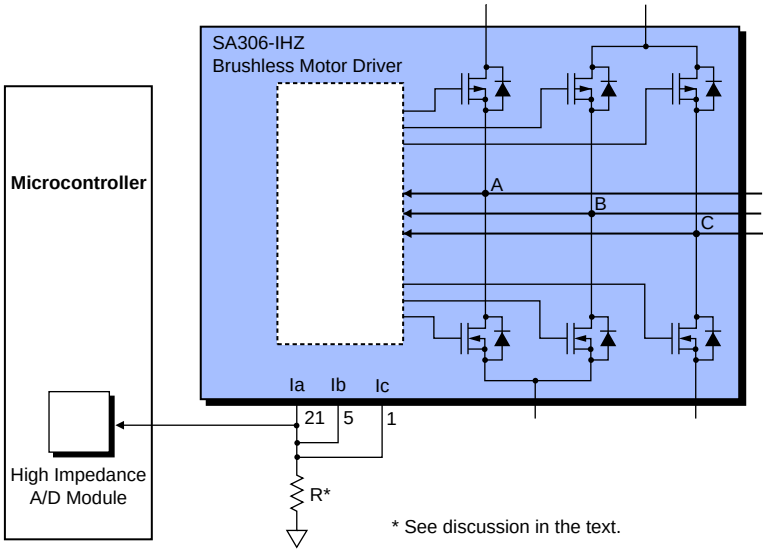


Figure 7. Current Monitoring Circuit

EXTERNAL FLYBACK DIODES

External fly-back diodes (D1 through D6), depicted in Figure 8, will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

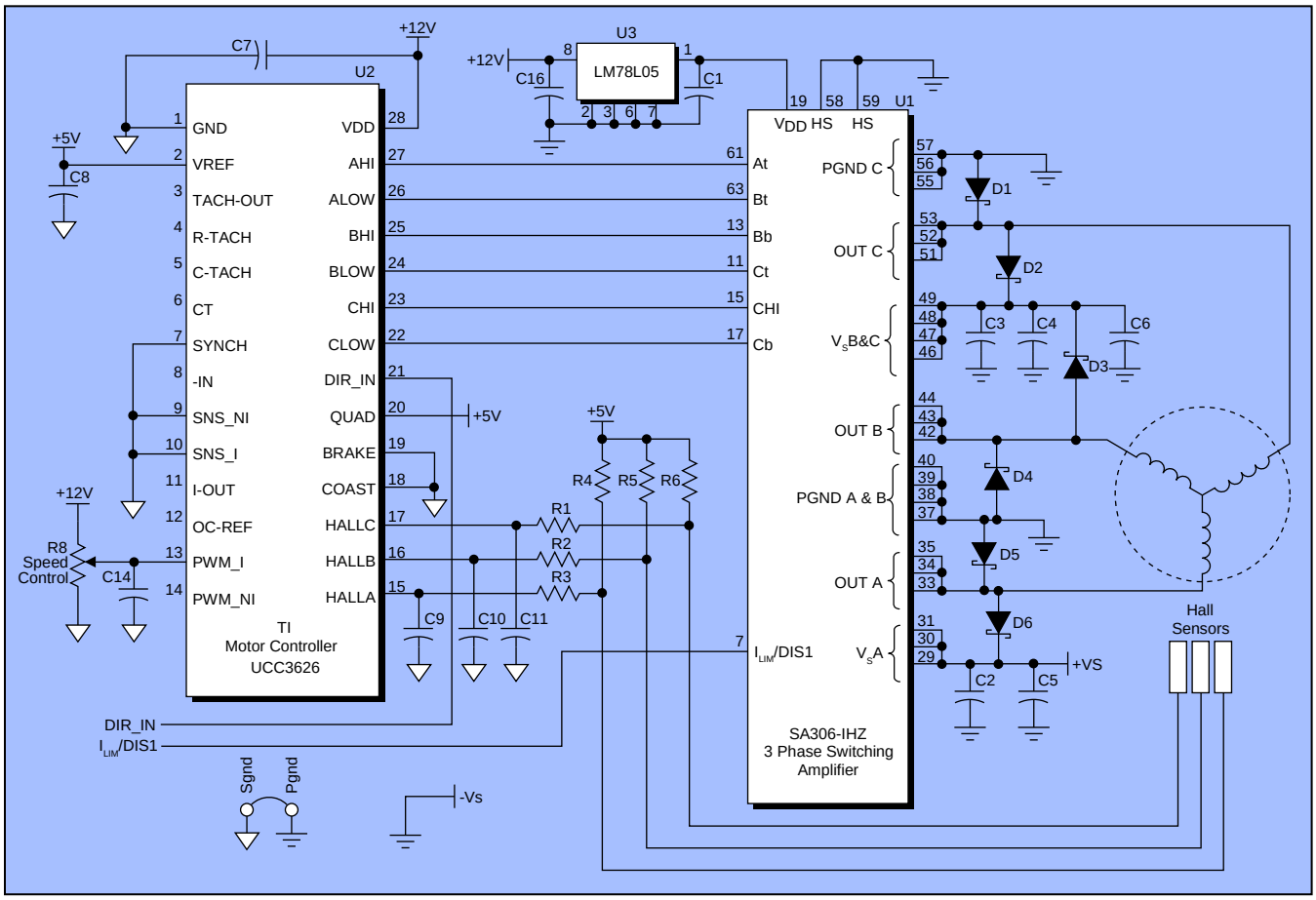


Figure 8. Three-Phase Motor Drive Circuit

A SPECIFIC EXAMPLE

Begin by choosing a motor that will exhibit the mechanical performance required — which is to say the torque, the efficiency, and other issues that will fulfill the motor drive requirements of your system. We have chosen as our example a low-inertia, brushless motor that delivers 557 mNm of torque at 2000 rpm. We selected a Maxon EC Flat motor www.maxonmotor.com. The characteristics of the windings of this motor are that any stator-winding pair exhibits a resistance (Rm) of 2.3 ohms and an inductance (Lm) of 2.5 millihenries. The torque constant (Kt) of the motor is 217 mMm oz-in/A.

DEMONSTRATION BOARD FOR THE SA306-IHZ

It is recommended that the designer acquire the DB64 Demonstration Board[3] and assemble a prototype. In the DB64 the SA306-IHZ input PWM control is achieved by means of a Texas Instrument on-board UCC3626 PW microcontroller[4]. The DB64 is designed to demonstrate the capabilities of the SA306-IHZ as a 3-phase brushless DC motor driver IC. From there one can easily convert the circuit developed with the DB64 Demonstration Board into a circuit similar to the one shown in Figure 8 which can serve as the base circuit for a production version.

LAYOUT CONSIDERATIONS

A simple two-layer printed circuit board construction is sufficient because of the convenient pinout of the SA306-IHZ PowerQuad package. Input signals are routed into one side of the SA306-IHZ package and high-power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise might corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. Use 1 nF capacitors with excellent high frequency characteristics to bypass the V_S motor supplies at each phase as well as switching grade electrolytic capacitors. The six 100 V Schottky diodes (D1 – D6) conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA306-IHZ. These diodes are rated for 5 A continuous. Mount them close to the SA306-IHZ to reduce inductance in the commutating current loop. For applications with continuous currents less than 5 A, the Schottky diodes may not be necessary, but one must consider the higher forward voltage internal body diodes and the associated power dissipation that results.

Output Traces – Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

Bypassing – The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25 µF per ampere of output current should be placed near the SA306-IHZ as well. Capacitor types rated for switching applications are the only types that should be considered. Note that phases B & C share a V_S connection and the bypass recommendation should reflect the sum of B & C phase current. The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1 µF to 0.47 µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

Ground Connections and Ground Planes – S_{GND} and P_{GND} pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back-to-back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections. Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

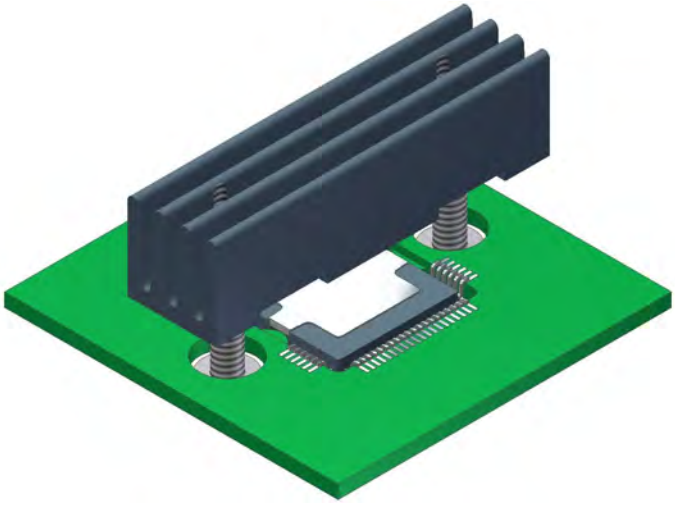
Table 2. Parts List for Figure 7

Reference Designation	Description
R1, R2, R3	470 Ω
R4, R5, R6	1 kΩ
R8	20 kΩ potentiometer (to control the PWM duty cycle)
R9, R10, R14, R15, R16, R17	5 kΩ
C1, C7, C8	1 µF
C2, C3, C4, C5, C6	1 nF
C9, C10, C11	2.2 nF
C14, C16	0.1 µF
D1, D2, D3, D4, D5, D6	PDS5100
U1	Apex Precision Power SA306-IHZ or SA306A-FHZ
U2	Texas Instrument UCC3626
U3	LM78L05

POWER DISSIPATION

The thermally-enhanced package of the SA306-IHZ allows for several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents.

Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs. The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA306-IHZ. Applications vary widely and various thermal techniques are available to match the required performance. The patent pending mounting technique shown in Figure 9, with the SA306-IHZ inverted and suspended through a cutout in the PCB, is adequate for power dissipation up to 17 W with the HS33 (a 1.5-inch long aluminum extrusion with four fins). In free air, mounting the PCB perpendicular to the ground, so that the heated air flows upward along the channels of the fins can provide a total $\theta_{J\text{-}A}$ of less than 14º C/W (9 W max average PD). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a $\theta_{J\text{-}A}$ of 16.66º C/W (7.5 W max average PD). For applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance. Also see References 5 and 6.



Patent Pending

Figure 9. HS33 Heatsink

Appendix

A Brief Overview of PWM

The first pulse width modulation (PWM) ICs appeared on the market some 40 years ago. So the concept of PWM is at least as old. Though the earliest applications were in switching power supplies, it was not much later that the technique was first employed to drive brushless motors. The principal benefit of PWM as a control technique becomes clear by examining Figure A1. The traditional linear power delivery technique for limiting power simply employs a variable resistance as depicted in Figure A1(a). When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded the pass element resistance again approaches infinity and losses again approach zero. However, the disadvantage of the linear circuit becomes clear in the midrange when the output level is in the vicinity of 50%. At these levels the resistance of the pass element is equal to the load resistance which means the heat generated in the amplifier is equal to the power delivered to the load! In other words, a linear control circuit exhibits a worst case efficiency of 50% when driving resistive loads at midrange power levels. What's more, when the load is reactive, this efficiency drops even further.

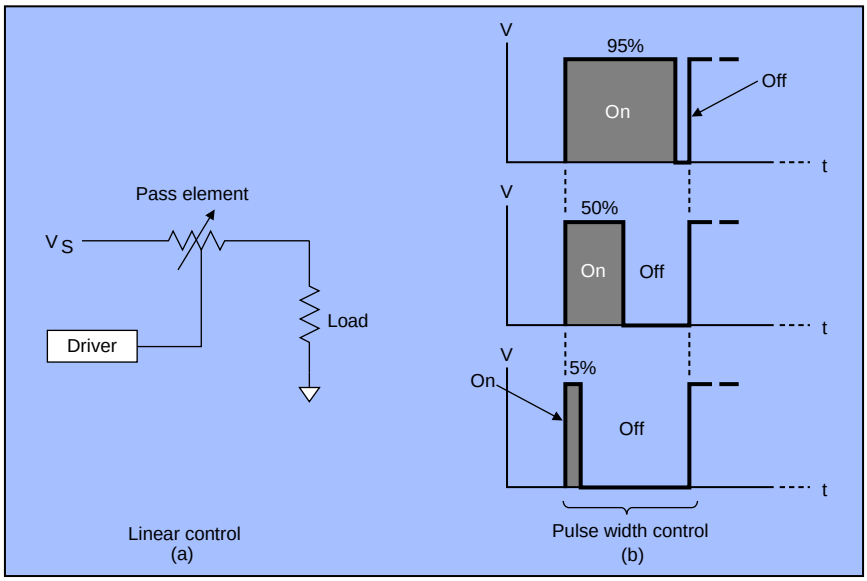


Figure A1. PWM versus Linear Control – PWM control in (b) exhibits far lower losses than the traditional linear control technique in (a)

Now consider PWM operation as depicted in figure A1(b). In a PWM control system an analog input level is converted into a variable-duty-cycle switch drive signal, The process of switching from one electrical state to another, which in this case is simply between OFF and ON, is called ‘modulation’, which accounts for why this technique is called ‘pulse width modulation’. Beginning at zero duty cycle, which is to say OFF all the time, the duty cycle is often advanced as the motor begins to rotate, until it is running at the speed and/or the torque required by the application. In the case of a PWM control circuit, the rather negligible losses are primarily due to the ON resistance of the switching FET and the flyback diode which is why efficiencies as high as 80% to 95% are routine. However, at high switching frequencies the energy required to turn the FETs on and off can become significant.

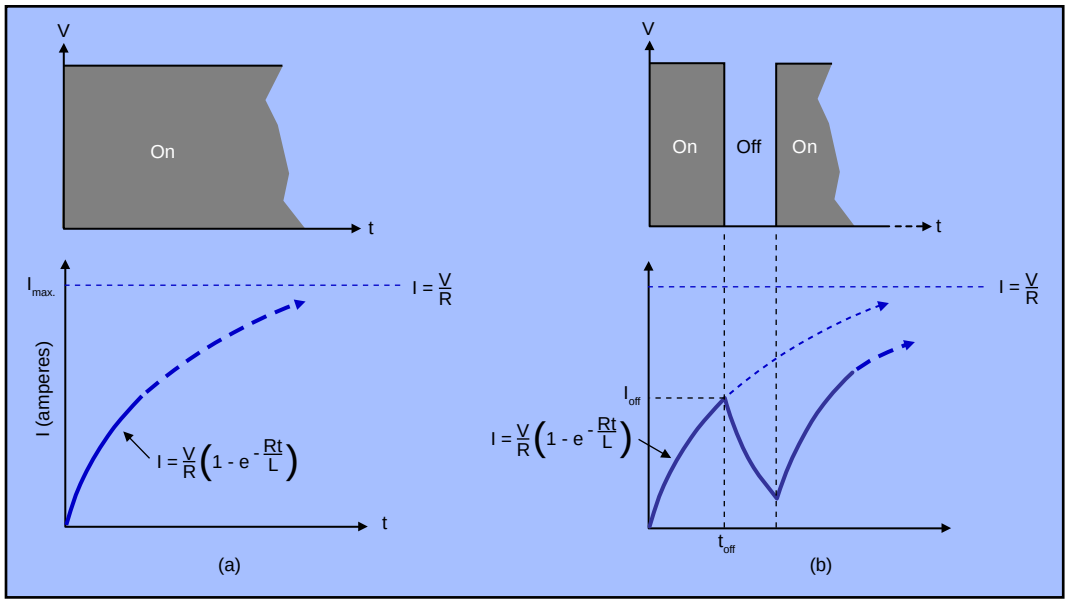


Figure A2. Linear versus PWM — Current behavior with a steady-state excitation in (a); Current behavior with PWM excitation in (b)

In addition to enhanced efficiency, PWM can play additional roles which include limiting the start-up current, controlling speed and controlling torque. The optimum switching frequency will depend on inertia and inductance of the brushless motor chosen and the application. The choice of the switching frequency affects both losses and the magnitude of the ripple current. A good rule of thumb is that raising the switching frequency increases the PWM losses. On the other hand, lowering the switching frequency limits the bandwidth of the system and can raise the heights of the ripple current pulses to the point that they become destructive or shut down the brushless motor driver IC. The ripple current pulses are depicted in Figure A2(a) and are discussed below.

BRUSHLESS MOTOR BEHAVIOR – AN OVERVIEW

One of the most critical moments with regard to a brushless motor – also true for a motor with brushes – is when power is first applied while the motor is at rest. At this time the rotor is stationary and is delivering no 'back EMF' (V_{BEMF}). V_{BEMF} can be expressed as:

$$V_{BEMF} = (K_b)(\text{Speed}) \qquad \text{(Equation1)}$$

Where: K_b = voltage constant (volts/1000 RPM)
Speed = revolutions per minute (expressed in thousands)

Once a voltage is applied to the motor, the rotor begins turning, generating a V_{BEMF} governed by (Equation 1). Ignore for the moment that the plan is to drive the motor with a PWM source, and assume the motor is driven by a steady-state voltage, then we can express the current by this equation:

$$I = [(V-V_{BEMF})/R_m][1-e^{-Rmt/Lm}] \qquad \text{(Equation 2)}$$

Where: V = the applied voltage
V_{BEMF} = back EMF
R_m = stator resistance (winding pair)
L_m = stator inductance (winding pair)

Note that in (Equation 2), the current (I) at any moment is a function of both the back EMF (V_{EMF}) and the time (t). The current when the motor is stopped (V_{BEMF} = 0) is illustrated in Figure A2(a) and is a familiar waveform for characterizing the current in any L-R circuit with its rise time governed by the time constant L/R.
Now let's exchange the steady-state excitation voltage for a PWM source, as shown in Figure A2(b). The current rises until the first ON pulse ends; when the voltage abruptly falls to zero at the end of the first applied voltage pulse, the current begins to decay towards zero. However, the next pulse will again drive the current upwards, and so forth, so that the current continues to rise. As the motor accelerates, the current waveform will exhibit a sawtooth profile. This sawtooth characteristic is also known as ripple. Because torque is directly proportional to current, the sequence of rising current pulses drive the motor, which develops a corresponding torque that accelerates the motor. But this is not so in the case of cycle-by-cycle current limit. Because in this case the current rise ceases immediately if the current reaches the limit value during any PWM pulse interval.

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Techniques for Stabilizing Power Operational Amplifiers

1.0 INTRODUCTION

It is unlikely that a power op amp would always be employed to drive a purely resistive load. For if that were the case, stability would never become a problem. On the other hand, a load which is largely capacitive does present stability issues as will become clear in this Application Note. In a pure capacitor, the voltage lags the charging current by 90 degrees, so there is a large phase delay in the loop response of a feedback circuit. Such a phase delay can be a significant contributor to instability.

Let's get started by considering any multistage amplifier. It will begin to exhibit a roll off in open loop gain (A_{OL}), as well as an increase in phase delay at higher frequencies because of the low-pass filters that are formed by nodes with finite source impedances driving capacitive loads within the amplifier stage[1]. So a load that is largely capacitive, together with the capacitance within a multistage amplifier, can bring about instability since the phase lag may be approaching, and perhaps exceed 180 degrees. It is this phase delay that is a key contributor to instability. When instability occurs, it can transform a power amplifier into an oscillator, inadvertently, and the device is likely to become quite hot and fail in as little as one second.

In the discussion that follows, there are some simple techniques for managing phase and gain relationships to maintain a stable circuit.

1.1 LOOP STABILITY VERSUS NON-LOOP STABILITY

In this Application Note we discuss Loop Stability. Whereas 'Non-Loop Stability' that denotes issues such as layout, power-supply bypassing and proper grounding are discussed in Reference 2. In this Application Note we will examine:

- Why capacitive loads create stability problems in standard op amp circuits.
- Closed loop gain (1/ß) and open loop gain (AOL) and their relationships to stability.
- How capacitors impact the open loop gain (AOL) curve
- Three ways to adjust the closed loop gain (1ß) and the open loop gain (AOL) responses to regain phase margin and stability, along with the advantages and disadvantages of each technique.

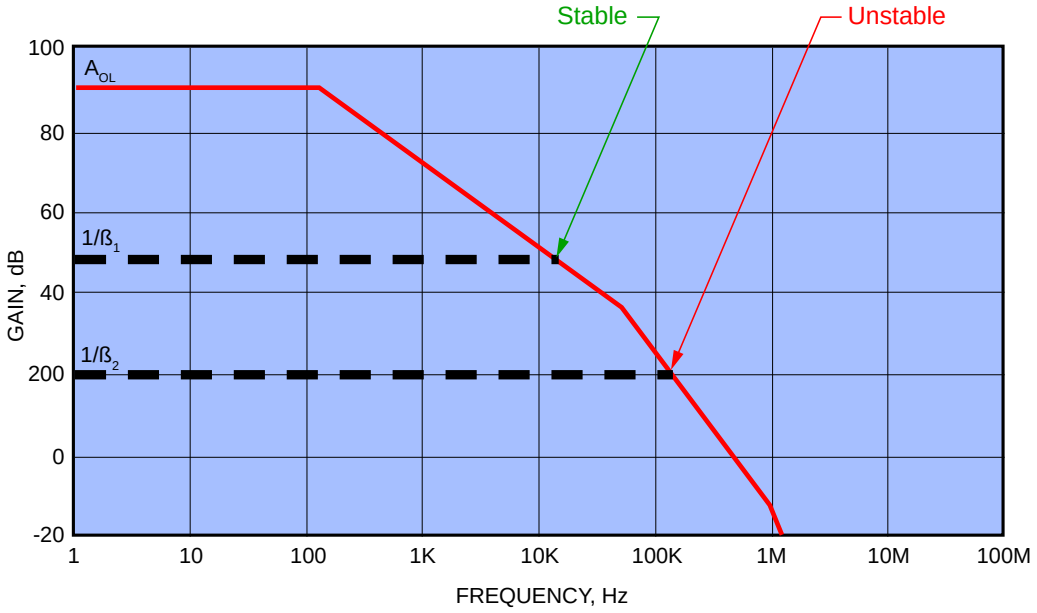


Figure 1. Stable or Unstable? − As we explain in this Application Note, modifying the closed loop gain (1/ß) is one of several effective ways of achieving stable operation.

Bode Plots in a nutshell

A Bode Plot of a power amplifier open loop gain (A_{OL}) response is usually a graph of the log of the magnitude plotted as a function of the log of the frequency, as depicted below. The magnitude axis is usually expressed in decibels. This transforms multiplication into a matter of simply adding vertical distances on the plot.

With this examination of the multistage amplifier, as discussed in Section 1.0, the open loop gain (A_{OL}) response is comparable to a single-pole low pass filter, as depicted in Figure 1.

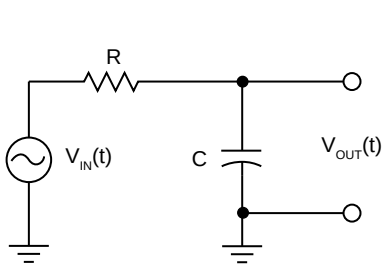
The Bode Plot of amplitude can be approximated by straight lines, as shown at the lower right. Note that as the straight-line approximation approaches the corner frequency the true value, shown by the dotted line, departs from the straight-line approximation and is actually 3.01 dB below the junction of the two intersecting straight line segments.

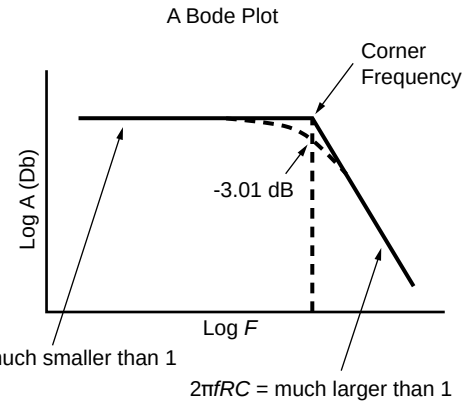
Note that for corner frequencies much lower than 1, the approximation is a straight line which covers the portion where the capacitive reactance is large. For frequencies much larger than the corner frequency the curve is approximated by the straight line descending at rate of 20 dB per decade. This is due to the diminishing capacitance reactance at higher frequencies.

One could also prepare a Bode Plot for the log of the phase relationship between the input and output, but this is dispensed with for the analysis employed in this Application Note.

Op amps often exhibit more than one pole in their open loop gain (A_{OL}) Bode Plots.

Note that at the first corner frequency or pole there is a 90-degree phase shift. If there is a second pole the phase shift becomes 180 degrees above that frequency.





$$V_{OUT}(t) = \frac{\frac{1}{j2\pi fC}}{\frac{1}{j2\pi fC} + R} V_{IN}(t)$$

$$V_{OUT}(t) = \frac{1}{(1 + j2\pi fRC)} V_{IN}(t)$$

$$f = \frac{1}{2\pi RC} \triangleq \text{“Corner Frequency or Pole”}$$

2.0 EVOLUTION OF AN OPERATIONAL AMPLIFIER

Reviewing the evolution of an op amp is useful because it aids the understanding of the stability techniques.

This example begins with an open loop amplifier (A_{OL}), with a gain as depicted in Figure 2(a).

So the open loop gain is simply:

$$V_{OUT} = A_{OL} V_{IN} \qquad (1)$$

Then add a summing point at the input as shown in Figure 2(b).

To convert the open loop amplifier into an operational amplifier we feed back a portion of the output which is $ßV_{OUT}$, as shown in Figure 2(c). Then label the inputs and outputs so that the equation for V_{OUT} can be written by inspection:

$$V_{OUT} = A_{OL}(V_{IN} - ßV_{OUT}) \qquad (2)$$

or:

$$V_{OUT}(1 + A_{OL}ß) = A_{OL}V_{IN}$$

so that the closed loop gain A_{CL} is :

$$A_{CL} = \frac{V_{OUT}}{V_{IN}} = \frac{A_{OL}}{1 + A_{OL}ß} \qquad (3)$$

Because A_{OL} is large compared with 1 therefore $A_{OL}ß$ will also be large compared with 1. Then the denominator $1 + A_{OL}ß$ is equal, approximately, to $A_{OL}ß$ and equation (3) becomes simply:

$$A_{CL} \approx 1/ß \equiv \text{Closed loop gain} \qquad (4)$$

Key relationships . . .

A_{OL}	=	Open Loop Gain
$1/ß$	=	Closed Loop Gain
$A_{OL} - 1/ß$	=	Loop Gain − the signal propagating around the loop and available to reduce errors and non-linearities.

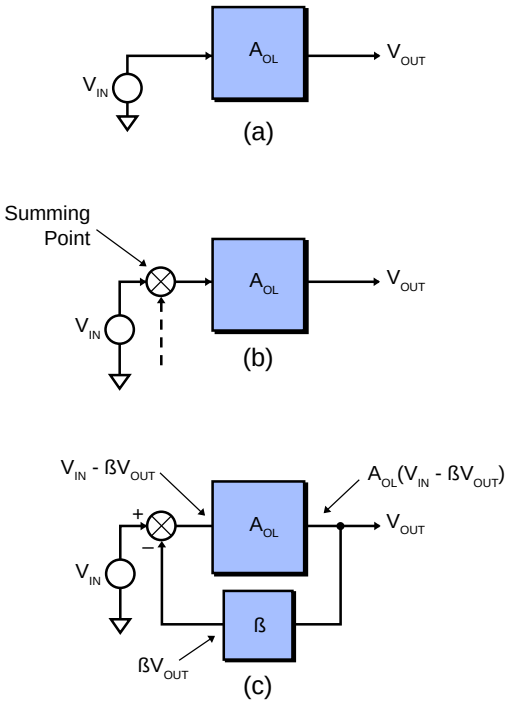


Figure 2. Evolution of an Op Amp

2.1 A CLOSER LOOK AT ß

Beta (ß) is the fraction of the output that is fed back to the input. In Figure 3(a) it is thereby given as:

$$V_{FB} = \frac{R_1}{R_1 + R_F} V_{OUT} \qquad (5)$$

$$V_{FB} = ß\, V_{OUT} \qquad (6)$$

Where: $ß = \frac{R_1}{R_1 + R_F}$

Or the non-inverting closed loop gain 1/ß is:

$$\frac{1}{ß} = \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1} \qquad (7)$$

(Keep in mind that the current flowing into the two inputs is virtually zero.) If ß comprises solely resistors R_I and R_F then the closed loop gain (1/ß) line will plot as a horizontal straight line on a bode plot.
This is depicted in Figure 1 in which the $1/ß_1$ and $1/ß_2$ lines, which are the closed loop small signal gains, are depicted as a constant and frequency independent.

However, if Z_I and Z_F are capacitors or inductors − or some combination of capacitors, inductors and resistors − then Z_I and Z_F are functions of frequency:

$$V_{FB} = \frac{Z_I(f)}{Z_I(f) + Z_F(f)} V_{OUT} \qquad (8)$$

This means the Closed loop gain (1/ß) line does not plot as a straight line on a bode plot.

2.2 HOW AN OP AMP BEHAVES AS THE SIGNAL FREQUENCY RISES

This section depicts the fact that if there is a critical frequency (F_{CL}) at which the loop gain (A_{OL} - 1/ß) becomes zero, then the operational amplifier simply degenerates into an open loop amplifier with an open loop gain of A_{OL}. If that occurs the amplifier no longer behaves as an operational amplifier and its benefits simply vanish.
This is depicted in Figure 4 in which the closed loop (1/ß) line is a constant – which means the components of ß are independent of the frequency – or purely resistive. Note how the 1/ß value subtracts from the open loop gain (A_{OL}) at low frequencie. But once the A_{OL} line reaches the frequency F_{CL}, the loop gain (A_{OL} - 1/ß) becomes zero. So for frequencies above F_{CL}, the op amp becomes an open loop amplifier with a gain of A_{OL}.
Is the power amplifier unstable? That depends on the phase relationship between the input and output for the amplifier for frequencies of F_{CL} and above, as discussed in Section 2.3 that follows.

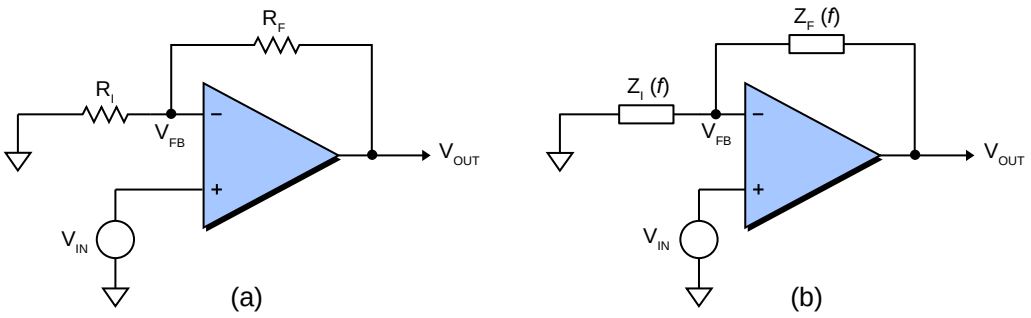


Figure 3. Beta – Frequency Independent (a) and Frequency Dependent (b)

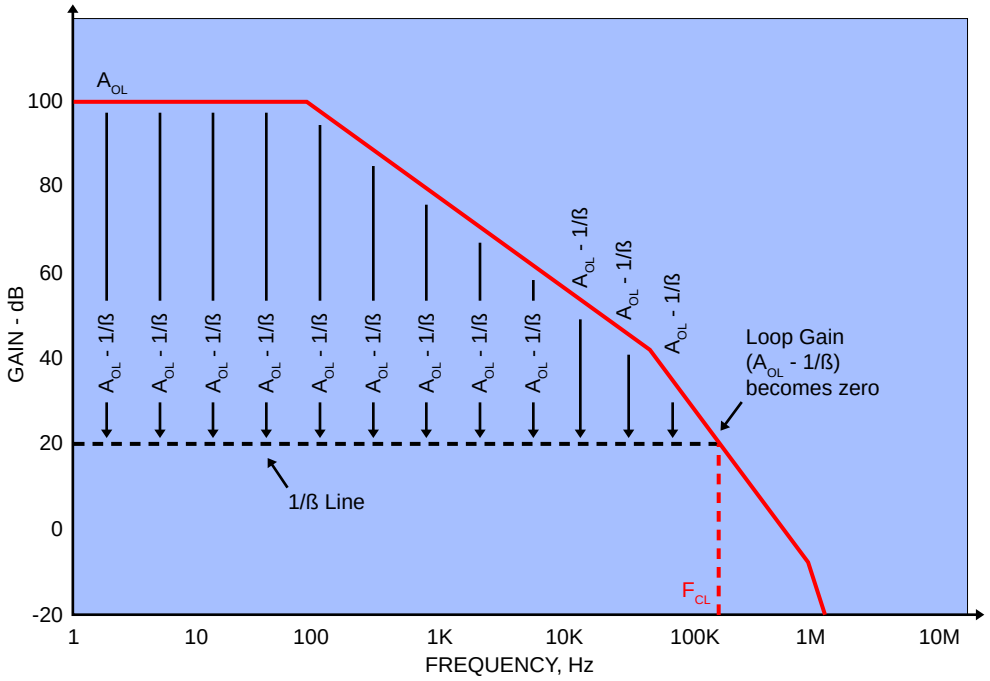


Figure 4. Closed Loop Constant – When the Loop Gain runs out of gas

2.3 PHASE MARGIN

Oscillation can occur if at a phase shift of 180 degrees the loop gain (1/ß) is one (0dB), or more. Consequently, the 'Phase Margin' is defined as how close the phase shift is to a full 180 degrees when the loop gain is 0dB, also called "The Point Of Intersection". A good rule of thumb is to design for 135 degrees of phase shift which constitutes a phase margin of 45 degrees. This will allow for events that occur during power up and power down – as well as other transient conditions which may cause changes in the open loop gain (A_{OL}) curve that could initiate transient oscillations.

Note that it is the included angle formed at the Point Of Intersection (closed loop gain = 0dB) which denotes stability (20dB/decade) or instability (40dB/decade, or more).

2.4 USABLE BANDWIDTH

The usable bandwidth is usually defined as the frequency at which the closed loop gain (A_{OL}-1/ß) falls to 20dB. The reason is that above this frequency the error rises above 10% so that the performance of the op amp is degraded significantly.

2.5 A FIRST ORDER CHECK FOR STABILITY

As we have explained, the loop gain (1/ß) is the amount of signal available for feedback to reduce errors and non-linearities. A first-order check for stability is to make sure that when the closed loop gain (1/ß) reaches the open loop gain (A_{OL}) line the phase shift is less than 180 degrees.

Shown in Figure 5 is a plot of an open loop gain A_{OL} which displays a descent rate of 20dB per decade at frequencies of approximately 100Hz to 80kHz. This denotes a phase shift of 90 degrees. At approximately 80kHz the descent rate changes to 40dB per decade. So above this frequency, the phase shift is 180 degrees.

Note that for a loop gain ($1/ß_1$) the plot intersects the open loop gain (A_{OL}) plot where its descent rate is 20 dB per decade. So this curve passes the first check for stability.

For a complete analysis we will need to check the phase shift of the open loop gain (A_{OL}) response over frequency. This is discussed in Section 4.

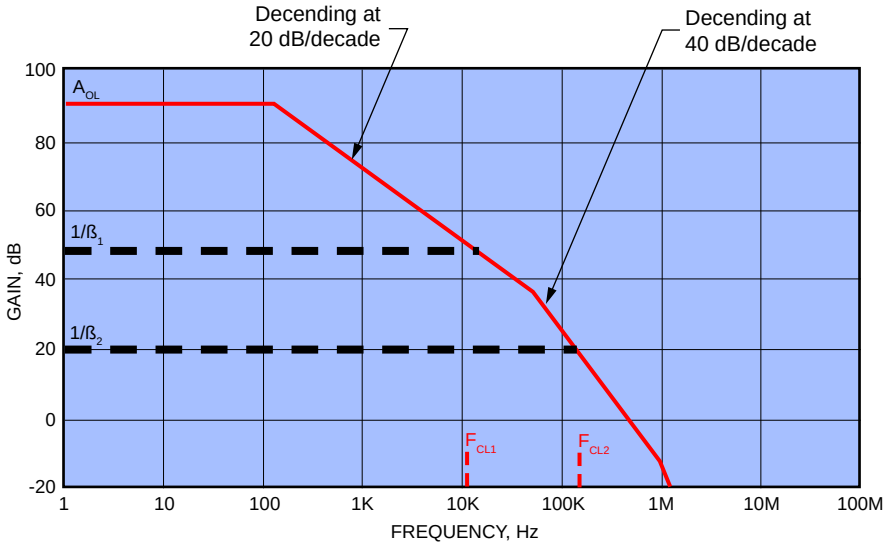


Figure 5. Stability Check – A first order check of stability

Note that the loop gain ($1/ß_2$) plot intersects the open loop gain (A_{OL}) plot where its rate of intersection is 40dB per decade. So this curve fails the first check for stability.

3.0 FOUR COMPENSATING TECHNIQUES – PHASE COMPENSATION

In most treatments of stability, phase compensation will never come up because most small signal amplifiers are internally compensated and therefore there is nothing that can be done externally to modify the amplifier. However, in almost every Apex Precision Power amplifier the phase compensation can be controlled by an external capacitance C_C that the user can select. This enables moving the first pole of the open loop gain (A_{OL}) plot left or right in frequency, as depicted in Figure 6. By raising the value of C_C, the open loop gain (A_{OL}) plot can be moved to the left and down so that what would otherwise be a problem pole − a descent at 40dB per decade − moves below 0dB. Therefore it is no longer a problem with regard to stability.

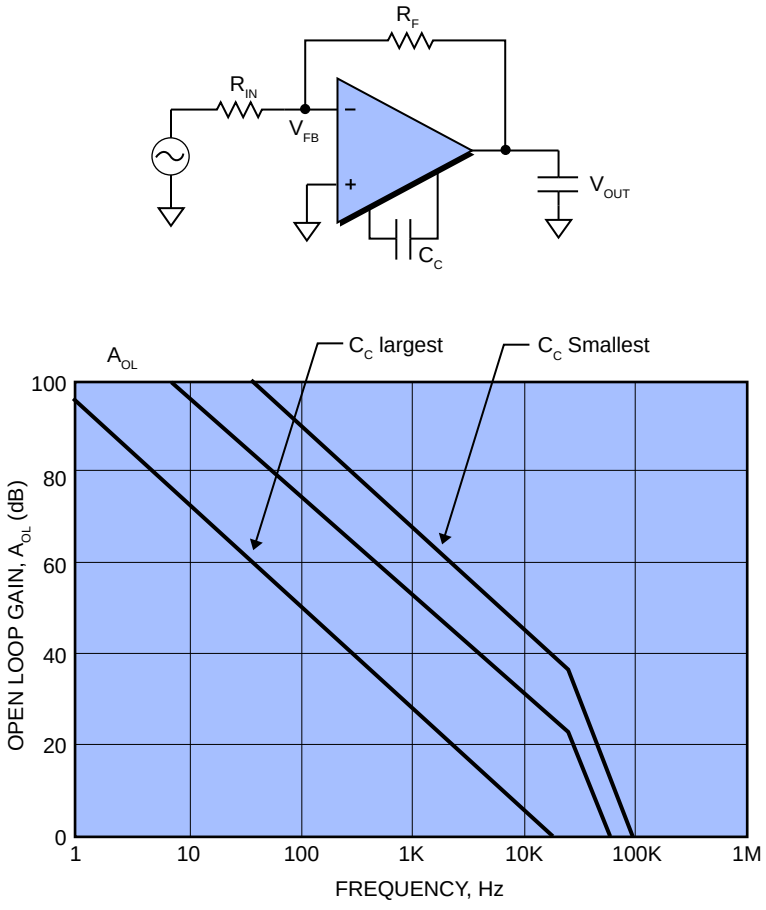


Figure 6. Phase Compensation

3.1 FEEDBACK ZERO COMPENSATION

As depicted in Figure 7, feedback zero compensation is a method of tailoring the op amp's performance for a given application. The goal is to alter the loop gain (1/ß) by adding a feedback capacitor C_F, placing a pole in the 1/ß plot so that it intersects the open loop gain (A_{OL}) line at 20db per decade instead of at 40dB per decade. The included angle of the intersection is now 20dB/decade. Hence it is stable. The usable bandwidth is approximately 10kHz.

This technique is very sensitive to the tolerances of the feedback because the loop gain (1/ß) plot is governed by the RC response of the feedback. Therefore the power amplifier is very susceptible to going in and out of stability

based on capacitor C_F, which may change in value with changes in temperature

To summarize, this compensation technique is easy to implement when the loop gain (1/ß) value is large. But the technique is somewhat sensitive to variations in component tolerances.

3.2 NOISE GAIN COMPENSATION

Figure 8 illustrates how noise gain compensation functions. This technique adds a parallel Z_I path through R_I and C_I, as shown in Figure 8. The objective with this technique is to close the loop gain early.

One way to view noise gain circuits is to view the amplifier as a summing amplifier. Consequently, there are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed via ground through the series combination of R_I and C_I. Since this is a summing amplifier, V_{OUT}/V_{IN} will be unaffected if we sum zero via the R_I-C_I network. However, in the small signal AC domain, we will be changing the loop gain (1/ß) plot of the feedback. Consequently, as C_I becomes a short as the frequency rises, and if $R_I << R_{IN}$, the signal gain will be set by R_F/R_I. Notice in Figure 9 that when the capacitive reactance of C_I is large, the loop gain ($1/ß_1$) line is governed by R_{IN}. However, when the capacitive reactance of C_I becomes small, then R_I supplants R_{IN} as the input resistor accounting for the shift to the loop gain ($1/ß_2$) line crosses the open loop (A_{OL}) line at 20dB per decade. The usable bandwidth is approximately 8kHz.

The noise gain technique is largely immune to component tolerance variations. However, it is only appropriate for non-inverting amplifiers, i.e., summing configurations, and it does sacrifice closed loop gain, and therefore loop bandwidth at higher frequencies.

3.3 ISOLATION RESISTOR COMPENSATION

Figure 10 illustrates isolation resistor compensation with resistor R_{ISO} connected in series with the load C_L. As depicted in Figure 11, the loop gain (1/ß) line, if uncompensated, would intersect the open loop gain (A_{OL}) line where the phase shift is 40dB per decade so that the circuit would be unstable. The resistor isolation compensation technique restores the 20dB per decade slope to the Bode Plot amplifier gain plot, as depicted by the red line in Figure 11, by inserting a resistor between the output of the amplifier and the capacitive load.

Note that resistor R_{ISO} adds a corner frequency or zero in the open loop (A_{OL}) plot, restoring a 20dB per decade slope before the 1/ß line intercepts it. The series impedance diminishes as the frequency rises so that at approximately 11kHz, the resistive load pre-

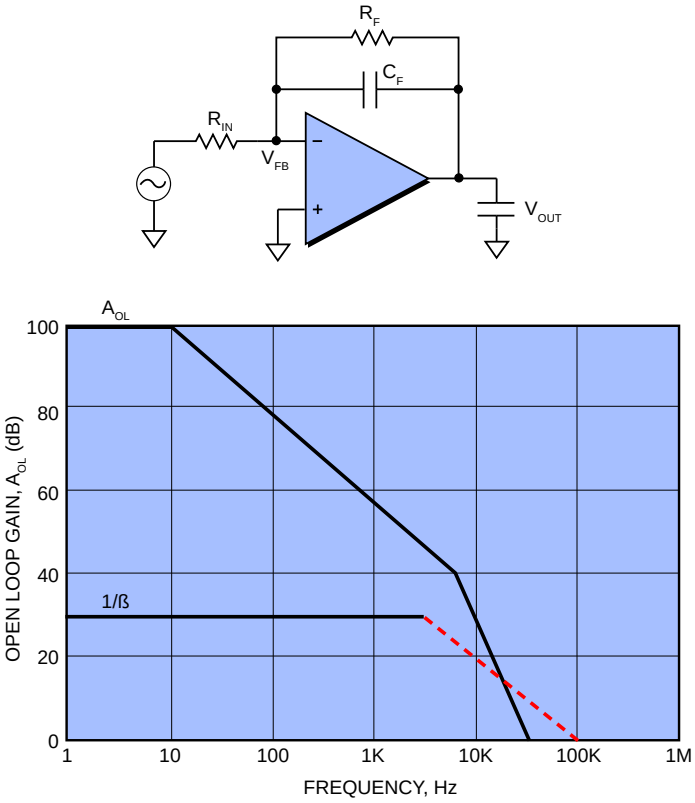


Figure 7. Feedback Zero Compensation

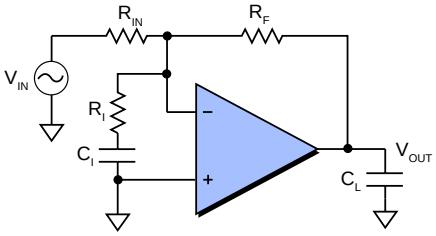


Figure 8. Noise Gain Compensation - Circuitry

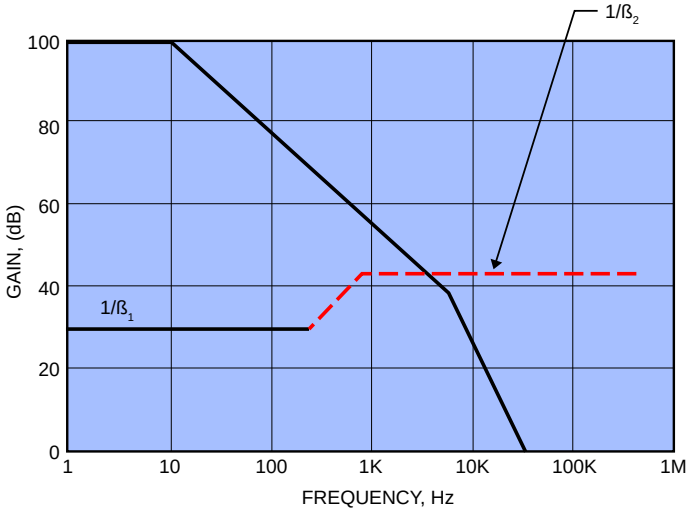


Figure 9. Noise Gain Compensation - Plots

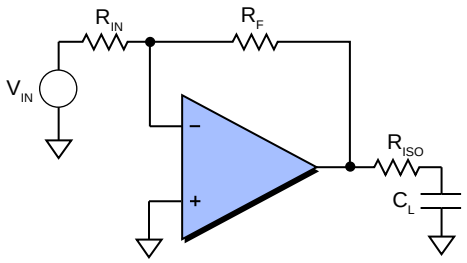


Figure 10. Isolation Resistor Circuitry

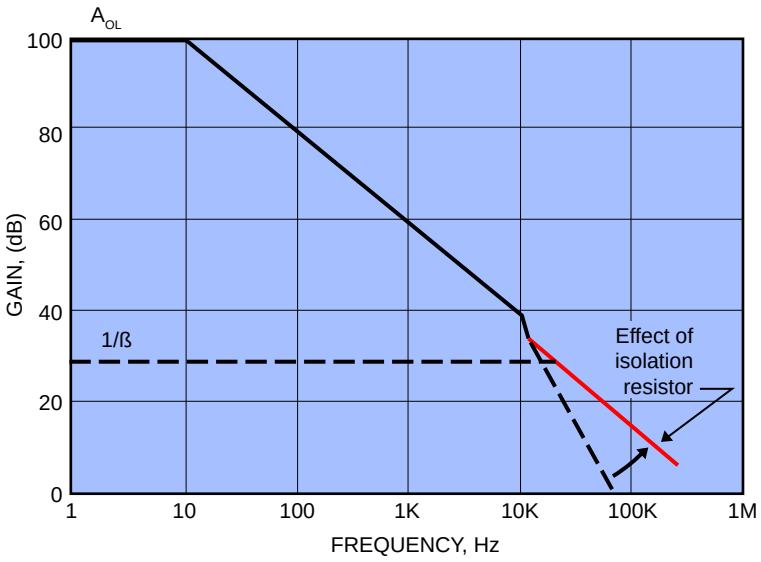


Figure 11. Isolation Resistor - Plot

dominates as the series load. This technique does not sacrifice any loop gain because the open loop gain (A_{OL}) line remains stationary. However, the power loss in the resistor can be significant. The usable bandwidth is approximately 3kHz.

It is worth noting that there is virtually no loss in the peak voltage across the capacitive load because the current and voltage are out of phase. Consequently, when the peak voltage is maximum, the applied current is low, minimizing the voltage loss across the isolation resistor. This isolation resistor compensation technique is relatively immune to variations in component values.

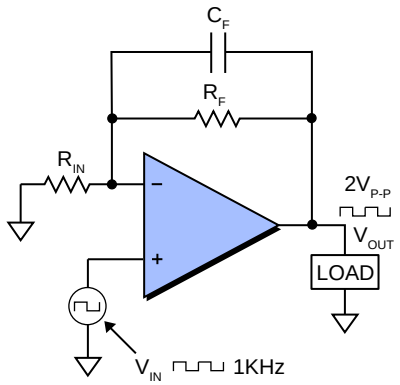


Figure 12. Square Wave Testing

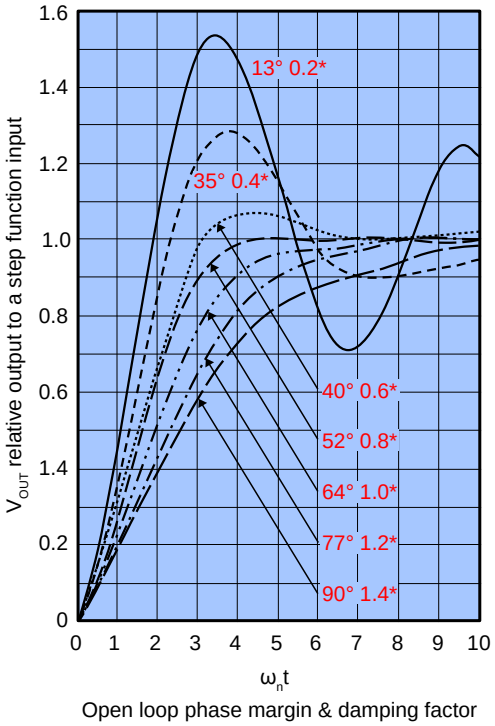


Figure 13. Phase Margin Versus Step Response

4.0 STABILITY TESTS

The following tests describe test techniques for ascertaining whether a design will indeed perform in a stable way.

4.1 SQUARE WAVE TESTING

In this test, a small-amplitude square wave is injected into the closed loop op amp circuit as the V_{IN} source, as depicted in Figure 12. This example uses components as close to the production version as possible − including power supplies, cables and circuit boards.

A frequency should be chosen that is well within the loop gain bandwidth, but high enough to make triggering of an oscilloscope easy. For most applications, 1kHz is a good test frequency. Since we are interested in the small signal AC behavior, adjust V_{IN} so that the output is 200mV_{P-P} or less. This is to avoid large signal limitations such as slew rate, output current limitations and output voltage saturation. Check the 1kHz output (V_{OUT}) for overshoot and undershoot while exercising the circuitry, including the power supply with low-frequency variations.

Phase margin for a given step response can be estimated from Figure 13.

4.2 DYNAMIC STABILITY TEST

This is an expansion of the square wave test described in Section 4.1. The dynamic stability test is depicted in Figure 14. In this test a small-signal AC square wave is imposed on a low-frequency, large signal AC sine wave to dynamically test the power op amplifier under all operating point conditions. The square wave impressed on the slow moving 10-Hz sweep is depicted in Figure 15. Note that the value of R_1 in parallel with R_2 in Figure 14 must be much greater than R_I. Otherwise, the input test impedances will adversely affect the compensation of the op amp undergoing test.

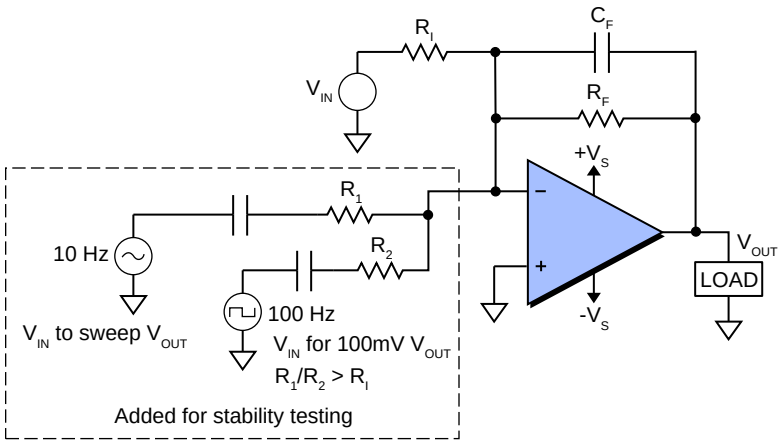


Figure 14. Dynamic Stability Test

5.0 EXAMPLES

Shown in Figure 16 is an uncompensated op amp. Its Bode Plot is depicted in Figure 17. In the following sections we shall show how this circuit can be stabilized using the various stabilization techniques initially described in Section 3.

Note that the 50k pole in the open loop gain (A_{OL}) is due to the capacitive load impedance. This circuit is unstable because the closed loop gain 1/ß intersects the open loop gain at a rate of 40dB per decade.

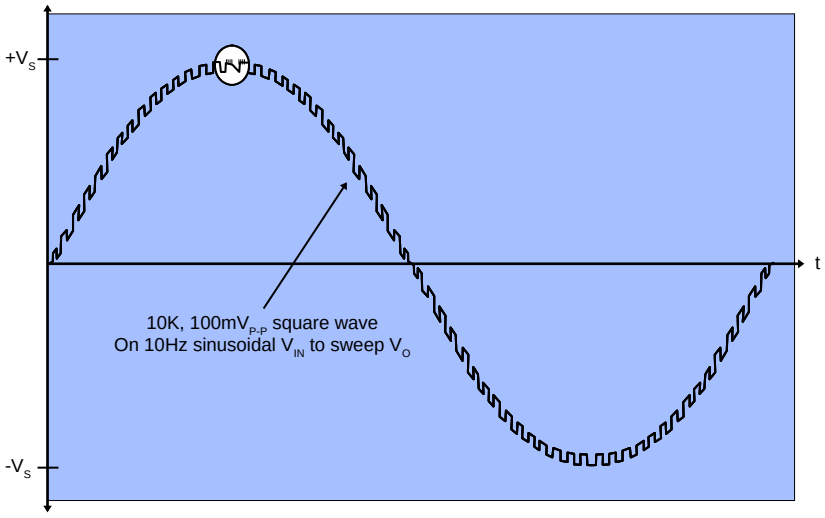
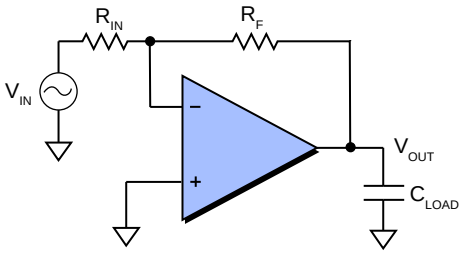


Figure 15. Square Wave Imposed on the Waveform



AMPLIFIER = PA241
C_{LOAD} = 20nF
R_{IN} = 2.5K
R_F = 22.5K
1/ß = 20dB

Figure 16. Uncompensated Op Amp

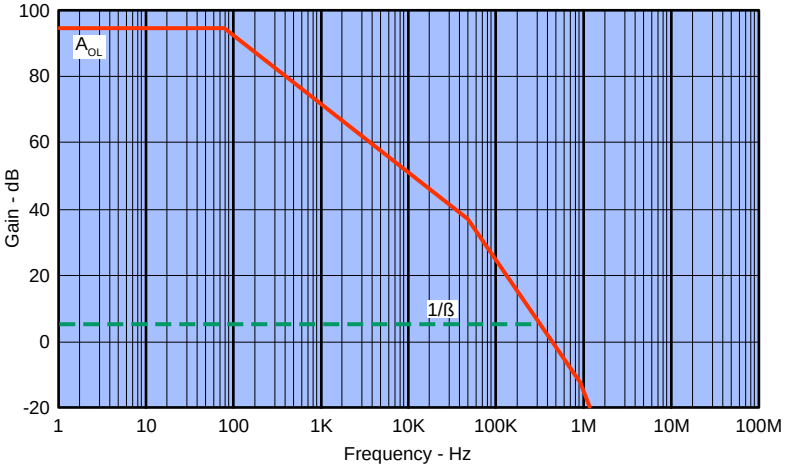


Figure 17. Uncompensated Op Amp − Bode Plot

5.1 FEEDBACK ZERO COMPENSATION

By adding a compensating capacitor C_F, to the circuit shown in Figure 16, the circuit becomes the one shown in Figure 18, and its corresponding bode response in Figure 19. By adding a feedback capacitor C_F to alter the 1/ß line, and placing a pole in the 1/ß plot so that it intersects the red line at an angle corresponding to less than 40db per decade, which happens to be just under 200kHz, the usable bandwidth is approximately 30KHz. This technique is very sensitive to the tolerances of the feedback capacitor. Note in the plot that the 20% capacitor moves that pole over a 100kHz range, so it is very susceptible to going in and out of stability based on that capacitor (which may change in value with changes in temperature).

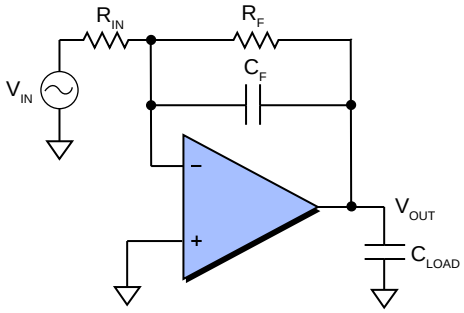


Figure 18. Compensated Capacitive Load – Schematic

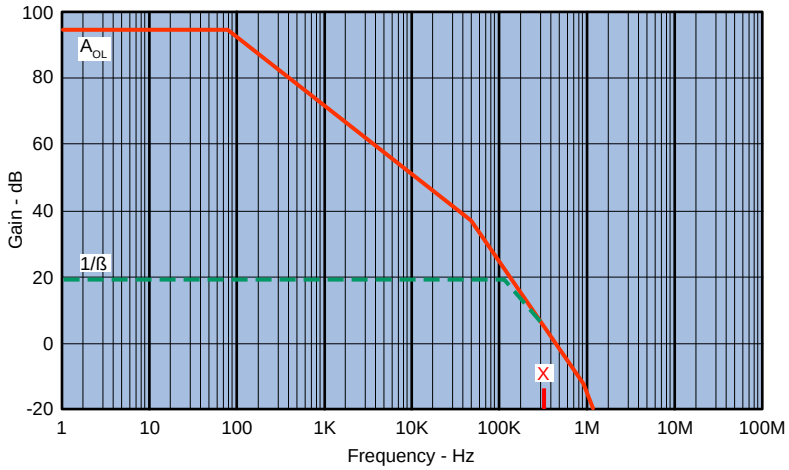


Figure 19. Compensated Capacitive Load – Bode Plot

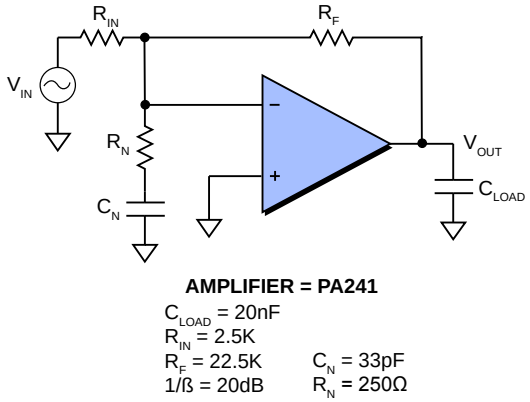


Figure 20. Noise Gain Compensated – Schematic

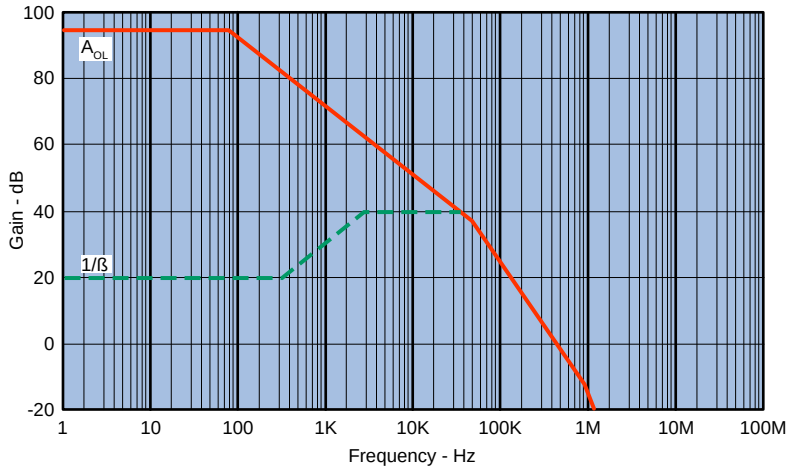


Figure 21. Noise Gain Compensated – Bode Plot

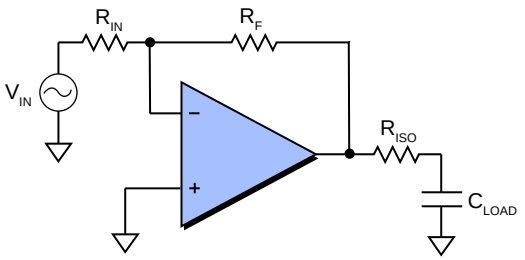
5.2 CAPACITIVE LOAD – NOISE GAIN COMPENSATED

Shown in Figures 20 and 21 is a circuit and its corresponding Bode amplitude plot for an op amp employing noise gain compensation. The impact of adding C_N is to bump up the 1/ß (the green line) so that it intersects the A_{OL} line above the pole where the plot shifts from 20dB per decade (stable) to 40dB per decade (unstable).
The usable bandwidth is approximately 3kHz.

5.3 CAPACITIVE LOAD – ISOLATION RESISTOR

Shown in Figures 22 and 23 is a circuit and its corresponding Bode amplitude plot for an op amp employing an isolation resistor R_{ISO}. The isolation resistor reduces the phase angle of the load so that it doesn't appear capacitive at higher frequencies. The usable bandwidth is approximately 30kHz.

With the isolation resistor, we sacrifice virtually no bandwidth. This can be a significant trade off. In this case, with an 80 V_{P-P} output at 25kHz, we are dissipating 0.75 watts in the resistor. Because the loss is load current related, it may or may not be a problem.



AMPLIFIER = PA241

C_{LOAD} = 20nF
R_{IN} = 2.5K
R_F = 22.5K
1/ß = 20dB R_{ISO} = 100Ω

Figure 22. Isolation Resistor Compensated – Schematic

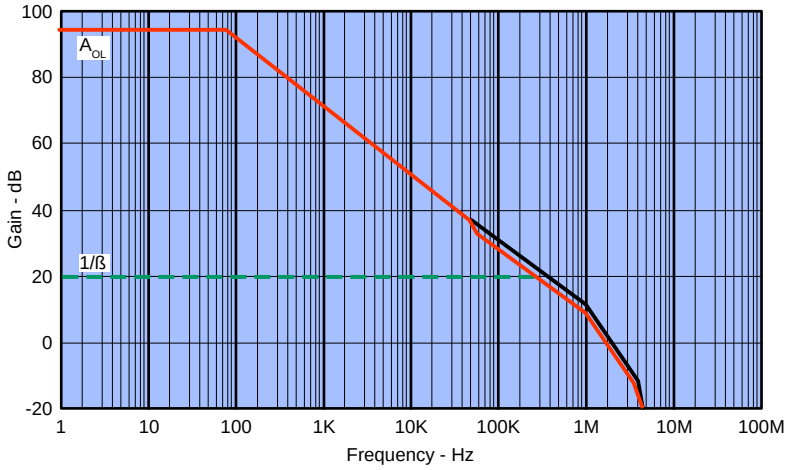
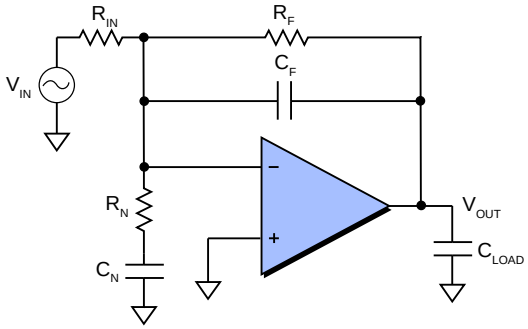


Figure 23. Isolation Resistor Compensated – Bode Plot

5.4 FEEDBACK ZERO AND NOISE GAIN COMPENSATED

Shown in Figures 24 and 25 is a circuit and its corresponding Bode amplitude plot for an op amp employing both feedback zero and noise gain compensation. The goal here is to use multiple techniques to lessen the impact of the trade offs. So with noise gain compensation bandwidth sacrificed, but with feedback zero compensation, circuit is quite sensitive to noise; however, with this combination we realize a usable bandwidth. It is back up in the neighborhood of 30kHz. The circuit is pretty much immune to component tolerance issues and finally there is good bit of phase margin.



AMPLIFIER = PA241

C_{LOAD} = 20nF
R_{IN} = 2.5K C_N = 33pF
R_F = 22.5K R_N = 250Ω
1/ß = 20dB C_F = 820pF

Figure 24. Capacitive & Noise Gain compensated – Schematic

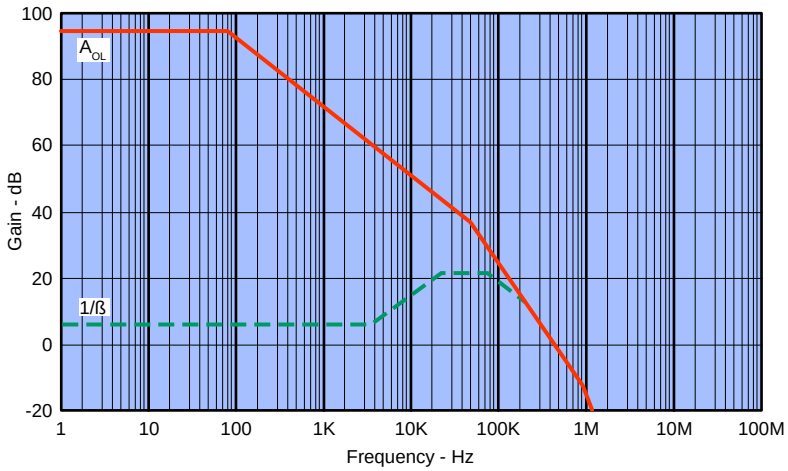


Figure 25. Capacitive & Noise Gain compensated – Bode Plot

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1. *The Art of Electronics, Second Edition*, Paul Horowitz and Winfield Hill, Cambridge University Press, 1989, p. 242
2. Apex Precision Power Application Note 19, *Stability For Power Operational Amplifiers*, Cirrus Logic, www.cirrus.com

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Intuitive Operational Amplifiers, Thomas M. Fredericksen, McGraw-Hill Book Co., 1988

REVISION HISTORY

Release	Date	Changes
REVA	APR 2008	Initial Release

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Increasing Output Swing in Power Operational Amplifiers

INTRODUCTION

Due to the typical circuit topologies used in the output stages of power operational amplifiers, the output voltage swing may be limited by as much as 12V less than the applied power supply voltage. The goal of this application note is to illustrate several practical techniques to drive the amplifier output closer to the rail voltages, which enables power output to increase significantly. In some applications, the output power can be increased by as much as 50%. Certain power operational amplifiers allow the user to apply a separate higher voltage supply to the input stage of the amplifier while the output stage is set to a lower voltage. This arrangement achieves close-to-rail voltage swing since the output devices, usually Enhancement Mode MOSFETs, are driven close to saturation by the higher voltage available to drive the gates. Another method to improve output voltage swing is to modify the amplifier's output stage by adding some external output components. This application note explores these approaches through the discussion of typical examples with the hope that users will create and develop circuits to meet their own specific requirements based on the techniques shown here.

GENERATING THE BOOST VOLTAGE

Many power operational amplifiers provide separate power supply pins for the input stage and output stage. This allows the user to apply a higher power supply voltage to the input circuitry than the supply voltage applied to the output stage. The voltage difference is usually between 5V and 15V. This enables the output devices to be driven close to their saturation. If this increased voltage swing is not needed, then the input and output power supply pins are connected together providing equal supply voltage to the input and output stages. As an example, the Apex Precision Power™ MP39 power operational amplifier[1], depicted in Figure 1, has separate pins for V_B, the input stage supply voltage, and V_S, the output stage supply voltage, so that the designer can tie them together or power them separately, as outlined below.

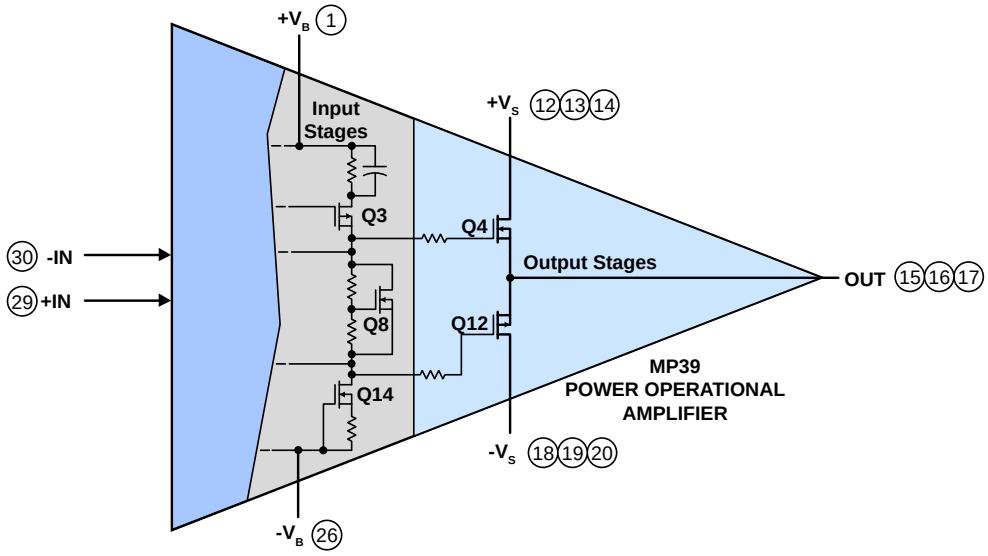


Figure 1. V_B and V_S are Separate — Because the DC power inputs for the input stage ($\pm V_B$) are separated from the output stage ($\pm V_S$) in the MP39, the designer has the option of applying higher potential to each V_B terminal, thereby allowing the output voltage to swing closer to the rail potentials ($\pm V_S$).

The Q4 and Q12 MOSFETs deliver a maximum output current of 10A to the load. In most applications, $+V_B$ and $+V_S$ are connected together. Since Q4 is an enhancement mode device, the gate voltage must be at least 10V higher than the source voltage to achieve the lowest source to drain voltage. In the case of Q12, the gate voltage must be 10V lower. This means the maximum output voltage, at full output current, will be at least 10V lower than V_S. By applying a higher voltage to V_B, the Q4 gate voltage is driven to a higher potential than V_S, forcing a higher Q4 source voltage. As indicated in the MP39 data sheet, the absolute maximum boost voltage, V_B, is specified at 20V higher than V_S and the maximum boost supply current is 22mA.

For applications requiring an output current of less than 500mA, a 10V to 15V zener diode placed between V_B and V_S may be adequate. In this configuration the power supply voltage would be connected to the V_B pin. This will automatically force the V_S input 10V to 15V lower than V_B. If this approach is followed, all of the output current would flow through the zener diode which would have to dissipate the resulting power. This is a simple solution, but not very practical because the MP39 can deliver output currents of up to 10A.

EMPLOYING ISOLATED DC-TO-DC CONVERTERS

Isolated DC-to-DC converters may be used to supply the boost voltage. There are many commercially available converters that are suitable for providing the boost voltage. A pair of CALEX 3W modules have been selected (available in either surface mount or through-hole configurations). The 48V input version offers an input voltage range from 36V to 72V and an isolated, regulated output of 12V. Two modules are required, one for the $+V_B$ and one for the $–V_B$. Our testing was performed with V_S set at 40V. One module was powered from the +40V supply ($+V_S$) and the other module was powered from the -40V supply ($-V_S$). Since the outputs are isolated, other input power supply arrangements could be used, as long as the supply voltages are within the module's operating input range. In the configuration depicted in Figure 2, the voltage potential between the $+V_B$ and the $–V_B$ terminals is 52V.

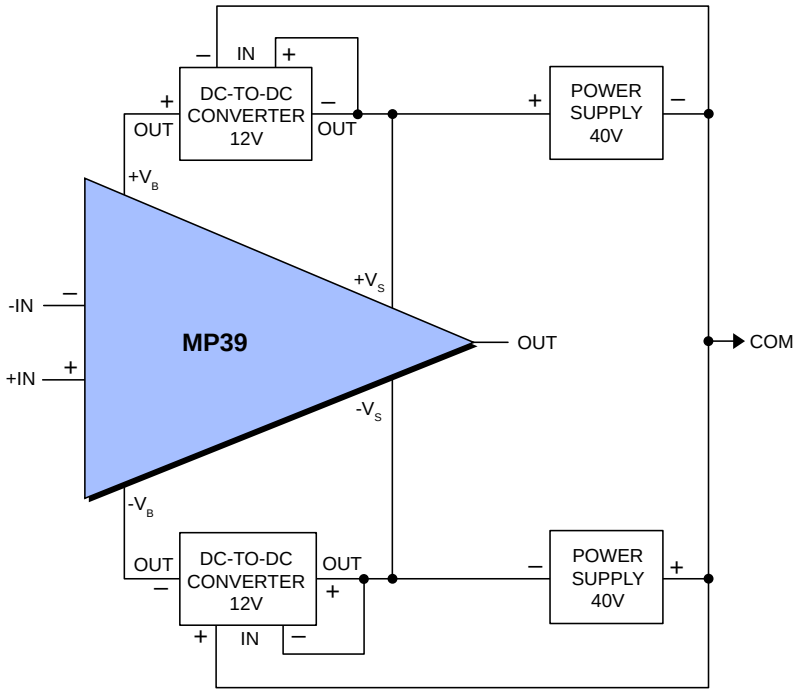


Figure 2. Obtaining the Boost

A pair of DC-to-DC converters connected as shown in Figure 2, are powered by the 40V power supplies that also provide the V_S voltages. The output of the DC-to-DC converters is connected between the V_S and V_B of the power operational amplifier terminals providing the required boost voltage. To maintain a balanced load across the power supplies, the output of one converter is connected in series with $+V_S$ supply and common, and the second converter between $–V_B$ and $–V_S$. The outputs are isolated so any convenient power sources can be applied as long as the total voltage applied to $–V_B$ and $+V_B$ does not exceed the specified input range.

DC-TO-DC CONVERTERS FROM OFF-THE-SHELF COMPONENTS

A low cost DC-to-DC converter can be assembled using off-the-shelf components commonly available through common catalog distributors. The schematic circuit diagram is shown in Figure 3. This converter was designed for the specific purpose of providing the V_{BOOST} for any Apex Precision Power power operational amplifier featuring separate power pins for the input and the power stages.

Note that the transformers T1, T2 and Inductor L1 are Coiltronics part numbers available from Cooper Bussman.

Because the two outputs are totally independent, a single converter will supply both the plus and minus V_{BOOST}. The input voltage range is specified from 20V to 100V allowing additional flexibility. The converter's switching frequency is approximately 20kHz and exhibits very low radiated and conducted noise components, assuming the circuit lay-

out and ground scheme are given careful attention. Transformer L1 is a common mode filter that rejects common mode noise due to the switching that occurs in the Timer X1, preventing it from feeding back to the V_S source voltage. The snubber circuit, consisting of Capacitor C13 and Resistor R11, counteracts ringing that would other wise occur in Transformers T1 and T2.

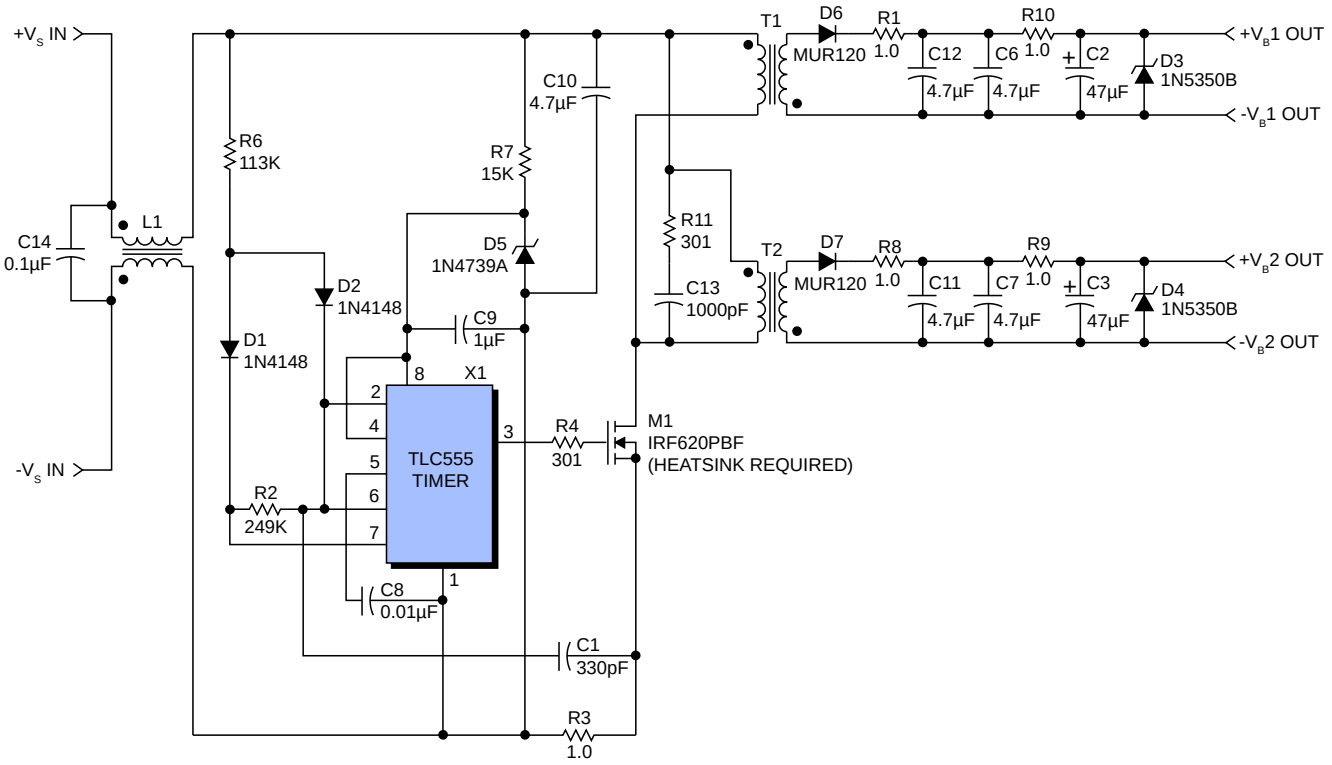


Figure 3. A Low-Cost DC-to-DC Converter — This converter can be employed to supply the boost voltages ($+V_B$ and $–V_B$) necessary to increase the output swing.

Table 1. Parts List for DC to DC Converter Circuit Shown in Figure 3

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER (DIGI-KEY)
C11, C12,C6,C7	CAPACITOR, X7R CERAMIC, 4.7µF, 25V, TDK	445-2886-ND
C1	CAPACITOR, COG CERAMIC, 330pF, 50V, MURATA	490-3724-ND
C2, C3	CAPACITOR, TANTALUM, 47µF, 25V, AVX, TAP476K025CCS	478-4181-ND
C8	CAPACITOR, X7R CERAMIC, 0.01µF, 100V, MURATA	490-3813-ND
C9	CAPACITOR, X7R CERAMIC, 1.0µF, 50V, TDK	445-2884-ND
C10	CAPACITOR, POLY FILM, 4.7µF, 250V, PANASONIC	EF2475-ND
C13	CAPACITOR, X7R CERAMIC, 1000pF, 200V, KEMET	399-4323-ND
C14	CAPACITOR, X7R CERAMIC, 0.1µF, 200V, KEMET	399-4387-ND
D1, D2	1N4148, DIODE, OR EQUIVALENT	
D3, D4	1N5350, 13V ZENER DIODE, 5W, ON SEMI	1N5350BRLGOSCT-ND
D5	1N4739, 9.1V ZENER DIODE, 1W, ON SEMI	1N4739ADICT-ND
D6, D7	MUR120, ULTRA FAST RECOVERY, RECTIFIER, ON SEMI	MUR120RLGOSCT-ND
D5	1N4739, 9.1V ZENER DIODE, 1W, ON SEMI	1N4739ADICT-ND
L1	100 µH CHOKE, COILTRONICS, DRQ-73-101-R	513-1251-1-ND
M1	IRF620PBF, MOSFET, 200V, 5.2A, VISHAY, IR	IRF620PBF-ND
R1,R3,R8,R9,R10	RESISTOR, FILM, 1.0Ω, 1W	
R2	RESISTOR, FILM, 249KΩ, 1%, 0.25W	

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER (DIGI-KEY)
R4, R11	RESISTOR, FILM, 301Ω, 1%. 0.25W	
R6	RESISTOR, FILM, 113KΩ, 1%, 0.25W	
R7	RESISTOR, FILM, 15KΩ, 1W	
T1, T2	100 µH CHOKE, COILTRONICS, DRQ-127-101-R	513-1314-1-ND
X1	TLC555 TIMER, I.C., TI	296-1857-5-ND

SAMPLE TEST CIRCUIT – A 200W POWER OPERATIONAL AMPLIFIER DRIVING AN 8Ω RESISTIVE LOAD

In this example an MP39 power operational amplifier is configured as an inverting amplifier with a gain of 5 and driving a resistive load of 8Ω, as depicted in Figure 4. The value of the compensation capacitor C_C, 220pf, complies with the recommendation specified in the MP39 data sheet for a gain of 3 or more, and less than 10. The power supply voltage, V_S, is set to ±40V. The boost voltages, $+V_B$ and $–V_B$, are set at 12V. The power delivered to the load is 200W PEAK with the boost voltage applied, and 144W PEAK with no boost voltage. This significant increase in realized power can be important in high-efficiency applications. The MP39 datasheet limit for output voltage swing is $±V_S$ ±8.8V. This means clipping could occur at 31.2V without the boost voltage.

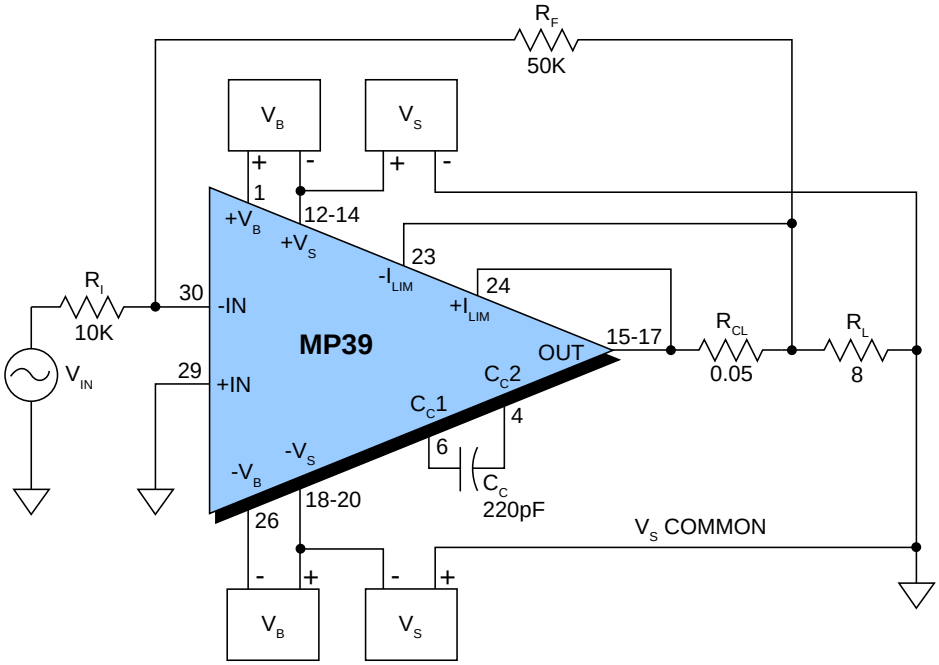


Figure 4. Test Circuit — This circuit with an inverting gain of 5, V_B of 12V and V_S of 40V, was used to obtain the plots in Figures 5 and Figures 6.

The waveforms shown below in Figure 5 depict the output without the boost circuits — the V_B terminals are tied to the V_S terminals. Note that clipping of the output waveform occurs at +34V and –34V respectively, because the output can be driven no higher. However, with the addition of boost circuits with potentials of 12V, the output is able to swing all the way to the supply rails, as depicted in Figure 6.

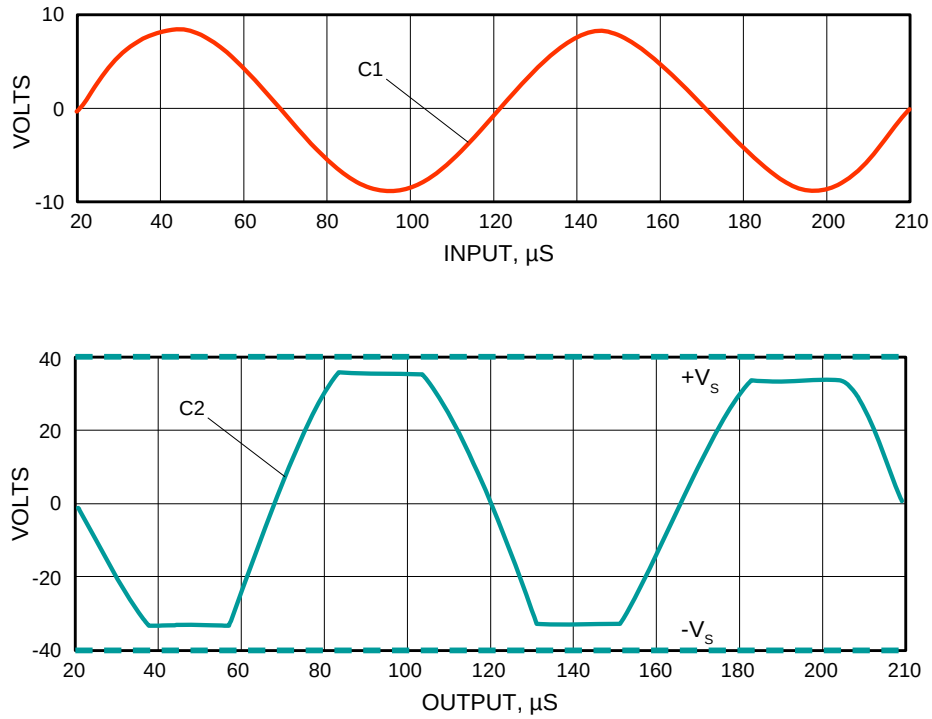


Figure 5. Without a Boost Circuit — With the V_B boost terminals tied to the V_S terminals the output voltages are clipped at ±34V. Consequently, the output swing is unable to reach the supply rails at +40V and – 40V, respectively. In this configuration the amplifier can only deliver 144W PEAK.

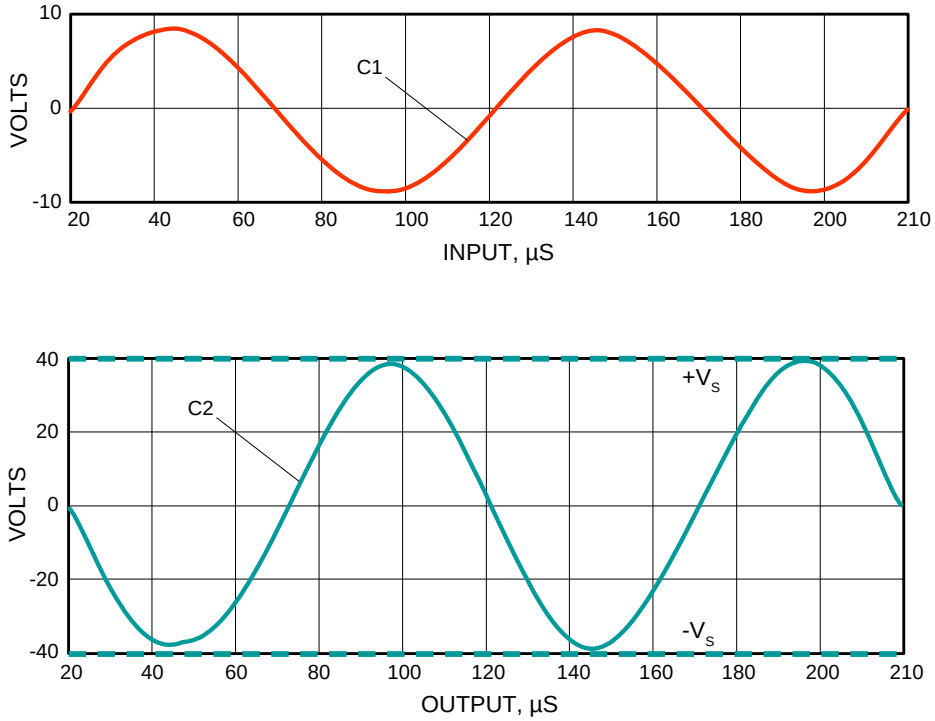


Figure 6. With a Boost Circuit — With the addition of $+V_B$ and $-V_B$ boost circuits, the output is able to swing all the way to the rail potentials at V_S and $-V_S$, respectively. The amplifier in this configuration is able to deliver 200W PEAK – approximately 39% more power than when the amplifier operates without the boost circuits.

MODIFICATION OF THE OUTPUT STAGE CAN IMPROVE OUTPUT VOLTAGE SWING

Shown in Figure 7 is a circuit based on the Apex Precision Power PA96 power operational amplifier[2] operating with power supply voltages of ±40V. Resistors R3 and R4 are selected so that the maximum quiescent current creates a voltage drop of approximately 0.5V to 0.6V across the base-to-emitter junctions of Q1 and Q2. This keeps the output transistors from turning on and conducting collector current when the output voltage is near zero. Resistors R5 and R6 are selected to provide sufficient base current to Q1 and Q2 as the output voltage approaches the rail allowing Q1 and Q2 to pull the output closer to the supplies. A note of caution: although the power operational amplifier is current limit protected, the output transistors (Q1 and Q2) have no overcurrent protection and will be damaged if their SOA (Safe Operating Area) requirements are exceeded.

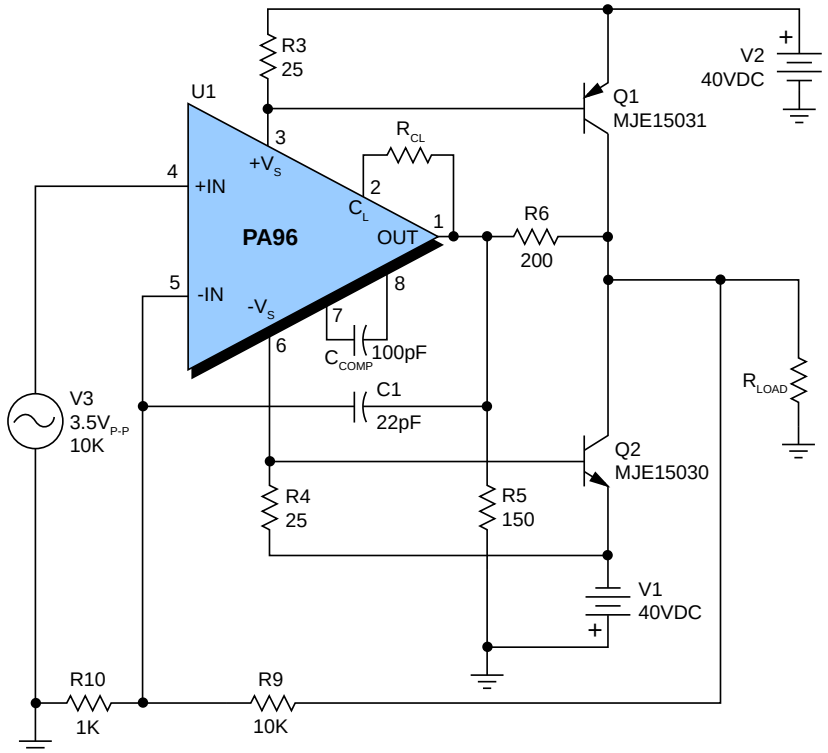
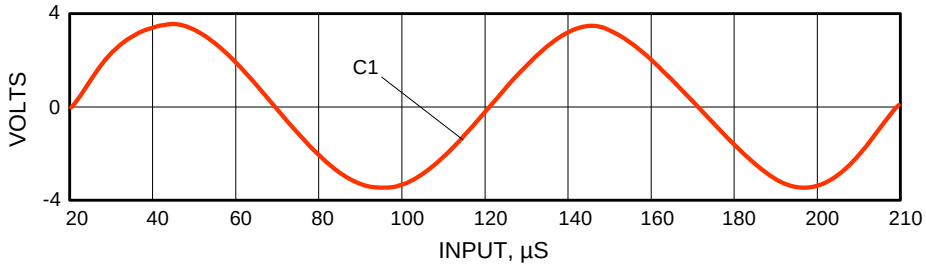


Figure 7. Composite Power Amplifier — A PA96 operational amplifier with additional output transistors, Q1 and Q2, and resistors R3, R4, R5, and R6. This modification creates a composite operational amplifier with extended output voltage swing.

Figure 8 below depicts how the circuit in Figure 7 reacts when resistors R3, R4, R5, and R6 are not used showing the circuit's output clipping. Figure 9 illustrates how the same circuit behaves when the three resistors have been added. Clipping no longer occurs.



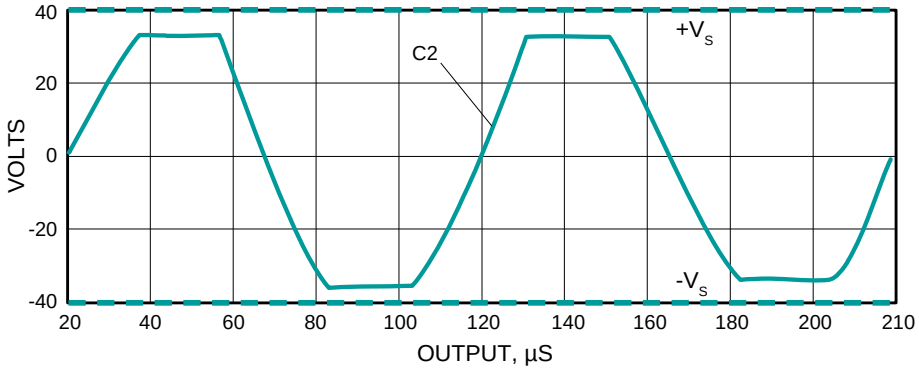
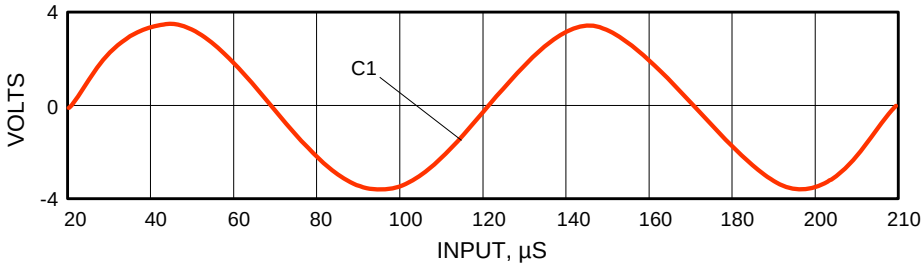


Figure 8. Composite Amplifier *without* Modifications



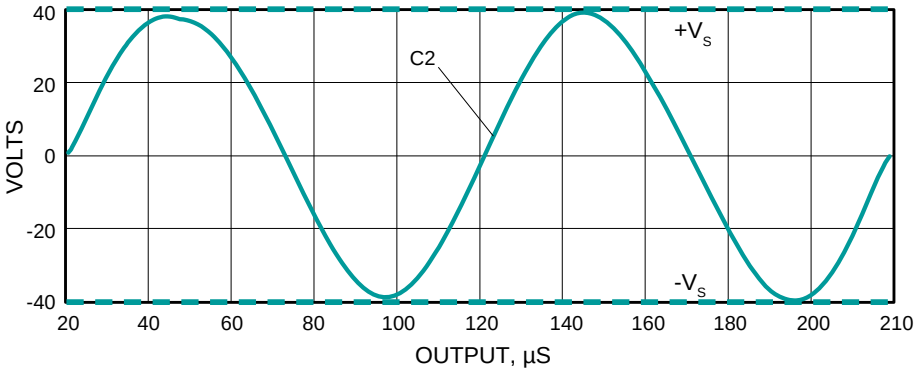


Figure 9. Composite Amplifier *with* Modifications

MAINTAINING LINEAR PERFORMANCE WITH OUTPUT VOLTAGES APPROACHING THE NEGATIVE RAIL

The circuit shown in Figure 10 accepts input voltage levels, including zero, and can deliver output voltages from zero to 10V with a single ended 18V power supply. The Apex Precision Power PA75 dual power operational amplifier[3] is used because the input voltage range includes the negative supply voltage. However, the PA75 output voltage does not swing very near to the rails. The PA75 consists of two operational amplifiers. One is pre-configured as a unity gain buffer, while the other can have its gain programmed and is employed in this circuit. This example enables the output voltage to drive a grounded load to zero volts. Diode D2 must be a low leakage zener diode for the circuit to function. Since the output voltage of the PA75 never reaches zero volts, any leakage current flows through the load resistor causing a non-zero voltage at the load. The feedback loop cannot correct for this once the output reaches it's minimum voltage. Notice the plot of Figure 11. The output response is quite linear with respect to the input from zero to 10V.

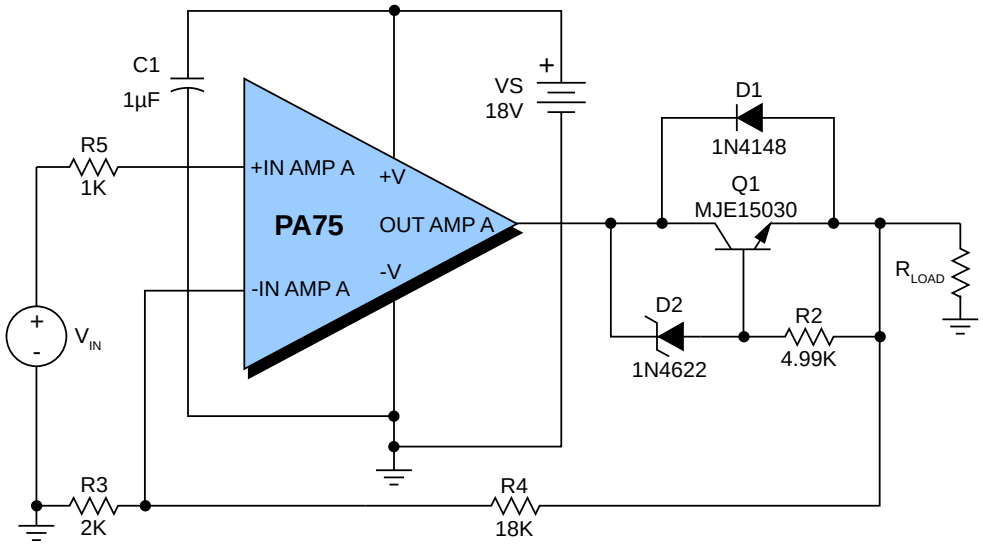


Figure 10. Single Ended Operation Delivering Output from Zero to 10V

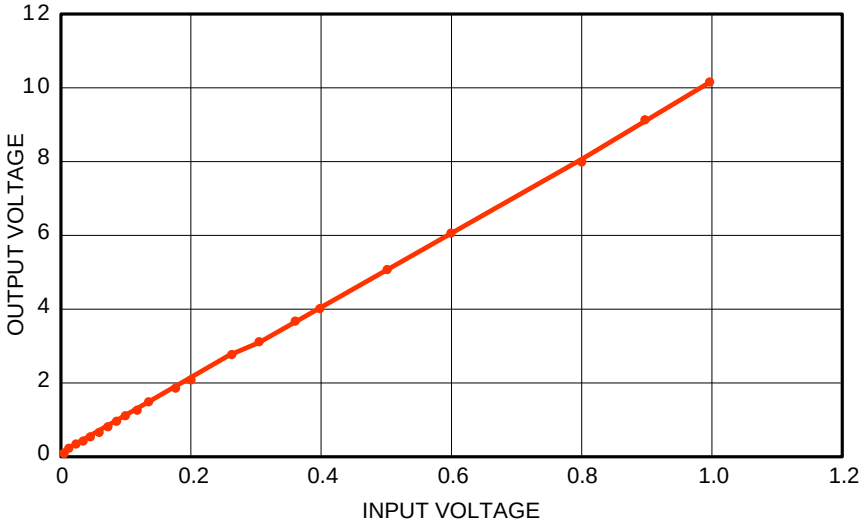


Figure 11. Output Response of the Circuit in Figure 10

CONCLUSIONS

Several methods for extending the output voltage swing of power operational amplifiers have been described. The circuits included in this application note have been developed and tested. The schematics may not include all components such as by-pass capacitors, resistors and diodes needed for a complete design. Circuit layout has not been addressed and is critical for all circuit configurations using Apex Precision Power™ products. The test results shown are based on the typical performance of a specific device used in each application. The differences in performance shown, with and without the modifications, will be more dramatic when compared to minimum voltage swing data sheet limits. For additional information concerning the use of power operational amplifiers with regard to stability, thermal management, device protection, and other topics, please refer to the relevant Application Note[4].

References

1. *MP39 Power Operational Amplifier* Data Sheet, Cirrus Logic, Apex Precision Power.
2. *PA96 Power Operational Amplifier* Data Sheet, Cirrus Logic, Apex Precision Power.
3. *PA75 Dual Power Amplifiers* Data Sheet, Cirrus Logic, Apex Precision Power.
4. *Techniques for Stabilizing Power Operational Amplifiers*, Application Note 47, Cirrus Logic, Apex Precision Power

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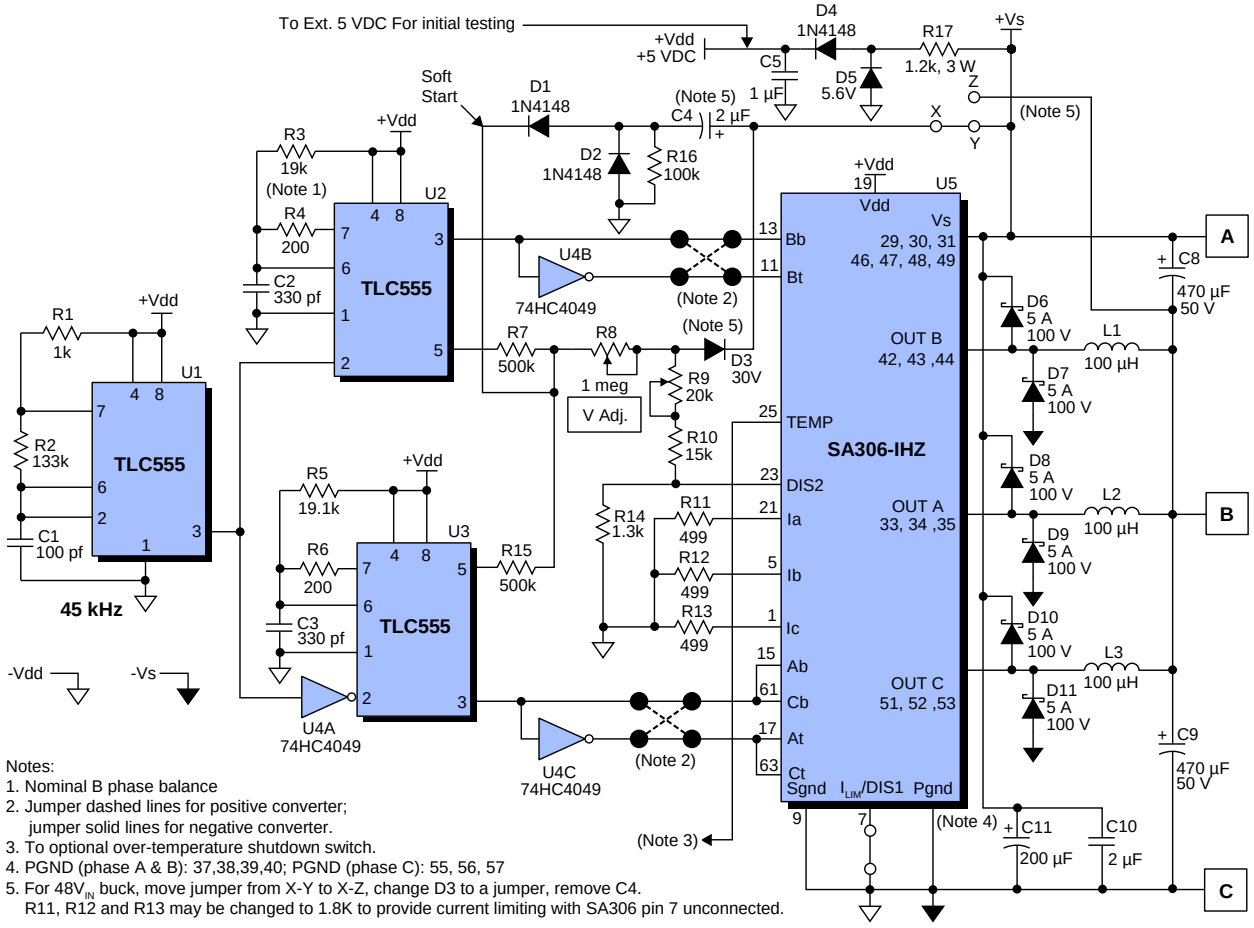
Jumper Configurable 400 Watt+ DC-to-DC Converter Fulfills Buck-Boost & Motor Drive Roles

INTRODUCTION

This Application Note describes a novel DC converter design concept that uses the SA306-IHZ monolithic three-phase switching amplifier[1,2]. The converter is depicted schematically in Figure 1. It can be thought of as a 'black box' module that is suitable for a variety of applications such as converting +28 volts to -48 volts (relative to the +28 volt input) and -20 volts (relative to the -28 volt input), and able to deliver a minimum of 8.5 amperes of combined output. The module is jumper configurable as a positive or negative input converter. A minor circuit change (Figure 1, Note 5) allows the module to convert +48 volts to +20 volts at 15 amperes of output (representing 91% efficiency), or -48 volts converted to -28 volts with 14 amperes (a 93% efficiency). For simplicity's sake, the design is limited in scope but has proven to be quite usable and robust despite the limitations listed below, and in the section entitled Miscellaneous Design Notes on page 9. This design assumes a well regulated voltage input because of limited loop gain. The output voltage regulation is ±1% to ±3% over the full output load range with an input voltage delta of 300 mV. There is no boost mode current limit circuit included for a number of reasons, one of which is that the input is diode coupled to the output — output currents in excess of 15 A will exceed the diode current/wire bond ratings. Transient load response is quite good with full recovery in about 3 milliseconds. Efficiencies of approximately 94% are realized with a 48 V output and approximately 85% with the 20 V output, as depicted in the application illustrations that follow.



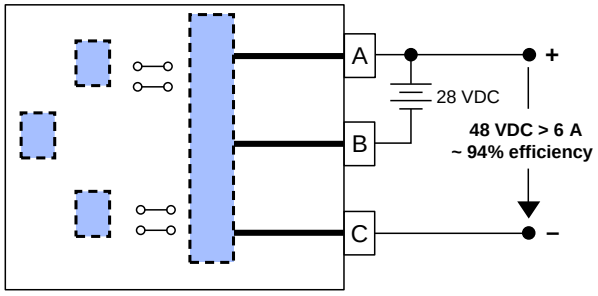
Notes:
1. Nominal B phase balance
2. Jumper dashed lines for positive converter; jumper solid lines for negative converter.
3. To optional over-temperature shutdown switch.
4. PGND (phase A & B): 37,38,39,40; PGND (phase C): 55, 56, 57
5. For 48V_{IN} buck, move jumper from X-Y to X-Z, change D3 to a jumper, remove C4. R11, R12 and R13 may be changed to 1.8K to provide current limiting with SA306 pin 7 unconnected.

Figure 1. Polarity is Easily Switched — DC-to-DC converter, three terminal module can be switched from a positive to a negative converter by simply interchanging the jumpers identified by Note 2. (**Caution:** Make sure the A,B,C terminal connections correspond to the new configuration, otherwise the SA306-IHZ will be destroyed when power is applied.)

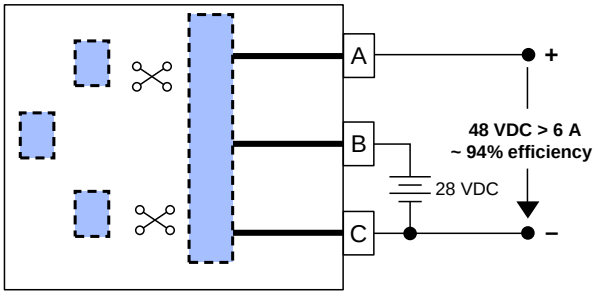
APPLICATIONS

In the following panel are shown a number of buck, boost and motor applications.

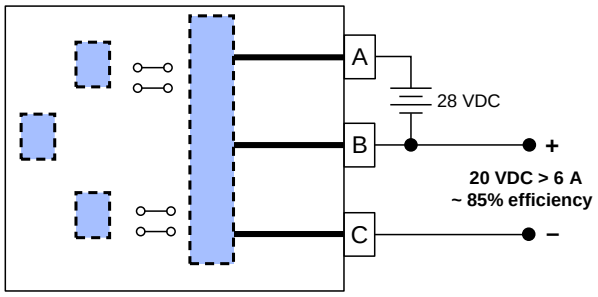
Buck-Boost Applications



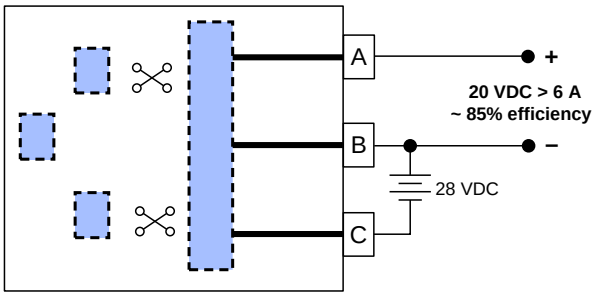
Negative Converter



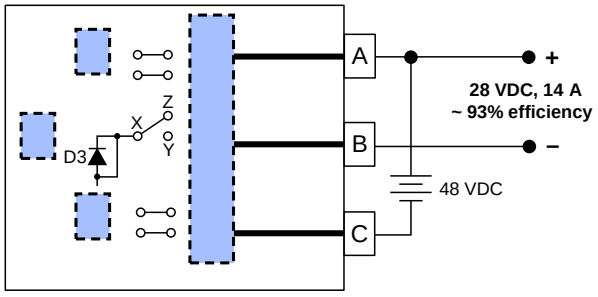
Positive Converter



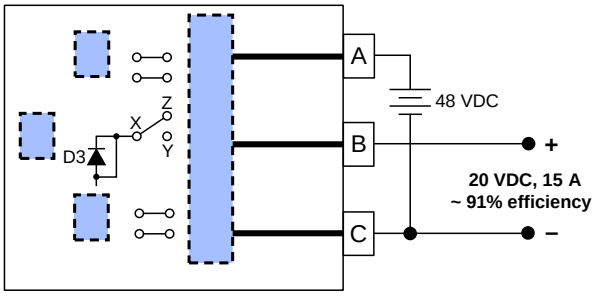
Negative Converter



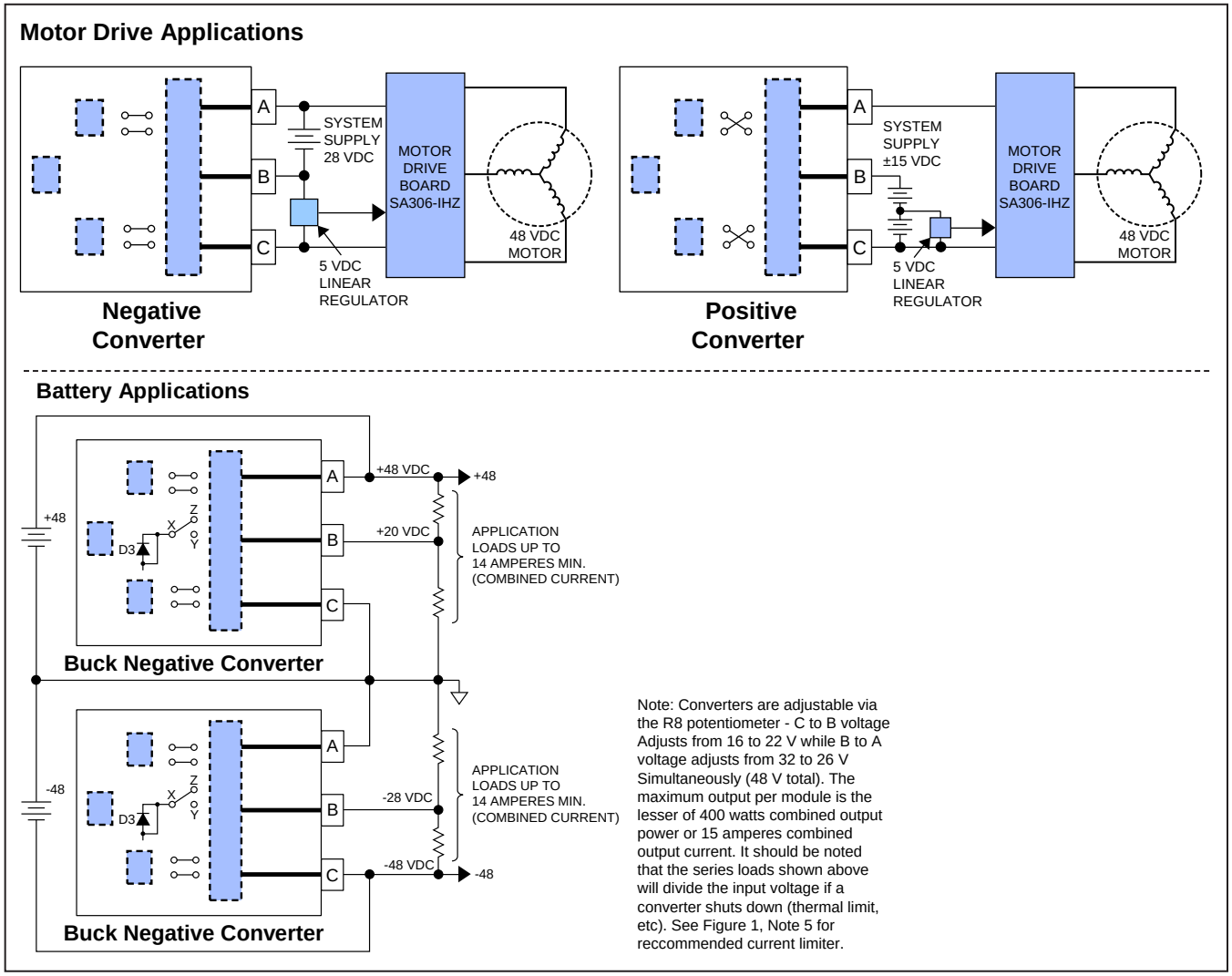
Positive Converter



Buck Negative Converter



Buck Negative Converter



U1, U2, U3, U4 and much of the associated circuitry could be replaced with an inexpensive micro-controller to provide other functions and voltage ranges than those shown above for all applications resulting in a low cost, low parts count converter module.

Theory of Operation – PWM Circuitry

The drive circuit shown in Figure 1 comprises three Texas Instruments TLC555 CMOS Timers, as well as the left block in Figure 2. In Figure 1, U1 serves as a 45 kHz oscillator. It, in turn, drives U2 and U3 which can be thought of as pulse width modulators (PWMs). As can be seen in Figure 1, U4A inverts the input to U3 so that it operates out of phase with its companion, U2. Even though the SA306-IHZ is a three-phase device with three sets of MOSFET half bridges, A, B and C operate in this application as a two-phase switch. Notice at the bottom of Figure 2 that Ab and Cb, as well as At and Ct are tied together, transforming the operation of the SA306-IHZ in to a two-phase operation. The two waveforms shown in Figure 2 are there to underscore the fact that the B phase (Bt and Bb) and the A & C phases (Ab, Cb) and (At, Ct), are always driven out of phase with each other. These out-of-phase signals toggle the inputs to the MOSFETs in the switching amplifier SA306-IHZ (U5). This alternating toggle arrangement distributes the power properly within the SA306-IHZ die, allowing maximum current throughput and reducing ripple current.

Maximum On Time – Because the Oscillator U1 is set at 45 kHz by timing components R1, R2 and C1, the period of the oscillator is 22 microseconds. The maximum ON time is 50%. Raising the voltage on U2 and U3 would provide a slight variation. This is employed in the Slow Start circuitry discussed in the “Charge Dynamics” section that follows. Raising the voltage applied to pin 5 of U2 and U3 raises the deadtime by increasing the threshold of these devices so the OFF time is extended. As the voltage applied through R7 and R15 goes up, the OFF time becomes longer.

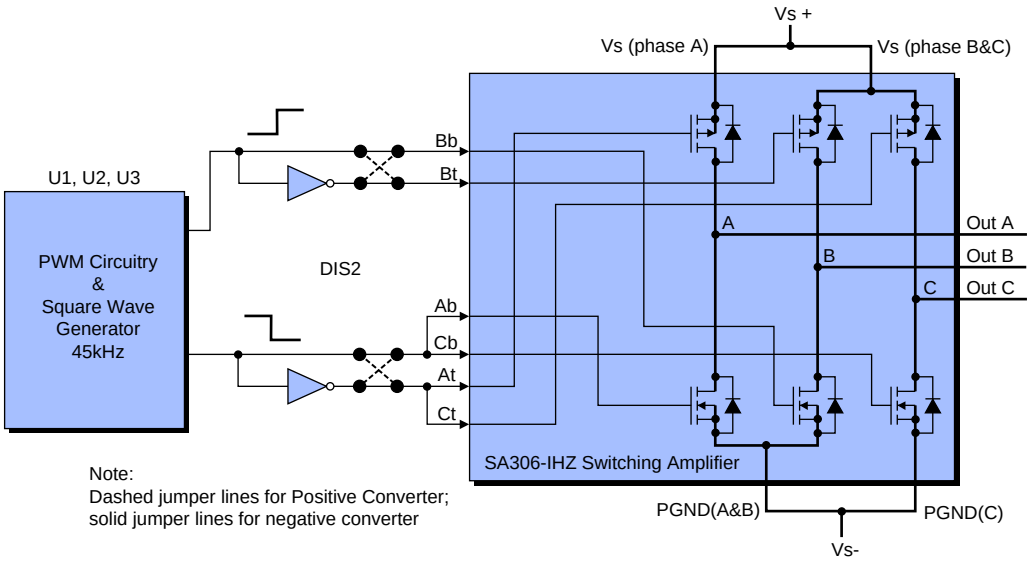


Figure 2. PWM Circuitry Interface with the SA306-IHZ Inputs – Simplified

Boost Circuitry

The voltage change technique employed in this converter is often called 'Boost Circuitry'. Each input inductor is charged through one SA306-IHZ output switch during a PWM 'charge' interval and then is synchronously rectified by the alternate MOSFET output switch during the PWM 'discharge' interval. Or to put it another way, energy is loaded into inductor L1, L2, or L3 and is then, during the discharge interval, delivered as a current to the output capacitors and/or the load. Because the PWM ON time is limited by design to 50% maximum, the voltage delivered at the output of the converter is limited to approximately twice Vs – which is the voltage delivered by the source. This inherent voltage limiting occurs because the 'synchronous rectifier' remains on during the entire PWM 'discharge' time and then transfers the current back from the output capacitor into the input capacitor. Note that in both the positive and negative versions of this converter, the current exits the SA306-IHZ, at either Vs+ or Vs-, entering the attached load.

A Soft Start circuit is required to confine turn on input current transients to safe levels and occurs any time the output capacitors ramp up. This is discussed in detail in the Soft Start section, below. The jumpers in the circuit ensure that the correct MOSFET switches are used for charging and discharging, thereby programming either positive or negative polarity input operation. The two jumpers must match – which is to say they must both be 'straight through' or 'crossed'.

CAUTION

Both jumpers must be reversed, at the same time, otherwise serious damage may occur. Also make sure that the A,B,C terminal connections correspond to the new configuration, otherwise the SA306-IHZ will be destroyed when power is applied.

Charge Dynamics

Positive Converter – For the positive converter configuration shown in Figure 3, inductor L1 is charged during the ON interval through the bottom MOSFET (Bb) switch. Inductor L1 sees Vs- on the left side and Vbat plus on the right; therefore, the current is essentially a ramp, as depicted in the figure because the voltage across the inductor is essentially constant and current is the integral of voltage. Then during the OFF interval the inductor discharges through the top MOSFET switch (Bt), exiting through terminal A to the attached load. Again, the same occurs for the A and C MOSFET switches during alternate cycles except their inputs are tied together, as shown in Figure 2, and therefore the At-Ct and Ab-Cb pairs are driven in unison.

Negative Converter – For the negative converter configuration shown below in Figure 4, inductor L1 is charged during the ON interval through the MOSFET (Bt) switch. When the Switch transfers to the "charge" mode, inductor L1 discharges through the bottom MOSFET switch (Bb) into the power ground. The same occurs for the A and C MOSFET switches during the alternate cycle except their inputs are tied together, as shown in Figure 2, and therefore At and Ct and Ab and Cb pairs are driven in unison.

Buck Negative Converter – This converter mode has the same charge dynamics as the negative converter. The difference is that power is applied via terminals A and C and removed via terminal B.

Soft Start (Boost Only)

If there were no constraint when start up occurs, the input current would become very high because the circuit would attempt to immediately restore the low output voltage. In order to manage this scenario, the PWM, which behaves, in effect, as an error amplifier, is prevented from overreacting and instead the duty cycle is controlled so that the duty cycle rises slowly. As Vs comes up, it would normally pass through the 30 V zener diode D3 and adjustment potentiometer R8 to the junction – or duty cycle node – between Resistors R7 and R15. Instead the Soft Start node is connected directly to the output through D1 – C4 to Vs+, thereby bypassing the output of the converter sensed by the R8 – D3 network until the Vs potential is reached.

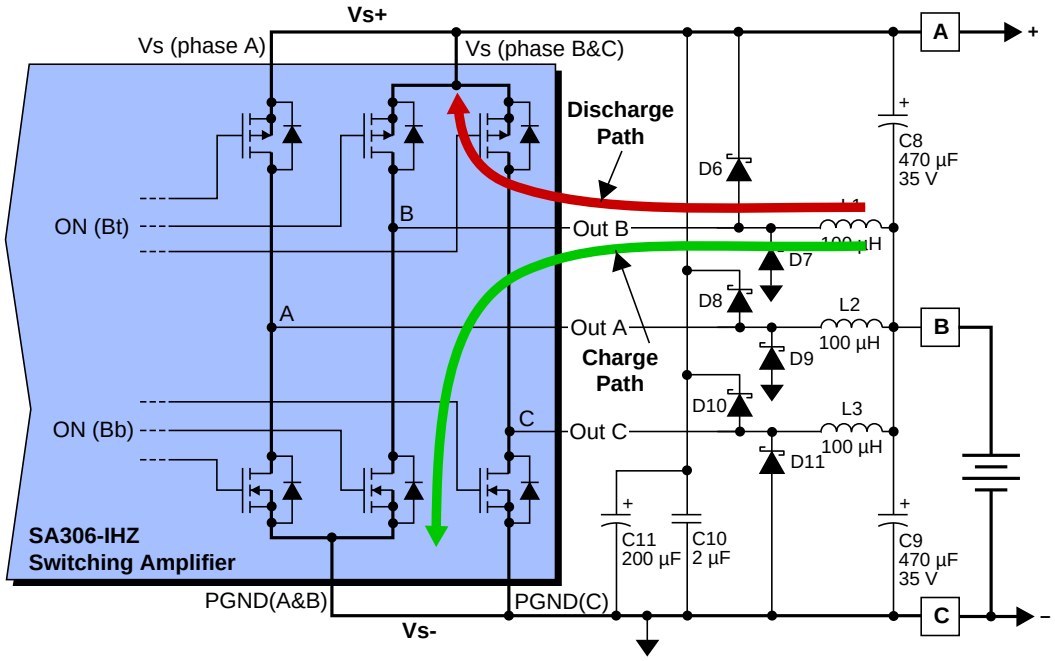


Figure 3 – Charge Dynamics – Positive Converter

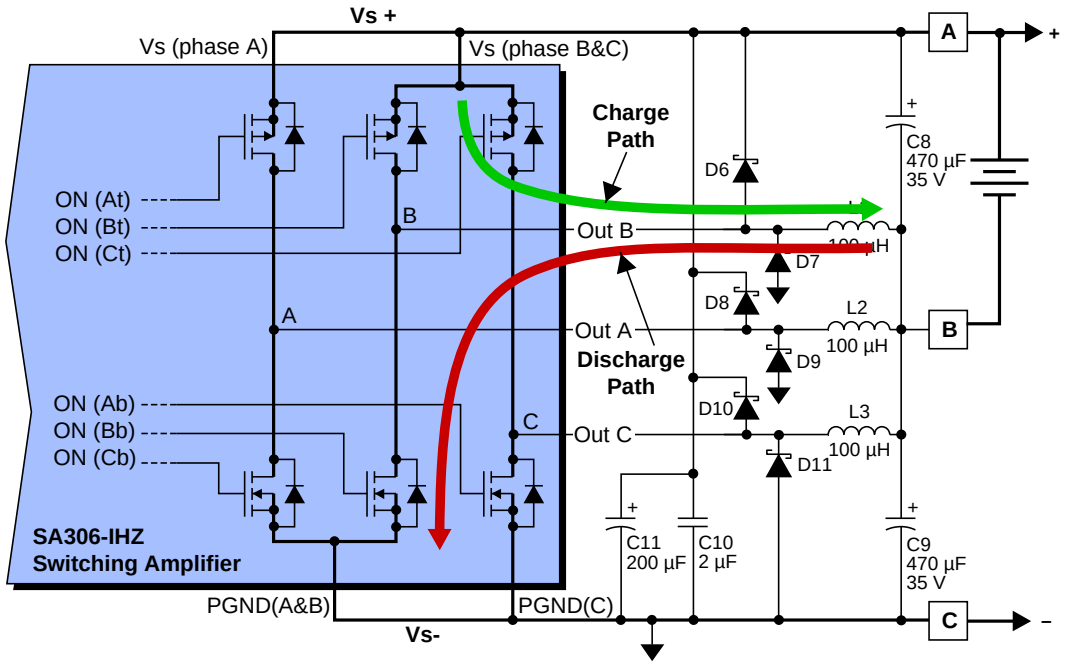


Figure 4 – Charge Dynamics – Negative Converter

Steady-State Waveforms

As shown in Figure 5a, when the signal from the PWM turns on Bt, the current contribution to L1 during the previous cycle starts to decay (Iout waveform). When Bt goes OFF, and Bb goes ON, the current flows into inductor L1, rising in a linear fashion as depicted. By examining the actual composite waveform resulting from the contributions of both the B phase and the A-C phase (which behaves as a single-phase switch driving one half the inductance of 100 microhenries), ripple current is reduced. This is true because during the A and C discharge interval, the two inductances, L1 and L3, are connected in parallel. So the effective inductance becomes 50 microhenries. This accounts for the fact that the two currents rising and falling out of phase with each other, only partially wash each other out. So that the delivered current is a fairly steady 4 amperes, but with a slight ripple, as depicted in Figure 6.

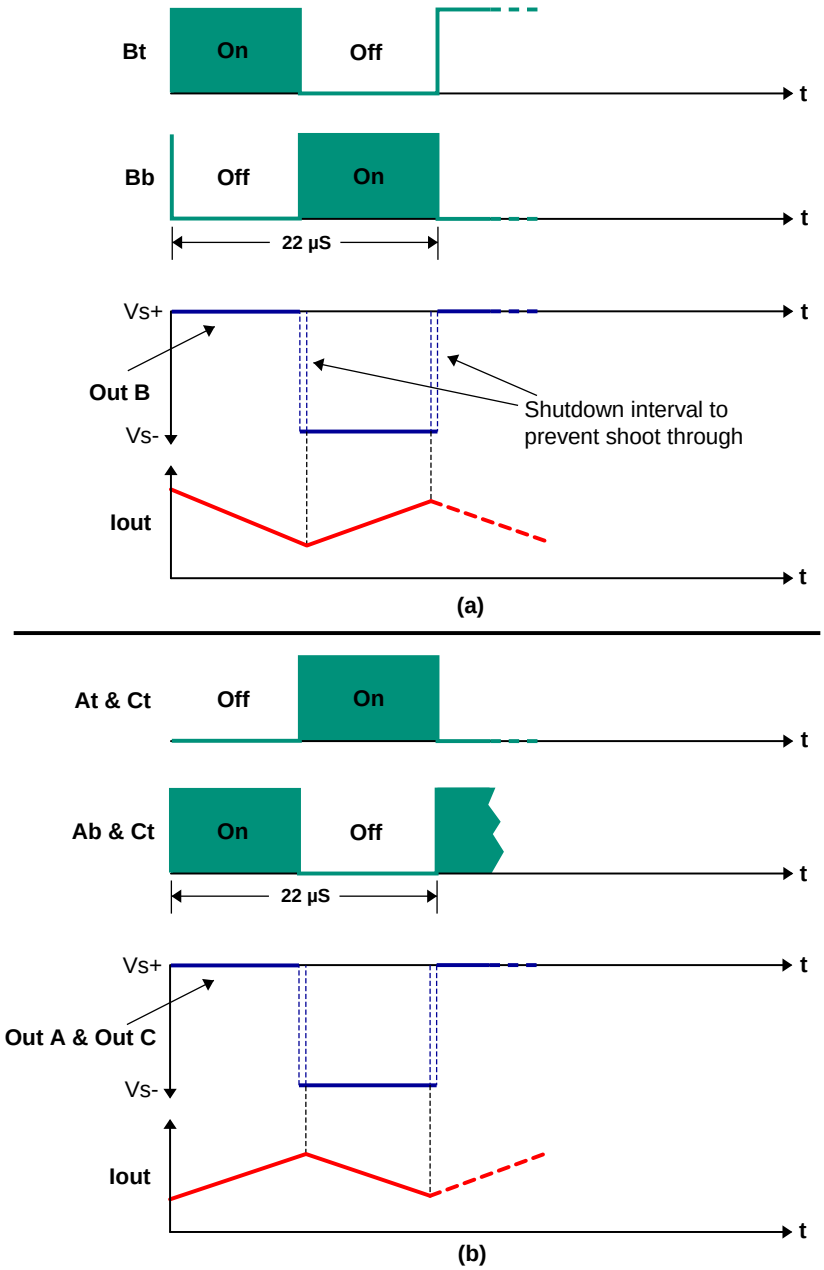


Figure 5 – (a) Phase B Discharge/Charge; (b) Phase A-C Charge/Discharge

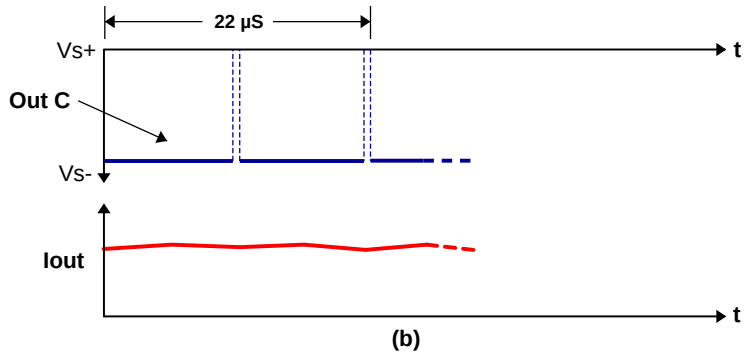


Figure 6 – Composite Waveforms – Phases A and B-C both delivering current

Thermal Protection

Shown in Shown in Figure 7 is a circuit that could be added to “burp” the SA306-IHZ via DIS2 (no external latch) if a thermal overload is detected at TEMP pin 25.

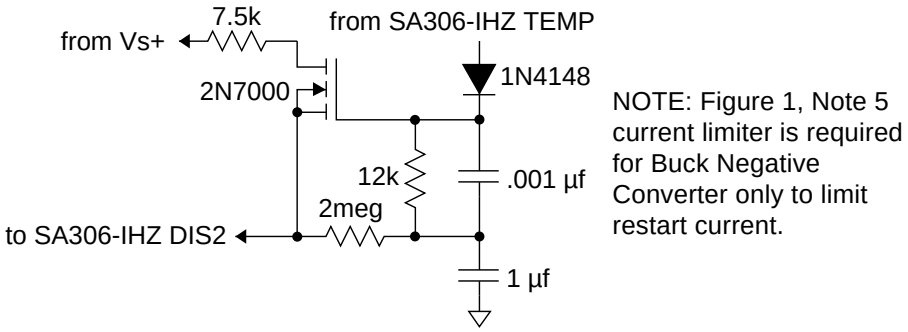


Figure 7 – Thermal Protection Circuit

An optional latch may be driven by the SA306-IHZ at TEMP pin 25 and its output could be used to shut down the converter via the DIS 1 pin 7, and/or shut down the 28 V supply in the event of a cooling failure. External current monitoring could also be gated to the same DIS1 pin 7 latch to protect the Boost Converter from load faults, etc. Note that pin 7 should be driven through a diode when current limiting is used (Buck mode only).

Overvoltage Protection (Boost Only)

Over voltage protection is set by Potentiometer R9 so that limiting begins when the output reaches 57 V.
This is essential because if there is no load connected, and the Boost Circuit is run off a 30 V power supply, it would be possible to obtain a 2 to 1 output voltage — plus, a small potential due to the inductance. This could destroy the SA306-IHZ. R9 should be set to maximum resistance when configured for Buck mode (Figure 1, Note 5).

Miscellaneous Design Notes

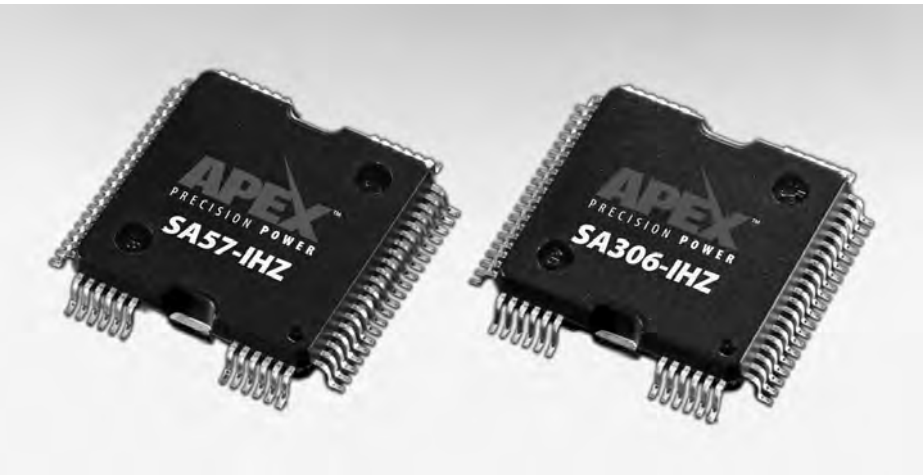
Capacitors C10 and C11 – Capacitors C10 and C11 are shown as bulk values in Figures 1, 3 and 4. These may be distributed between the Vs and the power ground terminals of the IC to provide adequate bypass.
Overvoltage Shutdown - The DIS2 pin 23 is employed to shut down the SA306-IHZ if a 1.7 V threshold at the pin is exceeded.
Voltage Trimming the Output voltage – Adjusting Potentiometer R8 enables trimming the output voltage slightly. The range is small because the shift in the duty cycle of the PWM (U2, U3) is small. The output voltage should be set to nominal with the output load set to one-half of its rated value to minimize the deviation from nominal under all load conditions.
Measuring the Phase Currents – Any of the phase currents can be measured by monitoring the voltage at the Ia, Ib, and Ic pins using a scope while the Boost Circuitry is configured as a negative converter and with the output loaded.
Input Voltage is Limited to 30 V – An input voltage above 30 V is not recommended without full characterization of the application. This is due to the fact the maximum duty factor is 50% and the output could conceivably rise above the 60 V rating of the SA306-IHZ under transient conditions.
Other Voltage and Current Options – It should be noted that the 30 V zener D3 could be changed to a 12 V zener (approximately) to configure a 20 V to 32 V and a 12 V, 8.5 A converter, for example.
Buck Negative Converter – Application of power should be done via inrush limiting circuitry due to the nominal 450 µF input capacitance (input transient LC "ringing" 60V maximum).

References

1. *SA306-IHZ Pulse Width Modulation Amplifier Data Sheet*, www.cirrus.com
2. *3-Phase Switching Amplifier Application Note #46*, www.cirrus.com
3. *TLC555 LinCMOS Timer*, www.ti.com

Optimizing Power Delivery in PWM Motor Driver ICs

Thermal Behavior of Single-Phase, Three-Phase Single-Chip PWM Amplifiers SA57-IHZ, SA306-IHZ



Contents

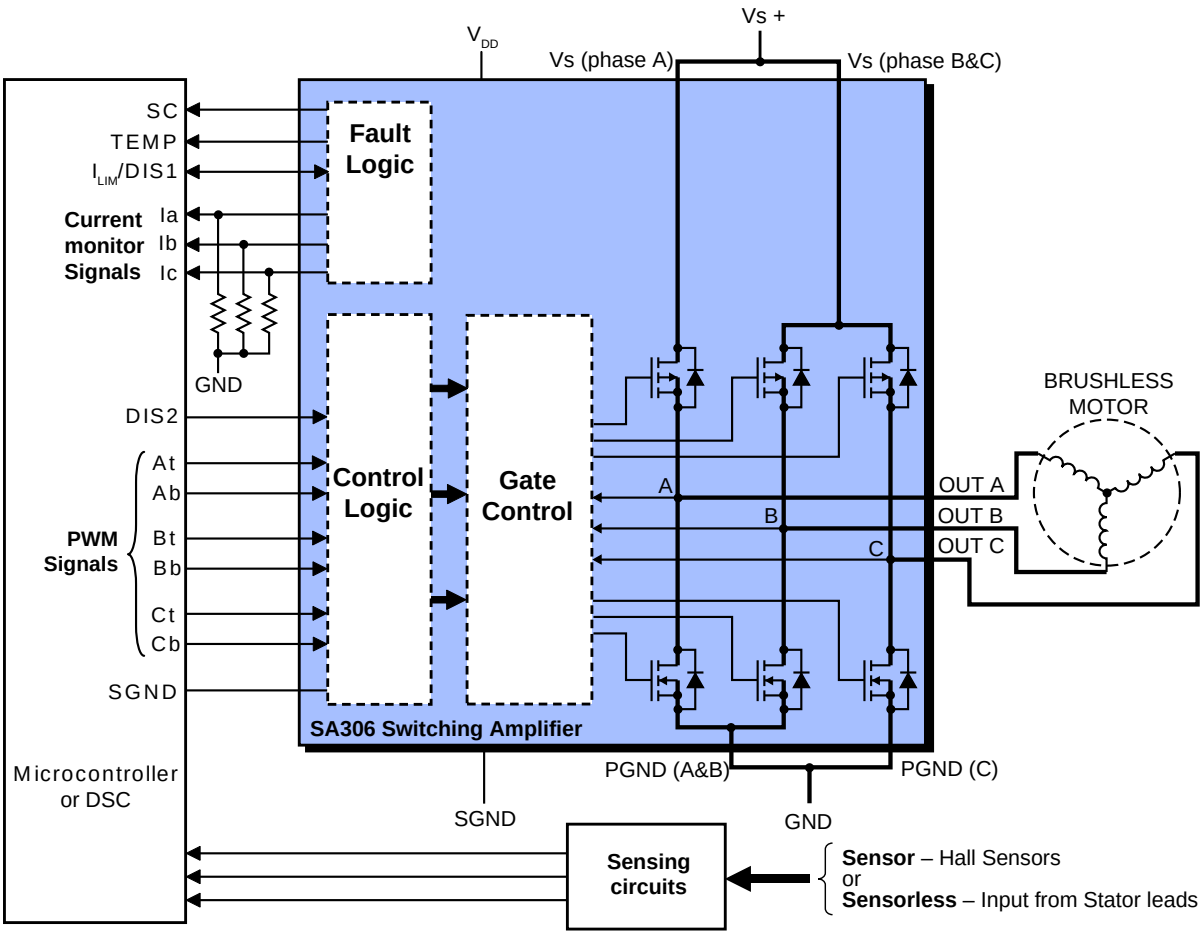


Figure 1. System Block Diagram using the 3-Phase SA306-IHZ Device

Introduction

The Apex SA306-IHZ is an advanced 3-phase single chip amplifier, designed for use as an independent power stage to drive 3-phase brushless DC motors. It incorporates a 3-phase PWM amplifier that accepts six independent control signals. This enables a designer to choose from a wide variety of control signals as appropriate for the commutation method chosen.

This Application Note discusses differences in the thermal behavior of the device relating to mounting techniques, methods of modulation of the power stage and examines some techniques to improve system performance and overall efficiency.

In order to choose the appropriate thermal design for a particular application and for the basic dimensioning of the heatsink, the calculation of the first-order thermal approximation is a good starting point. There are some application specific aspects to be taken into account before starting the basic system design. This Application Note covers some of these basic design steps, data and ideas to carry forward so the design can achieve the best results.

Device Overview

Both the SA306-IHZ and SA57-IHZ devices incorporate all of the sub-systems necessary to drive a brushed or brushless DC motor under the control of an MCU or DSP. At maximum output these devices are capable of safely operating motors approaching 0.5 hp. Like many traditional motor drive products, SA devices integrate control, power supply, gate drive and power stage into a single IC. Unlike competing devices, this series is specifically designed for MCU or DSP control and integrate features that enable implementation of modern commutation techniques, resulting in higher efficiency drive stages. Both SA306-IHZ and SA57-IHZ devices consist of major blocks, as shown in Figure 1. The primary difference between the two devices is the number of phases supported; the SA306-IHZ supports three phases while the SA57-IHZ supports two.

A key feature of this series is the ability to directly control the output FETs. This enables modern commutation schemes such as field-oriented, vector-oriented, and sinusoidal to be implemented within the controller with no in-

tervening circuitry. This architecture simplifies circuit design and reduces EMC/EMI. These devices take the inputs for each gate and provides buffering and drive to the companion FET.

Another significant feature is built-in current sense. Current sense is available for each of the phases from a separate output pin. The output current of the sense pins is ~1/5000th of the phase current. The current sense pins provide direct, real-time feedback to the controller. Current sense is performed at the high-side only. Sensing of low-side currents under braking or flyback conditions is not supported.

Over-temperature, short-circuit and current limit are also implemented. These fault signals provide important feedback to the system controller which can safely disable the output drivers in the event of a fault condition. These topics are discussed in greater detail in Reference 3.

Both the SA306-IHZ and SA57-IHZ implement a cycle-by-cycle current limit scheme. This allows variable user-defined current limit thresholds without damage to the device. However, even in this mode, the user must consider and plan for excessive current excursions which could result in excessive power dissipation.

The architecture of the SA306-IHZ and SA57-IHZ devices enables the designer to configure dynamically-changing current limiting in the device in response to changing system operating conditions. The SA306-IHZ or SA57-IHZ data sheets specify a peak current of 17 amperes. However, if desired the designer can choose to lower this limit or to disable the feature altogether.

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered. For example, a 1 A continuous motor might require a drive amplifier that can deliver well over 10 A PEAK in order to provide the required start-up torque. The cycle-by-cycle current limit feature enables the SA57-IHZ/SA306-IHZ to safely and easily drive a wide range of brush and brushless motors through a startup inrush condition. With limited current, the starting torque and acceleration are also limited. The plots in Figure 2 illustrate starting current and back EMF with and without current limit enabled.

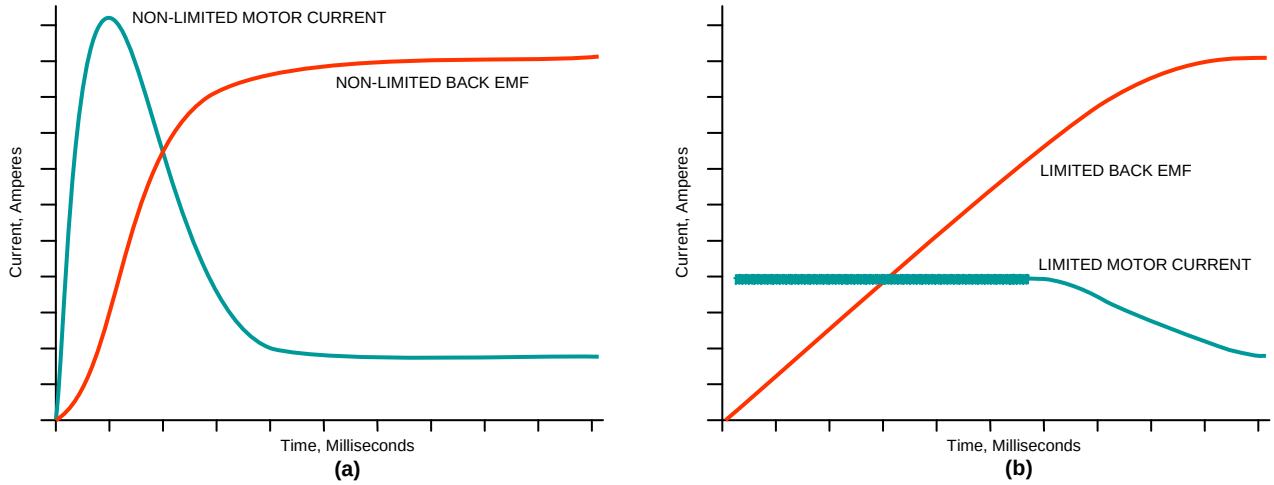


Figure 2. Motor Current Behavior at Startup — (a) Without cycle-by-cycle current limit. (b) With cycle-by-cycle current limit

More information on these and other features of the SA306-IHZ and SA57-IHZ can be found in the product data sheets, as well as any associated Application Notes listed in the Reference section found at the end of this document.

Optimizing Thermal Performance

All power devices, from FETs and IGBTs to large microprocessors, dissipate power in the form of heat. For devices whose primary purpose is power conversion or power transmission appropriate management of heat is the key to determining how much power can be safely processed by the device. This fact applies to specification limits as well. A device may be rated for 5 A continuous but the system designer must always take care that the power lost in the form of heat does not result in damage to the device.

It must be noted that total output power and total power dissipation are dependent on both the output current and operating voltage. For all mounting techniques discussed in this Application Note the effect of voltage and current levels will produce variations in power dissipation. For example, graphs of low power operation show heat dissipation for a given output power. Because power dissipation follows the formula $P=I^2R$, increasing operating voltage to the highest practical limit will result in greater output power at a given current (internal power dissipation). Conversely power dissipation can be reduced for a given output power by increasing voltage and reducing current.

Graphs are generally not provided for multiple combinations of current and voltage. Rather the emphasis is on the calculation of power dissipation and thermal resistance, thus enabling the designer to calculate die temperature for the system's combination of voltage, current, and heat sinking.

Shown in Figure 3 is an infrared image of a SA57-IHZ driving a brushed DC motor with a continuous current of 3 A at a supply voltage of 24 V. The numbers mark the local temperatures of the design. The high and low-side FETs of the active half-bridge can clearly be seen as white dots, representing a temperature of approximately 110°C. This picture shows the temperature gradients across the silicon.

The heat generated at the two hot-spots spreads over the silicon area. The result is a core temperature of approximately 90°C. The red area represents the heat slug of the IC. This temperature is nearly equal to the core temperature of the silicon. The heat is transferred to the heatsink on the backside (yellow) and in this case to the top and bottom layer (green) of the PCB, then dissipated into the ambient air. (Note that the apparent temperature difference of the screws is the result of emissivity differences between the screws and the rest of the test system. In steady-state operation the screws are approximately the same temperature as the heatsink).

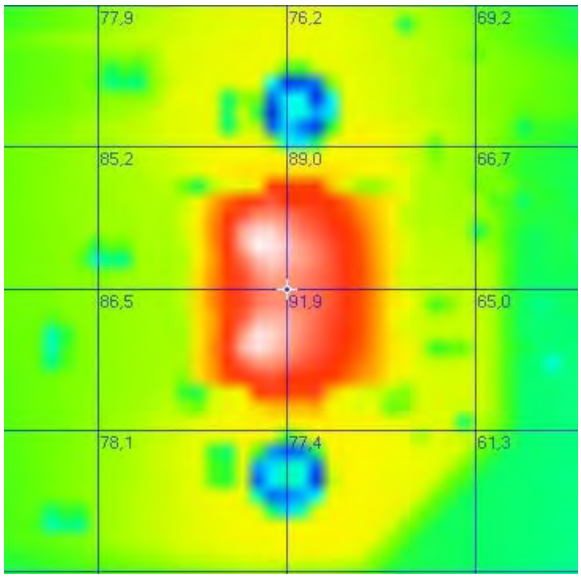


Figure 3. Infrared picture of a SA57 running at 3 amperes at 24 volts.

Optimized Motor Commutation Methods

The ON-resistance of the power FETs is the primary contributor to heat generation within a motor drive. In calculating the power lost to the ON resistance we use the standard power formula $P=I^2R$, where I = the current flowing through the motor and R = the ON-resistance of the IC. As the SA57-IHZ and SA306-IHZ offer direct access to each single FET, it is possible to use alternative commutation techniques to increase the system performance and to reduce thermal loads.

The best example for a simple system optimization is sinusoidal commutation of a 3-phase brushless DC motor. This method offers increased efficiency and reduced power dissipation. Alternate types of commutation are more feasible now that virtually every motor control system has some type of micro-controller or DSP/DSC available.

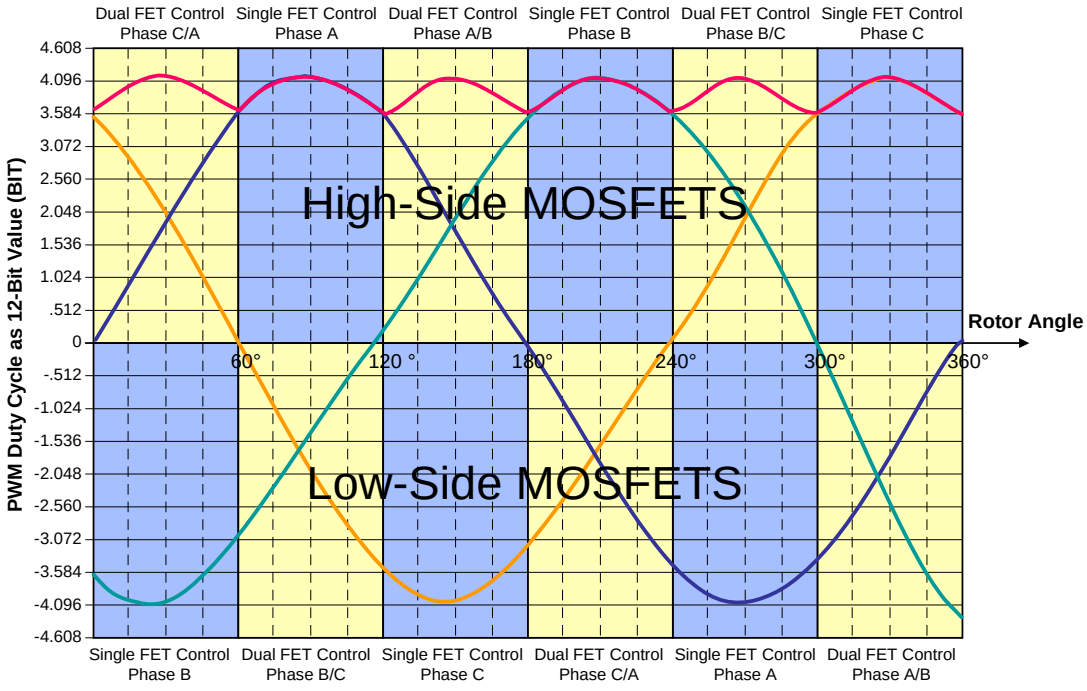


Figure 4. Power and voltage behavior in the case of 3-phase sinusoidal commutation.

Sinusoidal commutation of a 3-phase BLDC motor spreads the generated heat over a wider area of the silicon than with block commutation. This reduces localized heating in the die. During sinusoidal commutation the current through the motor is delivered by two high-side FETs and a single low-side FET or, in the next step, by using a single high-side FET and two low-side FETs. This means that there are always two active FETs in parallel which decreases the ON resistance of the two parallel conducting FETs. The resulting resistance is not linear because the on-time of each PWM signal of the two FETs connected in parallel follows a sinωt/cosωt relation. (See yellow areas in Figure 4)

The effective ON resistance across an electric commutation cycle can be calculated by dividing the ON-resistance value of the parallel high or low side FETs by √2. Using this commutation technique can, in addition to several other advantages, reduce the thermal load by approximately 10% to15%.

The undissipated power can be used to drive the motor or to reduce the total power consumption. In either case the overall efficiency of the system is increased.

Balancing the Electrical Load

As we have just discussed, the main heat generating contributor is the current flowing through the power FETs. Because the SA57-IHZ and the SA306-IHZ are high-voltage devices suitable for supply voltages up to 60 V, an increase in the supply voltage can lead to a decrease of the continuous current for a given power level and therefore to a decrease of the thermal load.

From this point of view, the basic idea is to increase the supply voltage while keeping the continuous current constant to reduce the thermal load. In a pulse-driven system with an inductive load, the relation between voltage and current is not linear so we have to take a closer look at switching losses and the current characteristics under various operation conditions.

An application is balanced when the forward and backward magnetization of the inductor is fully realized within a single PWM cycle. This should be the normal operating condition in applications with constant rotation speed and low dynamics, such as fans, pumps or unidirectional drives. In these applications, once accelerated, the motor runs at a constant speed with a constant mechanical load.

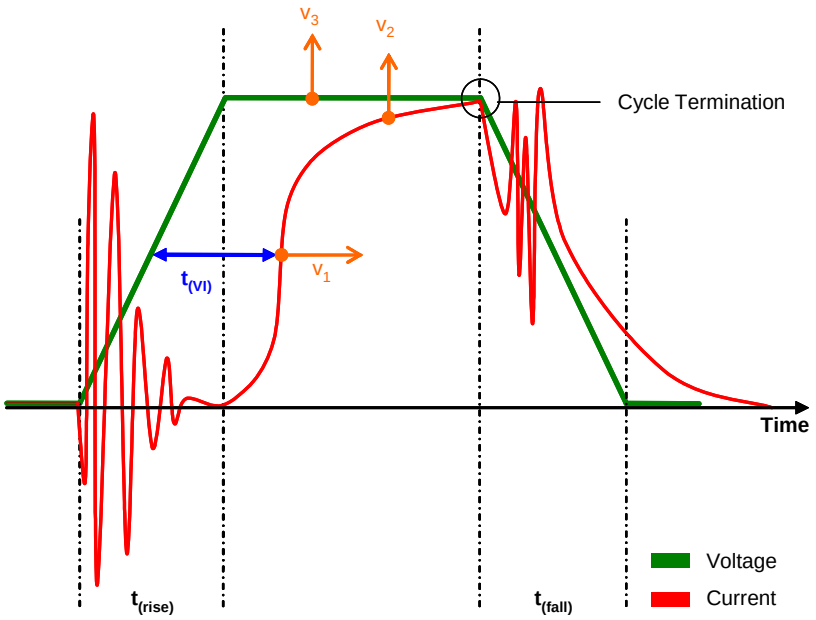


Figure 5: Characteristic of voltage and current during a PWM pulse in a balanced system

Shown in Figure 5 are the characteristics of the voltage and current during a PWM pulse in a balanced operating situation. The rising and falling edges of the voltage are nearly linear within the period given by the time value for the raising and falling edges – typically 200 nanoseconds. The current characteristic depends on the technical parameters of the motor winding. The windings produce a reverse voltage when the rising edge occurs. The current reaches its maximum when the supply voltage and the reverse voltage are more or less equal. The resulting phase shift is represented by t_{VI}. When the supply voltage v_3 is being increased, the phase shift t_{VI} becomes wider as shown by arrow v_1 and the rising edge of the current v_2 appears later. The termination of the duty cycle shuts down the current immediately and always at the same point in time. So when the supply voltage increases, both curves change in the directions indicated by the arrows labeled v_1, and v_2.

Shown in Figures 6 and 7 are voltage and current (overshoot not visible) plots resulting from a PWM pulse applied to phase A. Both 10 V and 30 V supply voltages are shown.

When we look at the falling edge of the PWM pulse, we see that the current drops with the same slew rate at a supply voltage of both 10 V and 30 V, but for a longer time interval because of the higher peak current. This means that the switching losses increase on the falling edge. At the rising edge of the PWM pulse the current is less, so that the switching losses on this side have decreased.

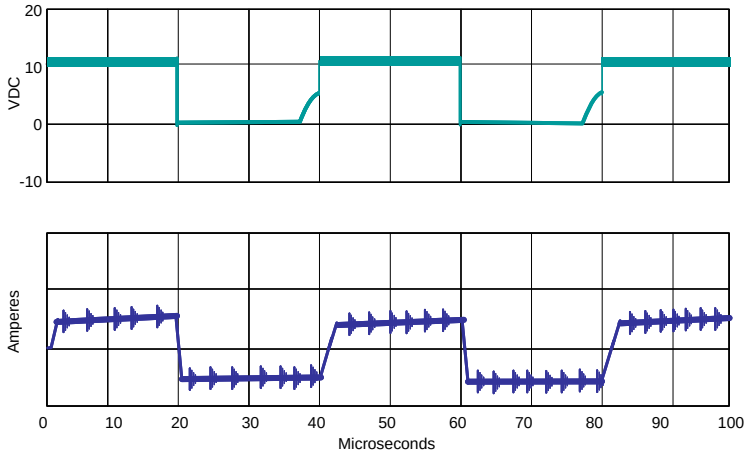


Figure 6. Voltage (green) and current (blue) during a PWM pulse on phase A at a supply voltage of 10 V DC, a 25 kHz switching frequency and a 50% duty cycle.

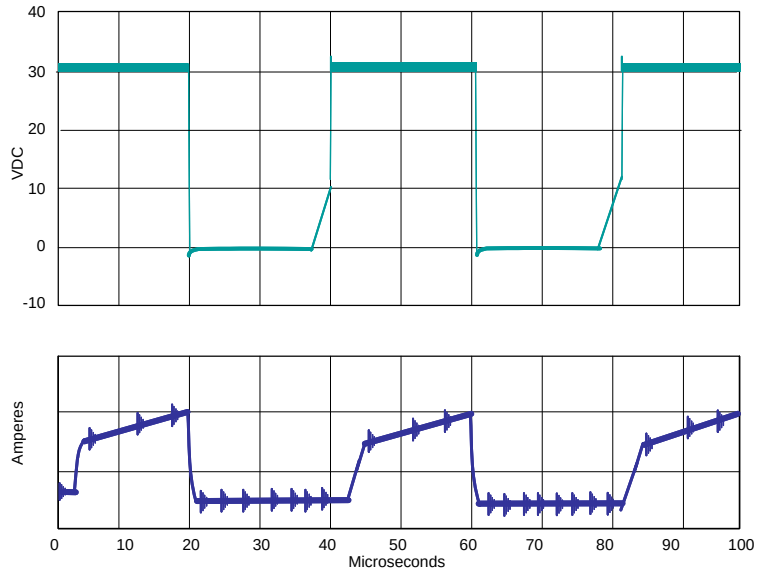


Figure 7. Voltage (green) and current (blue) during a PWM pulse on phase A at a supply voltage of 30 V DC, a 25 kHz switching frequency and a 50% duty cycle.

When we compare the total average current over time, we find similar values at a supply voltage of 10V and 30V. Although the peak current at 30 V is approximately 30% higher, the pulse width is 20% shorter and the slope of the pulse top is steeper than at 10 V. In an overall comparison the average current of both pulses is nearly constant with slightly increased switching losses.

Because the average current remains similar, the average temperature due to I^2R losses within the FETs is also similar. However, because voltage delivered to the motor does increase, there is greater power available to the motor windings. This fact results in increased efficiency by driving motors at higher voltages.

Defining a Movement Profile

In some applications, such as servo drives for positioning or robotics, we find a wide variety of specific operation modes, including periodic acceleration or stalled motor operation with high torque and low rotational speed. In these operating modes the system is not “balanced” since the motor windings are not allowed to achieve complete forward and backward magnetization within a single PWM cycle.

In these conditions the motor windings can become over energized, or saturated with power. As this begins to occur, increased motor current no longer produces proportional increases in torque and increased heating can occur in the FETs of the device. In some cases the motor windings are over energized to obtain the torque required to brake the mechanical load, resulting in a major change of the current waveform characteristic.

In these modes of operation, t_{VI} becomes smaller and a high current peak appears at the raising edge of the PWM pulse as shown in Figure 8. The more the supply voltage v_3 increases the higher the current peak v_2 will be. This current peak can reach multiples of the continuous current.

The plots in Figure 9 depict the relationship between duty cycle, continuous current and temperature at a supply voltage of 20 V DC.

By separating the performance graph in Figure 9 into two parts, the balanced operation (A) and the over energized operation (B) can be better analyzed. During balanced operation, the current and voltage waveforms follow the relationships shown in Figure 5. The phase shift t_{VI} increases so that the continuous current and temperature increase only slightly. When the motor winding starts being over energized (B), t_{VI} decreases rapidly as shown in Figure 8. The current peak at the rising edge of the PWM cycle increases the total average current and the thermal load. Over energized conditions normally happen in the 60-70% duty cycle range. This range corresponds with the knee of the curves in Figure 9. The exact point is dependent on both the quality of the motor and the operating condition. The operating condition with the expected maximal thermal load and its maximal time interval is the basis for the selection of the best mounting technique and heat sinking method.

The 64-pin Power QFP package used for the SA306-IHZ and SA57-IHZ lends itself to different kinds of mounting and heat sinking options which can be used under different operating conditions to realize the best results according to performance and total system cost. In the following sections suggestions are provided on how to select the best solution for your application.

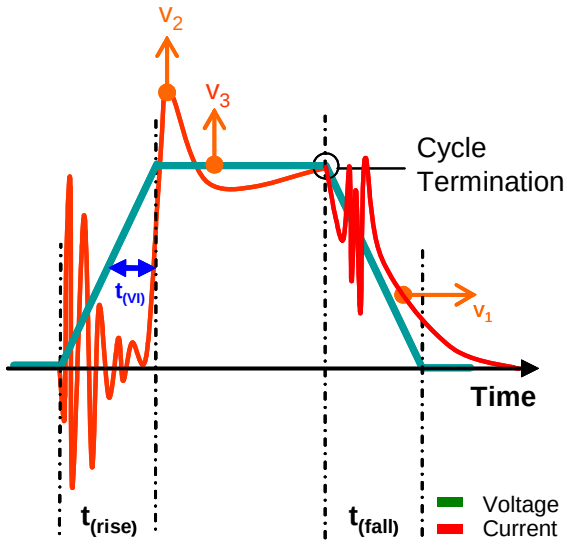


Figure 8. Voltage (green) and current (blue) during a PWM pulse over energizing a motor winding

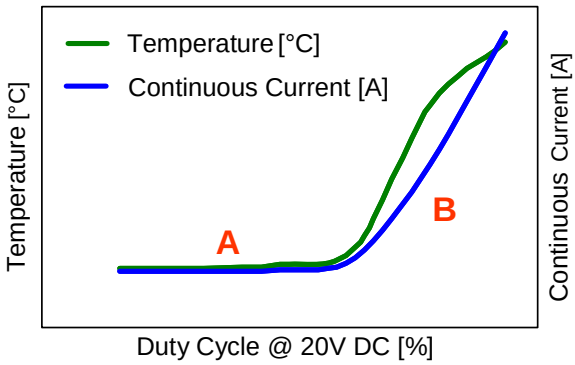


Figure 9. Temperature and continuous current vs. PWM duty cycle during a stalled motor operation

Cooling Options and Results with the 64-pin QFP Package

The size and orientation of the heatsink must be selected to manage the average power dissipation of the driver ICs. Applications vary widely and various thermal techniques are available to match the required performance. This section discusses several techniques that are appropriate for different power levels.

The following examples were developed to evaluate different mounting and cooling options and to define their basic capabilities. Derivation of maximum power and thermal system dynamics is shown in Appendix A.

Two different sets of tests were conducted on the SA306-IHZ. For the first set of tests the power devices were mounted on a PCB with a Digital Signal Controller (DSC). This DSC offers an enhanced motion control interface and allows a designer to commutate the motor in different ways. For the second set of tests a power test bench was used to show the effect of steady state currents on power dissipation and thermal performance.

SMT Mounting without Heatsink in Low-Power Applications

The most cost effective way of mounting either of the SA306-IHZ or SA57-IHZ devices is to solder them directly on a PCB without any further heat sinking components. The heat slug of the 64-pin QFP package offers optimized heat transfer to the PCB (as shown in Figure 10). The IC package, including the heat slug, can be soldered to the top layer of the PCB. Beneath the heat slug, several vias can be used to optimize heat transfer to the backside of the board. The copper area used for the power ground is also used for better thermal coupling to the ambient air.

As part of the tests, semiconductor temperature sensor was placed in the middle of the heat slug area to measure the backside (maximum) heat slug temperature. At an output power of 20 W, a temperature gradient of 99.6°K was obtained. This indicates that the junction temperature will be approximately 130°C at an ambient temperature of 30°C. The plots in Figure 11 denote a value of 136°C at an ambient temperature of 27°C with a total thermal resistance for the system of approximately 5.343 K/W.

Using the thermal resistance value, the maximum output power can be calculated for an application covering the industrial temperature range up to +85°C at approximately 9 W. This result is valid for static operation under the specific set of voltage and current conditions. In applications with frequent accelerations and decelerations it is important to know the thermal response time. This value provides an indication for the time required to transfer a specific amount of heat from the die to the backside of the board. Derivations for calculating thermal resistance and maximum power dissipation can be found in Appendix A. Shown in Figure 12 is the temperature characteristic of the ground plane from the ambient to the maximum temperature when the motor is driven continuously at an output power of 9 W.

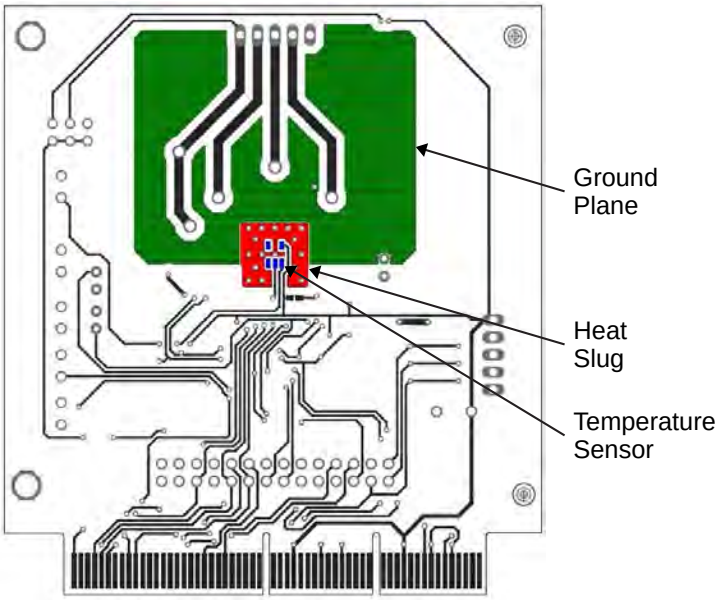


Figure 10. Bottom layer of the PICtail™ plus test board for low power applications

Conclusion

Although the maximum output power rating of 8 W to 9 W seems low, these devices are still capable of delivering PEAK currents up to 15 A for several seconds. In addition, increased voltage or reduced ambient temperature may result in increased power capability. This makes the SA57-IHZ and SA306-IHZ unusually well suited for applications using gears with high transmission rates where large mechanical loads have to be accelerated through start-up phase and end at high speeds with lower power requirements.

This mounting technique is appropriate for smaller, low-power or high-speed drives in cost sensitive applications such as fans, pumps, scanners, surveillance cameras, labeling machines or paper feeders – all where size and production costs are crucial.

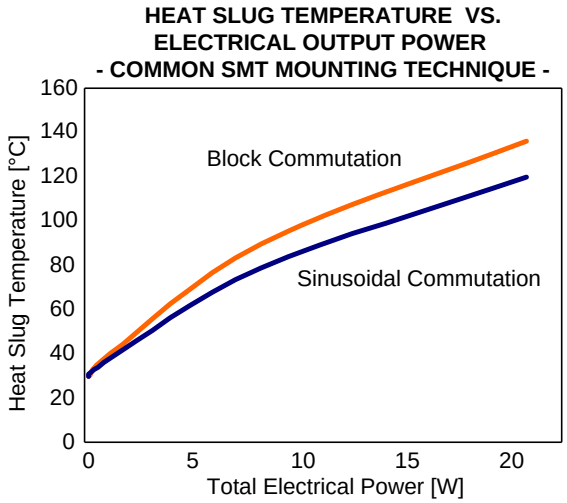


Figure 11. Temperature characteristic of the SA306-IHZ mounted on test board for low-power applications

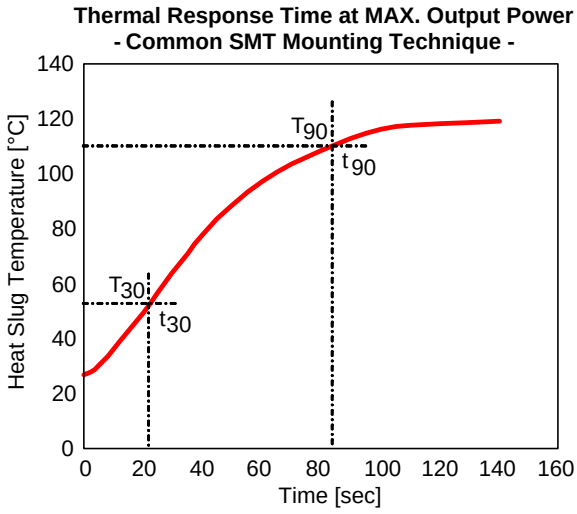


Figure 12. Thermal response time at MAX output power of 9 W

SMT Mounting with Thermal Pad and Heatsink for Mid-Range Power Applications

For applications where higher output power is required for a longer period of time, but ease of production is still a main design issue, an additional test board was designed where the SA306-IHZ is still mounted in the conventional manner. However, beneath the IC is a 100mm² cut out. A thermal pad is used to transfer the heat from the heat slug directly to the HS33 heatsink.

The thermal pad is made from a polymer that contains materials chosen for low thermal resistance, such as silver. These pads remain soft for years and therefore can accommodate any shifting that may occur to equalize between materials

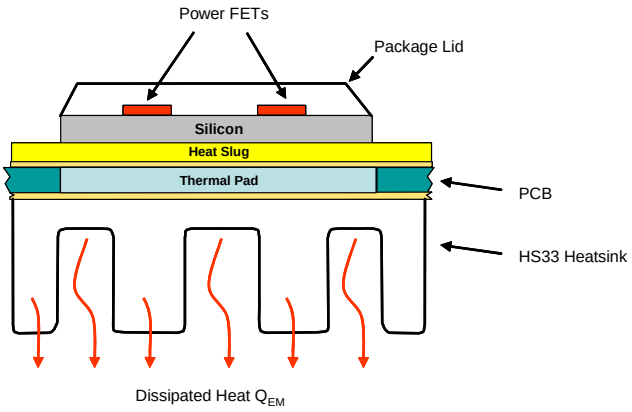


Figure 13. Simplified cross sectional view of the thermal system of the mid-power test board

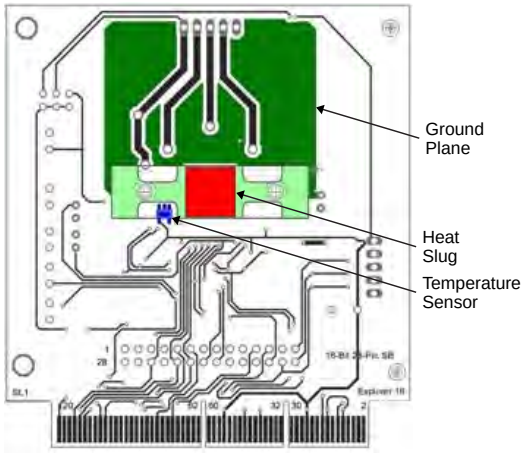


Figure 14. Bottom layer of the test board for mid-range power applications

with different coefficients of expansion that is likely to occur due to temperature changes. On the mid-power test board a 2mm thermal pad is used to fill the gap between the heat slug and the heatsink (see Figure 13). The thermal pad chosen is a Berquist™ Gap Pad 5000S35.The cutout area is 10mm x 10mm.

This board design provides three advantages:

- The SA306-IHZ is still mounted like a conventional SMT part, including the side-wings of the heat slug.
- Thermal coupling is always constant, even if the thickness of the PCBs varies from 1.5mm to 1.7mm.
- Accurate placement of the heatsink is not required.

Shown in Figure 14 is the back of the mid-power test board. The 100mm² heat slug area (red) has been cut out to accommodate the thermal pad. The temperature sensor has been moved to a natural cut out of the HS33 heatsink. The height of the sensor package is exactly the height of the cut out. The thermal coupling comes about due to the intimate contact of the package top with the heatsink.

The heatsink is mounted with two screws. Note that the light green area of the heatsink has direct contact with the dark-green ground plane area. With this mounting technique the total thermal resistance is reduced while the contact area is increased to ambient air. Although the HS33 heatsink is used on this test board, it is not essential. A thermal pad could also be used to couple the heat slug to the enclosure to improve the thermal path. The 100mm² x 1.5mm thick thermal pad with its thermal conductivity of 86 W/mK has a thermal resistance of 0.174 K/W. When this value is compared to the

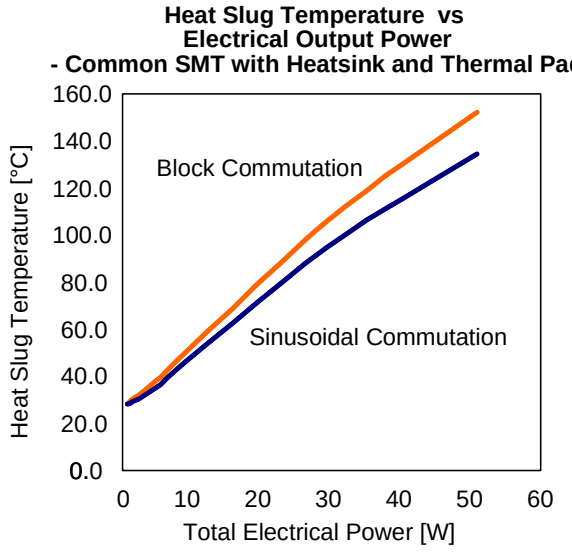


Figure 15. Temperature characteristic of the SA306-IHZ mounted on the test board for mid-range power applications using a thermal pad and the HS33 heatsink

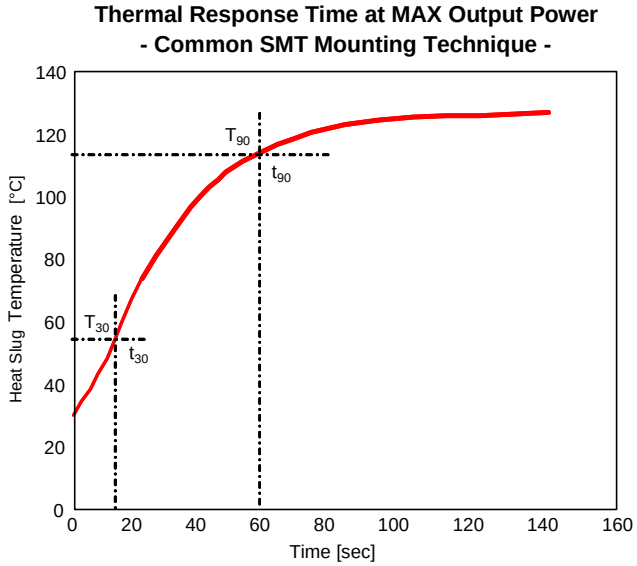


Figure 16. Thermal response time at output power of 20 W

previous model with vias, this solution provides less than a 10th of the thermal resistance.

Using the thermal pad, approximately 51 W of continuous output power is achieved with die temperatures of approximately +155°C at an ambient temperature of +26°C using block commutation. The maximum power output, up to +85°C for this configuration is approximately 20 W at the chosen voltage and current. With this solution it is possible to double the output power at similar system temperatures. What is most important is the improved performance over the short heat path to the heatsink due in part to the low thermal resistance through the thermal pad.

Conclusion

The thermal pad offers easy system assembly and good thermal performance at moderate power ratings. The short thermal path affords benefits in accelerating heavy mechanical loads for a longer time. This is an appropriate solution for a wide variety of industrial applications using gears and with production runs in mid-range volumes.

Flipped-Over SMT Mounting with Heatsink for High-Power Applications

The third test board uses the same heat sinking method as the Cirrus Logic Evaluation Boards DB63R and DB64R. This technique is also described in the *High-Power Heatsinking* section.

This time the SA306-IHZ is flipped over and mounted. The heatsink is then mounted directly onto the heat slug of the IC. This shortens the thermal path from the IC to the ambient air and reduces the total thermal resistance of the system to a minimum of 1.674 K/W.

Shown in Figure 17 is the assembly of the IC and heatsink on the test board for high-power applications. The position of the temperature sensor, the mounting method of the heatsink and the thermal coupling to the ground plane are still the same. The only difference is that the SA306-IHZ is flipped over and soldered in a precise cutout from the backside of the board. A picture of the actual mounting technique can be seen in Figure 20. As a result of this mounting technique, the characteristics of the temperatures in Figure 18 become quite linear across the whole power range. The output power at a die temperature of 135°C is approximately 52 W at +25°C and approximately 29 W at +85°C. This solution provides only a slightly higher maximum output power than the thermal pad. However, the short thermal path has its advantages in dynamic applications. The fast response time between the die and the heat slug provides benefits in applications where multiple accelerations occur over short time spans (see Figure 19).

Conclusion

The principal advantage of the flipped-over mounting is that it provides a short heat path for supporting high dynamic applications. The free access to the heat slug offers a wide variety of heat sinking methods and more effective cooling options.

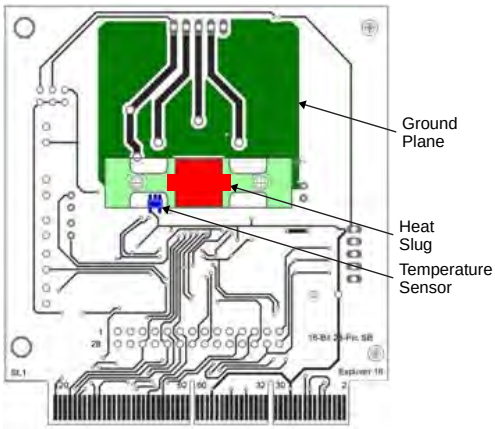


Figure 17. Bottom layer of the test board for high-power applications

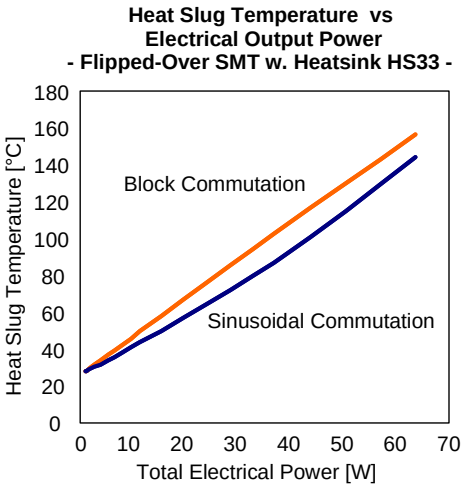


Figure 18. Temperature characteristic of the SA306-IHZ mounted flipped over on the test board for high power applications using the HS33 heatsink

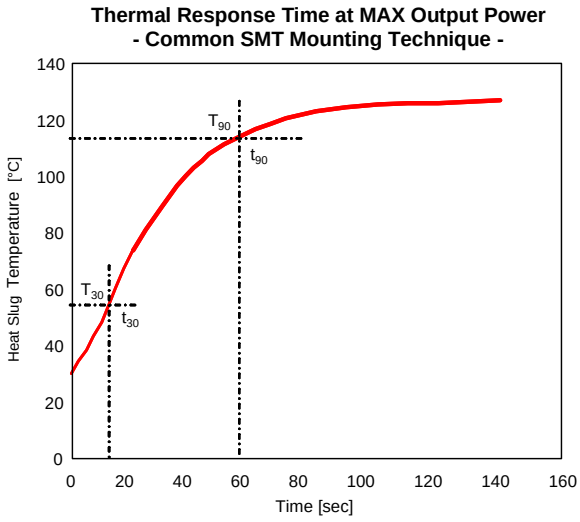


Figure 19. Thermal response time at a output power of 25 W

Comparisons of the Low-Power, Mid-Range Power and High-Power Test Board

The following table compares the benchmark values for each mounting technique in a side-by-side comparison. Please note that the columns for the maximum output power are rated for ambient temperatures of +25°C and +85°C. There is a more detailed chart for the power dissipation derating across ambient temperatures in the *Power Dissipation Derating* section.

Table 1. Temperature characteristics of the SA306-IHZ mounted flipped over on the PICtail™ Plus test board for high-power applications using the HS33 heatsink

Mounting Technique	Calculated MAX Output Power @ +85°C (W)	MAX Output Power at Test Voltage @ +25°C (W)	MAX Continuous Current at Test Voltage @ +25°C (A)	Total Thermal Resistance R_{TH} (K/W)	Average Thermal Response Time k90(K/sec)
Common SMT	9.0	19	0.93	2.789-5.343	1.323
Common SMT with Pad & Heatsink	19.8	38	2.73	0.628-2.529	1.869
Flipped Over with Heatsink	23.9	52	4.12	0.801-1.726	2.637

All values in this Section are the result of actual tests under laboratory conditions and should provide an indication of the capabilities of several design variants. The behavior of these ICs may differ under different design and operation conditions.

High-Power Heat Sinking

Since the SA306-IHZ is designed for higher power applications, it is also necessary to determine heat sinking factors that allow for higher power dissipation. Because of the concentration of heat as a result of power density, it is important to use heatsink types that provide short thermal paths. For this reason large extrusions with fins on wide centers have not been included in this evaluation.

Dissipation capacity with two types of aluminum extrusions were evaluated. The HS33 is a small heatsink, 0.4" x 0.4" x 1.5", that has four fins on 0.118-inch centers. This configuration places all four fins directly under the heat slug of the SA306-IHZ package. The HS33 heatsink is shown in Figure 20. This heatsink is used on the Cirrus Logic DB64R evaluation board for the SA306-IHZ.

The second heatsink in Figure 21 is a pin configuration with dimensions of 1" x 2" x 2". The pins are 0.070" in diameter on 0.137" centers. This highly effective heatsink provides multiple heat paths directly under the silicon. Because of its size, it is capable of safely dissipating much higher power levels than the HS33.

The test set-up for the HS33 used the Cirrus Logic DB64R evaluation board with an 8Ω resistive load. To increase power, the DC voltage across the board and load were increased. This set-up does not fully simulate the operation of a motor. However, it does allow stable temperatures to be achieved, thus facilitating measurement. This set-up met the goal of allowing power dissipation and die temperature measurements with varying heatsinks.

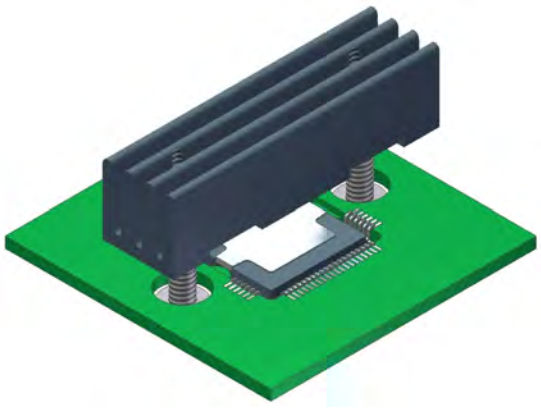


Figure 20. HS33 Finned Heatsink with SA306-IHZ

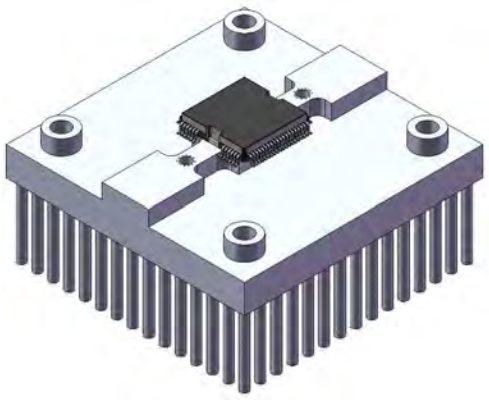


Figure 21. Pin Heatsink with SA306-IHZ

Table 2. Results of Thermal Testing

Configuration	Orientation	Convection	Dissipated Power (W)	Output Power @ 85% Efficiency (W)	Heatsink Temp MAX (ºC)	Junction Temp MAX (ºC)	Thermal Resistance (ºC/W)
HS33 and PCB	Horizontal, HS down	Natural	7.5	42.5	139	145	16
HS33 and PCB	Vertical, HS vertical	Natural	9	51	138	146	13
HS33 and PCB	Horizontal, HS down	Forced	17	96.3	127	140	6.8
Pin Heatsink	Horizontal, HS up	Natural	16	90.7	125	141	7.3
Pin Heatsink	Horizontal, HS down	Forced	39	221.0	79	113	2.3

Five different thermal configurations were tested, and the results are shown in Table 2. Note that consistent with real world applications, the differences in test set-up and measurement techniques between this test and the previous section produce different test results and power capabilities. This is to be expected and shows that designers must take into account their specific operating environment when evaluating thermal performance.

Three rows of HS33 data are shown in Table 2. The first two used convection cooling only. As one might assume, placing the heatsink in a horizontal position does not produce as effective a cooling surface as placing the heatsink vertically. With a vertical heatsink under convection conditions the heatsink dissipates 9 W, allowing 50 W of motor power at a +140°C junction temperature. Thermal resistance results with the vertical heatsink measured 13°C/W junction to air.

The third HS33 test was performed using a small fan blowing across the board. The object was to simulate an enclosed housing with a fan providing outside air, similar to a PC. In this case, dissipation improved to 17 W and allowing almost 100 W at the motor at 85% efficiency. Thermal resistance junction-to-case also improved dramatically to 6.8°C/W.

Subsequent testing with this configuration suggests that use of a small fan, in this case a 1" Sunon unit (PN GM0502PFV1-8, similar to MPU or graphics chip FAN), directed onto the HS33, allows heatsink dissipation in excess of 21 W and suggesting motor power of approximately 120 W. Under these conditions, die temperature should not exceed +140°C.

For full-power applications, the pin heatsink was tested. The pin heatsink was tested under both convection and forced-air conditions. The test board and fan can be seen in Figure 22. The fan used was a 2" Sunon (PN KDE1205PHV2) capable of 595 linear feet per minute of air flow. The retaining screws for the fan also hold the heatsink and the device in place on the board. The test configuration for the pin heatsink used a modified PCB layout and a 4Ω resistive load.

Under normal convection conditions, this heatsink was able to dissipate 16 W of power, allowing motor power of 91 W, similar to the HS33 with airflow. However, when using forced air with this heatsink, power dissipation within the heatsink increased to almost 40 W, allowing for greater than 220 W of power to the motor. In addition, the junction temperature dropped to +113°C, suggesting this is a high reliability configuration with room for increased power output. The junction to air thermal resistance also improved dramatically, measuring 2.3°C/W. With some increase in die temperature and a well designed system, the pin heatsink in a forced air configuration will allow the full 48 W and 5 A rating of the device.

Use of a heatsink does increase system cost. In some cases, the designer may find that a small amount of airflow across an HS33-type heatsink provides sufficient dissipation and lower costs versus a larger heatsink. However, for full power dissipation, use of a large heatsink with forced air may be necessary.

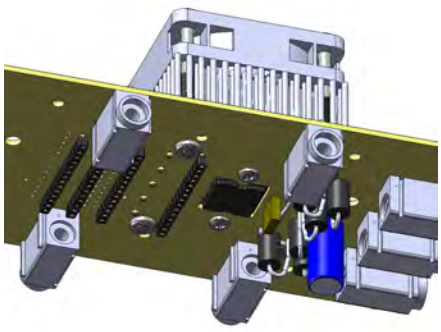


Figure 22. Pin heatsink and test board with fan attached

Power Dissipation Derating

To provide high-reliability operation, the die temperature must be kept to a safe level. The designer must consider total power, heatsink capability and ambient temperature in order to make appropriate system choices. The graph in Figure 23 shows derating curves for power. Curves are given for load power versus heatsink and ambient temperatures. In addition, curves are given for single-sided and double layer PCBs.

Figure 23 also shows that below +25°C the SA306-IHZ can operate above 300 W, assuming die temperatures are held to a reliable level. Above +30°C improved heat sinking must be employed or the device may need to be derated. Again, actual power capability is a function of operating voltage, efficiency, ambient temperature and heatsink capability. Actual derating will vary based on these factors. It should also be noted that the derating of heatsinks themselves change with temperature and therefore with power dissipation. As shown in Figure 24 for the HS33, both airflow and ambient temperature play a role in accurately modeling the dissipation capability of the heatsink.

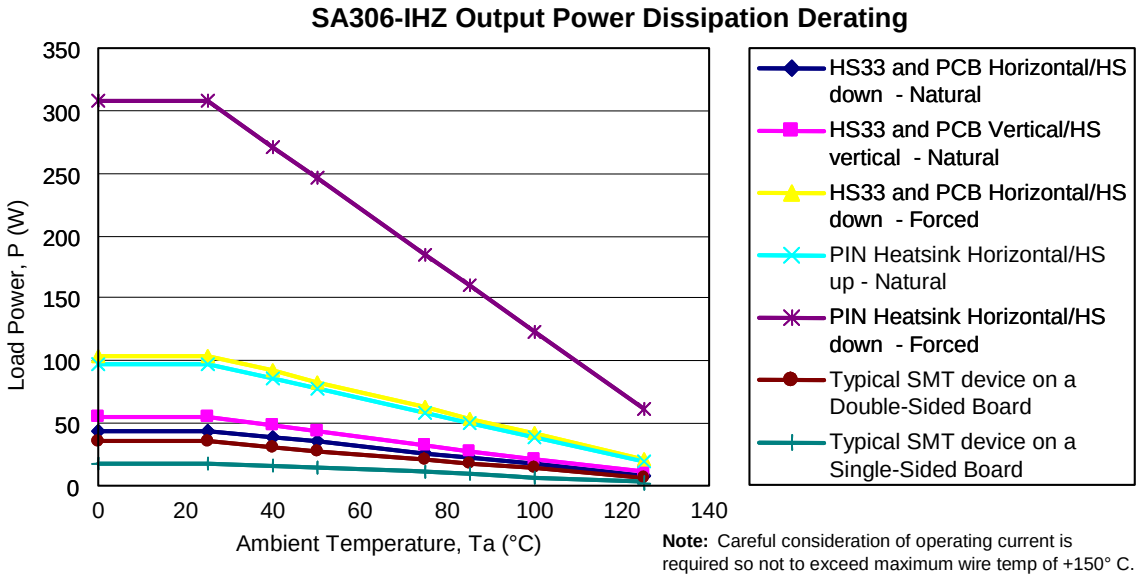


Figure 23. Load power derating curves for ambient temperature, Ta (°C)

Conclusion

Applications vary widely and various thermal techniques are available to match the required performance. The size and orientation of the heatsink must be selected to manage the average power dissipation of the IC. Standard PCB mounting techniques enable these devices to dissipate as much as 9 W. The use of a heat pad or the patent-pending mounting technique shown in Figure 20, with the SA306-IHZ inverted and suspended through a cutout in the PCB, is adequate for power dissipation exceeding 20 W.

In free air, mounting the PCB perpendicular to the ground, so that the heated air flows upward along the channels of the fins, can provide improved cooling. In applications in which higher power dissipation or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve performance. A pin heatsink can successfully dissipate the thermal energy generated when driving motors in excess of 200 W. By using the techniques in this Application Note, the SA57-IHZ and SA306-IHZ can provide long-term, reliable motor control in a very compact package.

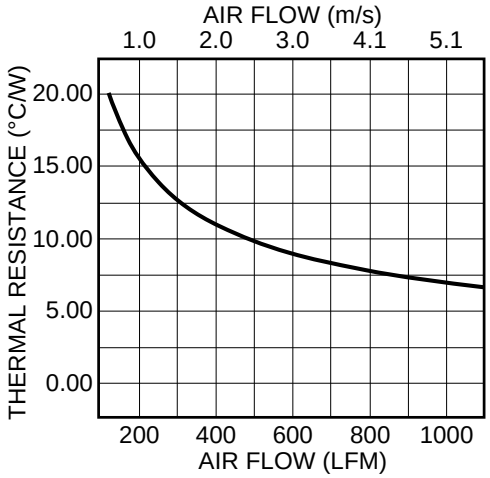


Figure 24. Heatsink thermal resistance versus air flow

References

1. *SA57-IHZ Pulse Width Modulation Amplifier* Data Sheet, www.cirrus.com
2. *SA306-IHZ Pulse Width Modulation Amplifier* Data Sheet, www.cirrus.com
3. *3-Phase Switching Amplifier* Application Note SA306-IHZ, AN46, www.cirrus.com

Appendix A – Derivation of Maximum Power and Thermal Dynamics Values for PCB Based Tests

Section A.1 Result for Common SMT Mounting with Heatsink in Low-Power Applications

The total thermal resistance of the common SMT model for a SA306-IHZ is 4.98 K/W (Kelvin per watt). To calculate the maximum output power for this mounting technique without specific values for voltage or current, we have to transform the equation:

$$T_0 - T_2 = \left(\frac{1}{\alpha A} + R_{th}\right) \bullet R_{DS(ON)} \bullet I_C^2$$

$$T_0 - T_2 = \left(\frac{1}{\alpha A} + R_{th}\right) \bullet P_E \quad (12)$$

Where:

T_0 = SA306-IHZ or SA57-IHZ junction temperature
T_2 = ambient air temperature
P_E = electrical output power

The plots in Figure 7 denote a value of +136°C at an ambient temperature of +27°C with a thermal resistance of approximately 5.343 K/W. The difference is due to the fact that the factor includes the thermal resistance into the ambient air and is therefore a combined value for $(\alpha A)^{-1} + R_{th}$.
When we use the value for the thermal resistance of the PICtail™ Plus Test Board to calculate the maximum output power for an application covering the whole industrial ambient temperature range up to +85°C, the maximum continuous output power is approximately 9 W:

$$P_{MAX} = \frac{T_0 - T_2}{R_t}$$

$$P_{MAX} = \frac{135°C - 85°C}{5.343\ \frac{K}{W}} = 9.4W \quad (13)$$

Where:

T_0 = SA306-IHZ orSA57-IHZ junction temperature
T_2 = ambient air temperature
R_T = total thermal conductivity
P_{MAX} = MAX electrical output power

Shown in Figure 12 is the temperature characteristic of the ground plane from the ambient to the maximum temperature, when the motor is driven continuously at a maximum power of 9 W. For later comparisons the focus is on the transfer ratio $\Delta T_{30}/\Delta t_{30}$ and $\Delta T_{90}/\Delta t_{90}$, described by a quotient K for the slew rate from the cold state to 30% and 90%, respectively, of the maximum temperature.
The slew rate quotient *k* is an indication for the quality of the dynamic behaviour of the thermal system:

$$k = \frac{\Delta\theta}{\Delta t} = \frac{T_1 - T_0}{t_1 - t_0}$$

$$k_{30} = \frac{54.5°C - 26.8°C}{21\ sec} = 1.317\ \frac{K}{sec} \quad (14a)$$

$$k_{90} = \frac{109.7°C - 26.8°C}{84\ sec} = 0.988\ \frac{K}{sec} \quad (14b)$$

Where:

k = slew rate quotient in Kelvin per second
$\Delta\theta$ = temperature difference in Kelvin
Δt = duration in seconds
T_0= temperature at time t_0
T_1 = temperature at time t_1

Section A.2 SMT Mounting with a Thermal Pad and Heatsink for Mid-Range Power Applications

The first order approximation of the thermal model gives a thermal resistance of 2.678 K/W. The following equation is used to verify the real value of the complete system:

$$T_0 - T_2 = \left(\frac{1}{\alpha A} + R_{th}\right) \bullet P_E$$

$$\frac{T_0 - T_2}{P_E} = \left(\frac{1}{\alpha A} + R_{th}\right)$$

$$R_t = \frac{155°C - 26°C}{51W} = 2.529\ \frac{K}{W} \qquad (15)$$

Where:
T_0= SA306-IHZ or SA57-IHZ junction temperature
T_2 = ambient air temperature
P_E = electrical output power
R_t = total thermal conductivity

Next is to find the maximum power rating to cover the total industrial range for ambient temperatures up to +85°C at a maximum die temperature of +135°C.

$$P_{MAX} = \frac{T_0 - T_2}{R_t}$$

$$P_{MAX} = \frac{135°C - 85°C}{2.529\ \frac{K}{W}} = 19.8W \qquad (16)$$

Where:
T_0 = SA306-IHZ or SA57-IHZ junction temperature
T_2 = ambient air temperature
R_t = total thermal conductivity
P_{MAX} = Max. electrical output power

The chart in Figure 12 shows the improvements of the thermal dynamics. The slew rate quotients k_{30} and k_{90} are:

$$k = \frac{\Delta\theta}{\Delta t} = \frac{T_1 - T_0}{t_1 - t_0}$$

$$k_{30} = \frac{55.8°C - 26.8°C}{15\ sec} = 1.938\ \frac{K}{sec} \qquad (17a)$$

$$k_{90} = \frac{114.7°C - 26.8°C}{63\ sec} = 1.407\ \frac{K}{sec} \qquad (17b)$$

Where:
k = slew rate quotient in K/s
Δθ = temperature difference in Kelvin
Δt = duration in seconds
T_0 = temperature at time t_0
T_1 = temperature at time t_1

Section A.3 Flipped Over SMT Mounting with Heatsink for High-Power Applications

The following equations are used to calculate the estimated maximum output power for ambient temperatures of +85°C:

$$\frac{T_0 - T_2}{P_E} = \left(\frac{1}{\alpha A} + R_{th}\right)$$

$$R_t = \frac{135°C - 26°C}{52W} = 2.096\ \frac{K}{W}$$

$$P_{MAX} = \frac{T_0 - T_2}{R_t}$$

$$P_{MAX} = \frac{135°C - 85°C}{2.096\ \frac{K}{W}} = 28.97W \quad (18)$$

Where:
T_0 = SA306-IHZ/SA57-IHZ junction temperature
T_2 = ambient air temperature
R_t = total thermal conductivity
P_{MAX} = MAX electrical output power

Using this mounting technique, the following values are obtained for k_{30} and k_{90}:

$$k = \frac{\Delta\theta}{\Delta t} = \frac{T_1 - T_0}{t_1 - t_0}$$

$$k_{30} = \frac{58.5°C - 26.8°C}{12\ sec} = 2.638\ \frac{K}{sec} \quad (19a)$$

$$k_{90} = \frac{121.8°C - 26.8°C}{53\ sec} = 1.792\ \frac{K}{sec} \quad (19b)$$

Where:
k = slew rate quotient in K/s
Δθ = temperature difference in Kelvin
Δt = duration in seconds
T_0 = temperature at time t_0
T_1 = temperature at time t_1

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Thermal Modeling of Power Devices in a Surface Mount Configuration

Introduction

This Application Note demonstrates how to develop a thermal model for power ICs. It then explains how the modeling of power ICs can be used to calculate the maximum power delivery possible during normal operation.

The Basic Model

Shown in Figure 1 is the cross-section of a power IC with the heat generating sources identified in red. The heat passes through the silicon substrate, a copper heat slug, and then into the foil layer on top of the printed circuit board. The heat transfers through the copper-plated vias which pass through the board transversely. The heat finally exits the assembly through the copper foil layer on the bottom of the printed circuit board. The first step is to define the heat source and represent the various paths by thermal resistance values and then calculate the power losses inside the power stage. The power loss over a time interval of Δt represents the amount of heat power fed into the system.

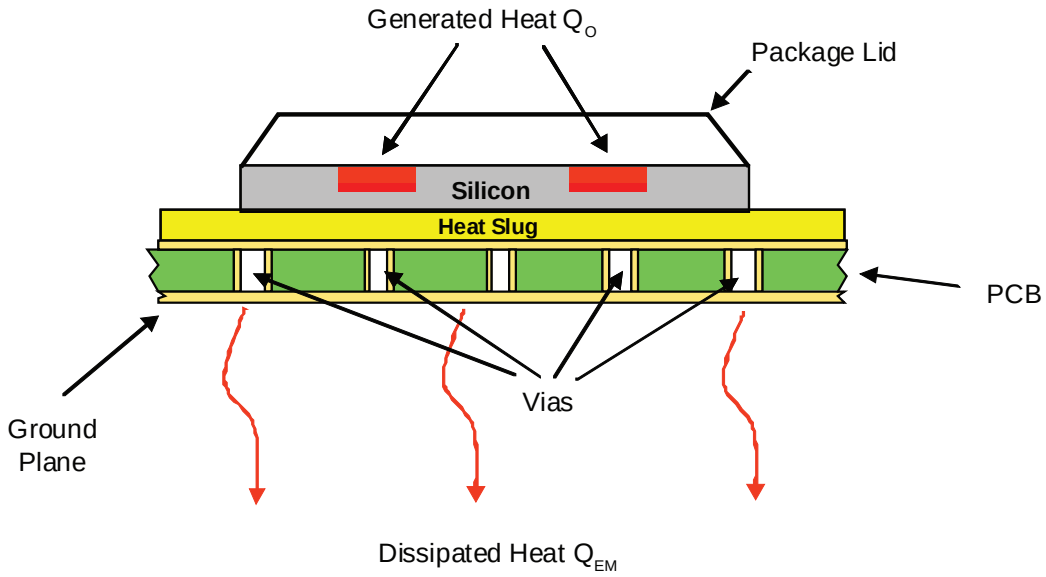

Figure 1: A Cross-sectional view of an IC thermal system

The copper foil directly beneath the heat slug serves as the thermal junction between the heat slug and the PCB. The PCB laminate itself is essentially a thermal isolator because of its high thermal resistance; therefore several vias are used to improve the heat transfer through the PCB. The bottom of the PCB features a large copper area (ground plane) because of its excellent thermal conductivity and the ability to optimize the heat dissipation into the air. This assembly can be depicted by the simple equivalent circuit shown in Figure 2. The Ohm's Law of heat transfer is similar to the Ohm's law for an electric circuit. Therefore we use familiar electrical symbols to describe the relations, as depicted in Figure 2.

Defining the Heat Source

The heat generated and depicted as Q_O in Figure 1 is attributed to three sources:

- Heat due to the current flow in the active devices of the logic circuit
- Heat generated as the result of switching losses
- Heat caused by the ON-resistance of each of the power FETs

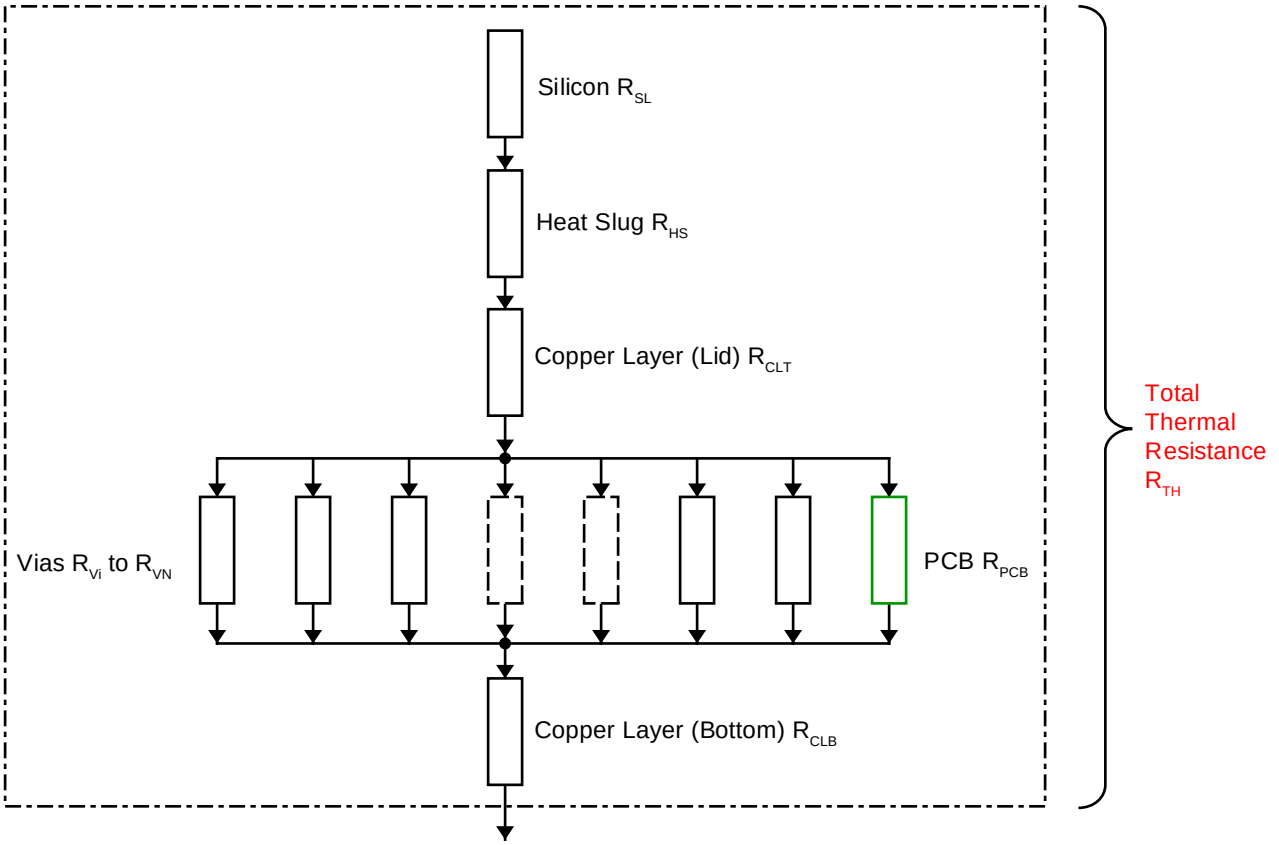

Figure 2: Equivalent thermal circuit for the power IC – circuit board configuration

The heat – expressed as power – developed in the logic circuit is more or less stable at 0.025 W. This is less than one hundredth of the power caused by the power FETs and therefore can be neglected in our analysis. The switching losses depend on the switching frequency, duty cycle and the supply voltage and will not be discussed in the following examples. However, in some applications it may be necessary to account for these losses in the heat source model.

The third source of heat is the most significant: The power FETs exhibit an ON resistance (RDS_{ON})when turned on. Therefore a voltage drop occurs across the FETs, caused by the current flowing through them. The amount of heat expressed as power dissipated by this process can be expressed by the familiar relationship:

$$P_L = V_D \times I_C \qquad (1)$$

Where:

P_L = power loss
V_D = voltage drop across the power FETs
I_C = continuous current

In normal block commutation, two of the FET switches – one high-side FET and one low-side FET – are ON during each commutation step in the rotation sequence. To calculate the voltage drop, use the sum of the two ON-resistances – the one high-side and one low-side FET:

$$V_D = (R_{DS(ON)High\ Side} + R_{DS(ON)Low\ Side}) \times I_C \qquad (2)$$

Where:

V_D = voltage drop across the two ON power FETs
R_{DS} = ON-resistance of a single ON power FET
I_C = continuous current

When these two terms are combined, it is possible to calculate the complete power loss:

$$P_L = (I_C)^2 (R_{DS(ON)High\ Side} + R_{DS(ON)Low\ Side})$$

$$P_L = (I_C)2\ R_{DS(ON)} \qquad (3)$$

The values for the ON-resistance can be found in the product data sheets of the SA306-IHZ and SA57-IHZ. The typical data given for the high-side (300 milliohms) and low-side (250 milliohms) power FETs is used for the calculation. To be able to use this equation for the definition of the heat source, power must be transformed into energy. The energy is defined by:

$$\Delta Q_0 = P_L \times \Delta t \qquad (4)$$

Where:

ΔQ_0 = dissipated energy
P_L = power losses
Δt = time interval

The equivalent term for the thermal energy of the heat source is:

$$\Delta Q_{th} = \Phi_{th} \times \Delta t \qquad (5)$$

Where:

$\Delta \Phi_{th}$ = heat energy
Φ_{th} = heat current
Δt = time

With the definition given for the heat current $\Phi_{th} = \Delta T/R_{th}$ we obtain:

$$\Delta Q_{th} = \frac{\Delta T}{R_{th}} \bullet \Delta t \qquad (6)$$

Where:

ΔQ_{th} = heat energy
ΔT = temperature gradient
R_{th} = total thermal resistance
Δt = time

The last thing to do is to set these two increments of energy equal so that the dissipated electric energy becomes the input to the thermal system:

$$\Delta Q_0 = \Delta Q_{th}$$

$$P_L \bullet \Delta t = \frac{\Delta T}{R_{th}} \bullet \Delta t$$

$$I_C^2 \bullet R_{DS(ON)} = \frac{\Delta T}{R_{th}}$$

$$\Delta T = (R_{DS(ON)} \bullet R_{th}) \bullet I_C^2 \qquad (7)$$

Taking a closer look at equation (7), there is a term for the temperature gradient ΔT as a function of the continuous current flowing through the power FETs. Both terms in the brackets are constant because neither the electric ($R_{DS(ON)}$) nor the thermal resistance (R_{th}) of the FET changes during operation. Also note that the temperature gradient will increase as the square of the continuous current. Equation (7) can be used to calculate the temperature gradient between the junction and ground-plane temperature that will be caused by a specific continuous current, or conversely as the maximum continuous current as a function of a specific temperature difference.

Calculating Total Thermal Resistance

Before using equation (7), the total thermal resistance of the system layers needs to be calculated. The thermal resistance depends on the layers and materials used. The thermal resistance of a solid state body is defined as:

$$R_{th} = \frac{s}{\lambda A} = \rho_{th}\frac{s}{A} \qquad (8)$$

Where:

R_{th} = total thermal resistance
s = length of the thermal path
λ = thermal conductivity of the material
ρ_{th} = thermal density of the material
A = cross-section of the object

For further calculations, the middle term will be used containing the thermal conductivity λ to calculate the thermal resistance. According to the Ohm's law of heat transfer theory the complete equation for the model shown in Figure 1 is:

$$R_{th} = R_{SL} + R_{HS} + R_{CLT} + \left(\frac{1}{R_{PCB}} + \sum_{i=1}^{n}\frac{1}{R_{Vi}}\right)^{-1} + R_{CLB} \qquad (9)$$

Where:

R_{th} = total thermal resistance
R_{SL} = resistance from the FETs into the silicon
R_{HS} = resistance from silicon into the heat slug
R_{CLT} = resistance from the heat slug into the top layer of the PCB
R_{Vi} = resistance from the top layer of the PCB into a single via
R_{PCB} = resistance from the top layer of the PCB into the PCB
R_{CLT} = resistance from the PCB via into the bottom layer of the PCB

Shown in Table 1 are the parameters used for the calculation of the total resistance:

Table 1. Parameters for the Calculation of the Total Thermal Resistance

Component	Length ($x10^{-3}$ meter)	Cross-Section A($x\ 10^{-6}\ m^2$)	Thermal Conductivity λ (W/mK)
Silicon	0.38	15.8/23.7	148
Heat Slug	1	100	220
Top Layer	0.035	100	384
PCB	1.5	100	0.26
Via	1.5	$6.28x10^{-8}$	384
Bottom Layer	0.035	2160	384

Shown in Table 2 are the results for the thermal resistance of each component in the heat flow path. Note that in Table 2, the value for the thermal resistance for the SA57-IHZ and the SA306-IHZ differ.

Table 2. Total Thermal Resistance

Component	Thermal Resistance R_{th} (K/W)	
	SA57-IHZ	**SA306-IHZ**
Silicon	0.405	2.264
Heat Slug	0.045	
Top Layer	0.912×10^{-3}	
PCB + Vias	2.479	
Bottom Layer	0.140×10^{-3}	
Total	**2.913 K/W**	**2.789 K/W**

Why Heat Spread Depends on the Number of Active FETS

When a brushed DC motor is driven, only a single pair of FETs is in use continuously. In this case the area for heat transfer into the silicon is simply twice the area of a single FET structure. However, in the case of a 3-Phase BLDC motor application, the pairs of FETs change in accordance with the electric angle of the rotor. This means that all six FETs become active in an alternating sequence. Although only two FETs are active at any instant, the heat is spread over three times the area. However, in practical tests it has been determined that the effective heat transfer has the value of the single half-bridge operation divided by √2.

Active and Passive Heat Dissipation

A model is now in place that transfers the heat from the power FETs through several layers into a ground plane on the backside of the PCB. An additional step is required to calculate the heat that dissipates into the ambient air. This heat transfer from a solid state body into air is defined by:

$$\Delta Q_{EM} = \alpha \bullet A \bullet \Delta T \bullet \Delta t \qquad (10)$$

Where:

ΔQ_{EM} = dissipated heat energy
α = heat transfer coefficient
A = heat dissipating area
ΔT = temperature gradient between air and dissipating ground plane area
Δt = time

To calculate the results for a static operation, it makes sense to eliminate time. The equation for the heat energy can be easily transformed into an equation for heat power by eliminating the time factor:

$$P_H = \alpha \bullet A \bullet \Delta T \qquad (11)$$

The value for the heat power is given by equation (11). The thermal current multiplied by the input power (= electric power losses) gives the amount of power in watts that has to be dissipated into air.
Therefore:

$$\Delta T_1 = (R^{DS(ON)} \times R_{th}) \bullet I_C^2$$

with ΔT_1 = temperature gradient between the junction temperature and the temperature of the backside of the PCB and:

$$\Delta T_2 = \frac{1}{\alpha \bullet A} P_H$$

with ΔT_2 = temperature gradient between the temperature of the backside of the PCB and the ambient air.
The thermal system is in balance, when the dissipated heat power P_H is equal to the electrical power losses P_L:

$$P_H = P_L$$

$$\alpha \bullet A \bullet \Delta T_2 = R_{DS(ON)} \bullet I_C^2$$

$$\Delta T_2 = \frac{1}{\alpha \bullet A} \bullet R_{DS(ON)} \bullet I_C^2$$

$$\Delta T_1 - \Delta T_2 = \frac{1}{\alpha \bullet A} \bullet R_{DS(ON)} \bullet I_C^2$$

Where:

$$\Delta T_1 = (R_{DS(ON)} \times R_{th}) \times I_C^2$$

$$T_0 - T_1 = (R_{DS(ON)} \times R_{th}) \times I_C^2$$

These two equations can be combined into:

$$T_0 - T_2 = \left(\frac{1}{\alpha A} + R_{th}\right) \bullet R_{DS(ON)} \bullet I_C^2 \qquad (12)$$

Where:

T_0 = SA306-IHZ or SA57-IHZ junction temperature
T_2 = ambient air temperature

With this equation it is possible to calculate the temperature offset as a function of a specific continuous current, and vice versa.

Calculating the Maximum Continuous Current

To calculate the maximum continuous current, transform equation (11) into:

$$I_C = \sqrt{(T_0 - T_2) \bullet \left[\left(\frac{1}{\alpha A} + R_{th}\right) \bullet R_{DS(ON)}\right]^{-1}} \qquad (13)$$

The absolute maximum current can be calculated for a maximum continuous junction temperature T_0 of +135°C and a maximum ambient temperature T_2 of +85°C. At these operating conditions, a maximum temperature gradient can be set of 50K into equation (13).

When the temperature gradient is set, the value for the absolute maximum continuous current depends only on the heat-transfer coefficient α. The other parameters such as the size of the heatsink, the thermal resistance and the ON-resistance, are fixed by the system design. However, the heat transfer coefficient α is not a fixed constant and can vary according to the air movement. Commonly there are three main ranges for α defined for different flow speeds along a metal area:

Static (still air):	3.5 to 35 (inside a case)
Passive cooling:	23 to 70 (convection)
Active cooling:	58 to 290 (fan)

For valid dimensioning it makes sense to calculate the first-order approximation for a worst case scenario; therefore, the lower value should be used for each cooling alternative.

5. References

1. *SA57 Pulse Width Modulation Amplifier* Data Sheet, www.cirrus.com
2. *SA306 Pulse Width Modulation Amplifier* Data Sheet, www.cirrus.com
3. *3-Phase Switching Amplifier* Application Note SA306, www.cirrus.com
3. *Optimizing Power Delivery in PWM Driver ICs*, Application Note AN50, www.cirrus.com

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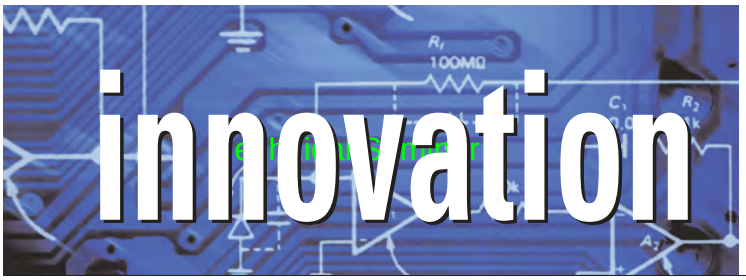

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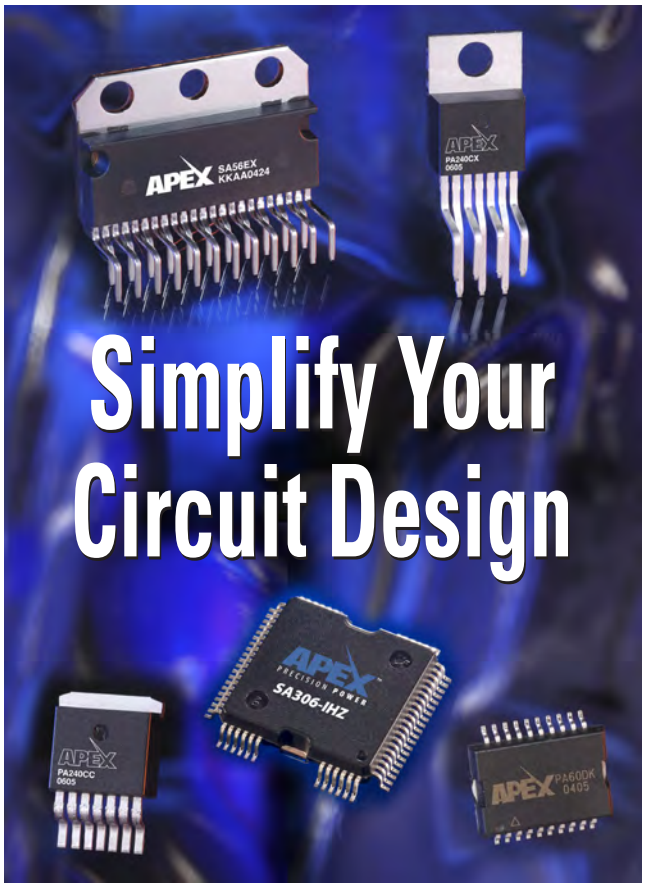

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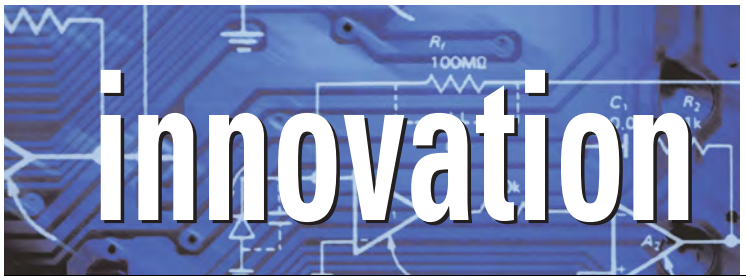

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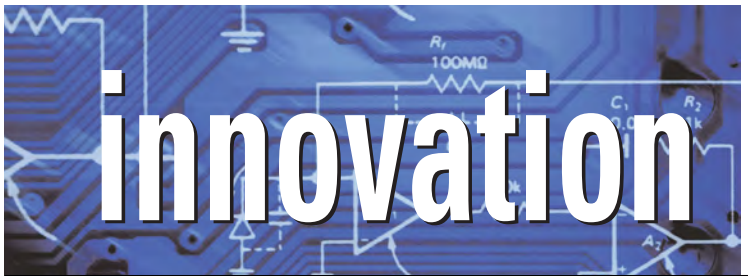

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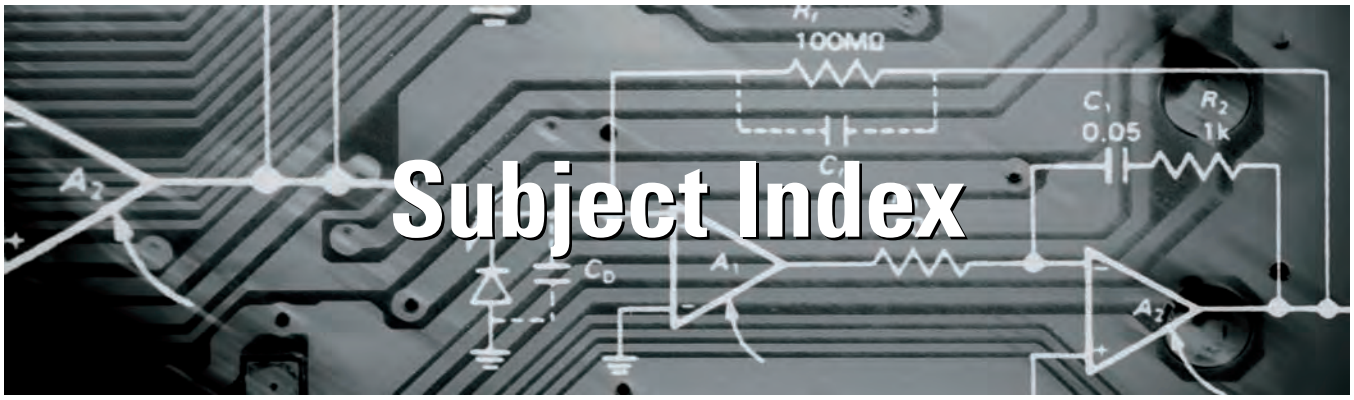

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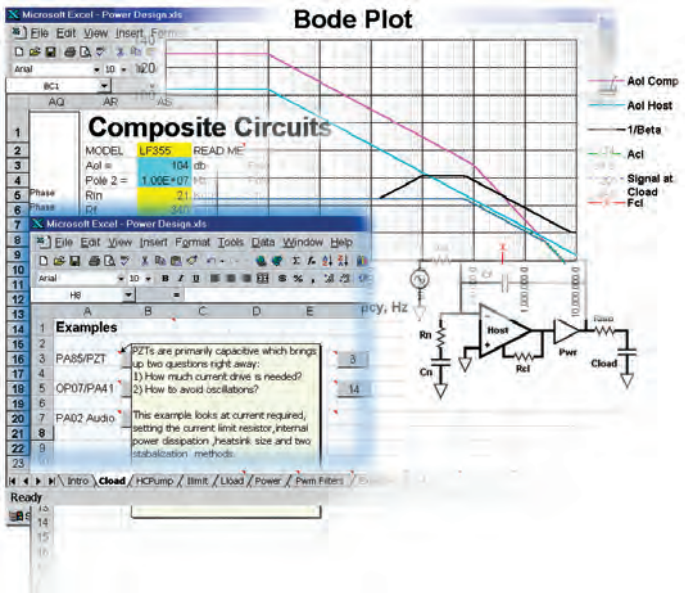

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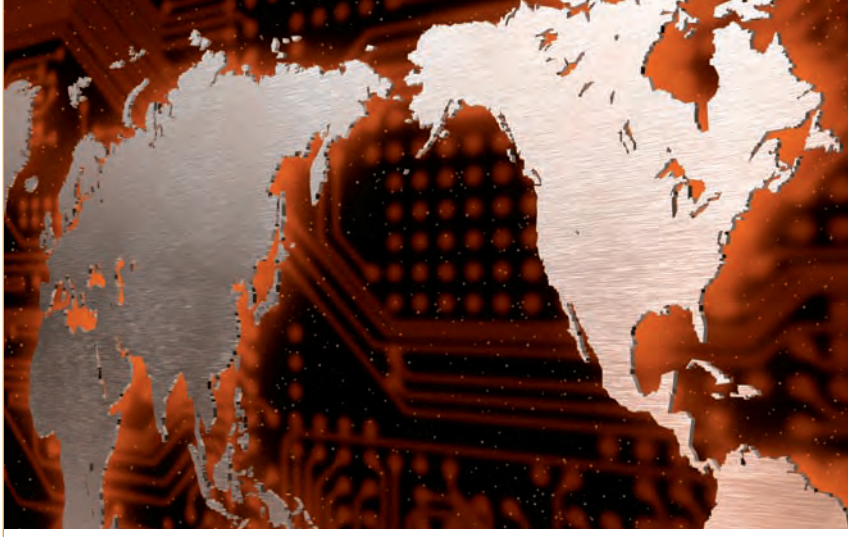

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